FAIRCHILD SEMICONDUCTOR®

April 2012

FSUSB74
4:1 High-Speed USB Multiplexer/Switch

Features

Switch Type	4:1
USB	USB 2.0 High–Speed Compliant USB 2.0 Full-Speed Compliant
R_{ON}	6.5Ω
C_{ON}	7.5pF
ESD (IEC61000-4-2)	15kV (Air) 8kV (Contact)
V_{CC}	2.7 to 4.4V
I_{CCSLP}	<1µA
I_{CCACT}	9µA
Package	16- Lead UMLP 1.80 x 2.60 x 0.55mm, 0.40mm Pitch 16-Lead MLP 3 x 3 x 0.7mm, 0.5mm Pitch
Ordering Information	FSUSB74UMX (UMLP) FSUSB74MPX (MLP)

Description

The FSUSB74 is a bi-directional, low-power, high-speed USB 2.0 4:1 MUX. It is optimized for switching from four high-speed (480Mbps) sources or any combination of high-speed and full-/low-speed USB/UART sources to one USB 2.0 connector.

Applications

- MP3 Portable Media Players
- Cellular Phones, Smart Phones
- Netbooks, Mobile Internet Devices (MID)

Related Resources

- *For samples and questions, please contact: Analog.Switch@fairchildsemi.com.*
- *FSUSB74 Demonstration Board*
- *FSUSB74 Evaluation Board*

Typical Application

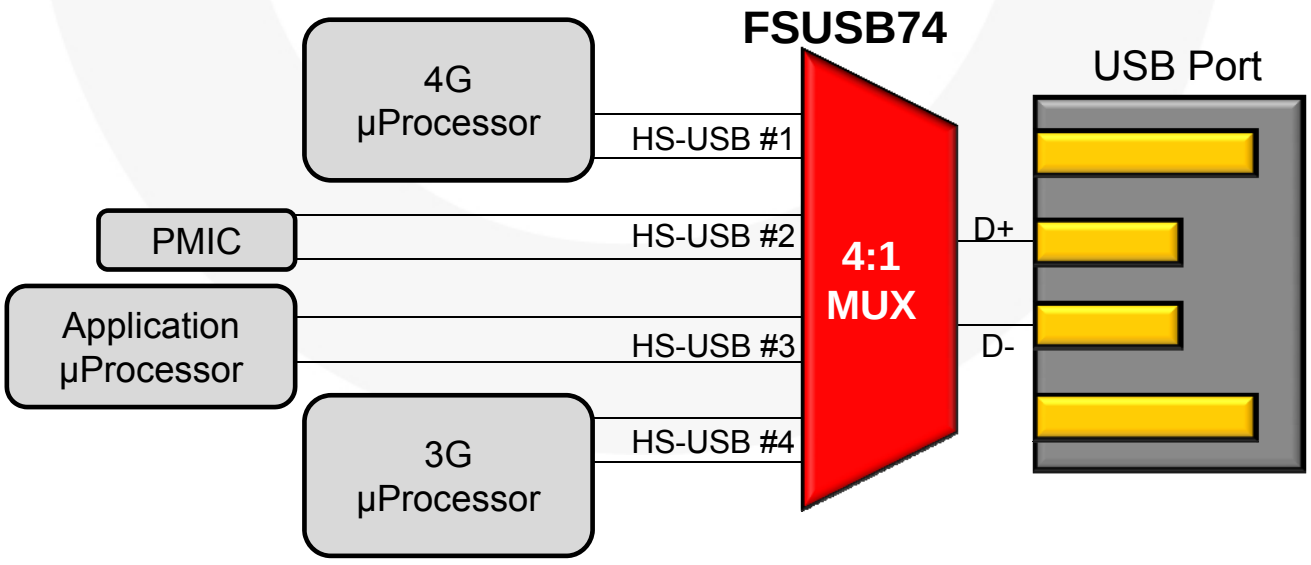


Figure 1. Mobile Phone Example

Pin Configurations

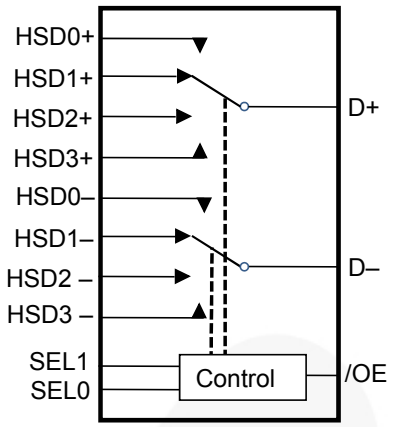


Figure 2. UMLP Analog Symbol

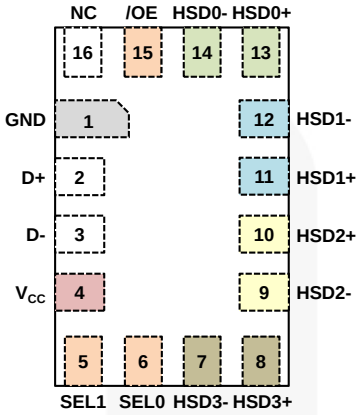


Figure 3. UMLP (Top View)

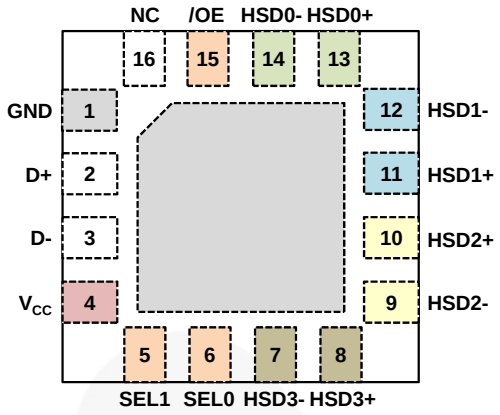


Figure 4. MLP (Top View)

Pin Descriptions

Pin #	Name	Type	Description
1	GND	Ground	Ground
2	D+	I/O	D+ common port (HS or FS USB)
3	D-	I/O	D- common port (HS or FS USB)
4	V_{CC}	Power Supply	Supply Voltage
5	SEL1	Input	Path Selection Control Input (see truth table below)
6	SEL0	Input	Path Selection Control Input (see truth table below)
7	HSD3-	I/O	D- from fourth source path (HS or FS USB)
8	HSD3+	I/O	D+ from fourth source path (HS or FS USB)
9	HSD2-	I/O	D- from third source path (HS or FS USB)
10	HSD2+	I/O	D+ from third source path (HS or FS USB)
11	HSD1+	I/O	D+ from second source path (HS or FS USB)
12	HSD1-	I/O	D- from second source path (HS or FS USB)
13	HSD0+	I/O	D+ from first source path (HS or FS USB)
14	HSD0-	I/O	D- from first source path (HS or FS USB)
15	/OE	Input	Enable Control Input (see truth table below)
16	NC		No Connect

Truth Table

/OE	SEL1	SEL0	Function
1	X	X	D+, D- Switch Paths Open
0	0	0	D+=HSD0+, D-=HSD0-
0	0	1	D+=HSD1+, D-=HSD1-
0	1	0	D+=HSD2+, D-=HSD2-
0	1	1	D+=HSD3+, D-=HSD3-

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	5.25	V
V_{CNTRL}	DC Input Voltage (SEL1, SEL0, /OE, SELS)(1)		-0.50	V_{CC}	V
V_{SW}	DC Switch I/O Voltage(1)		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	Level
ESD	IEC61000-4-2 System on USB connector pins D+ & D-	Air Gap	15		kV
		Contact	8		
	Human Body Model, JEDEC: JESD22-A114	D+,D- to GND	6		
		Power to GND	12		
		All Other Pins	2		

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	4.4	V
V_{CNTRL}(2)	Control Input Voltage (SEL1, SEL0, /OE, and SELS)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	4.4	V
T_A	Operating Temperature	-40	+85	°C

Note:
2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
R_{ON}[3]	HS Switch On Resistance	V_{SW}=0.4V, I_{ON}=-8mA, Figure 5	3.3		6.5	9.0	Ω
ΔR_{ON}[3]	HS Delta Ron[4]	V_{SW}=0.4V, I_{ON}=-8mA	3.3		0.5		Ω
I_{IN}	Control Input Leakage	All Combinations of /OE, SEL1 & SEL0 in the Truth Table (1=V_{CC}, 0=0V)	4.4	-1		1	µA
I_{OZ}	Off State Leakage	0 ≤ Dn, HSD0n, HSD1n, HSD2n, HSD3n ≤ 4.4V	4.4	-1		1	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}=0V to 4.4V, V_{CC}=0V, Figure 6	0	-1		1	µA
I_{CCSLP}	Sleep Mode Supply Current	/OE=V_{CC}	4.4			1	µA
I_{CCACT}	Active Mode Supply Current	All Active Modes in Truth Table	4.4		9	18	µA
I_{CCT}	Increase in I_{CC} Current per Control Input and V_{CC}	V_{CNTRL}=1.8V	4.4		3.3	4.0	µA
		V_{CNTRL}=1.2V	4.4		4.9	6.0	µA
V_{IK}	Clamp Diode Voltage	I_{IN}=-18mA	2.5			-1.2	V
V_{IH}	Control Input Voltage High	SEL1, SEL0, /OE	2.5 to 4.4	1.0			V
V_{IL}	Control Input Voltage Low	SEL1, SEL0, /OE	2.5 to 4.4			0.35	V

Notes:

3. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for V_{CC}=3.3V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time when Switching from One USB Path (or Disabled i.e. /OE=1) to Another USB Path	R_L=50Ω, C_L=35pF, V_{SW}=0.8V, Figure 7, Figure 8	2.5 to 4.4	126		400	µs
t_{OFF}	Turn-Off Time, Turning Off Any of the USB Paths	R_L=50Ω, C_L=35pF, V_{SW}=0.8V, Figure 7, Figure 8	2.5 to 4.4			80	ns
t_{PD}	Propagation Delay(5)	C_L=5pF, R_L=50Ω, Figure 7, Figure 9	3.3		0.25		ns
t_{RF}	Slow Turn-On/Off Switch Paths(5)	C_L=5pF, Dn at 0V or 3.6V, 40.5Ω in series with switch 10% to 90%	3.3		4.5		ns
t_{BBM}	Break-Before-Make Time(5)	R_L=50Ω, C_L=35pF, V_{SW1}=V_{SW2}=0.8V, Figure 11	2.5 to 4.4	126		400	µs
O_{IRR}	Off Isolation(5)	R_L=50Ω, f=240MHz, Figure 13	2.5 to 4.4		-40		dB
Xtalk	Channel-to-Channel Crosstalk(5)	R_L=50Ω, f=240MHz, Figure 14	2.5 to 4.4		-40		dB
$t_{SK(P)}$	Pulse Skew(5)	V_{SW}=0.2V$diff_{PP}$, Figure 10, C_L=5pF	2.5 to 4.4		25		ps
$t_{SK(I)}$	Skew Between Differential Signals Within a Pair(5)	V_{SW}=0.2V$diff_{PP}$, Figure 10, C_L=5pF	2.5 to 4.4		25		ps

Note:
5. Guaranteed by characterization.

Capacitance Characteristics

All typical values are for V_{CC}=3.3V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	Typical	Unit
C_{IN}	Input Capacitance(6)		0	3	pF
C_{ON}	D+/D- On Capacitance(6)	Any Switch Path Enabled, f=1MHz, Figure 16	3.3	7.5	
C_{OFF}	HSD0n, HSD1n, HSD2n, HSD3n Off Capacitance(6)	If V_{CC}=3.3V, then /OE=3.3V; f=1MHz, Figure 15	0 or 3.3	2.2	

Note:
6. Guaranteed by characterization.

Test Diagrams

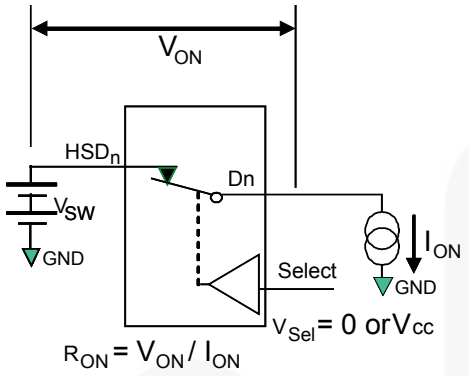
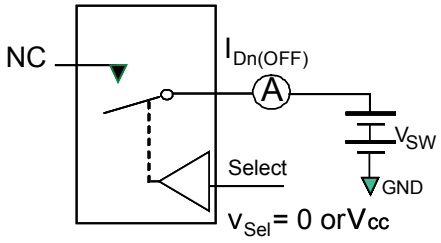
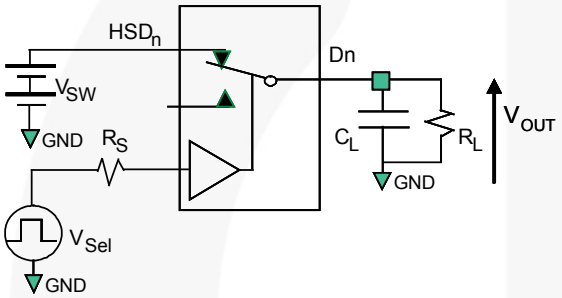


Figure 5. On Resistance



**Each switch port is tested separately

Figure 6. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 7. AC Test Circuit Load

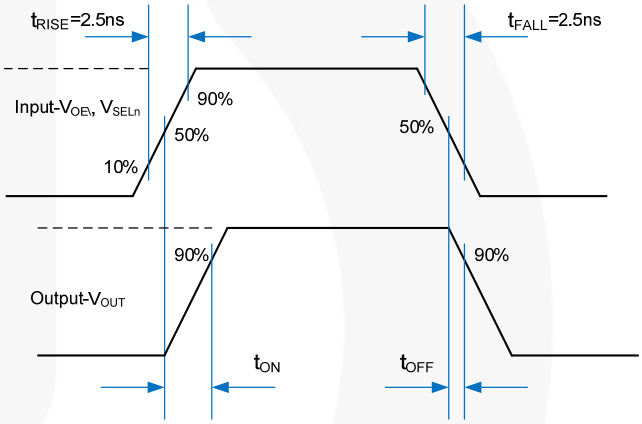


Figure 8. Turn-On / Turn-Off Waveforms

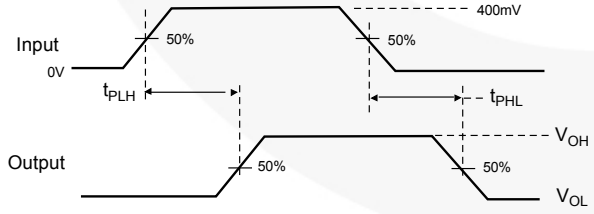


Figure 9. Propagation Delay ($t_R t_F$ – 500ps)

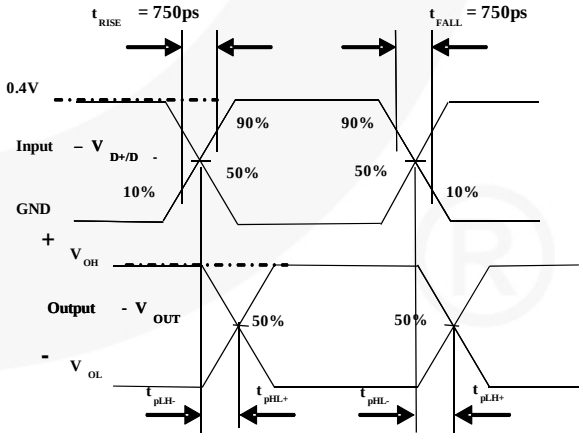
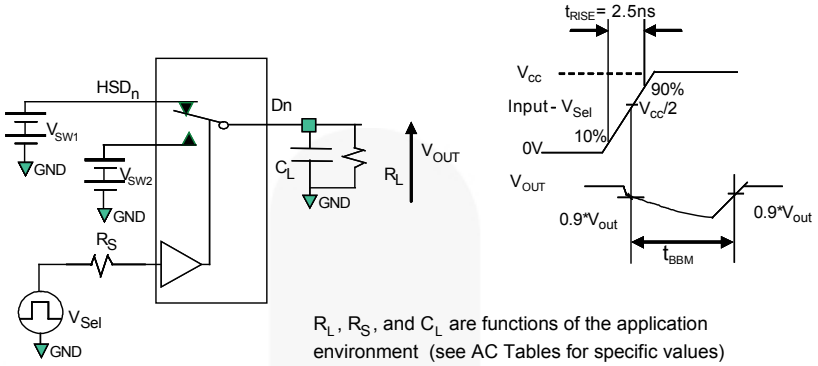


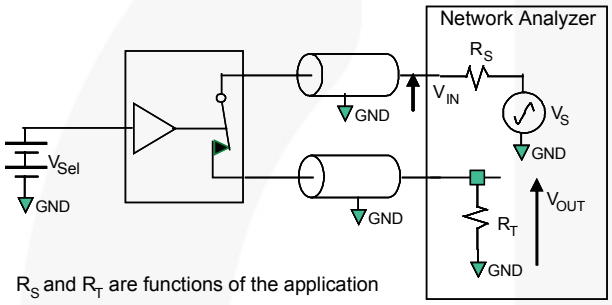
Figure 10. Skew Test Waveforms
$t_{SK(P)}$ = | $t_{PLH-} - t_{PHL-}$ | or | $t_{PLH+} - t_{PHL+}$ |
$t_{SK(I)}$ = | $t_{PLH-} - t_{PHL+}$ | or | $t_{PLH+} - t_{PHL-}$ |

Test Diagrams (Continued)



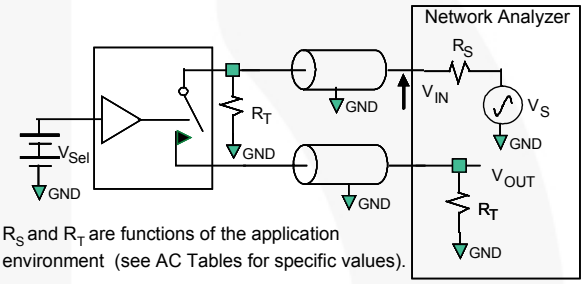
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 11. Break-Before-Make Interval Timing



R_S and R_T are functions of the application environment (see AC Tables for specific values).

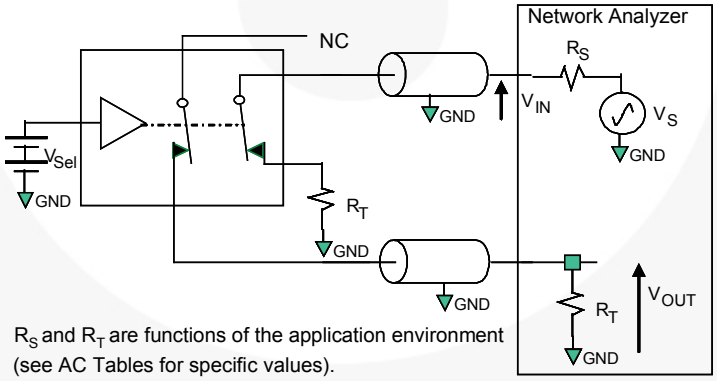
Figure 12. Bandwidth



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 13. Channel Off Isolation



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 14. Non-Adjacent Channel-to-Channel Crosstalk

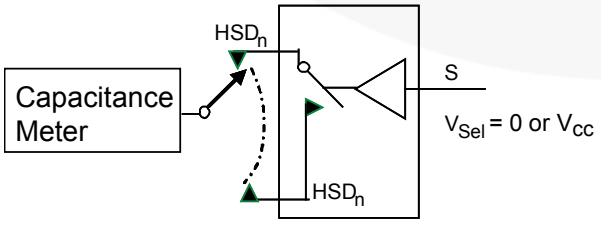


Figure 15. Channel Off Capacitance

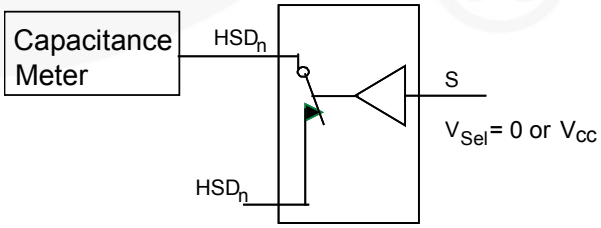
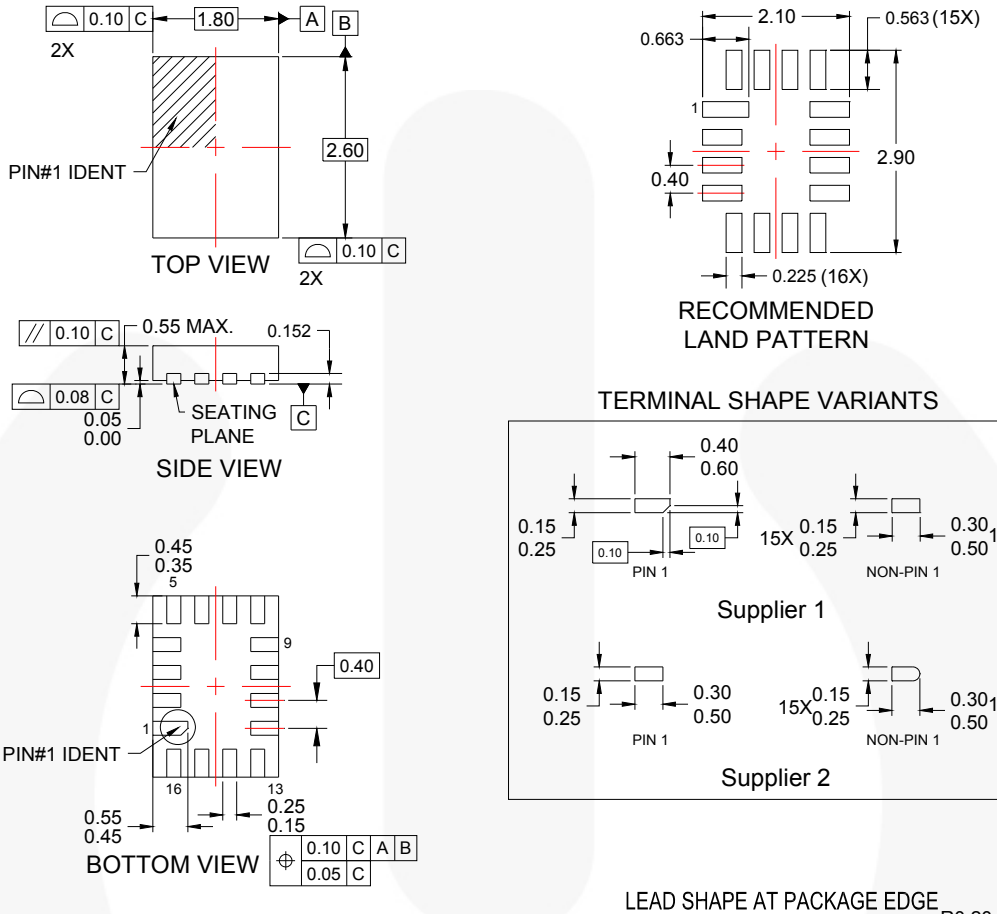


Figure 16. Channel On Capacitance

Physical Dimensions



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E. DRAWING FILENAME: MKT-UMLP16Arev4.
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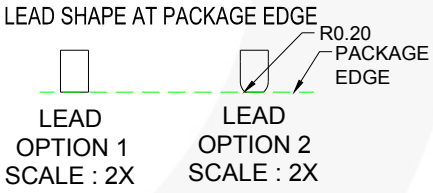

Figure 17. 16-Pin, Ultrathin Molded Leadless Package (UMLP)

Order Number	Operating Temperature Range	Package Description	Packing Method
FSUSB74UMX	-40 to 85°C	16-Terminal, Ultrathin Molded Leadless Package (UMLP)	Tape & Reel

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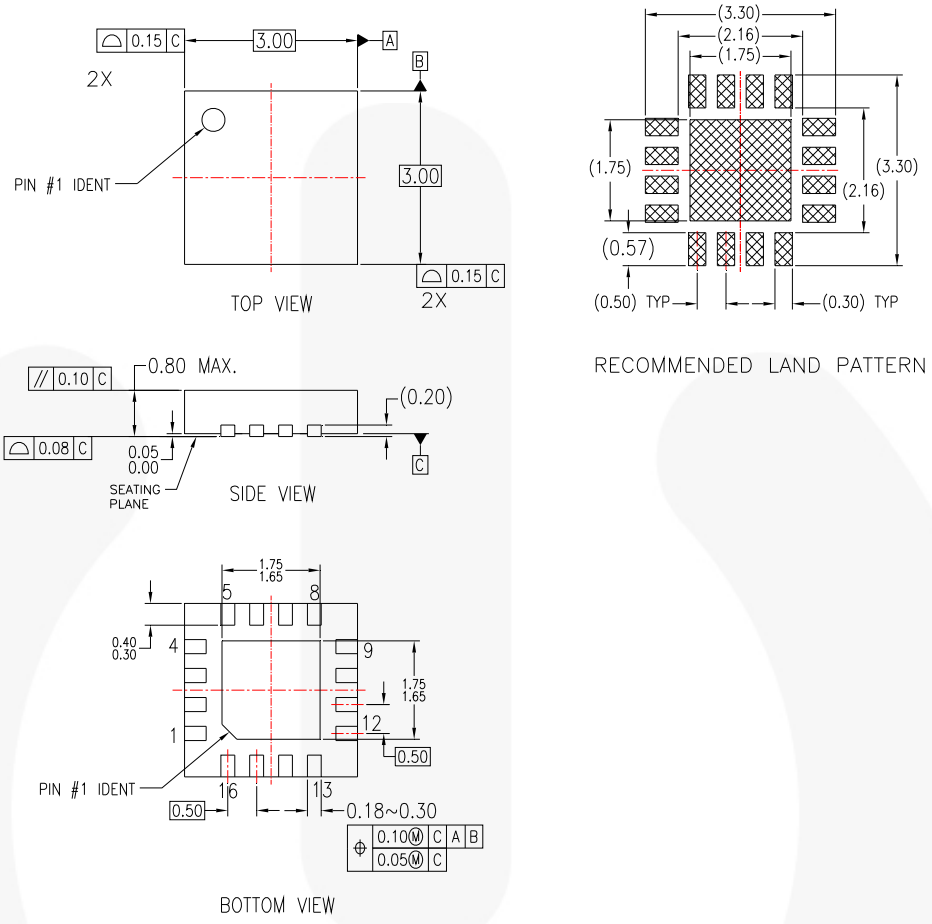
Physical Dimensions



NOTES:

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MLP16BrevB

Figure 18. 16-Lead, Quad Molded Leadless Package (MLP)

Order Number	Operating Temperature Range	Package Description	Packing Method
FSUSB74MPX	-40 to 85°C	16-Lead, Quad, Molded Leadless Package (MLP), 3mm x 3mm	Tape & Reel

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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