SIEMENS

ICs for Communications

3-Channel ISDN PC Adapter Circuit
3PAC

PSB 2113 Version 1.1

Product Overview 07.97

T2113-XV11-O1-7600

PSB 2113 Revision History:		Current Version: 07.97
Previous Version: None		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)

Edition 07.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL TS

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Table of Contents **Page**

1 Overview

The 3-Channel ISDN PC Adapter Circuit 3PAC integrates all B-channel and D-channel functions for a host based ISDN access solution on a single chip. Especially for U-interface applications only a transceiver needs to be connected to the 3PAC.
The 3PAC is pin compatible to the ISDN PC Adapter Circuit IPAC PSB 2115 which is a one chip solution featuring a 3 channel controller + S-interface.

It includes an HDLC controller for the D-channel and two protocol controllers for the B-channels. They can be used for HDLC protocol or transparent access. The system integration is simplified by several host interface configurations selected via pin strapping. They include multiplexed and demultiplexed interface options as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations.

The 3PAC combines the functions of the ISDN Communication Controller (ICC PEB 2070) and the High-Level Serial Communications Controller Extended (HSCX-TE PSB 21525) providing additional features and enhanced functionality.

The FIFO size of the B-channel buffers is 2x64 bytes per direction.

An auxiliary I/O port with interrupt capabilities on two input lines is available. These I/O lines may be used to connect a DTMF receiver or other peripheral components to the 3PAC which need software control or have to forward status information to the host. Peripheral data controllers can transfer data on a PCM interface which is mapped into the B-channels on the IOM-2 interface.

The 3PAC is produced in advanced CMOS technology.

SIEMENS

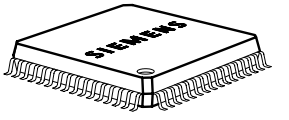
3-Channel ISDN PC Adapter Circuit 3PAC

PSB 2113

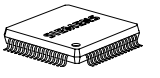
Version 1.1

CMOS

1.1 Features



P-MQFP-64



P-TQFP-64

- Integrates D-channel and B-channel protocol controller
- Replaces solutions based on ICC PEB 2070 and HSCX-TE PSB 21525
- Easy adjustment of software using ICC and HSCX-TE
- Pin compatible and software compatible to IPAC PSB 2115
- Various types of protocol support depending on operating mode (Non-auto mode, transparent mode)
- Efficient transfer of data blocks from/to system memory by DMA (for one B-channel) or interrupt request (for both B-channels)
- Enlarged FIFO buffers for B-channels (2x64 byte)
- FIFO buffers for D-channel (2x32 byte)
- Additional I/O interface with 2 interrupt inputs
- PCM interface for non IOM-2 compatible peripheral data controllers
- Reduced register address space due to indirect address mode option
- Programmable timer (1 ... 63 ms) for continuous or single interrupts
- 3 programmable LED outputs
- 8-bit multiplexed or demultiplexed bus interface
- Siemens/Intel or Motorola µP interface

Type	Ordering Code	Package
PSB 2113 H	Q67223 - H1057	P-MQFP-64 (SMD)
PSB 2113 F	Q67223 - H1058	P-TQFP-64 (SMD)

1.2 Logic Symbol

The logic symbol shows all functions of the 3PAC. It must be noted, that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.

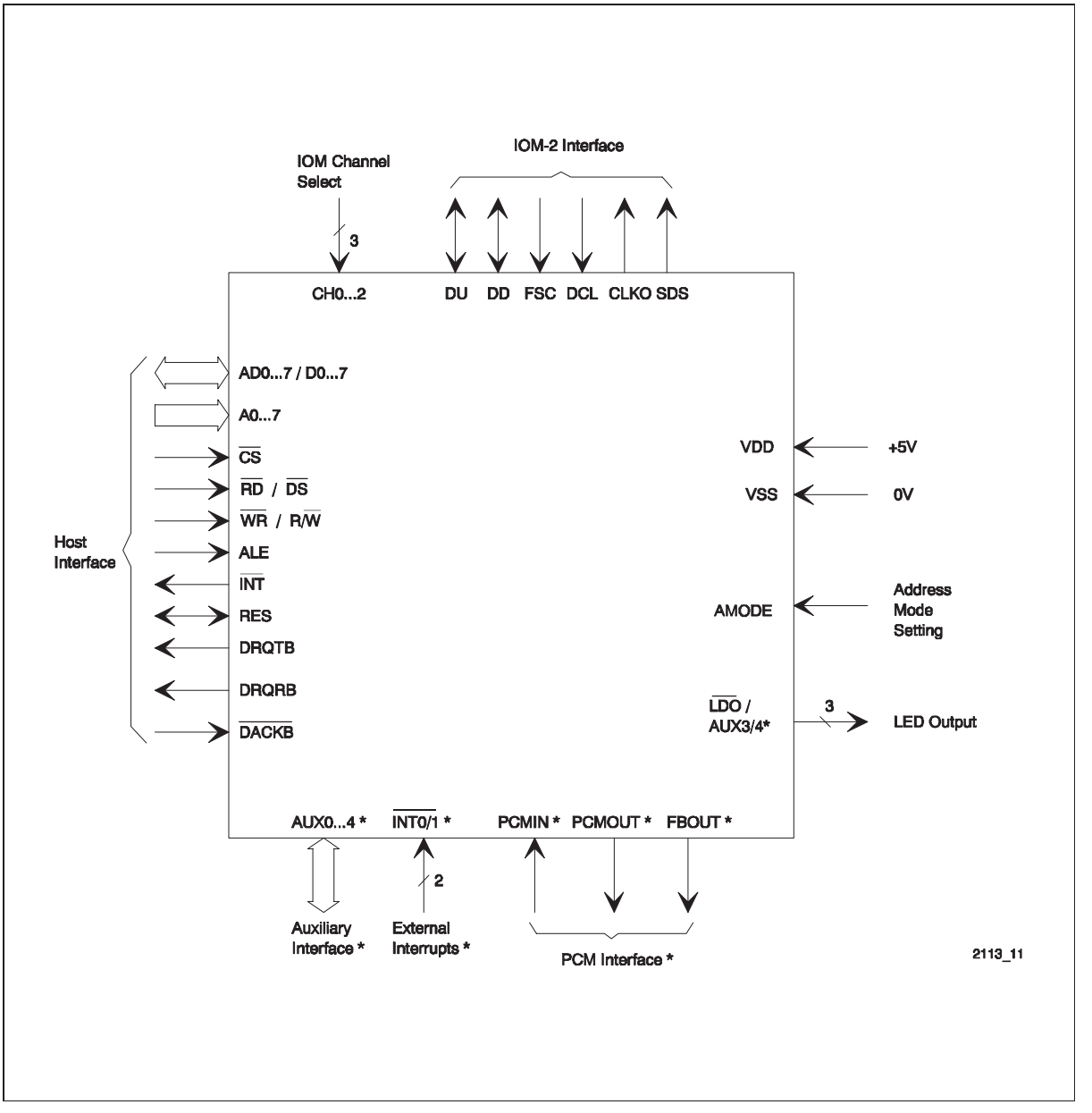


Figure 1
Logic Symbol

1.3 Pin Configuration

Figure 2 shows the pin configuration for P-MQFP-64 and for P-TQFP-64 packages.

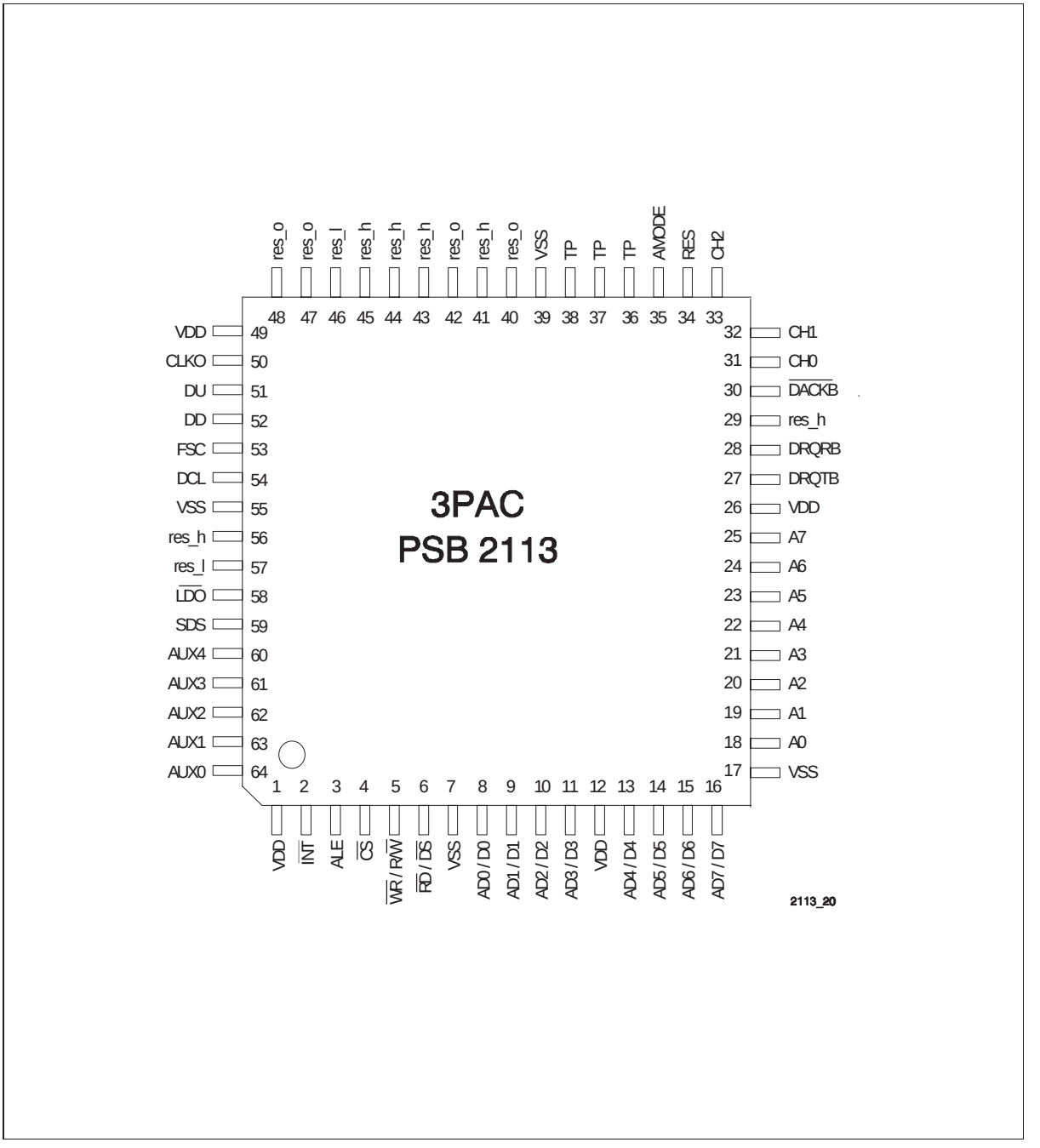


Figure 2
Pin Configuration

1.4 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Microprocessor Bus Interface			
8 9 10 11 13 14 15 16	AD0-7 D0...7	I/O I/O	**Multiplexed Bus Mode:** **Address/data bus** Transfers addresses from the host system to the 3PAC and data between the host system and the 3PAC. **Non-Multiplexed Bus Mode:** **Data bus.** Transfers data between the host system and the 3PAC.
18 19 20 21 22 23 24 25	A0-A7	I	**Non-Multiplexed Bus Mode:** Address bus transfers addresses from the host system to the 3PAC. For indirect address mode only A0 is valid. **Multiplexed Bus Mode** Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD.
6	$\overline{RD}$ $\overline{DS}$	I I	**Read** Indicates a read access to the registers (Intel bus mode). **Data Strobe** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
5	$\overline{WR}$ R/$\overline{W}$	I I	**Write** Indicates a write access to the registers (Intel bus mode). **Read/Write** A high level identifies a valid host access as a read operation and a low level identifies a valid host access as a write operation (Motorola bus mode).
4	$\overline{CS}$	I	**Chip Select** A LOW on this line selects the 3PAC for a read/write operation.

Pin No.	Symbol	Input (I) Output (O)	Function
3	ALE	I	**Address Latch Enable** A HIGH on this line indicates an address on the external address/data bus (multiplexed bus type only). ALE also selects the microprocessor interface type (multiplexed or non multiplexed).
2	$\overline{\text{INT}}$	OD	**Interrupt Request** This signal is activated when the 3PAC requests an interrupt. It is an open drain output.
34	RES	I/O	**Reset** A HIGH on this input forces the 3PAC into a reset state. The minimum pulse length is four DCL-clock periods (if oscillator clock is settled) or four ms (if oscillator is not yet settled). If the terminal specific functions are enabled, the 3PAC may also supply a reset signal.
27	DRQTB	O	**DMA Request Transmitter** (channel B) The transmitter of the 3PAC requests DMA data transfer by activating this line. The DRQTB remains HIGH as long as the transmit FIFO requires data transfer. The amount of data bytes to be transferred from system memory to the 3PAC (= byte count) must be written first to the XBCH, XBCL register. Always blocks of data (n x 64 bytes + REST, n=0, 1, ..) are transferred till the byte count is reached. DRQTB is deactivated immediately following the falling edge of the last $\overline{\text{WR}}$ cycle.
28	DRQRB	O	**DMA Request Receiver** (channel B) The receiver of the 3PAC requests DMA data transfer by activating this line. The DRQRB remains HIGH as long as the receive FIFO requires data transfer, thus always blocks of data (64, 32, 16, 8 or 4 bytes) are transferred. DRQRB is deactivated immediately following the falling edge of the last read cycle.

Pin No.	Symbol	Input (I) Output (O)	Function
30	$\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel B) When LOW, this input signal from the DMA controller indicates to the 3PAC, that the requested DMA cycle controlled via DRQTB and DRQRB is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with $\overline{\text{RD}}$, if DMA has been requested from the receiver, or with $\overline{\text{WR}}$, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If $\overline{\text{DACKB}}$ is active, the input on pins A0-7 is ignored and the FIFO's are implicitly selected. If the $\overline{\text{DACKB}}$ signals are not used, these pins must be connected to VDD.

Auxiliary Interface

64	AUX0	I/O	• **PCM interface enabled:** **FBOUT (output) - FSC/BCL Output** This pin is programmable to output either an FSC clock which is derived from the DCL input divided by 192 or a single bit clock from the IOM-2 interface, especially to serve non IOM-2 compatible peripheral devices on the PCM interface. • **PCM interface disabled:** **AUX0 (input/output)** If the PCM interface is switched off, this pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.

Pin No.	Symbol	Input (I) Output (O)	Function
63	AUX1	I/O	• **PCM interface enabled:** **PCMIN (input) - PCM Data Input** On this line the 3PAC receives 8-bit data, which is transmitted from a peripheral device. This data is mapped to a B-channel timeslot on IOM-2. • **PCM interface disabled:** **AUX1 (input/output)** If the PCM interface is switched off, this pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.
62	AUX2	I/O	• **PCM interface enabled:** **PCMOUT (output) - PCM Data Output** On this line the 3PAC transmits 8-bit data, which is received by a peripheral device. This data is taken from a B-channel timeslot on IOM-2. • **PCM interface disabled:** **AUX2 (input/output)** If the PCM interface is switched off, this pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.
61 62	AUX3 AUX4	I/O	**$\overline{\text{INT0/1}}$** These pins are programmable as general input/output. The state of the pins can be read from (input) / written to (output) a register. Additionally, as inputs they can generate a maskable interrupt to the host, which is either edge or level triggered. An internal pull up resistor is connected to these pins. As outputs an LED with pre-resistance can directly be connected to these pins.

Pin No.	Symbol	Input (I) Output (O)	Function
IOM-2 Interface			
53	FSC	I	**Frame Sync** Synchronisation signal. The rising edge indicates the beginning of the IOM frame (HIGH during channel 0).
54	DCL	I	**Data Clock** IOM clock signal of twice the IOM data rate. Rising edge is used to transmit data, 2nd falling edge is used to sample data.
51	DU	I/O(OD)	**Data Upstream** IOM data signal in upstream direction.
52	DD	I/O (OD)	**Data Downstream** IOM data signal in downstream direction.
50	CLKO	O	**Clock Output** At pin CLKO a clock equal to DCL/2 is provided.
59	SDS	O	**Serial Data Strobe** Programmable strobe signal, selecting either one or two channels (8 or 16 bit strobe length) on the IOM-2 or PCM interface.
General Control Functions			
35	AMODE	I	**Address Mode** Selects between direct and indirect register access. A HIGH selects indirect address mode and a LOW selects the direct register access.
31	CH0	I	**IOM-2 Channel Select 0** Together with CH1 and CH2, this pin selects one of eight channels on the IOM-2 interface.
32	CH1	I	**IOM-2 Channel Select 1** Together with CH0 and CH2, this pin selects one of eight channels on the IOM-2 interface.
33	CH2	I	**IOM-2 Channel Select 2** Together with CH0 and CH1, this pin selects one of eight channels on the IOM-2 interface.

Pin No.	Symbol	Input (I) Output (O)	Function
58	$\overline{\text{LDO}}$	O	**LED Output** This pin functions as a programmable output. An LED with pre-resistance may directly be connected to $\overline{\text{LDO}}$.

Power Supply

1 12 26 49	VDD	I	**Power Supply Voltage** +5V (+/- 5%)
7 17 39 55	VSS	I	**Ground**, 0V

Reserved Pins

36 37 38	TP	I	**Test Pins** These pins are not used for normal operation. They must be connected to GND.
29 41 43 44 45 56	res_h	I	**Reserved High** These pins must be connected to VDD.
46 57	res_l	I	**Reserved Low** These pins must be connected to VSS.
40 42 47 48	res_o	O	**Reserved Open** These pins may be left not connected.

Note: OD = Open Drain

1.5 Functional Block Diagram

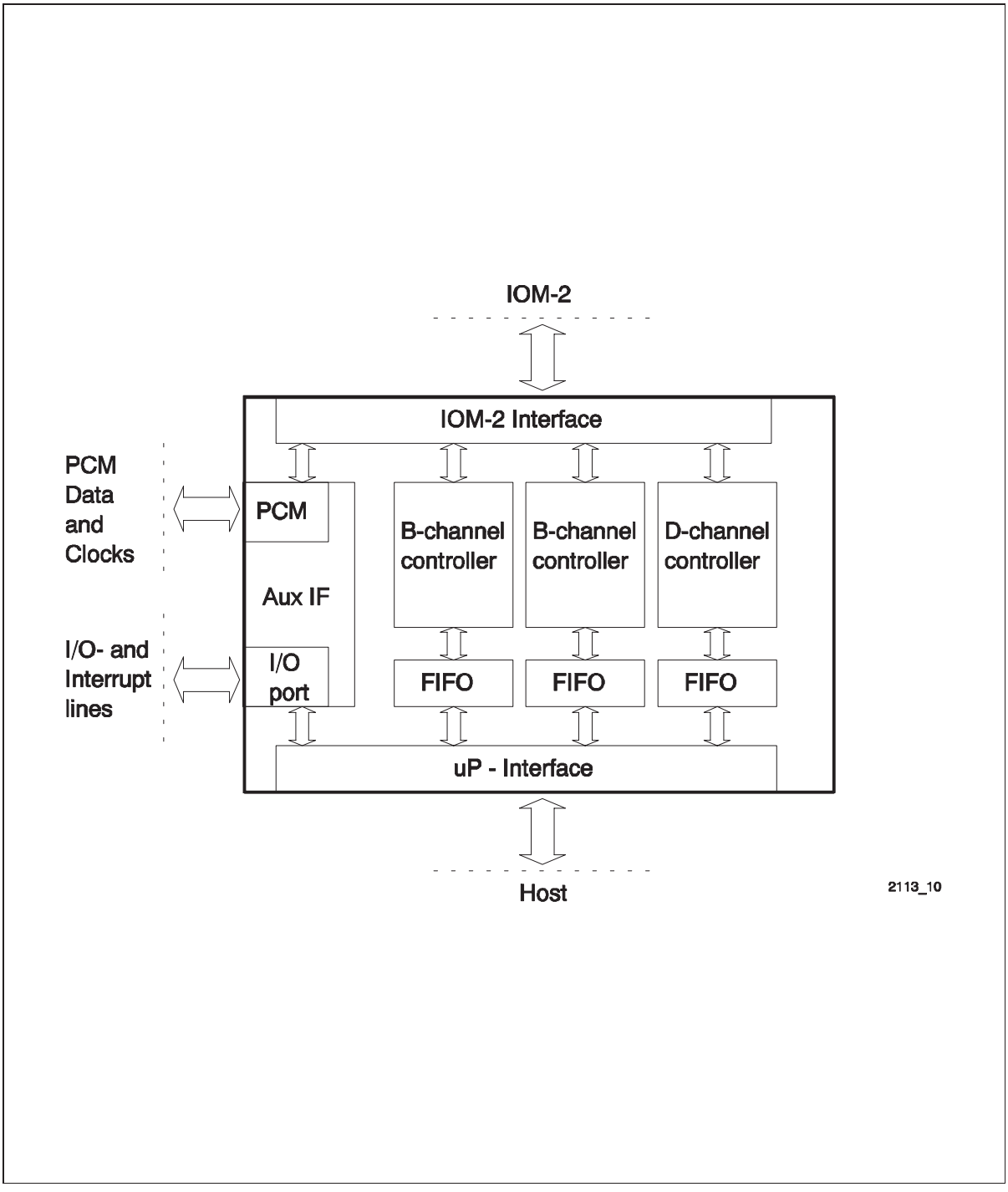


Figure 3
Block Diagram

1.6 System Integration

The 3PAC is suited for all host based applications.

ISDN PC Adapter Card for U Interface

An ISDN adapter card which supports the U interface (2B1Q line coding), especially required in the Northamerican market, may be realized using the 3PAC together with the PSB 21911 IEC-Q TE (**figure 4**). The 3PAC provides two B-channel HDLC controllers and another controller for the D-channel access.

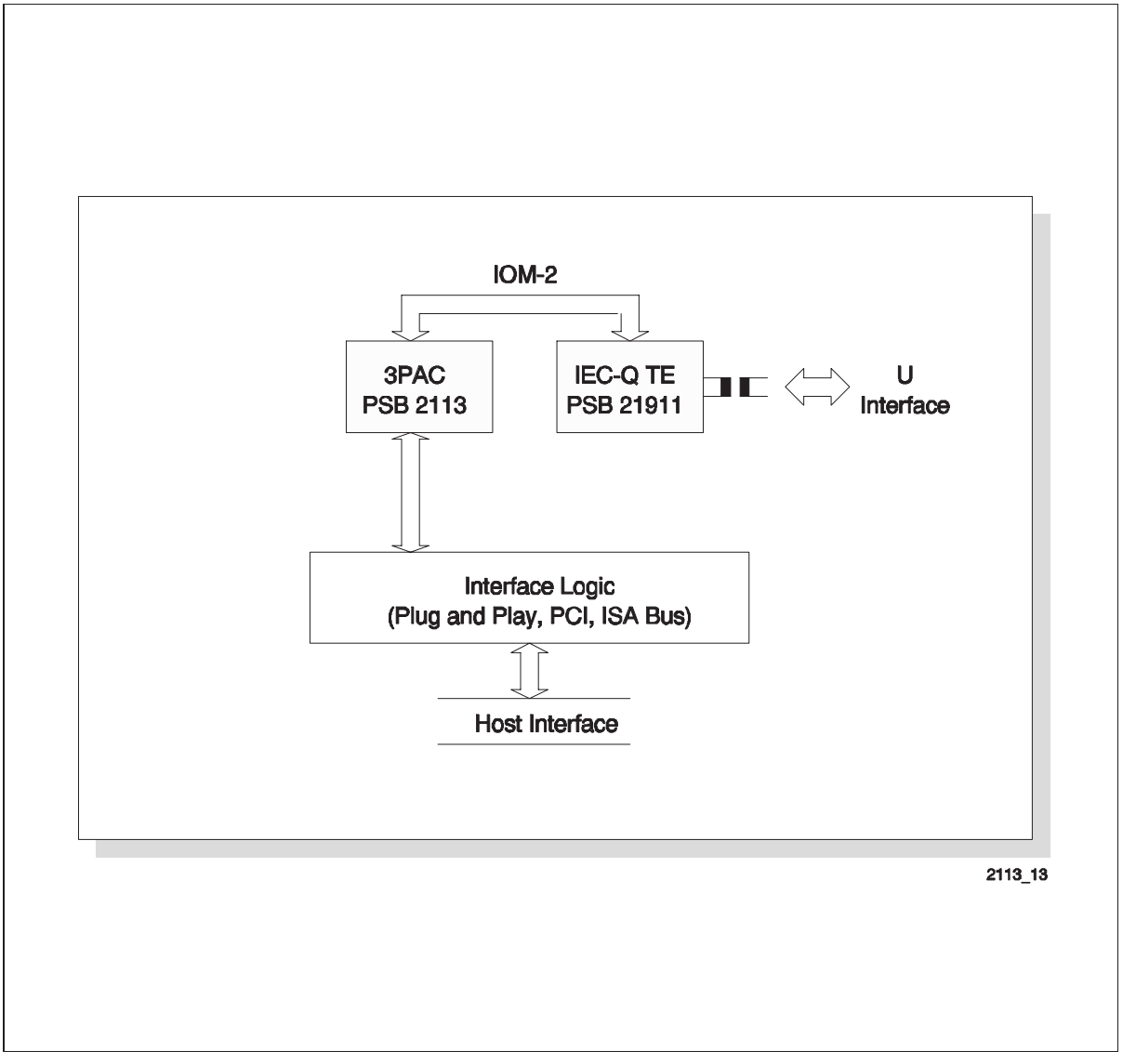


Figure 4
ISDN PC Adapter Card for U Interface (2B1Q)

ISDN Voice/Data Terminal

Figure 5 shows a voice data terminal developed on a PC card, where the 3PAC provides its functionality as a data controller within a three chip solution. During ISDN calls the ARCOFI-SP PSB 2163 provides for speakerphone functions and includes a DTMF generator. Additionally, a DTMF receiver or keypad may be connected to the auxiliary interface of the 3PAC.

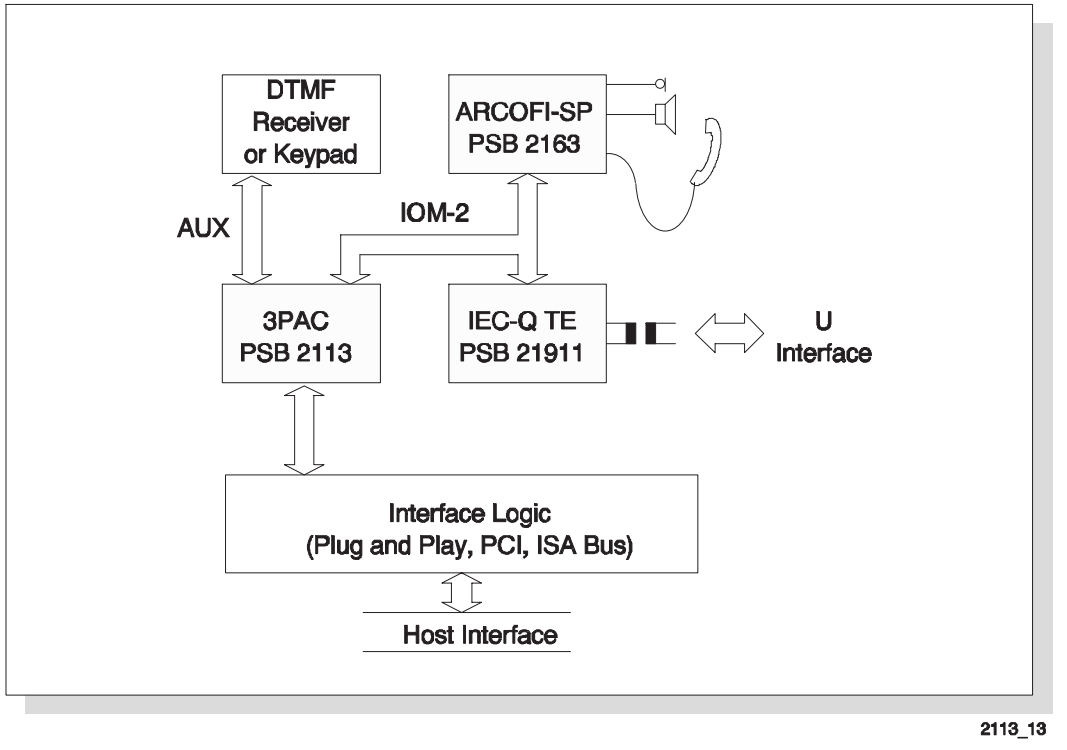


Figure 5
ISDN Voice/Data Terminal

ISDN Stand-alone Terminal with POTS interface

The 3PAC can be integrated in a microcontroller based stand-alone terminal (**figure 6**) that is connected to the communications interface of a PC. The SICOFI2-TE PSB 2132 enables connection of analog terminals (e.g. telephones or fax) to its dual channel POTS interface.

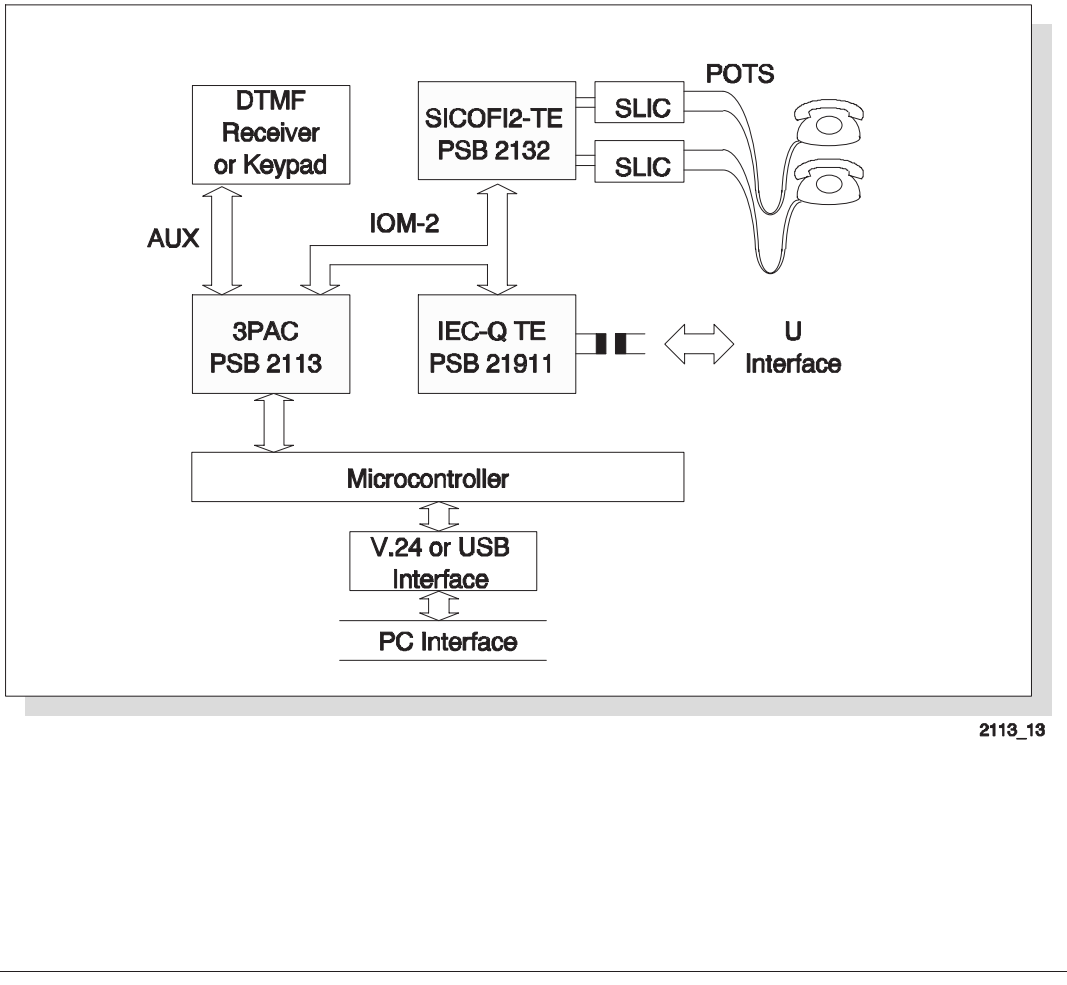


Figure 6
ISDN Stand-alone Terminal with POTS Interface

Multiline PC-Adapter

Three U-interfaces can be combined via the IOM-2 interface using the PCM interface of the 3PAC to transfer data in 6 B-channels. All three 3PACs exchange user data with the data controller (e.g. a videocodec) via the PCM interface. The IEC-Q PEB 2091 is configured to NT-PBX mode and an external PLL generates the FSC and DCL clocks for all devices connected to the IOM-2 interface. The U-transceivers are programmed via the IOM-2 MONITOR channel (as shown in **figure 7**) or via the parallel host interface.

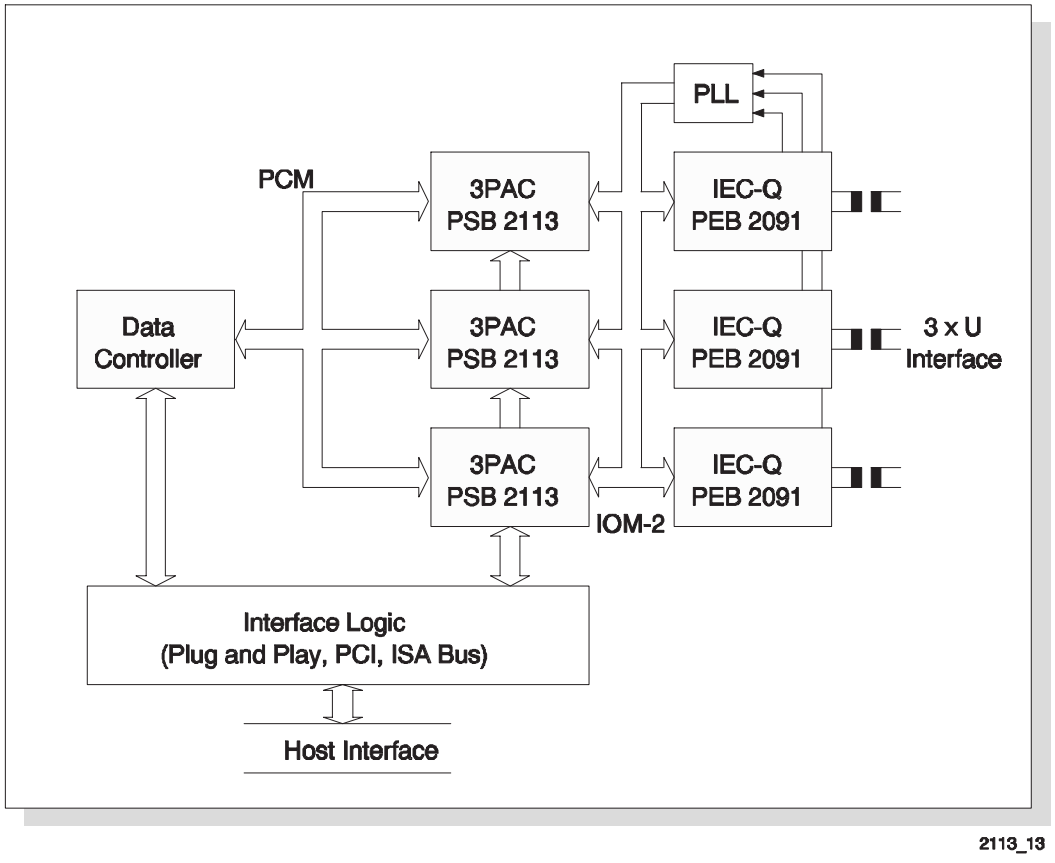


Figure 7
Multiline PC-Adapter

2 Functional Description

The 3-Channel ISDN PC Adapter Circuit 3PAC provides reduced functionality compared with the well known IPAC PSB 2115. The S-transceiver is omitted, however besides the layer-1 part the 3PAC provides the same functionality.

This specification provides an overview on the functional blocks of the 3PAC, a detailed description of these functional blocks can also be found in the data sheet of the IPAC PSB 2115.

2.1 Operating Modes

The HDLC controller of each B-channel and of the D-channel can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies most requirements.

There are 4 different operating modes for the B-channels which can be set via the MODEB register:

- Non-Auto Mode (MODEB: MDS1, MDS0 = 01)
- Transparent Mode 1 (MODEB: MDS1, MDS0, ADM = 101)
- Transparent Mode 0 (MODEB: MDS1, MDS0, ADM = 100)
- Extended Transparent Modes 0; 1 (MODEB: MDS1, MDS0 = 11)

5 different modes which are similar as for the B-channels can be set for the D-channel in the MODED register:

- Auto mode (MODED: MDS2, MDS1 = 00)
- Non-Auto Mode (MODED: MDS2, MDS1 = 01)
- Transparent Mode 1 (MODED: MDS2, MDS1, MDS0 = 101)
- Transparent Mode 0 (MODED: MDS2, MDS1, MDS0 = 110)
- Transparent Mode 0 (MODED: MDS2, MDS1, MDS0 = 111)

The D-channel controller supports S/G-bit (stop/go) evaluation and the TIC bus access mechanism if more than one D-channel source is connected.

Two C/I channel handler are used to convey commands and indications between the layer-2 function and a layer-1 device (C/I0) and to exchange real time status information between the 3PAC and various non layer-1 devices (C/I1).

The MONITOR channel handler is used for information exchange between the 3PAC and other devices attached to the IOM-2 interface.

2.2 Host Interface

2.2.1 Register Set

The communication between the host and the 3PAC is done via a set of directly or indirectly accessible 8-bit registers. The host sets the operating modes, controls function sequences and gets status information by writing or reading these registers (Command/ Status transfer).
Each of the two B-channels of the 3PAC is controlled via an equal, but totally independent register file (channel A and channel B). Additional registers are available for D-channel control, the PCM and the Auxiliary interface.

2.2.2 Data Transfer Mode

Data transfer between the system memory and the 3PAC for both transmit and receive direction is controlled by either interrupts (Interrupt Mode), or independently from host interaction using the 3PAC's 2-channel DMA interface (DMA Mode).

After RESET, the 3PAC operates in Interrupt Mode, where data transfer must be done by the host. The user selects the DMA Mode by setting the DMA bit in a register.

Only channel B can be operated either in Interrupt or DMA mode, channel A can only be operated in Interrupt mode.

2.2.3 Interrupt Interface

Special events in the 3PAC are indicated by means of a single interrupt output, which requests the host to read status information from the 3PAC or transfer data from/to the 3PAC.

Since only one $\overline{\text{INT}}$ request output is provided, the cause of an interrupt must be determined by the host reading the 3PAC's interrupt status registers.

The structure of the interrupt status registers is shown in **figure 8**.

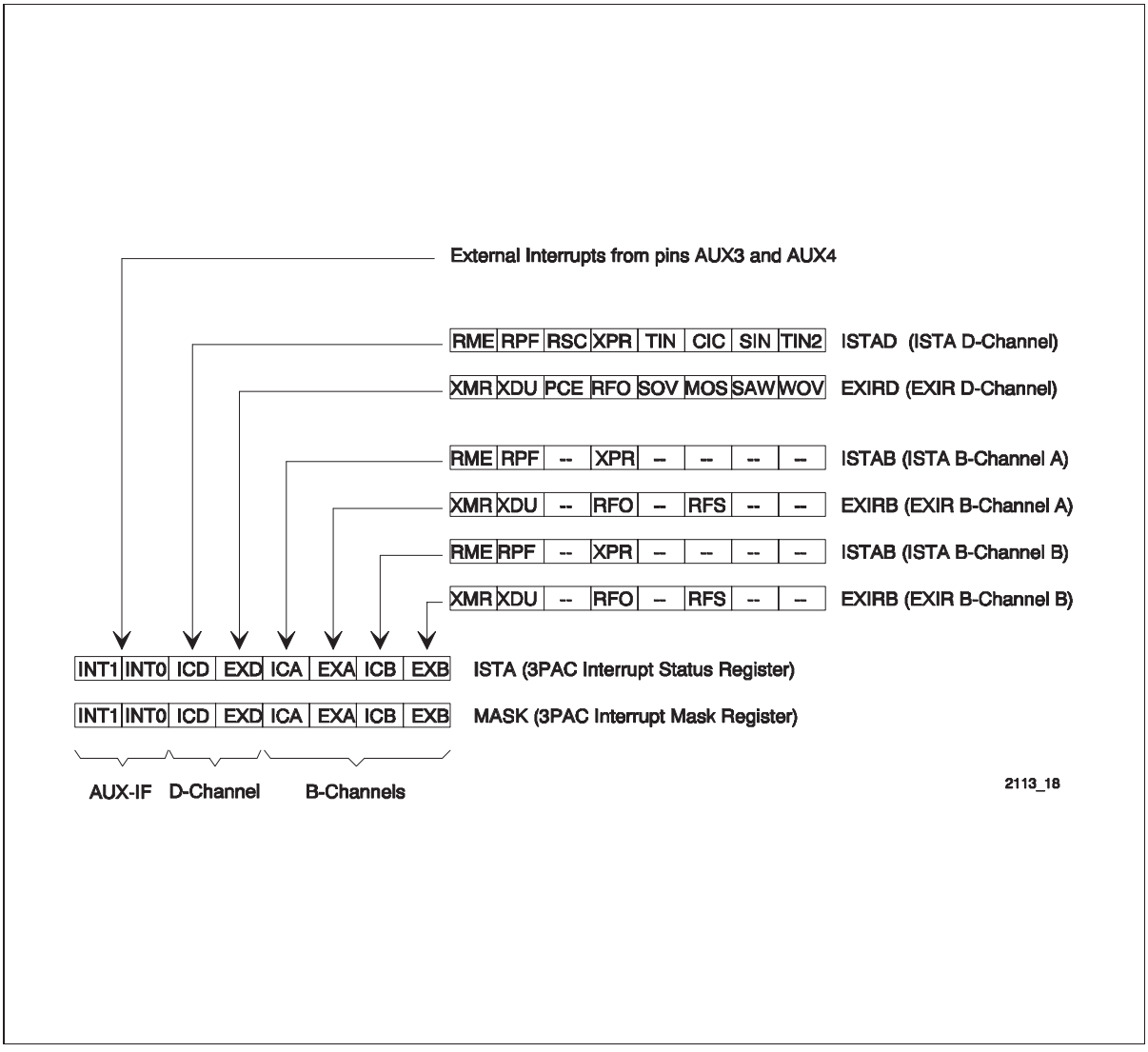


Figure 8
3PAC Interrupt Status Registers

Two interrupt indications can be read directly from the ISTA register and another six interrupt indications from separate interrupt status registers and extended interrupt registers for the B-channels (ISTAA, EXIRA, ISTAB, EXIRB) and the D-channel (ISTAD, EXIRD).

After the 3PAC has requested an interrupt by setting its $\overline{INT}$ pin to low, the host must first read the 3PAC interrupt status register (ISTA) in the associated interrupt service routine. The six lowest order bits (bit 5-0) of ISTA (ICD, EXD, ICA, EXA, ICB, EXB) point to those registers in which the actual interrupt source is indicated. It is possible that several interrupt sources are indicated referring to one interrupt request (e.g. if the ICA bit is set, at least one interrupt is indicated in the ISTA register of channel A).

An interrupt source from the general I/O pins AUX3 and AUX4 of the auxiliary interface is directly indicated in bits 6 and 7 of the ISTA register, therefore these bits must always be checked.

The $\overline{INT}$ pin of the 3PAC remains active until all interrupt sources are cleared by reading the corresponding interrupt register. Therefore it is possible that the $\overline{INT}$ pin is still active when the interrupt service routine is finished.

For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF_H into the MASK register) and write back the old mask to the MASK register.

Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register. Masked interrupt status bits are not indicated when the status register is read, but they remain internally stored and pending until the mask bit is reset.

2.2.4 DMA Interface

The 3PAC comprises a 2-channel DMA interface (B-channel B with receive and transmit direction) for fast and effective data transfer.

A separate DMA Request Output for transmit (DRQTB) and receive direction (DRQRB) as well as a DMA Acknowledgment ($\overline{\text{DACKB}}$) input is provided.

The 3PAC activates the DRQRB line as long as data transfer is needed from/to the specific FIFO (level triggered demand transfer mode of DMA controller).

It's the responsibility of the DMA controller to perform the correct amount of bus cycles. Either read cycles will be performed if the DMA transfer has been requested from the receiver, or write cycles if DMA has been requested from the transmitter. If the DMA controller provides a DMA acknowledge signal (input to the 3PAC's $\overline{\text{DACKB}}$ pin), each bus cycle implicitly selects the top of the FIFO and neither address (via A0-A6) nor chip select need to be supplied (I/O to memory transfers). If no $\overline{\text{DACKB}}$ signal is supplied, normal read/write operations (providing addresses) must be performed (memory to memory transfers).

The 3PAC deactivates the DRQRB line immediately after the last read/write cycle of the data transfer has started.

2.2.5 Host Interface Operation

The 3PAC is programmed via an 8-bit parallel microprocessor interface. Easy and fast microprocessor access is provided by 8-bit address decoding on the chip.

At the 3PAC three types of µP buses are provided (see table 1), which are selected via pin ALE:

Table 1
Bus Operation Modes

(1)	ALE tied to V_{DD}	**Motorola** type with control signals **$\overline{CS}$, R/$\overline{W}$, $\overline{DS}$**
(2)	ALE tied to V_{SS}	**Siemens/Intel non-multiplexed** bus type with control signals **$\overline{CS}$, $\overline{WR}$, $\overline{RD}$**
(3)	Edge on ALE	**Siemens/Intel multiplexed** address/data bus type with control signals **$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE**

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

Note: If the multiplexed address/data bus type (3) is selected, the unused address pins A0-A7 must be tied to V_{DD}.

Register Addressing Modes

The 3PAC provides two different ways to read and write its registers. The common way is for non-multiplexed mode to set the register address to the address bus and then access the register location. In multiplexed mode, the address on the address/data bus is latched in, before a read or write access to the register is performed. This mode is selected, if the address select mode pin AMODE is set to 0.

As a second option, the 3PAC allows for indirect access of the registers (AMODE=1). Only the LSB (A0) of the address line is used to select either the ADDRESS register or the DATA register. The host writes the register address to the ADDRESS register, before it reads/writes data from/to the corresponding register location through the DATA register. **Figure 9** shows both register addressing modes.

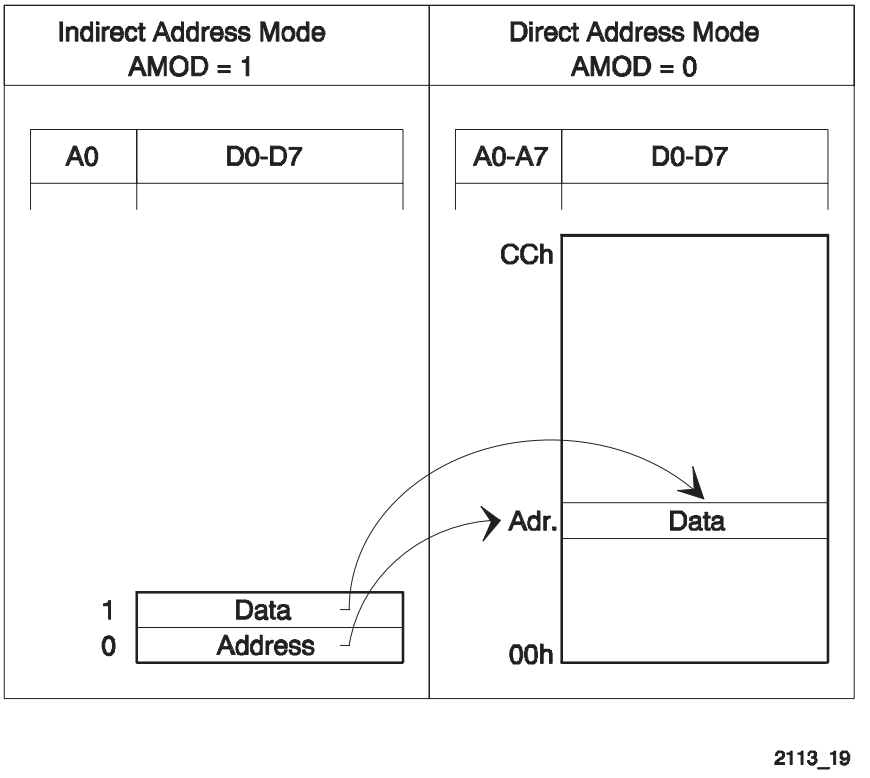


Figure 9
Indirect register address mode

2.3 Auxiliary Interface

The AUX interface provides for various, programmable functions (see **table 2**).

Two PCM receive and transmit lines are available for connection to other data controllers (e.g. datapump, video processor). In this way non IOM compatible devices with standard PCM interface can operate on any timeslot on the IOM-2 interface. A BCL output or FSC output (for IOM-2 frame sync signal) is available which is derived from the DCL input by an internal divider.
The PCM interface can be disabled, so AUX0-2 are available as general purpose I/O pins. Two pins INT0 and INT1 can be used as programmable I/O with optional interrupt input capability.

Table 2
AUX pin functions

Pin	Function
AUX0	AUX0 / FBOUT
AUX1	AUX1 / PCMIN
AUX2	AUX2 / PCMOUT
AUX3	$\overline{\text{INT0}}$
AUX4	$\overline{\text{INT1}}$

AUX0-2

These pins can be used as programmable I/O lines. This function is multiplexed with the PCM interface, i.e. the host can select either PCM functionality or standard I/O characteristic on AUX0-2.

As inputs the state at the pin is latched in when the host performes a read operation.

As outputs the value of the corresponding register is driven on the pins with a minimum delay after the write operation to this register is performed. They can be configured as open drain or push/pull outputs.

$\overline{\text{INT0}}$, $\overline{\text{INT1}}$

Two pins can be used as programmable I/O lines with optional interrupt input capability.

The $\overline{\text{INT0/1}}$ pins are general input or output pins like AUX0-2 (see description above).
In addition to that, as inputs they can generate an interrupt to the host which is maskable. The interrupt input is either edge or level triggered.
As outputs both pins are able to sink I_{OL}= 5 mA which allows for direct connection of LEDs in standalone applications for example.

PCMIN, PCMOUT

PCMIN and PCMOUT are receive and transmit lines of the general PCM interface. If enabled, the B-channels on the IOM-2 interface can flexibly be switched to any timeslot of the PCM interface.

If the PCM Interface is not used, these pins serve as general I/O pins.

FBOUT (FSC/BCL Output)

This pin can be programmed to one of two possible functions:

- FSC Output:
  An FSC clock is output which is derived from the DCL input divided by 192. This is especially suitable for multiline applications, where one of several IPACs generates the common FSC.
- BCL Output:
  The pin can output a single bit clock (DCL input divided by 2) equal to the IOM-2 data rate, especially to serve non IOM-2 compatible peripheral devices on the PCM interface.

If the PCM Interface is not used, this pin serves as a general I/O pin.

2.4 PCM Interface

The 3PAC provides a PCM interface that can be disabled, so that the PCM pins can be used as general I/O pins (see previous **chapter 2.3**).

Through its standard PCM interface the 3PAC can be connected to devices in general TDM (time division multiplex) systems. In this way data controllers, which are not IOM-2 compatible, can indirectly be connected to the IOM-2 interface, since the programmed PCM timeslots are reflected in the corresponding IOM-2 B-channel timeslots.

The data and signal lines to be used with the PCM interface depend on the mode of operation and the type of interface of the external device:

PCMIN	Receive Data: The 3PAC receives data from a peripheral device on PCMIN. The received data is then mapped to a B-channel on the IOM-2 interface.
PCMOUT	Transmit Data: The 3PAC transmits data to a peripheral device on PCMOUT. This data is originated from a B-channel on the IOM-2 interface.
FSC	Frame Sync: FSC is used on the IOM-2 interface to indicate the beginning of a new IOM-2 frame. It is also used for the PCM interface to mark the beginning of new frame.
DCL	Bit Clock (double rate): DCL is the reference clock according to which data is written to PCMOUT and read from PCMIN. For peripheral devices supporting double rate bit clock, the clock signal is directly provided by the system. DCL is the same clock as used for the IOM-2 interface.
BCL (FBOUT)	Bit Clock (single rate): For peripheral devices supporting single rate bit clock, the clock signal is provided at FBOUT. It is derived from the system clock by an internal divider (division by 2).
FSC (FBOUT)	Frame Sync: The frame sync signal is multiplexed with BCL (see above) and output at FBOUT. It is derived from the system clock by an internal divider (division by 192).

The frame sync signal FSC and the data clock DCL which are used on the IOM-2 interface also serve as the reference clocks on the PCM interface.

The PCM interface can be used to build a connection between non IOM-2 compatible voice/data controllers and the IOM-2 interface in order to transfer B-channel data from/ to the external device. Receive data on the DD line can be mapped to any timeslot on the PCMOUT line. Data received from the external device on any timeslot on PCMIN can be mapped to the DU line (see **figure 10**).
Data which is received on PCMIN is forwarded to the DU line with the next IOM-2 frame. Similar for the opposite direction, data on DD is forwarded to the PCMOUT line with the next FSC frame.

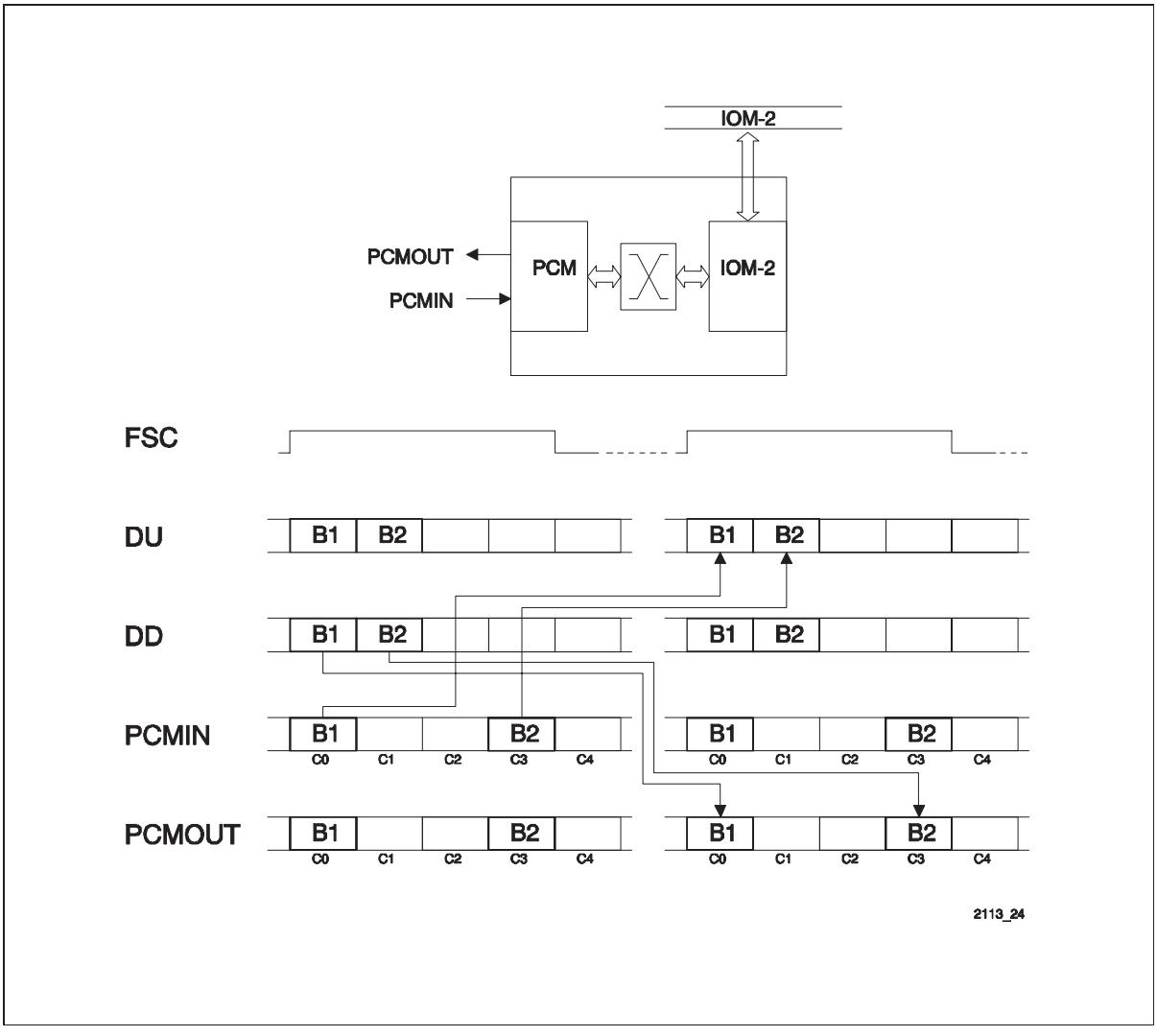


Figure 10
Switching Data between PCM and IOM-2

For test purposes data on PCMIN can be mapped to DD and B-channel data on DU can be mapped to PCMOUT.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias:	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 150	°C
Voltage on any pin with respect to ground	V_S	– 0.3 to V_{DD} + 0.3	V
Maximum voltage on any pin	V_{max}	7	V

Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

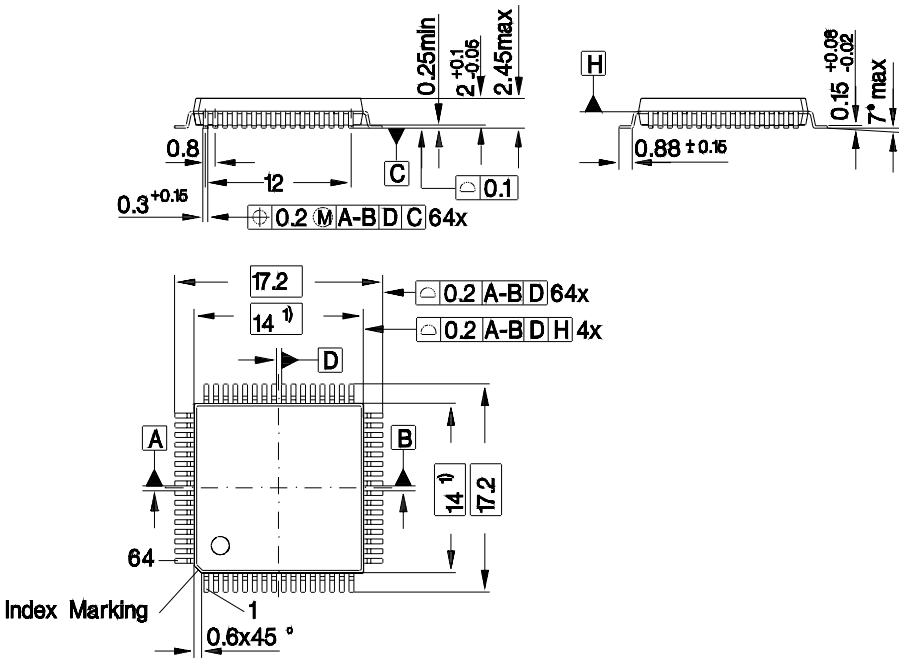
3.2 DC-Characteristics

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
L-input voltage	V_{IL}	-0.3	0.8	V	(all pins except XTAL1/2)
H-input voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
L-output voltage	V_{OL}		0.45	V	I_{OL}= 7 mA (DU, DD) I_{OL}= 5 mA ($\overline{LDO}$, AUX3, 4, AD0-7) I_{OL}= 2 mA (all others)
H-output voltage	V_{OH}	2.4		V	I_{OH}= - 5 mA (AD0-7) I_{OH}= - 400 µA (all others)
		V_{DD} - 0.5		V	I_{OH}= -100 µA
Power supply current - power down	I_{CC}		3	mA	V_{DD} = 5V, Inputs at V_{DD}/V_{DD} , No output loads, DCL = 1536 kHz
Power supply current - operational			19	mA	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

4 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)

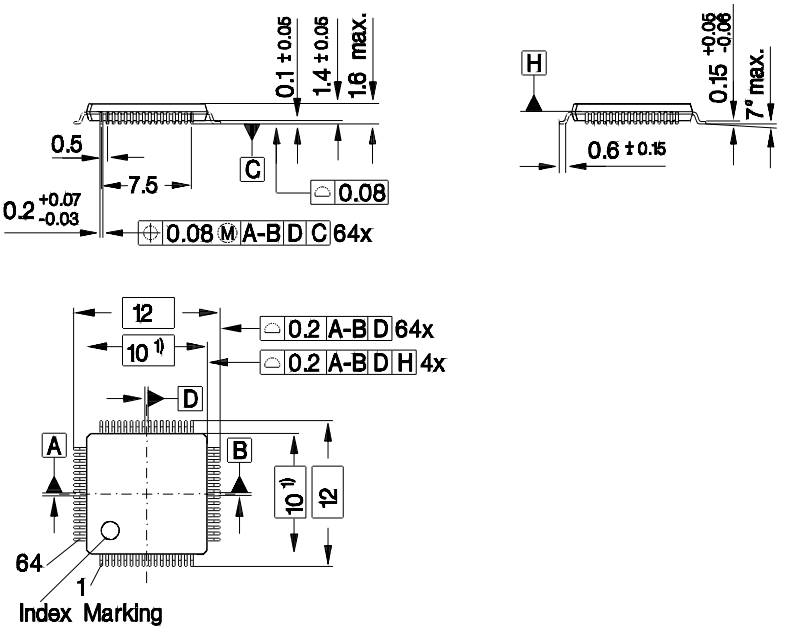


Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-64
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05613

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm