

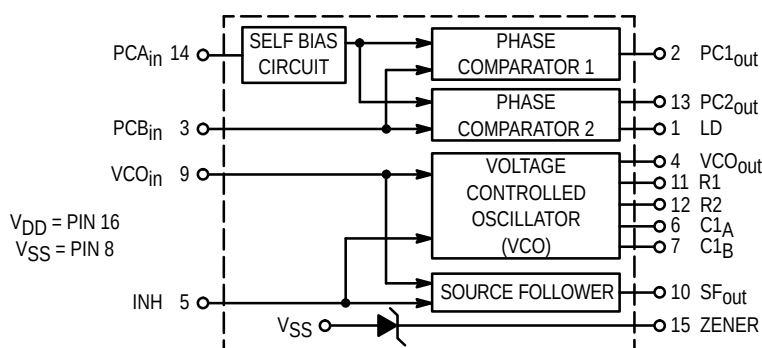
Phase Locked Loop

The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA_{in} and PCB_{in} . Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, $PC2_{out}$ and LD , and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1A$, $C1B$, $R1$, and $R2$. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh , when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

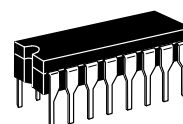
Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

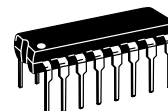
BLOCK DIAGRAM



MC14046B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT

LD	1	16	V_{DD}
$PC1_{out}$	2	15	ZENER
PCB_{in}	3	14	PCA_{in}
VCO_{out}	4	13	$PC2_{out}$
INH	5	12	R2
$C1A$	6	11	R1
$C1B$	7	10	SF_{out}
V_{SS}	8	9	VCO_{in}



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	– 0.5 to + 18	Vdc
Input Voltage, All Inputs	V _{in}	– 0.5 to V _{DD} + 0.5	Vdc
DC Input Current, per Pin	I _{in}	± 10	mAdc
Power Dissipation, per Package†	P _D	500	mW
Operating Temperature Range	T _A	– 55 to + 125	°C
Storage Temperature Range	T _{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	– 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage # (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	– 1.2	—	– 1.0	– 1.7	—	– 0.7	—	mAdc
		5.0	– 0.25	—	– 0.2	– 0.36	—	– 0.14	—	
		10	– 0.62	—	– 0.5	– 0.9	—	– 0.35	—	
		15	– 1.8	—	– 1.5	– 3.5	—	– 1.1	—	
	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) I _{nh} = PCA _{in} = V _{DD} , Zener = VCO _{in} = 0 V, PCB _{in} = V _{DD} or 0 V, I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current† (I _{nh} = "0", f ₀ = 10 kHz, C _L = 50 pF, R ₁ = 1.0 MΩ, R ₂ = ∞ R _{SF} = ∞, and 50% Duty Cycle)	I _T	5.0 10 15	I _T = (1.46 μA/kHz) f + I _{DD} I _T = (2.91 μA/kHz) f + I _{DD} I _T = (4.37 μA/kHz) f + I _{DD}							mAdc

#Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

† To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left(\frac{V_{COin} - 1.65}{R_1} + \frac{V_{DD} - 1.35}{R_2} \right)^{3/4} + 1.6 \times \left(\frac{V_{COin} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$

$$1 \times 10^{-1} V_{DD}^2 \left(\frac{100\% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_Q \quad \text{where: } I_T \text{ in } \mu A, C_L \text{ in pF, } V_{COin}, V_{DD} \text{ in Vdc, } f \text{ in kHz, and}$$

R₁, R₂, R_{SF} in MΩ, C_L on VCO_{out}.

ELECTRICAL CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Minimum	Typical	Maximum	Units
			Device		Device	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	— — —	180 90 65	350 150 110	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	100 50 37	175 75 55	ns

PHASE COMPARATORS 1 and 2

Input Resistance — PCA_{in}	R_{in}	5.0	1.0	2.0	—	$M\Omega$
		10	0.2	0.4	—	
		15	0.1	0.2	—	
— PCB_{in}	R_{in}	15	150	1500	—	$M\Omega$
Minimum Input Sensitivity AC Coupled — PCA_{in} C series = 1000 pF, $f = 50 \text{ kHz}$	V_{in}	5.0 10 15	— — —	200 400 700	300 600 1050	mV p-p
DC Coupled — PCA_{in} , PCB_{in}	—	5 to 15	See Noise Immunity			

VOLTAGE CONTROLLED OSCILLATOR (VCO)

Maximum Frequency $(VCO_{in} = V_{DD}, C1 = 50 \text{ pF})$ $R1 = 5.0 \text{ k}\Omega$, and $R2 = \infty$	f_{max}	5.0 10 15	0.5 1.0 1.4	0.7 1.4 1.9	— — —	MHz
Temperature — Frequency Stability $(R2 = \infty)$	—	5.0 10 15	— — —	0.12 0.04 0.015	— — —	%/ $^\circ\text{C}$
Linearity ($R2 = \infty$) $(VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}, R1 > 10 \text{ k}\Omega)$ $(VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}, R1 > 400 \text{ k}\Omega)$ $(VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}, R1 \geq 1000 \text{ k}\Omega)$	—	5.0 10 15	— — —	1.0 1.0 1.0	— — —	%
Output Duty Cycle	—	5 to 15	—	50	—	%
Input Resistance — VCO_{in}	R_{in}	15	150	1500	—	$M\Omega$

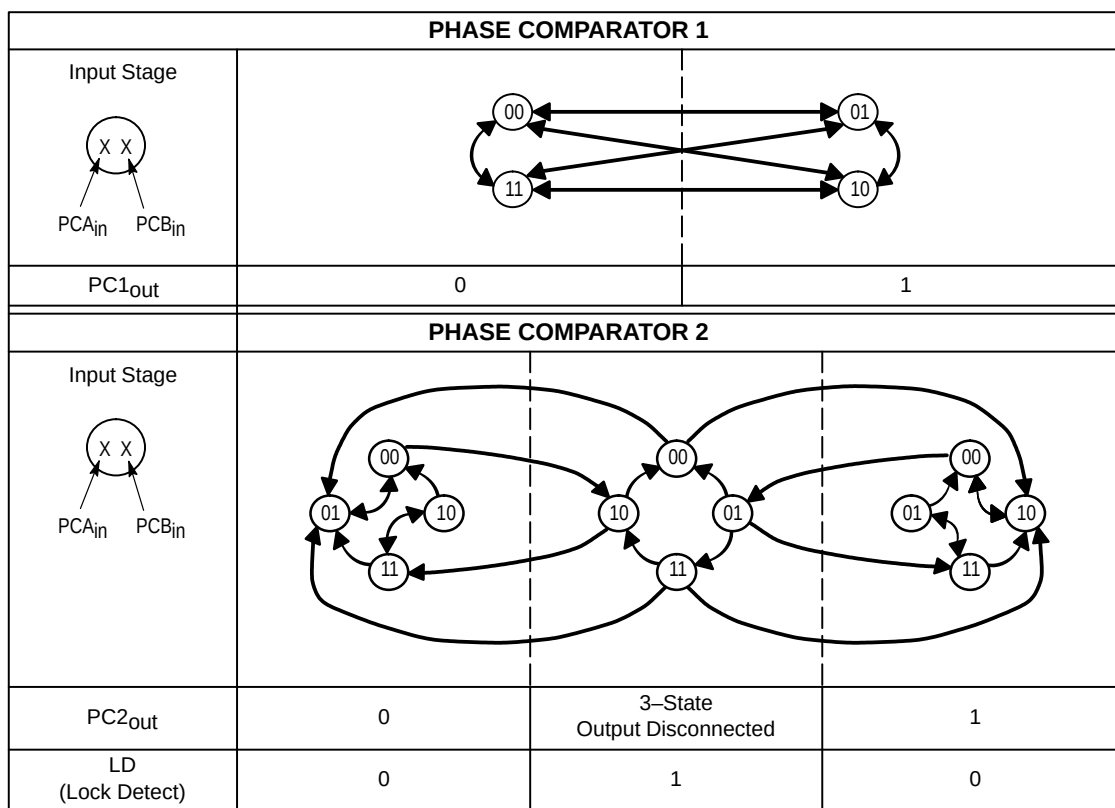
SOURCE-FOLLOWER

Offset Voltage $(VCO_{in} \text{ minus } SF_{out}, RSF > 500 \text{ k}\Omega)$	—	5.0 10 15	— — —	1.65 1.65 1.65	2.2 2.2 2.2	V
Linearity $(VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}, RSF > 50 \text{ k}\Omega)$ $(VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}, RSF > 50 \text{ k}\Omega)$ $(VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}, RSF > 50 \text{ k}\Omega)$	—	5.0 10 15	— — —	0.1 0.6 0.8	— — —	%

ZENER DIODE

Zener Voltage ($I_Z = 50 \mu\text{A}$)	V_Z	—	6.7	7.0	7.3	V
Dynamic Resistance ($I_Z = 1.0 \text{ mA}$)	R_Z	—	—	100	—	Ω

* The formula given is for the typical characteristics only.

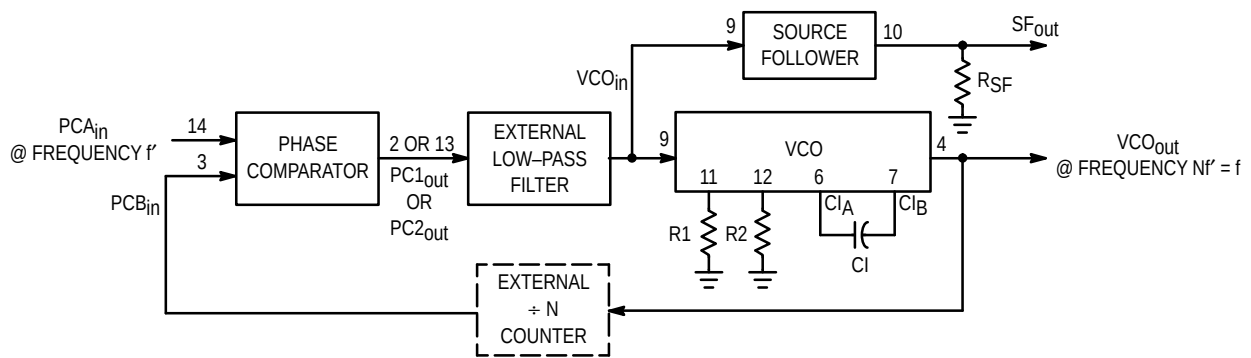


Refer to Waveforms in Figure 3.

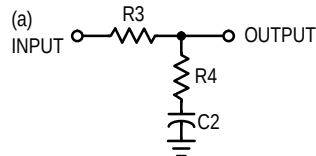
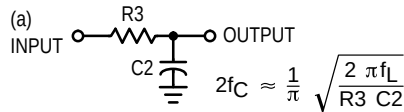
Figure 1. Phase Comparators State Diagrams

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA _{in} .	VCO in PLL system adjusts to center frequency (f ₀).	VCO in PLL system adjusts to minimum frequency (f _{min}).
Phase angle between PCA _{in} and PCB _{in} .	90° at center frequency (f ₀), approaching 0° and 180° at ends of lock range (2f _L)	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f _L).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2f _L = full VCO frequency range = f _{max} – f _{min} .	
Capture frequency range (2f _C).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f _C ≤ f _L	f _C = f _L
Center frequency (f ₀).	The frequency of VCO _{out} , when VCO _{in} = 1/2 V _{DD}	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min}$ (V_{CO} input = V_{DD}) Where: 10K ≤ R₁ ≤ 1 M 10K ≤ R₂ ≤ 1 M 100pF ≤ C₁ ≤ .01 μF	
Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.		

Figure 2. Design Information



Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{\max}} - \frac{N}{2\pi \Delta f}$$

$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{\max}^2} - R_4 C_2$$

$$\Delta f = f_{\max} - f_{\min}$$

NOTE: Sometimes R_3 is split into two series resistors each $R_3/2$. A capacitor C_C is then placed from the midpoint to ground. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_n . In Figure B, the ratio of R_3 to R_4 sets the damping, $R_4 \approx (0.1)(R_3)$ for optimum results.

LOW-PASS FILTER

Definitions: N = Total division ratio in feedback loop

$K_\phi = V_{DD}/\pi$ for Phase Comparator 1

$K_\phi = V_{DD}/4\pi$ for Phase Comparator 2

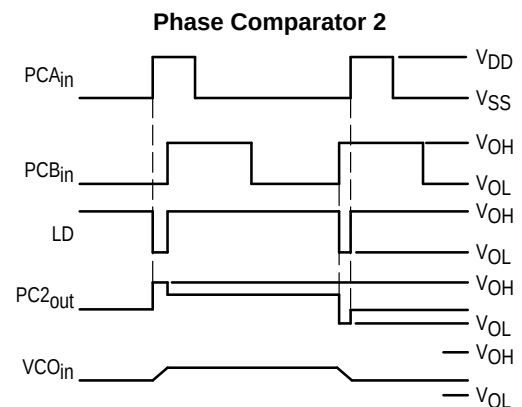
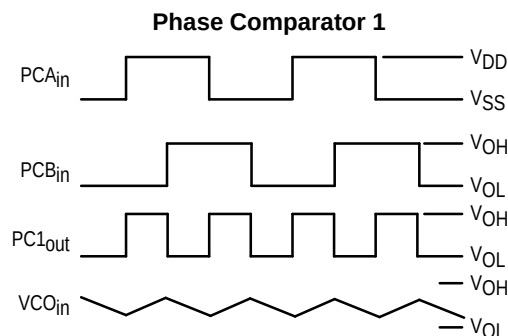
$$K_{VCO} = \frac{2\pi \Delta f_{VCO}}{V_{DD} - 2V}$$

for a typical design $\omega_n \approx \frac{2\pi f_r}{10}$ (at phase detector input)

$$\zeta \approx 0.707$$

Filter A	Filter B
$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_3 C_2}}$	$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$	$\zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K_\phi K_{VCO}})$
$F(s) = \frac{1}{R_3 C_2 s + 1}$	$F(s) = \frac{R_3 C_2 s + 1}{s(R_3 C_2 + R_4 C_2) + 1}$

Waveforms



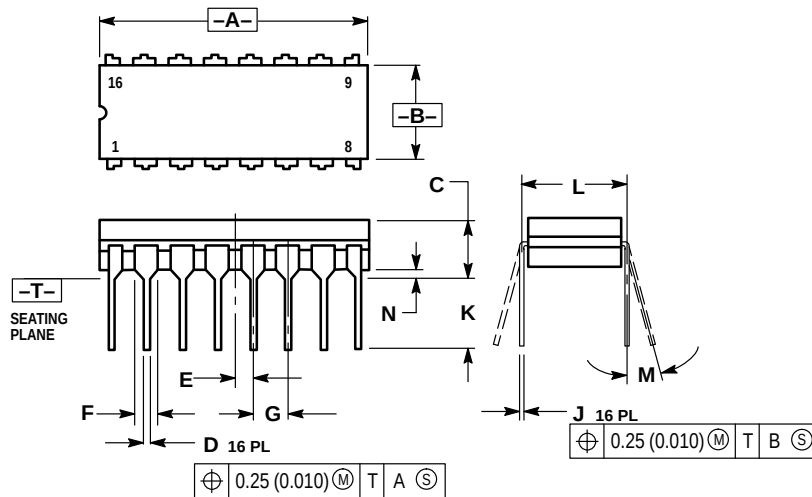
Note: for further information, see:

- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
- (4) A. B. Przepelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.

Figure 3. General Phase-Locked Loop Connections and Waveforms

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

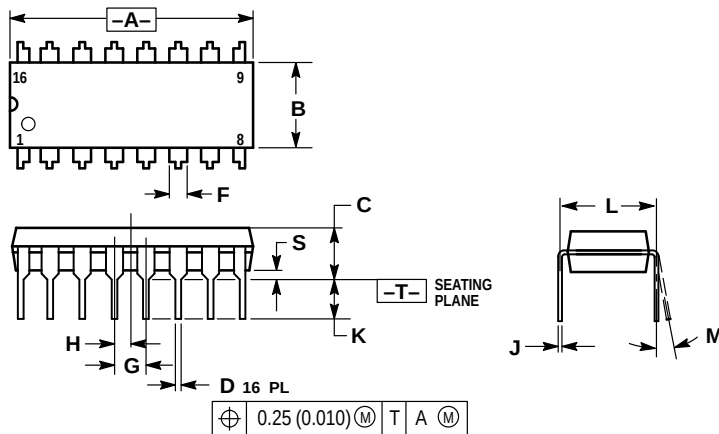


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



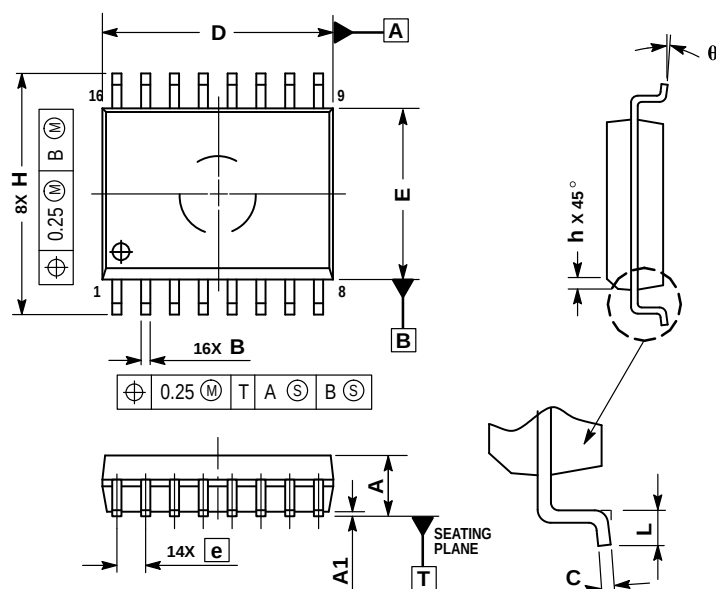
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

DW SUFFIX PLASTIC SOIC WIDE PACKAGE CASE 751G-03 ISSUE B



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

Customer Focus Center: 1-800-521-6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609
Motorola Fax Back System – US & Canada ONLY 1-800-774-1848
– http://sps.motorola.com/mfax/

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

HOME PAGE: <http://motorola.com/sps/>



MC14046B/D