NBSG53ABAEVB

Evaluation Board Manual for NBSG53A

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EVALUATION BOARD MANUAL

DESCRIPTION

This document describes the NBSG53A evaluation board and the appropriate lab test setups. It should be used in conjunction with the device data sheet, which includes specifications and a full description of device operation.

The board is used to evaluate the NBSG53A GigaComm™ multi−function device, which can be configured as a differential D flip–flop (DFF), or a divide−by−2 clock divider (DIV/2). The output function is determined by the state of the Reset and Select pins. The Reduced Swing ECL (RSECL) output ensures minimal noise and fast switching edges.

The board is implemented in two layers and provides a high bandwidth 50 Ω controlled impedance environment for higher performance. The first layer or primary trace layer is 5 mils thick Rogers RO6002 material, which is engineered to have equal electrical length on all signal traces from the NBSG53A device to the sense output. The second layer is 32 mils thick copper ground plane.

For standard lab setup and test, a split (dual) power supply is required enabling the 50 Ω impedance from the scope to be used as termination of the ECL signals ($V_{TT} = V_{CC} - 2.0$ V, in split power supply setup V_{TT} is the system ground, $V_{CC} = 2.0$ V and V_{EE} is –0.5 V or –1.3 V see setup Step 1).

Device Measurements

The following measurements can be performed in the single–ended[(1)] or differential mode of operation:

- Output Amplitude vs. Frequency (V_{OH} /V_{OL})
- Output Rise and Fall Time
- Output Skew
- Eye pattern generation
- Jitter
- V_{IHCMR} (Input High Common Mode Range)

1. Single−ended measurements can only be made at $V_{CC} - V_{EE} = 3.3$ V using this board setup.

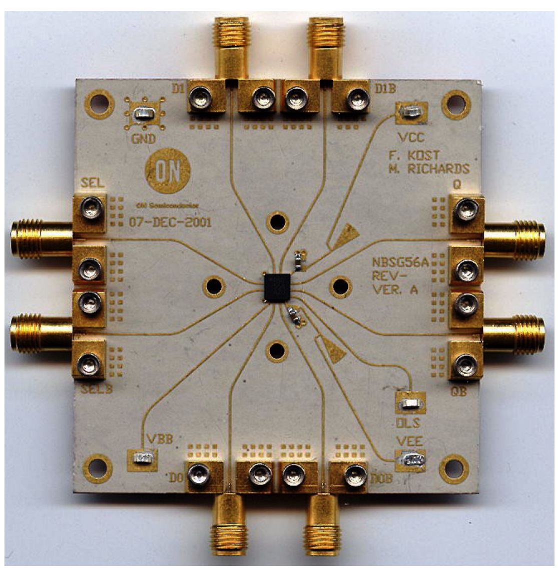

Figure 1. NBSG53A Evaluation Board

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Setup for Time Domain Measurements

Table 1. Basic Equipment Needed

Description	Example Equipment (Note 1)	Qty.
Power Supply with 2 outputs	HP6624A	1
Oscilloscope	TDS8000 with 80E01 Sampling Head (Note 2)	1
Differential Signal Generator	HP 8133A, Advantest D3186	1
Matched high speed cables with SMA connectors	Storm, Semflex	6
Power Supply cables with clips		3

1. Equipment used to generate example measurements within this document.
2. 50 GHz sample module used (for effective rise, fall and jitter performance measurement).

D Flip−Flop Mode Setup

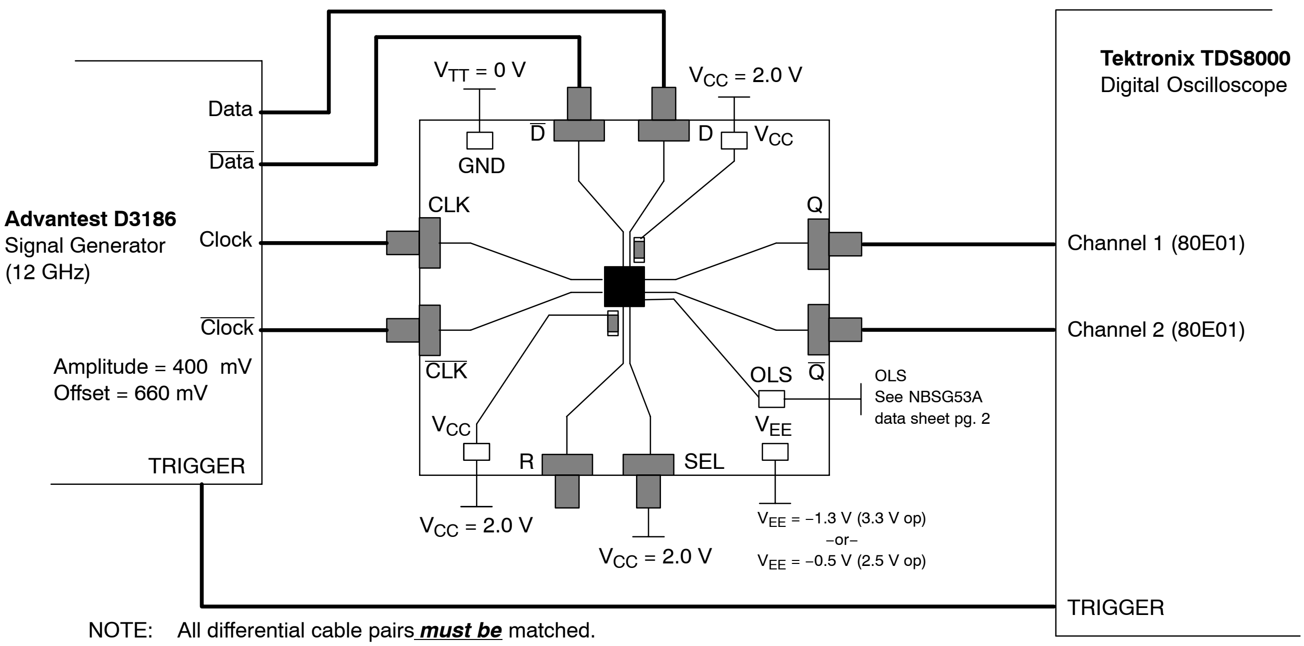


Figure 2. Time Domain Setup for the Differential D Flip−Flop Mode (DFF)

Step 1:

Connect Power

1a: Connect the following supplies to the evaluation board via the surface mount clips.

Power Supply Summary Table	
3.3 V Setup	**2.5 V Setup**
V_{CC} = 2.0 V (Two Places)	V_{CC} = 2.0 V (Two Places)
V_{TT} = GND (One Place)	V_{TT} = GND(One Place)
V_{EE} = −1.3 V (One Place)	V_{EE} = −0.5 V (One Place)

D Flip−Flop Mode Setup (continued)

Step 2:

Connect the Inputs

For Differential Mode (3.3 V and 2.5 V operation)

2a: Connect the Select input to V_{CC}. (Note 3)
2b: Leave the Reset input open (it will default LOW when open). (Note 3)
2c: Connect the differential Clock outputs of the generator to the differential Clock inputs of the device. (CLK and $\overline{CLK}$)
2d: Connect the differential Data outputs of the generator to the differential Data inputs of the device. (D and $\overline{D}$)
2e: Connect the generator trigger to the oscilloscope trigger.

For Single−Ended Mode (3.3 V operation only)

2a: Connect the Select input to V_{CC}. (Note 3)
2b: Leave the Reset input open (it will default LOW when open). (Note 3)
2c: Connect an AC−coupled output of the generator to the desired differential input of the device.
2d: Connect the unused differential input of the device to V_{TT} (GND) through a 50 Ω resistor.
2e: Connect the generator trigger to the oscilloscope trigger.

For All Modes

Connect OLS (Output Level Select) to the required voltage to obtain desired output amplitude. Refer to the NBSG53A device data sheet page 2 OLS voltage table.

3. If using an ECL signal on the Reset or Select input pin, a proper ECL driver termination should be used, such as 50 Ω to V_{TT} = V_{CC} −2 V = GND. A pad is available on the evaluation board to solder on a 50 Ω termination resistor.

Step 3:

Setup Input Signals

3a: Set the signal generator amplitude to 400 mV.

NOTE: The signal generator amplitude can vary from 75 mV to 900 mV to produce a 400 mV DUT output amplitude.

3b: Set the signal generator offset to 660 mV (the center of a nominal RSECL output).
3c: Set the generator output for a square wave clock signal with a 50% duty cycle, or for a PRBS data signal.

NOTE: The V_{IHCMR} (Input High Voltage Common Mode Range) allows the signal generator offset to vary as long as V_{IH} is within the V_{IHCMR} range. Refer to the device data sheet for further information.

Step 4:

Connect Output Signals

4a: Connect the outputs of the evaluation board (Q0, $\overline{Q0}$) to the oscilloscope. The oscilloscope sampling module must have internal 50 Ω termination to ground.

NOTE: Where a single output is being used, the unconnected output for the pair **must be** terminated to VTT through a 50 Ω resistor for best operation. Unused pairs may be left unconnected. Since VTT = 0 V, a standard 50 Ω SMA termination is recommended.

Clock Divider Mode Setup

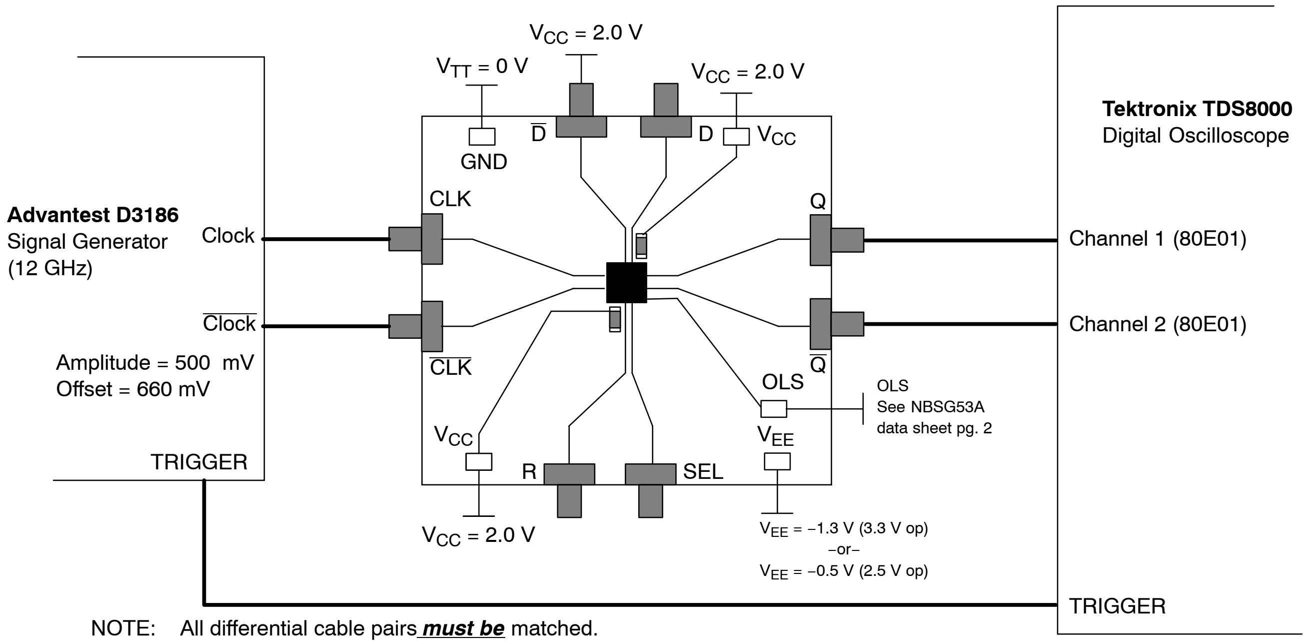


Figure 3. Time Domain Setup for the Differential Clock Divider Mode (DIV/2)

Step 1:

Connect Power

1a: Connect the following supplies to the evaluation board via the surface mount clips.

Power Supply Summary Table	
3.3 V Setup	**2.5 V Setup**
V_{CC} = 2.0 V (Two Places)	V_{CC} = 2.0 V (Two Places)
V_{TT} = GND (One Place)	V_{TT} = GND (One Place)
V_{EE} = −1.3 V (One Place)	V_{EE} = −0.5 V (One Place)

Clock Divider Mode Setup (continued)

Step 2:

Connect the Inputs

For Differential Mode (3.3 V and 2.5 V operation)

2a: Leave the Select input open (it will default LOW when open). (Note 4)
2b: Leave the Reset input open (it will default LOW when open). (Note 4)
2c: Connect the differential Clock outputs of the generator to the differential Clock inputs of the device. (CLK, $\overline{CLK}$)
2d: Leave the D input open .
2e: Connect the $\overline{D}$ input to V_{CC}.
2f: Connect the generator trigger to the oscilloscope trigger.

For Single−Ended Mode (3.3 V operation only)

2a: Leave the Select input open (it will default LOW when open). (Note 4)
2b: Leave the Reset input open (it will default LOW when open). (Note 4)
2c: Connect an AC−coupled output of the generator to the desired differential Clock input of the device.
2d: Connect the unused differential Clock input of the device to V_{TT} (GND) through a 50 Ω resistor.
2e: Leave the D input open.
2f: Connect the $\overline{D}$ input to V_{CC}.
2g: Connect the generator trigger to the oscilloscope trigger.

For All Modes

Connect Output Level Select (OLS) to the required voltage to obtain desired output amplitude. Refer to the NBSG53A device data sheet page 2 OLS voltage table.

4. If using an ECL signal on the Reset or Select input pin, a proper ECL driver termination should be used, such as 50 Ω to $V_{TT} = V_{CC} - 2$ V = GND. A pad is available on the evaluation board to solder on a 50 Ω termination resistor.

Step 3:

Setup Input Signals

3a: Set the signal generator amplitude to 400 mV.

NOTE: The signal generator amplitude can vary from 75 mV to 900 mV to produce a 400 mV DUT output amplitude.

3b: Set the signal generator offset to 660 mV (the center of a nominal RSECL output).
3c: Set the generator output for a square wave clock signal with a 50% duty cycle, or for a PRBS data signal.

NOTE: The V_{IHCMR} (Input High Voltage Common Mode Range) allows the signal generator offset to vary as long as V_{IH} is within the V_{IHCMR} range. Refer to the device data sheet for further information.

Step 4:

Connect Output Signals

4a: Connect the outputs of the evaluation board (Q0, $\overline{Q0}$) to the oscilloscope. The oscilloscope sampling head must have internal 50 Ω termination to ground.

NOTE: Where a single output is being used, the unconnected output for the pair **must be** terminated to V_{TT} through a 50 Ω resistor for best operation. Unused pairs may be left unconnected. Since V_{TT} = 0 V, a standard 50 Ω SMA termination is recommended.

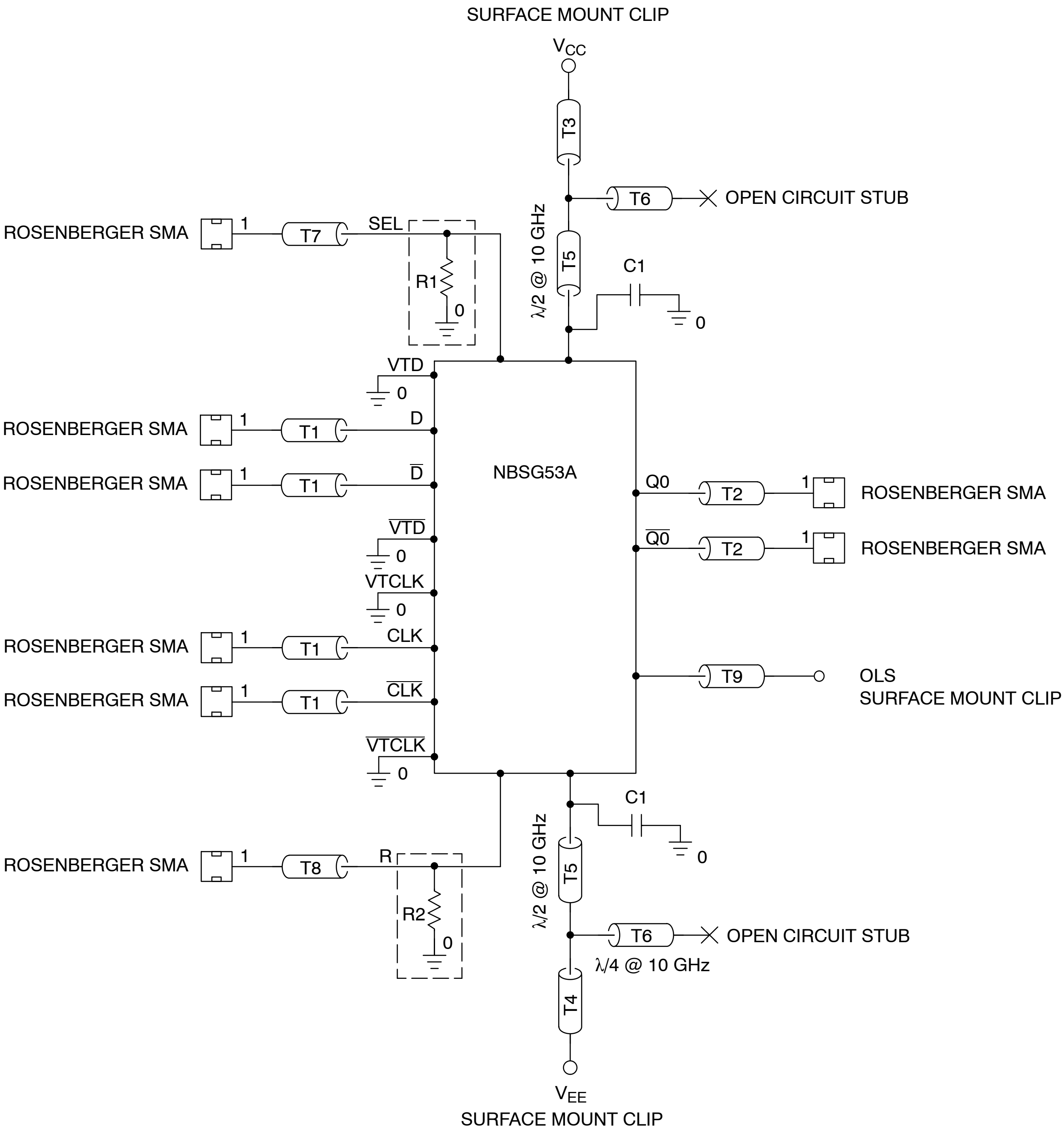
More Information About Evaluation Board

Design Considerations for >10 GHz operation

While the NBSG53A is specified to operate at 12 GHz, this evaluation board is designed to support operating frequencies up to 20 GHz.

The following considerations played a key role to ensure this evaluation board achieves high−end microwave performance:

- Optimal SMA connector launch
- Minimal insertion loss and signal dispersion
- Accurate Transmission line matching (50 Ω)
- Distributed effects while bypassing and noise filtering



NOTE: C1 = Decoupling cap (broadband cap with the range from 2 MHz to 30 GHz)
Tx = 50 Ω Transmission line
R1 and R2 are optional see Setup Note 3.

Figure 4. Evaluation Board Schematic

Table 2. Parts List

Part No	Description	Manufacturer	Qty	WEB address
NBSG53ABAHTBG	SiGe Selectable Differential Clock and Data D Flip−Flop / Clock Divider with Reset and OLS	ON Semiconductor	1	http://www.onsemi.com
32K243−40ME3	Gold Plated Connector	Rosenberger	6	http://www.rosenberger.de
CO6BLBB2X5UX	2 MHz – 30 GHz capacitor	Dielectric Laboratories	2	http://www.dilabs.com
5015KCT−ND	TP_SMT_KEYSTONE Surface Mount Clip	Keystone	2	http://www.digikey.com/

Table 3. Board Material

Material	Thickness
Rogers 6002	5.0 mil
Copper Plating	32 mil

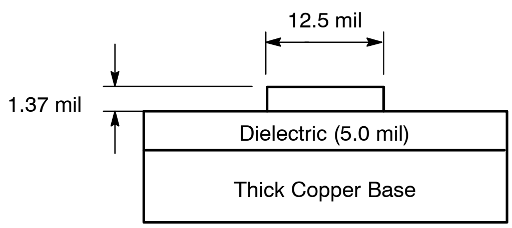


Figure 5. Board Stack−up

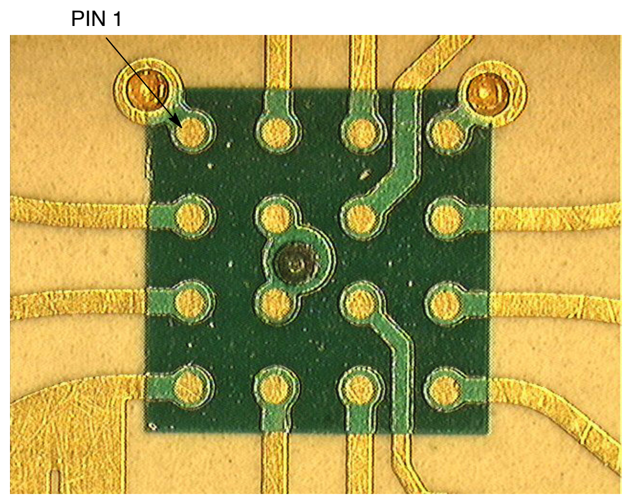
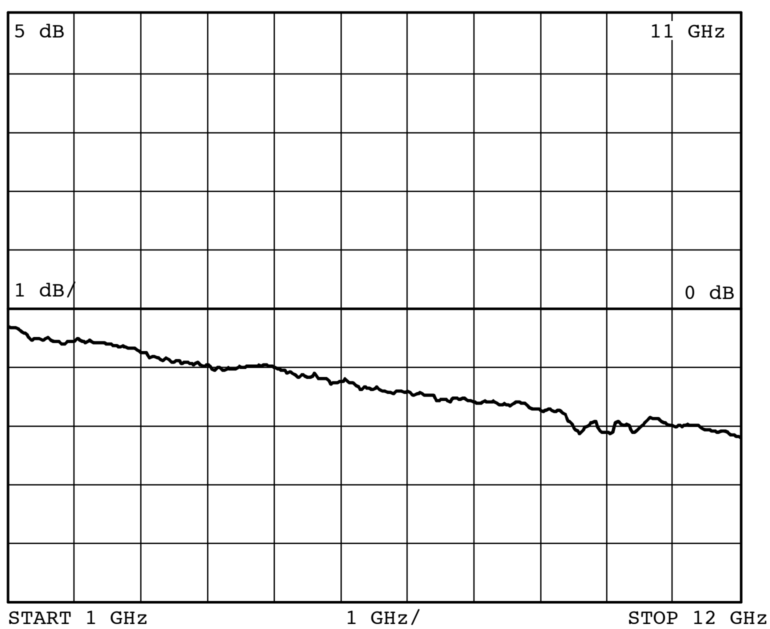


Figure 6. Layout Mask for NBSG53A



NOTE: The insertion loss curve can be used to calibrate out board loss if testing under small signal conditions.

Figure 7. Insertion Loss

EXAMPLE MEASUREMENTS IN TIME DOMAIN

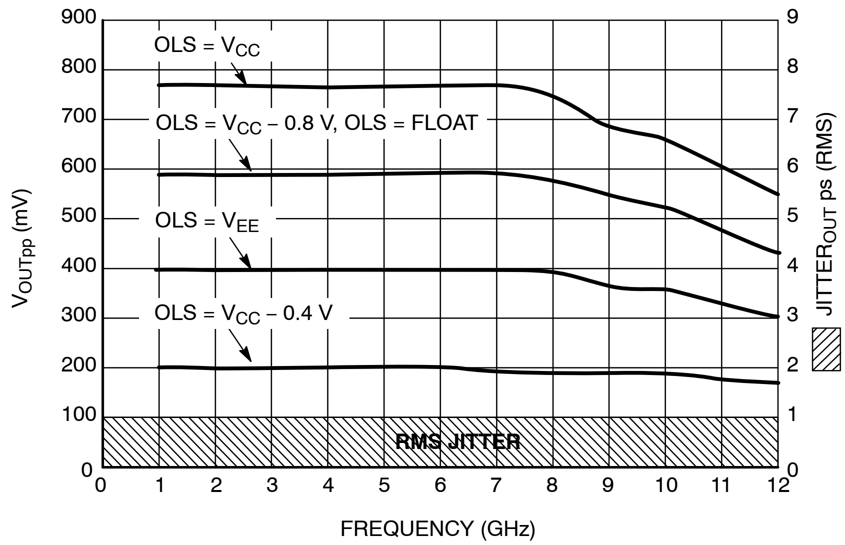


Figure 8. V_{OUT}/Jitter vs. Frequency for DFF Mode
(V_{CC} – V_{EE} = 2.5 V @ 25°C; Repetitive 1010 Input Data Pattern)

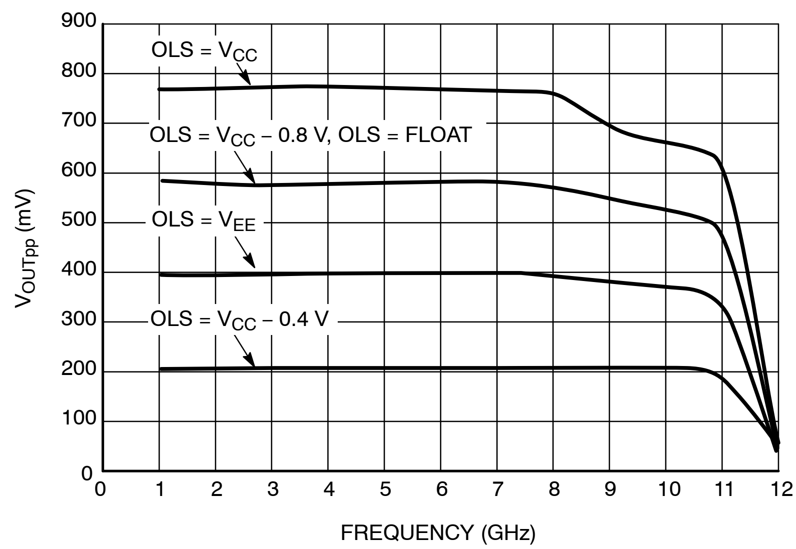


Figure 9. V_{OUT} vs. Frequency for DIV/2 Mode
(V_{CC} – V_{EE} = 2.5 V @ 25°C)

EXAMPLE MEASUREMENTS IN TIME DOMAIN

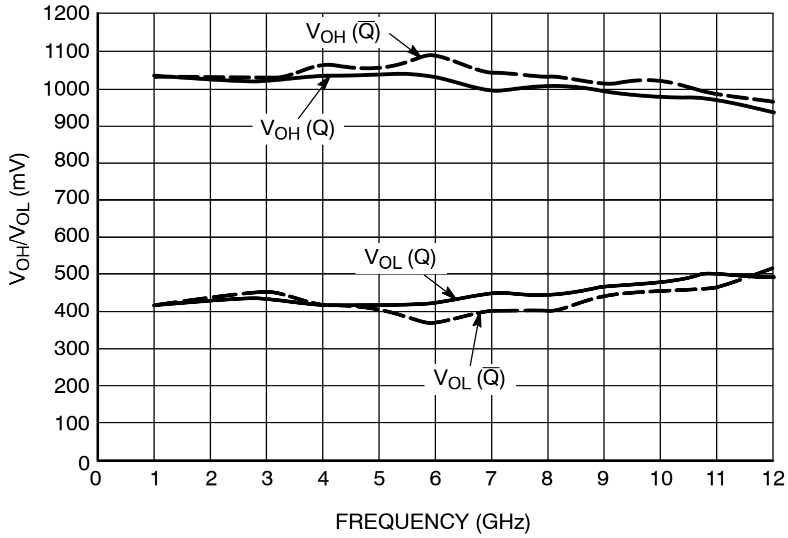


Figure 10. V_{OH}/V_{OL} ($Q/\overline{Q}$) vs. Frequency for DFF Mode
(V_{CC} – V_{EE} = 3.3 V @ 25°C and OLS = V_{CC} – 0.8 V, OLS = FLOAT)

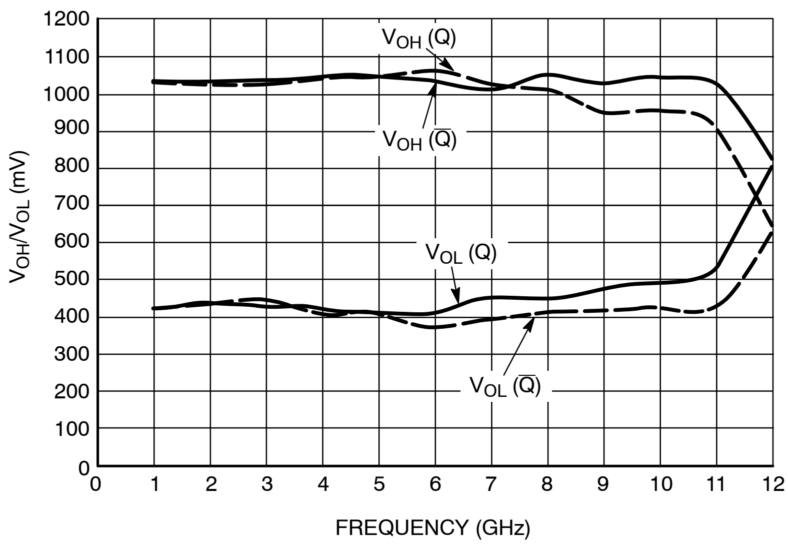


Figure 11. V_{OH}/V_{OL} ($Q/\overline{Q}$) vs. Frequency for DIV/2 Mode
(V_{CC} – V_{EE} = 3.3 V @ 25°C and OLS = V_{CC} – 0.8 V, OLS = FLOAT)

EXAMPLE MEASUREMENTS IN TIME DOMAIN

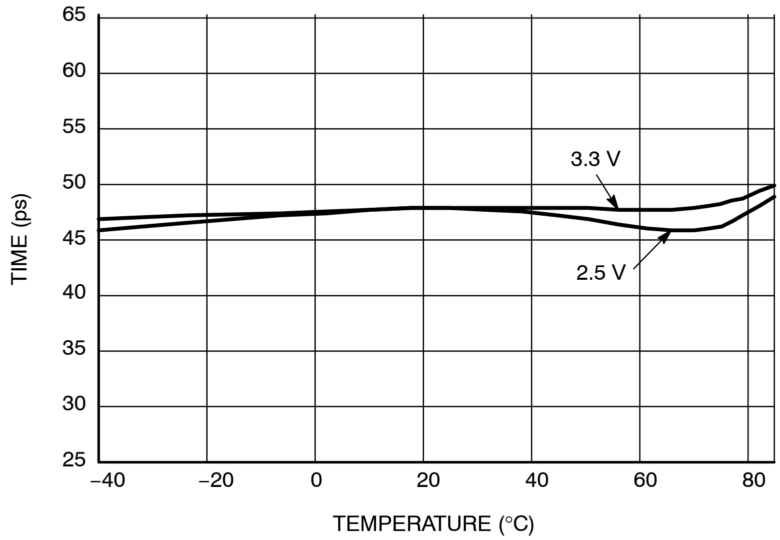


Figure 12. t_r vs. Temperature and Power Supply

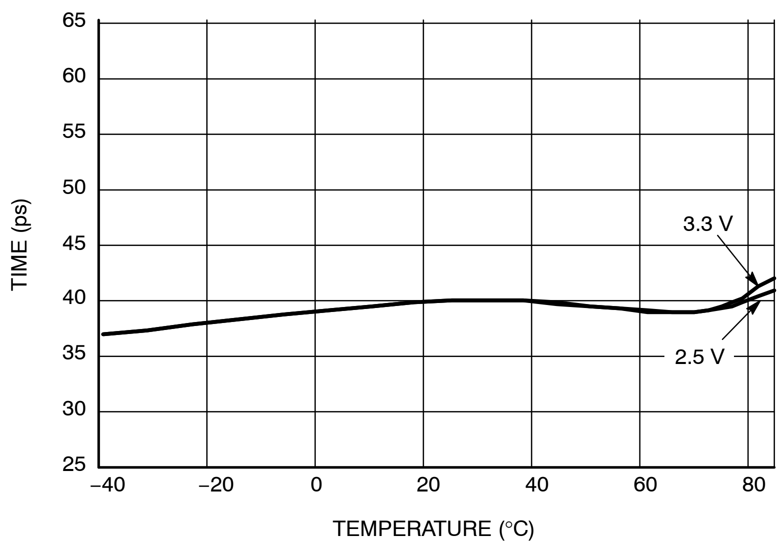


Figure 13. t_f vs. Temperature and Power Supply

ADDITIONAL INFORMATION

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In all cases, the most up−to−date information can be found on our website.

- Sample orders for devices and boards
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References

AND8077/D, Application Note, *GigaComm™ (SiGe) SPICE Modeling Kit.*

AND8075/D, Application Note, *Board Mounting Considerations for the FCBGA Packages.*

BRD8017/D, Brochure, *Clock and Data Manage Solutions.*

NBSG53A/D, Data Sheet, *NBSG53A, 2.5V/3.3V SiGe Selectable Differential Clock and Data D Flip−Flop/Clock Divider with Reset and OLS*

ORDERING INFORMATION

Orderable Part No	Description	Package	Shipping
NBSG53ABAHTBG	SiGe Selectable Differential Clock and Data D Flip−Flop / Clock Divider with Reset and OLS	4X4 mm FCBGA/16	500 Units/Reel
NBSG53ABAEVB	NBSG53A Evaluation Board		

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