
ERRATA

TO THE TSB21LV03C DATA SHEET

(TEXAS INSTRUMENTS LITERATURE NO. SLLS331, FEBRUARY 1999)

This document contains corrections and additions to information in the TSB21LV03C data sheet (TI Literature Number SLLS331, FEBRUARY 1999).

- a. The SUBACTION_GAP on the TSB21LV03C occurs 40 ns prior to the SUBACTION_GAP specified in the IEEE 1394-1995 STD. This does not cause a problem in real life applications. The PHY in the network starts to arbitrate for the bus during a fairness interval after a SUBACTION_GAP and ARB_DELAY time. The SUBACTION_GAP plus ARB_DELAY time is always larger than the SUBACTION_GAP of IEEE 1394-1995 PHY. This ensures that all nodes in the network detect a SUBACTION_GAP.
- b. The TSB21LV03C detection of a ARB_RESET_GAP is 20 ns to 1200 ns longer than the time specified IEEE 1394-1995 STD. The delay is dependent on the gap count values, and does not occur when the gap count is 1. TSB21LV03C starts to arbitrate for the bus after ARB_RESET_GAP and ARB_DELAY time at the end of the fairness interval. The TSB21LV03C delays the arbitration for the bus by 80 ns more than specified in the IEEE 1394-1995 STD. This does not cause problems in real-life applications. This timing ensures that all the nodes detect an ARB_RESET_GAP.
- c. The DATA_END time measured is 20 ns less than the time specified in the IEEE 1394-1995 STD. This does not cause problems in real-life applications.
- d. RESET_WAIT: The delay in the RESET_WAIT time makes the TSB21LV03C more likely to be root unless another PHY on the bus has its root holdoff bit set. This does not cause any problems in real-life applications.
- e. TPBias leakage. If the TSB21LV03C PHY is powered on, connected to an active IEEE 1394-1995 PHY supplying TPBias, and then powered down, the TSB21LV03C may not power up correctly when power is again applied to the device. This is caused by the TPBias from the connected node partially powering the TSB21LV03C. This only occurs if the method of resetting the TSB21LV03C is a single 0.1- μ F capacitor connected from RESET to PHY GND. If the reset line is actively driven, instead of only a passive capacitor, this problem will not occur.

Workaround:

1. To ensure the TSB21LV03C properly powers back up when not actively driving the RESET terminal, the schematic with the TSB21LV03C should include an approximately 110-k Ω resistor connected from the RESET terminal to PHY GND. This resistor will be in parallel with the recommended 0.1- μ F capacitor.
2. If the boards are designed with the capability of powering the PHY from bus power, and if bus power supply will always be provided in the system, this will keep the PHYs powered at all times and the leakage problem will not occur.

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