

# CD40257B Types

## CMOS

### Quad 2-Line-to-1-Line Data Selector/Multi- plexer

High-Voltage Types (20-Volt Rating)

■ CD40257B is a Data Selector/Multi-  
plexer featuring three-state outputs which  
can interface directly with and drive data  
lines of bus-oriented systems.

The CD40257B types are supplied in 16-lead  
hermetic dual-in-line ceramic packages  
(F3A suffix), 16-lead dual-in-line plastic  
packages (E suffix), 16-lead small-outline  
packages (M, M96, MT, and NSR suffixes), and  
16-lead thin shrink small-outline packages  
(PW and PWR suffixes).

#### MAXIMUM RATINGS, Absolute-Maximum Values:

##### DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> + 0.5V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA

##### POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

##### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C

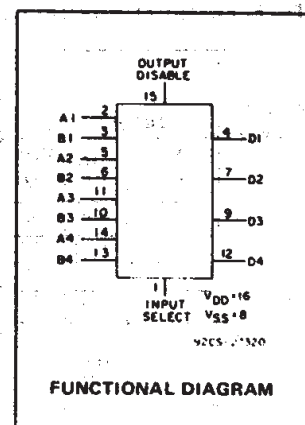
STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C

##### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

#### Features:

- 3-state outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V  
over full package-temperature range;  
100 nA at 18 V and 25°C
- Noise margin (over full package-  
temperature range):  
1 V at V<sub>DD</sub> = 5 V  
2 V at V<sub>DD</sub> = 10 V  
2.5 V at V<sub>DD</sub> = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC  
Tentative Standard No. 13A, "Standard  
Specifications for Description of 'B'  
Series CMOS Devices"



#### Applications:

- Digital Multiplexing
- Shift-right/shift-left registers
- True/complement selection

#### RECOMMENDED OPERATING CONDITION

For maximum reliability, nominal operating  
conditions should be selected so that operation  
is always within the following ranges:

| CHARACTERISTIC                                                                    | LIMITS |      | UNITS |
|-----------------------------------------------------------------------------------|--------|------|-------|
|                                                                                   | Min.   | Max. |       |
| Supply-Voltage Range<br>(For T <sub>A</sub> = Full Package-<br>Temperature Range) | 3      | 18   | V     |

#### TRUTH TABLE

| 3-STATE<br>OUTPUT<br>DISABLE | INPUTS |     | OUTPUT |
|------------------------------|--------|-----|--------|
|                              | SELECT | A B |        |
| 1                            | X      | X X | Z      |
| 0                            | 0      | 0 X | 0      |
| 0                            | 0      | 1 X | 1      |
| 0                            | 1      | X 0 | 0      |
| 0                            | 1      | X 1 | 1      |

X = DON'T CARE LOGIC 1 = HIGH  
LOGIC 0 = LOW Z = HIGH IMPEDANCE

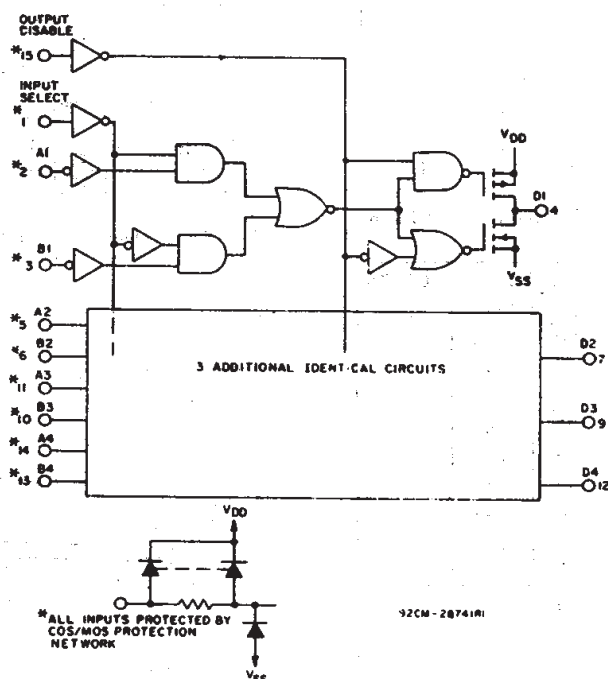


Fig. 1 - Logic diagram for CD40257B.

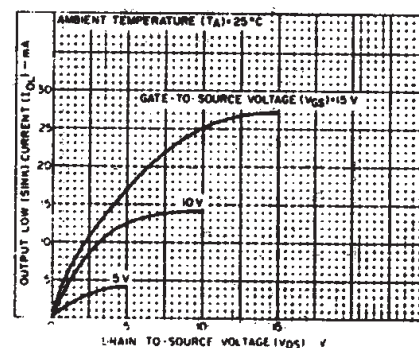


Fig. 2 - Typical output low (sink)  
current characteristics.

# CD40257B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                       | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                      | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|                                                      |                       |                        |                        |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current I <sub>DD</sub> Max.        | —                     | 0.5                    | 5                      | 1                                     | 1     | 30    | 30    | —     | 0.02              | 1    | μA    |
|                                                      | —                     | 0.10                   | 10                     | 2                                     | 2     | 60    | 60    | —     | 0.02              | 2    |       |
|                                                      | —                     | 0.15                   | 15                     | 4                                     | 4     | 120   | 120   | —     | 0.02              | 4    |       |
|                                                      | —                     | 0.20                   | 20                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
| Output Low (Sink) Current, I <sub>OL</sub> Min.      | 0.4                   | 0.5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|                                                      | 0.5                   | 0.10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|                                                      | 1.5                   | 0.15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High (Source) Current, I <sub>OH</sub> Min.   | 4.6                   | 0.5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    |       |
|                                                      | 2.5                   | 0.5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                      | 9.5                   | 0.10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                      | 13.5                  | 0.15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.      | —                     | 0.5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                      | —                     | 0.10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                      | —                     | 0.15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.     | —                     | 0.5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                      | —                     | 0.10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                      | —                     | 0.15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low Voltage, V <sub>IL</sub> Max.              | 0.5, 4.5              | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                      | 1.9                   | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                      | 1.5, 13.5             | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High Voltage, V <sub>IH</sub> Min.             | 0.5, 4.5              | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                      | 1.9                   | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                      | 1.5, 13.5             | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current, I <sub>IN</sub> Max.                  | —                     | 0.18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |
| 3-State Output Leakage Current I <sub>OUT</sub> Max. |                       | 0.18                   | 18                     | ±0.4                                  | ±0.4  | ±12   | ±12   | —     | ±10 <sup>-4</sup> | ±0.4 | μA    |

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$ ; Input  $t_r, t_f = 20$  ns,  $C_L = 50$  pF,  $R_L = 200$  K $\Omega$

| CHARACTERISTIC                                                   | TEST CONDITIONS | LIMITS      |           | UNITS |
|------------------------------------------------------------------|-----------------|-------------|-----------|-------|
|                                                                  |                 | $V_{DD}(V)$ | Typ. Max. |       |
| Propagation Delay Time: Data Input to Output, $t_{PHL}, t_{PLH}$ |                 | 5           | 150 300   | ns    |
|                                                                  |                 | 10          | 70 140    |       |
|                                                                  |                 | 15          | 50 100    |       |
| Select to Output, $t_{PHL}, t_{PLH}$                             |                 | 5           | 190 380   | ns    |
|                                                                  |                 | 10          | 85 170    |       |
|                                                                  |                 | 15          | 65 130    |       |
| Output Disable to Output, $t_{PHL}, t_{PLH}$                     |                 | 5           | 95 190    | ns    |
|                                                                  |                 | 10          | 50 100    |       |
|                                                                  |                 | 15          | 40 80     |       |
| Transition Time, $t_{THL}, t_{TLH}$                              |                 | 5           | 100 200   | ns    |
|                                                                  |                 | 10          | 50 100    |       |
|                                                                  |                 | 15          | 40 80     |       |
| Input Capacitance, $C_{IN}$                                      | Any Input       | —           | 5 7.5     | pF    |

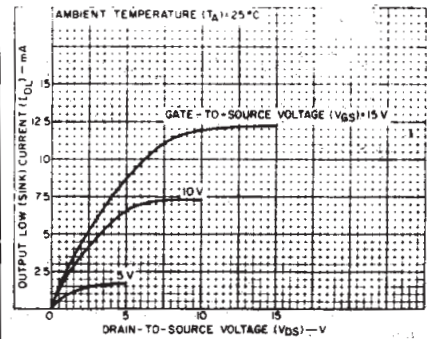


Fig.3 — Minimum output low (sink) current characteristics.

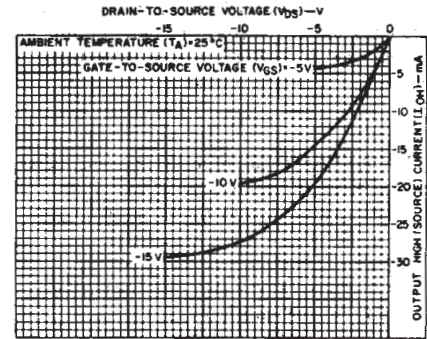


Fig.4 — Typical output high (source) current characteristics.

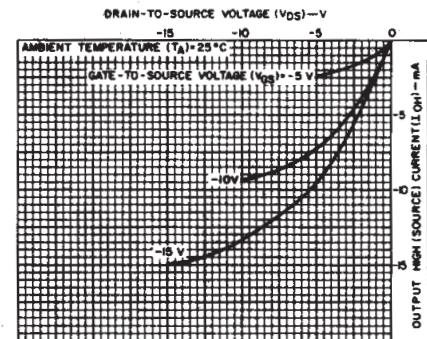


Fig.5 — Minimum output high (source) current characteristics.

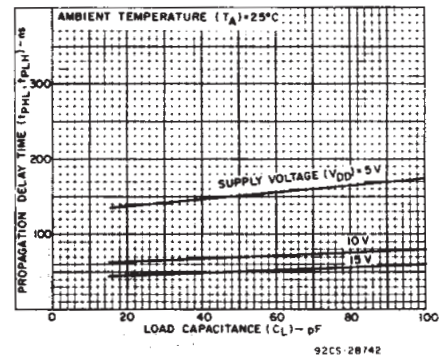


Fig.6 — Typical propagation delay time as a function of load capacitance (DATA INPUT to OUTPUT).

## CD40257B Types

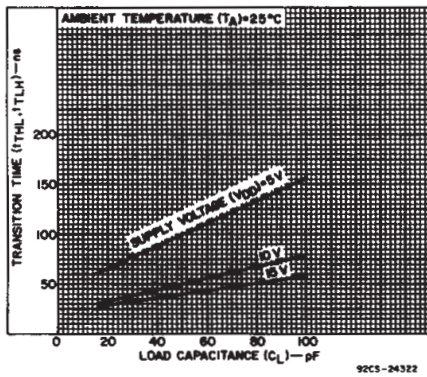


Fig. 7 - Typical transition time as a function of load capacitance.

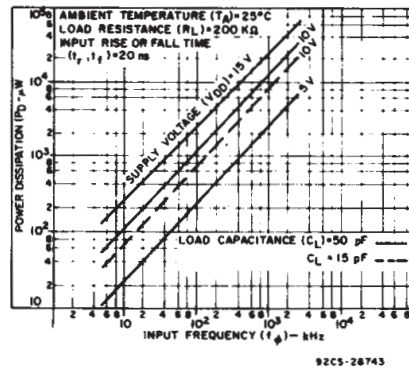


Fig. 8 - Typical dynamic power dissipation as a function of input frequency (one INPUT to one OUTPUT).

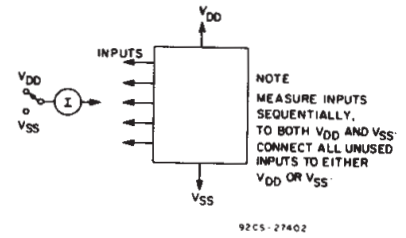


Fig. 9 - Input current test circuit.

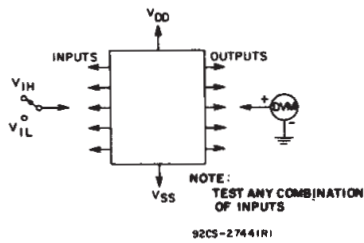


Fig. 10 - Input voltage test circuit.

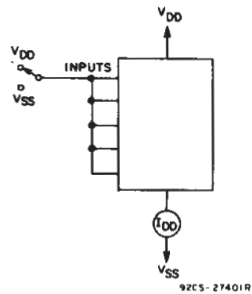
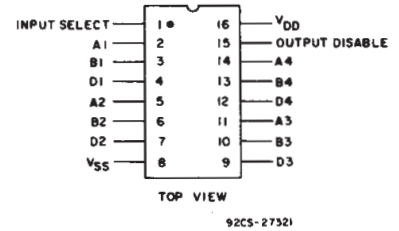
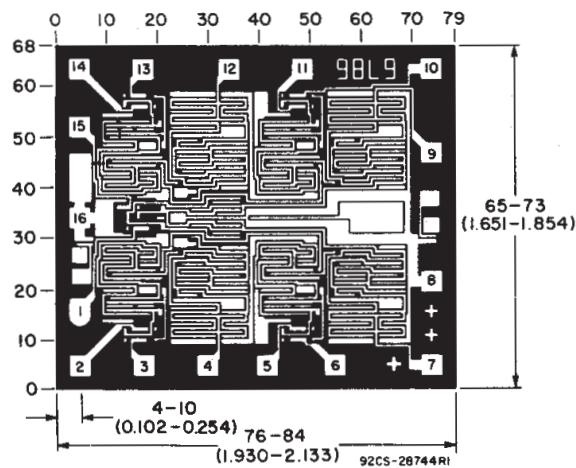


Fig. 11 - Quiescent device current test circuit.



TERMINAL ASSIGNMENT

Dimensions and pad layout for CD40257BH.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD40257BE</a>   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40257BE           |
| CD40257BE.A                 | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40257BE           |
| CD40257BEE4                 | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40257BE           |
| <a href="#">CD40257BF3A</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD40257BF3A         |
| CD40257BF3A.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD40257BF3A         |
| <a href="#">CD40257BM</a>   | Active        | Production           | SOIC (D)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD40257BM           |
| CD40257BM.A                 | Active        | Production           | SOIC (D)   16  | 40   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD40257BM           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD40257B, CD40257B-MIL :**

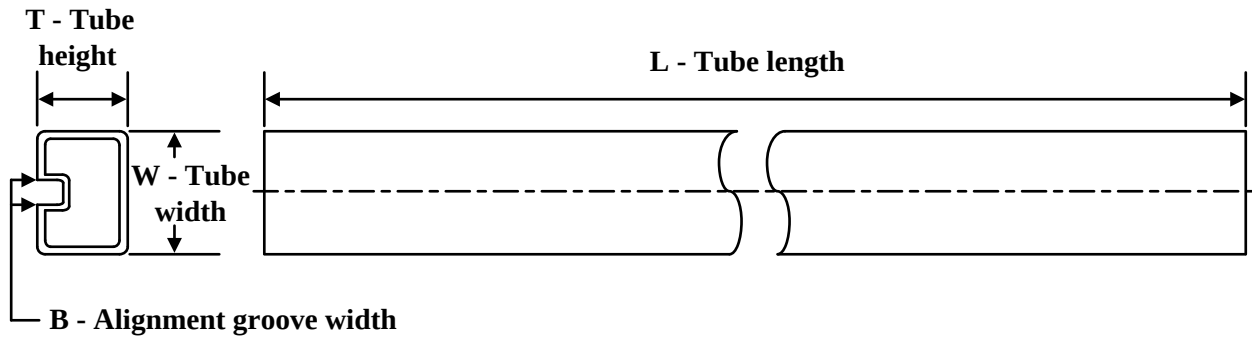
- Catalog : [CD40257B](#)
- Military : [CD40257B-MIL](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



## TUBE

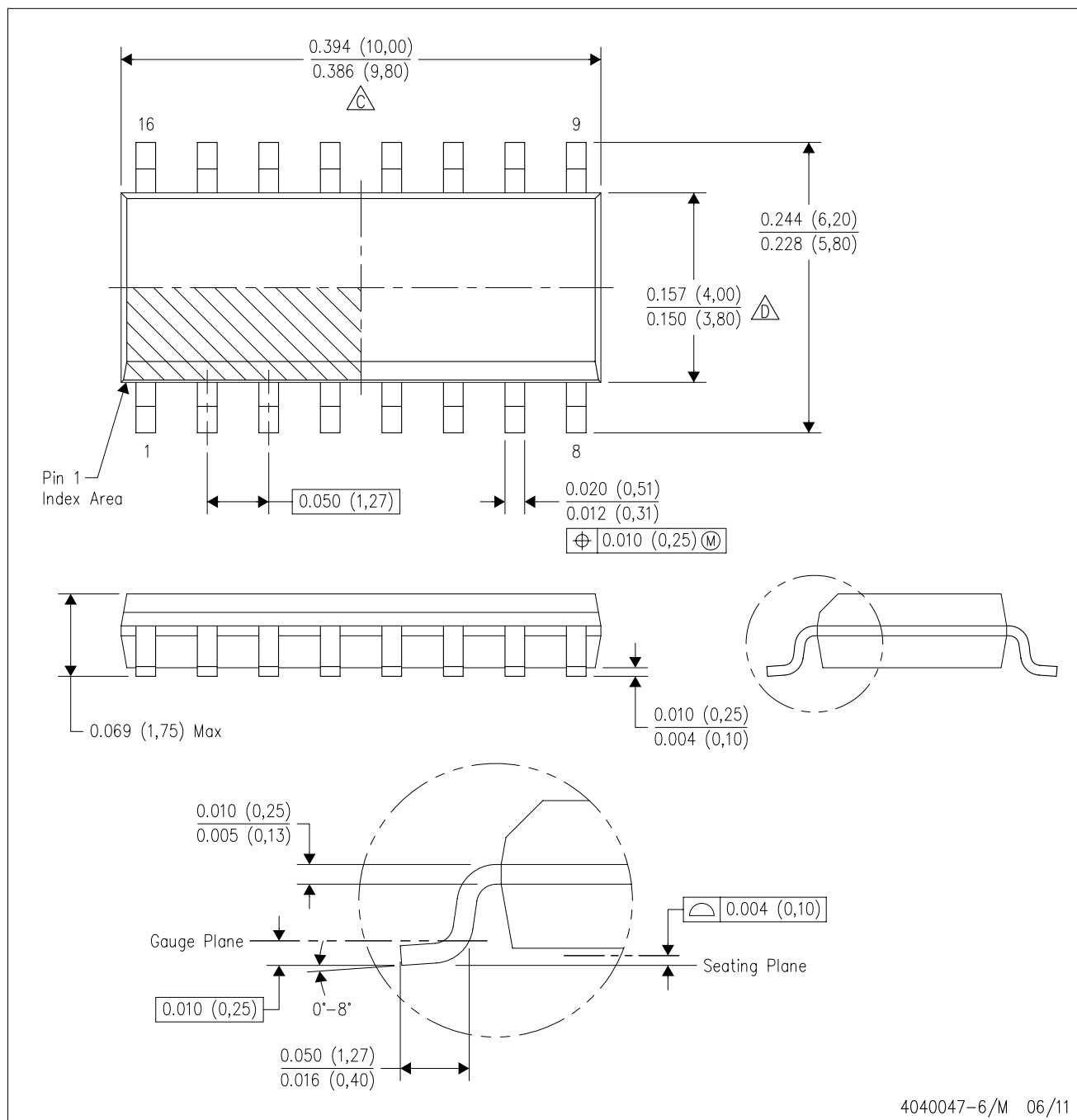


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD40257BE   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40257BE   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40257BE.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40257BE.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40257BEE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40257BEE4 | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40257BM   | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |
| CD40257BM.A | D            | SOIC         | 16   | 40  | 507    | 8      | 3940   | 4.32   |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

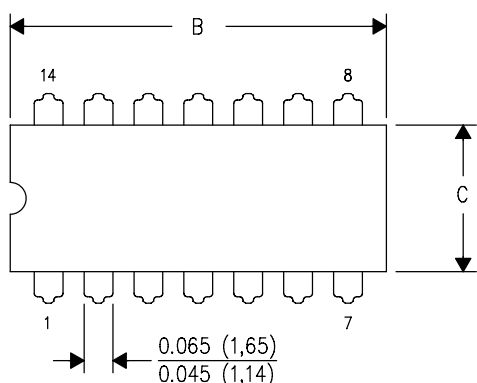
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

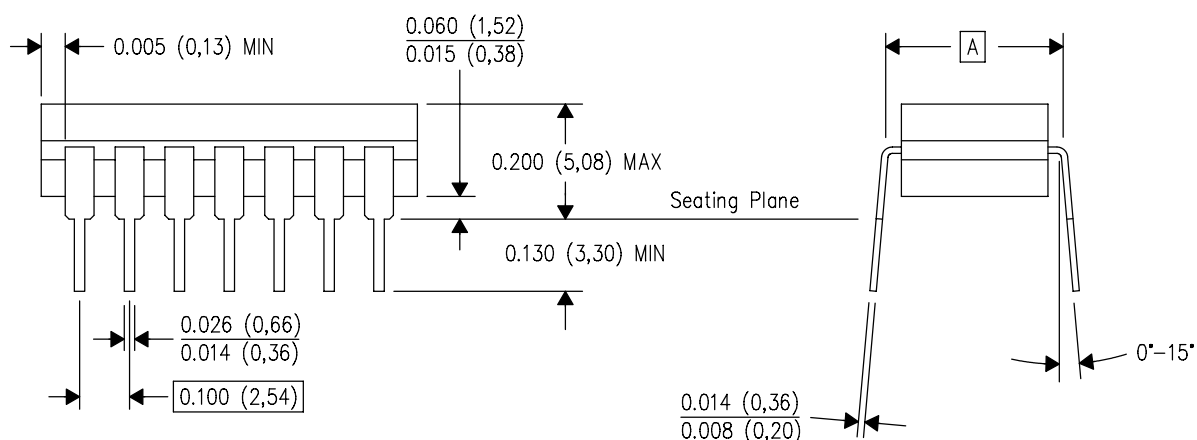
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

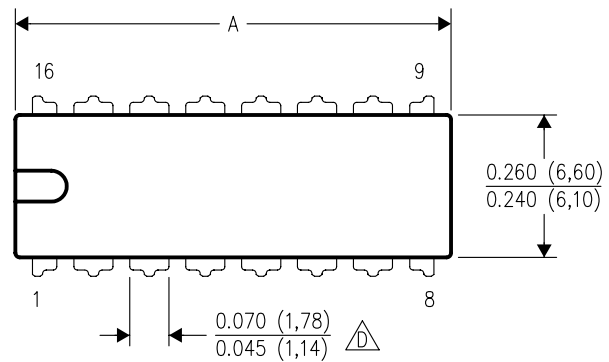
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



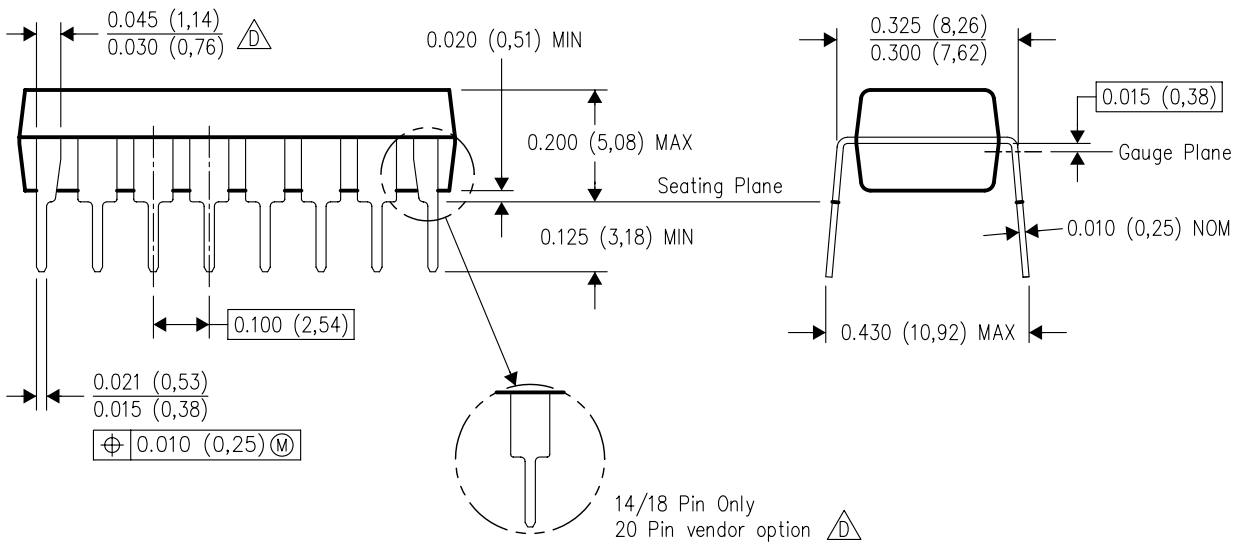
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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