

# SN54LVT574, SN74LVT574

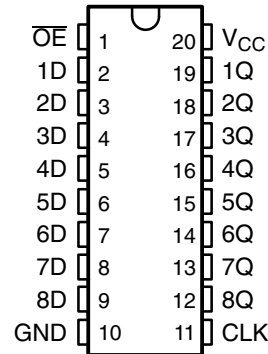
## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

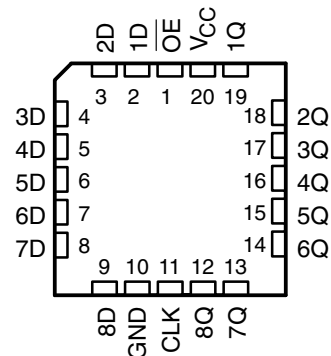
SCBS139D – MAY 1992 – REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT574 . . . J OR W PACKAGE  
SN74LVT574 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LVT574 . . . FK PACKAGE  
(TOP VIEW)



## description

These octal flip-flops are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT574 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LVT574 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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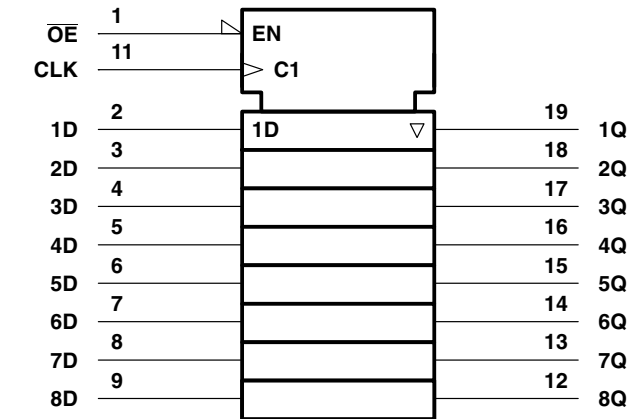
# SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each flip-flop)

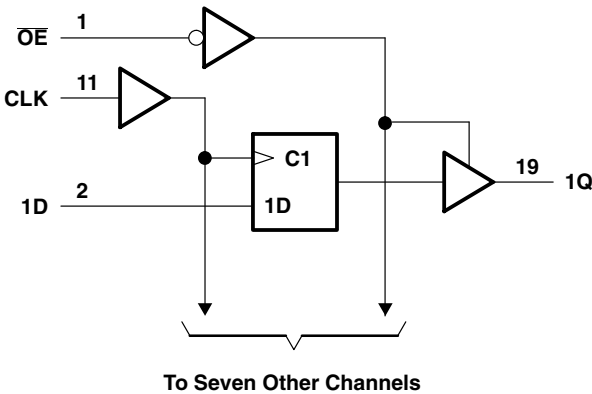
| INPUTS |        |   | OUTPUT<br>Q    |
|--------|--------|---|----------------|
| OE     | CLK    | D |                |
| L      | ↑      | H | H              |
| L      | ↑      | L | L              |
| L      | H or L | X | Q <sub>0</sub> |
| H      | X      | X | Z              |

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$  | –0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1)   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)  | –0.5 V to 7 V   |
| Current into any output in the low state, $I_O$ : SN54LVT574                                  | 96 mA           |
| SN74LVT574  | 128 mA          |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVT574                     | 48 mA           |
| SN74LVT574  | 64 mA           |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )   | –50 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )  | –50 mA          |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package | 0.6 W           |
| DW package  | 1.6 W           |
| PW package  | 0.7 W           |
| Storage temperature range, $T_{stg}$  | –65°C to 150°C  |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

# SN54LVT574, SN74LVT574

## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 4)

|                 |                                    |                 | SN54LVT574 |     | SN74LVT574 |     | UNIT |
|-----------------|------------------------------------|-----------------|------------|-----|------------|-----|------|
|                 |                                    |                 | MIN        | MAX | MIN        | MAX |      |
| V <sub>CC</sub> | Supply voltage                     |                 | 2.7        | 3.6 | 2.7        | 3.6 | V    |
| V <sub>IH</sub> | High-level input voltage           |                 | 2          |     | 2          |     | V    |
| V <sub>IL</sub> | Low-level input voltage            |                 |            | 0.8 |            | 0.8 | V    |
| V <sub>I</sub>  | Input voltage                      |                 |            | 5.5 |            | 5.5 | V    |
| I <sub>OH</sub> | High-level output current          |                 |            | –24 |            | –32 | mA   |
| I <sub>OL</sub> | Low-level output current           |                 |            | 48  |            | 64  | mA   |
| Δt/Δv           | Input transition rise or fall rate | Outputs enabled |            | 10  |            | 10  | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     |                 | –55        | 125 | –40        | 85  | °C   |

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

# SN54LVT574, SN74LVT574

## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER            | TEST CONDITIONS  |   |                  | SN54LVT574           |      | SN74LVT574           |      | UNIT |
|----------------------|--|---|------------------|----------------------|------|----------------------|------|------|
|                      |  |   |                  | MIN                  | TYP† | MAX                  | MIN  |      |
| V <sub>IK</sub>      | V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA   |   |                  | −1.2                 |      | −1.2                 |      | V    |
| V <sub>OH</sub>      | V <sub>CC</sub> = MIN to MAX‡, I <sub>OH</sub> = −100 μA   |   |                  | V <sub>CC</sub> −0.2 |      | V <sub>CC</sub> −0.2 |      | V    |
|                      | V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = − 8 mA  |   |                  | 2.4                  |      | 2.4                  |      |      |
|                      | V <sub>CC</sub> = 3 V  | I <sub>OH</sub> = − 24 mA               |                  | 2                    |      |                      |      |      |
|                      |  | I <sub>OH</sub> = −32 mA                |                  |                      |      | 2                    |      |      |
| V <sub>OL</sub>      | V <sub>CC</sub> = 2.7 V  | I <sub>OL</sub> = 100 μA                |                  | 0.2                  |      | 0.2                  |      | V    |
|                      |  | I <sub>OL</sub> = 24 mA                 |                  | 0.5                  |      | 0.5                  |      |      |
|                      | V <sub>CC</sub> = 3 V  | I <sub>OL</sub> = 16 mA                 |                  | 0.4                  |      | 0.4                  |      |      |
|                      |  | I <sub>OL</sub> = 32 mA                 |                  | 0.5                  |      | 0.5                  |      |      |
|                      |  | I <sub>OL</sub> = 48 mA                 |                  | 0.55                 |      |                      |      |      |
|                      |  | I <sub>OL</sub> = 64 mA                 |                  |                      |      | 0.55                 |      |      |
| I <sub>I</sub>       | V <sub>CC</sub> = 0 or MAX‡, V <sub>I</sub> = 5.5 V  |   |                  | 50                   |      | 10                   |      | μA   |
|                      | V <sub>CC</sub> = 3.6 V  | V <sub>I</sub> = V <sub>CC</sub> or GND | Control inputs   | ±1                   |      | ±1                   |      |      |
|                      |  | V <sub>I</sub> = V <sub>CC</sub>        | Data inputs      | 1                    |      | 1                    |      |      |
|                      |  | V <sub>I</sub> = 0                      |                  | −5                   |      | −5                   |      |      |
| I <sub>off</sub>     | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V   |   |                  |                      |      | ±100                 |      | μA   |
| I <sub>I(hold)</sub> | V <sub>CC</sub> = 3 V  | V <sub>I</sub> = 0.8 V                  | Data inputs      | 75                   |      | 75                   |      | μA   |
|                      |  | V <sub>I</sub> = 2 V                    |                  | −75                  |      | −75                  |      |      |
| I <sub>OZH</sub>     | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V  |   |                  | 1                    |      | 1                    |      | μA   |
| I <sub>OZL</sub>     | V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V  |   |                  | −1                   |      | −1                   |      | μA   |
| I <sub>CC</sub>      | V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND                         |   | Outputs high     | 0.13                 | 0.39 | 0.13                 | 0.19 | mA   |
|                      |  |   | Outputs low      | 8.7                  | 14   | 8.7                  | 12   |      |
|                      |  |   | Outputs disabled | 0.13                 | 0.39 | 0.13                 | 0.19 |      |
| ΔI <sub>CC</sub> §   | V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND |   |                  | 0.3                  |      | 0.2                  |      | mA   |
| C <sub>i</sub>       | V <sub>I</sub> = 3 V or 0  |   |                  | 4                    |      | 4                    |      | pF   |
| C <sub>o</sub>       | V <sub>O</sub> = 3 V or 0  |   |                  | 8                    |      | 8                    |      | pF   |

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

|                    |                                 | SN54LVT574                         |     |                         |     | SN74LVT574                         |     |                         |     | UNIT |
|--------------------|---------------------------------|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|-------------------------|-----|------|
|                    |                                 | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 2.7 V |     |      |
|                    |                                 | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX | MIN                     | MAX |      |
| f <sub>clock</sub> | Clock frequency                 | 0                                  | 150 | 0                       | 150 | 0                                  | 150 | 0                       | 150 | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low | 3.3                                |     | 3.3                     |     | 3.3                                |     | 3.3                     |     | ns   |
| t <sub>su</sub>    | Setup time, data before CLK↑    | 2                                  |     | 2.4                     |     | 2                                  |     | 2.4                     |     | ns   |
| t <sub>h</sub>     | Hold time, data after CLK↑      | 0.9                                |     | 0.9                     |     | 0.3                                |     | 0                       |     | ns   |



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**SN54LVT574, SN74LVT574**  
**3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT) | TO<br>(OUTPUT) | SN54LVT574                                    |     |                         |     | SN74LVT574                                    |      |     |                         | UNIT |     |
|------------------|-----------------|----------------|---|-----|-------------------------|-----|---|------|-----|-------------------------|------|-----|
|                  |                 |                | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |      |     | $V_{CC} = 2.7\text{ V}$ |      |     |
|                  |                 |                | MIN   | MAX | MIN                     | MAX | MIN   | TYP† | MAX | MIN                     |      | MAX |
| f <sub>max</sub> |                 |                | 150   |     | 150                     |     | 150   |      |     | 150                     |      | MHz |
| t <sub>PLH</sub> | CLK             | Q              | 1   | 5.9 |                         | 6.6 | 1.7   | 3.6  | 5.4 |                         | 6.2  | ns  |
| t <sub>PHL</sub> |                 |                | 1   | 6.1 |                         | 6.8 | 2.4   | 4.3  | 5.9 |                         | 6.6  |     |
| t <sub>PZH</sub> | $\overline{OE}$ | Q              | 0.5   | 5.9 |                         | 7.1 | 1   | 2.9  | 4.8 |                         | 5.9  | ns  |
| t <sub>PZL</sub> |                 |                | 0.5   | 5.3 |                         | 6.4 | 1.3   | 3.4  | 5.1 |                         | 6.2  |     |
| t <sub>PHZ</sub> | $\overline{OE}$ | Q              | 0.7   | 5.9 |                         | 6.6 | 1.9   | 4    | 5.5 |                         | 5.9  | ns  |
| t <sub>PLZ</sub> |                 |                | 0.5   | 5.1 |                         | 5.1 | 1.7   | 3.2  | 4.5 |                         | 4.5  |     |

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

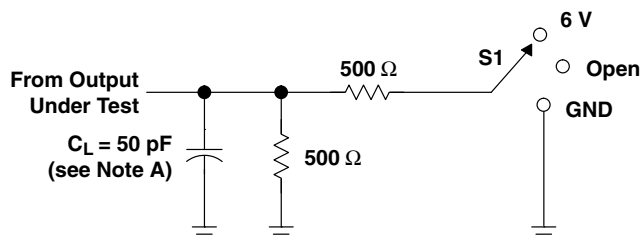
# SN54LVT574, SN74LVT574

## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

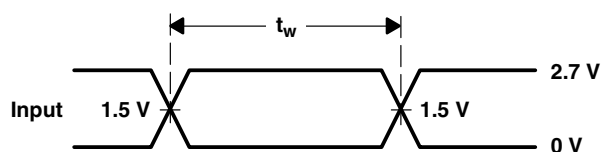
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#### PARAMETER MEASUREMENT INFORMATION

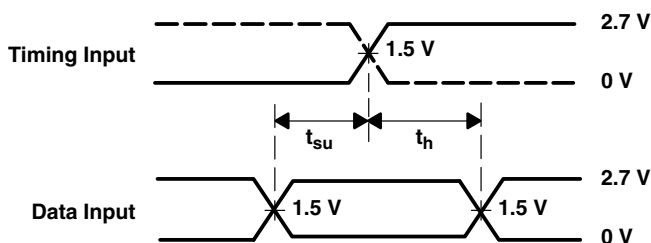


| TEST                               | S1   |
|------------------------------------|------|
| t <sub>PLH</sub> /t <sub>PHL</sub> | Open |
| t <sub>PLZ</sub> /t <sub>PZL</sub> | 6 V  |
| t <sub>PHZ</sub> /t <sub>PZH</sub> | GND  |

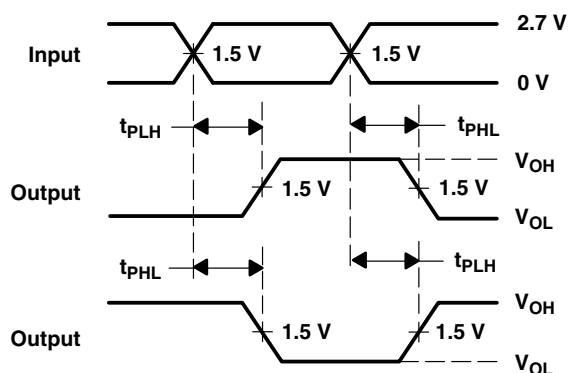
LOAD CIRCUIT FOR OUTPUTS



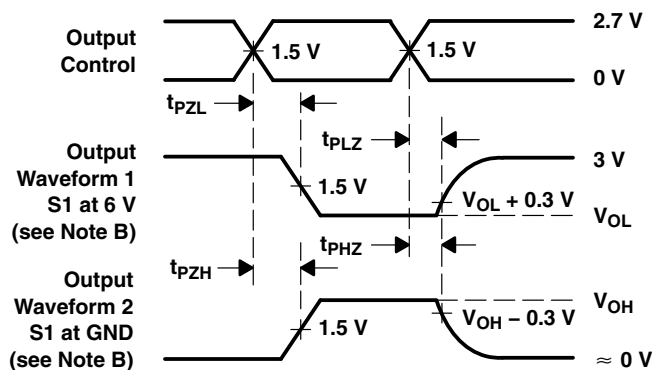
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| SN74LVT574DW     | NRND          | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT574                  |         |
| SN74LVT574DWR    | NRND          | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LVT574                  |         |
| SN74LVT574PWR    | NRND          | TSSOP        | PW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | LX574                   |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVT574DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74LVT574PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVT574DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74LVT574PWR | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

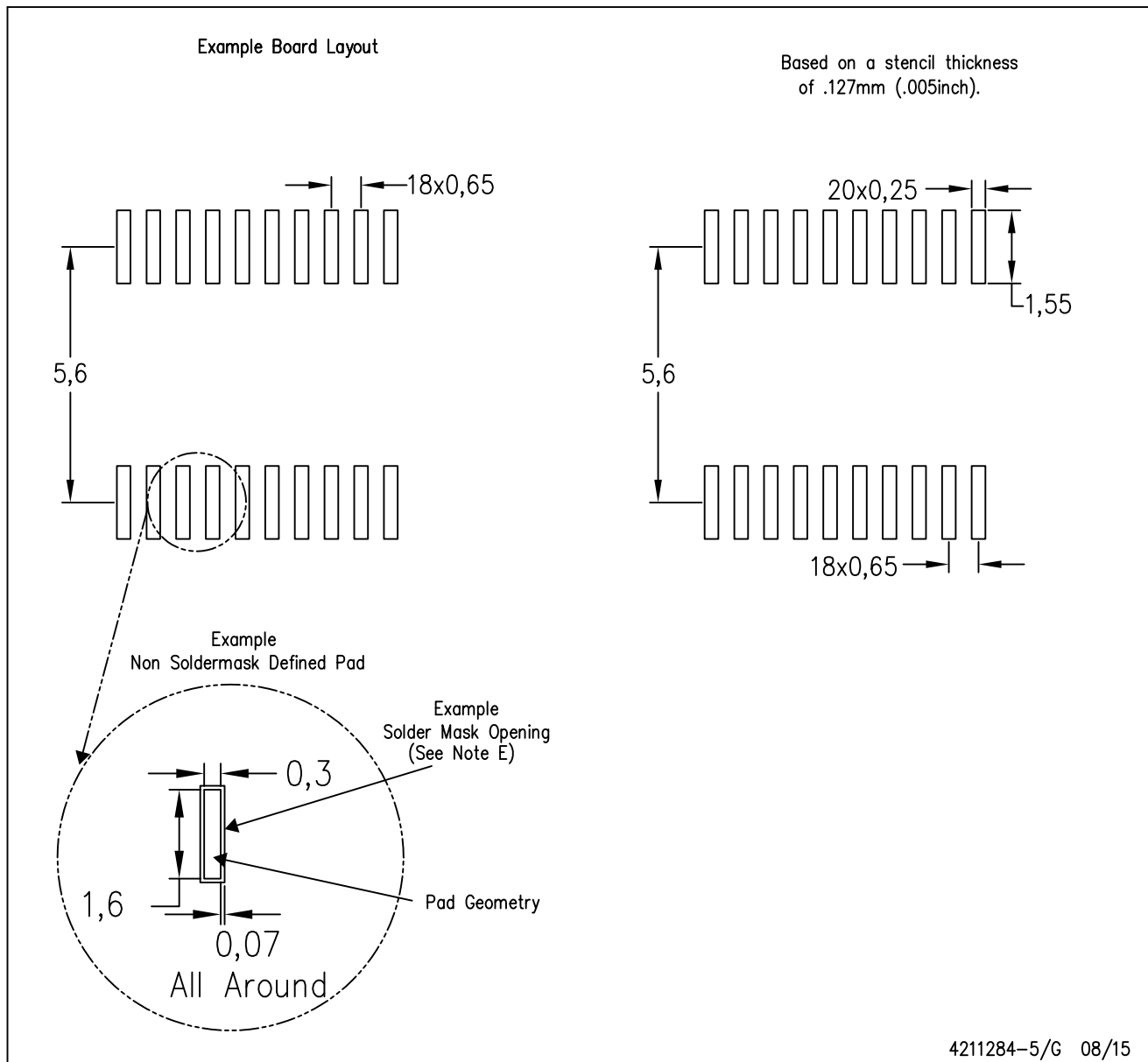


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

## PW (R-PDSO-G20)

# PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

**DW0020A**

## SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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