AK4584

24Bit 96kHz Audio CODEC with DIT/DIR

GENERAL DESCRIPTION

AK4584 is a high-performance 24-bit CODEC for 96kHz consumer audio and digital recording applications. The on-board analog-to-digital converter has an impressive dynamic range, thanks in part to AKM's Enhanced Dual-Bit architecture. The DAC features the newly developed Advanced Multi-Bit architecture and achieves low out-of-band noise and high jitter tolerance through the use of Switched Capacitor Filter (SCF) technology. The AK4584 also has a S/PDIF-AES/EBU digital audio transmitter (DIT) and a digital audio receiver (DIR) that are compatible with 24-bit, 192kHz formats. The AK4584 can automatically detect NON-PCM bit streams like AC-3, MPEG and DTS. Either the ADC or the digital audio input can be routed directly to the digital audio output. The AK4584 has an input Programmable Gain Amplifier and is well suited for computer DAWs, MiniDisc, DVD-R, hard disk and CD-R recording/playback systems.

*AC-3 is a trademark of Dolby Laboratories. DTS is a trademark of Digital Theater Systems, Inc.

FEATURES

1. 24bit 2ch ADC
- **fs: max 96kHz**
- **Single-end Input**
- **S/(N+D): 90dB**
- **Dynamic Range, S/N: 100dB**
- **Digital HPF for offset cancellation**
- **Input PGA with +18dB gain & 0.5dB step**
- **Input DATT with –72dB ATT**
- **I/F format: MSB justified or I^2S**

2. 24bit 2ch DAC
- **fs: max 192kHz**
- **24bit 8 times Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 75dB**
- **Single-end Output**
- **S/(N+D): 94dB**
- **Dynamic Range, S/N: 104dB**
- **De-emphasis for 32kHz, 44.1kHz, 48kHz sampling**
- **Digital Attenuator with soft-transition**
- **Soft Mute**
- **Zero Detect Function**
- **I/F format: MSB justified, LSB justified or I^2S**

3. 3 Outputs 24 bit 192kHz DIT
- **3-Channel Transmission Outputs (2 Through outputs & DIT Output)**
- **40 bits Channel Status Buffer**

4. 4 Inputs 24bit 192kHz DIR
- **Supports AES3, IEC60958, S/PDIF, EIAJ CP1201**
- **Low Jitter Analog PLL**
- **PLL Lock Range: 32k ~ 192kHz**
- **Clock Source: PLL or X'tal**
- **4 Digital Receive Channel inputs**
- **Detect Function**
  - **Non-PCM Bit Stream Detection**
  - **DTS-CD Bit Stream Detection**
  - **Validity Flag Detection**
  - **Sampling Frequency Detection**
  - **Unlock & Parity Error Detection**
- **40 bits Channel Status Buffer**
- **Burst Preamble bit Pc, Pd Buffer for Non-PCM bit Stream**

5. Support External Audio Clock Input
- **Master Clock Input**
  - **256fs, 384fs, 512fs, 768fs (fs = 44.1kHz ~ 48kHz)**
  - **256fs, 384fs (fs = 88.2kHz ~ 96kHz)**
  - **128fs, 192fs (fs = 176.4kHz ~ 192kHz)**

6. Support Master & Slave Mode

7. Serial μP I/F: 4-wire serial

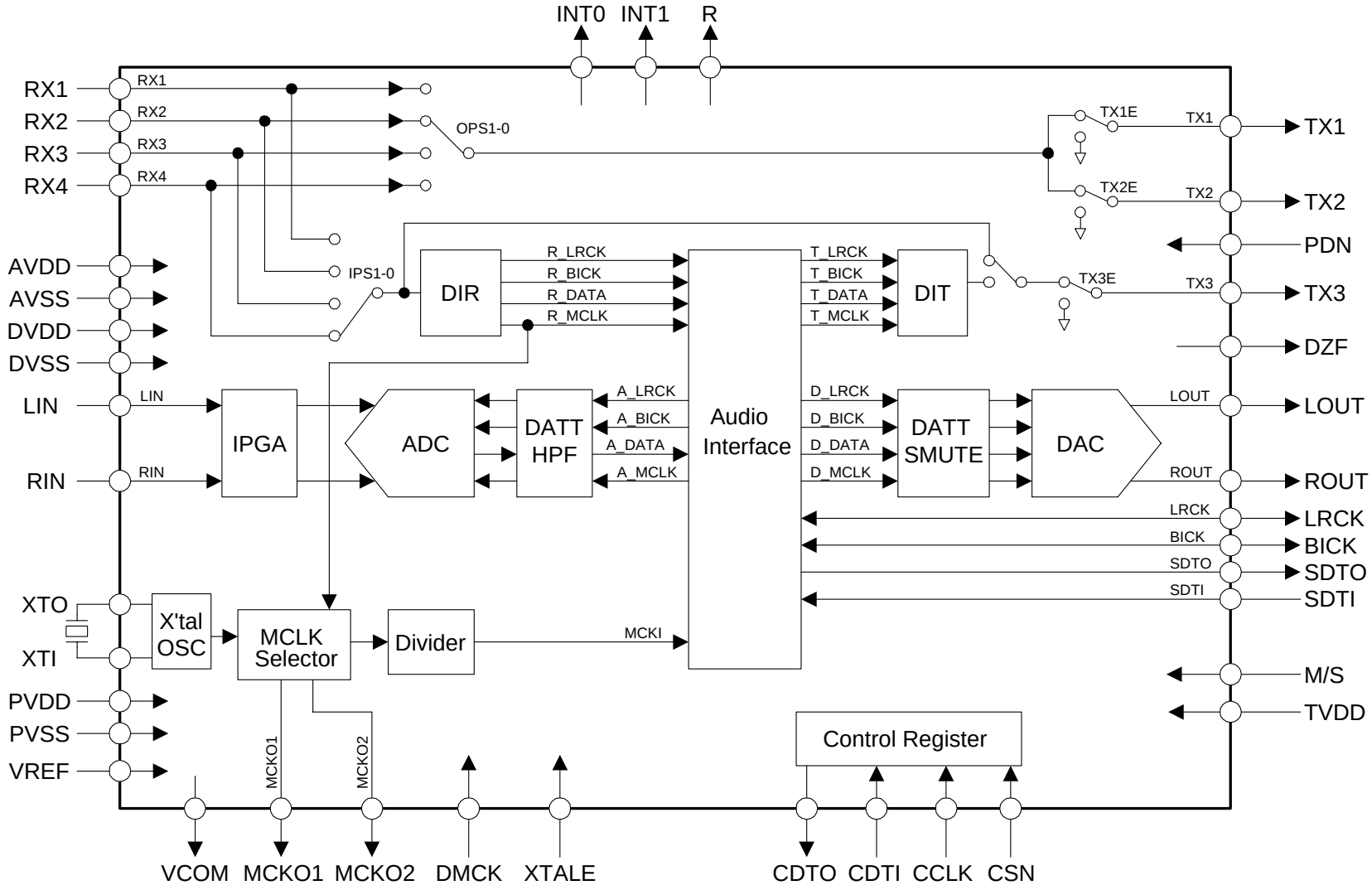
8. 5V operation

9. 3V Power Supply Pin for 3V I/F

10. 44pin LQFP Package

11. Ta: –10 to 70°C

■ Block Diagram

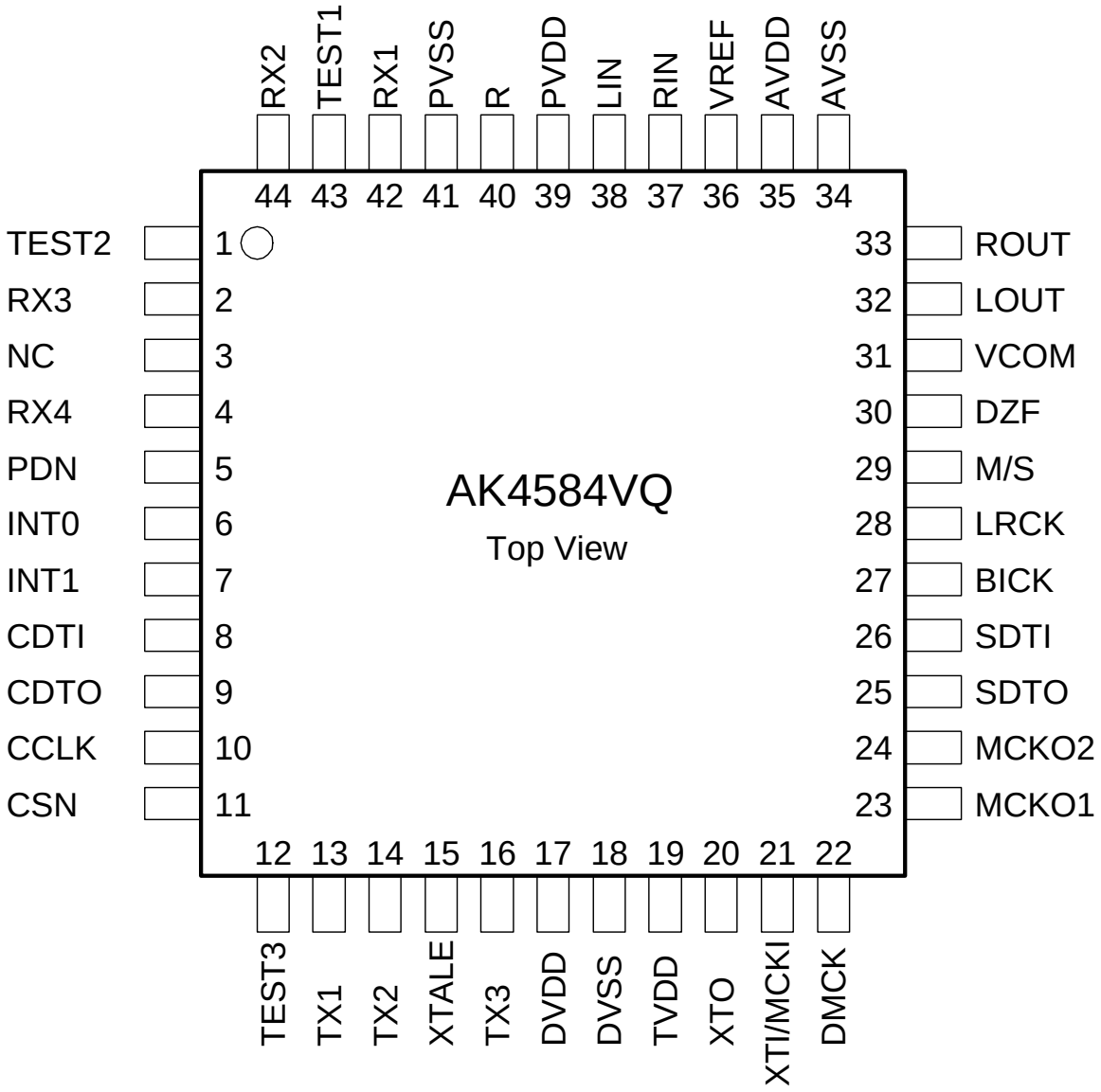


Block Diagram

■ Ordering Guide

AK4584VQ	−10 ~ +70°C	44pin LQFP (0.8mm pitch)
AKD4584	Evaluation Board for AK4584	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	TEST2	I	Test 2 Pin (Internal pull-down pin)
2	RX3	I	Receiver Input 3 with Amp for 0.2Vpp
3	NC	I	NC Pin (No Internal bonding pin, Fixed to "AVSS")
4	RX4	I	Receiver Input 4 with Amp for 0.2Vpp
5	PDN	I	Power-Down Mode Pin "H": Power up, "L": Power down reset and initialize the control registers.
6	INT0	O	Interrupt 0 Pin
7	INT1	O	Interrupt 1 Pin
8	CDTI	I	Control Data Input Pin
9	CDTO	O	Control Data Output Pin
10	CCLK	I	Control Data Clock Pin
11	CSN	I	Chip Select Pin
12	TEST3	I	Test 3 Pin (Fixed to AVSS)
13	TX1	O	Transmitter 1 Output Pin
14	TX2	O	Transmitter 2 Output Pin
15	XTALE	I	X'tal Osc Enable Pin "H" : Enable, "L" : Disable
16	TX3	O	Transmitter 3 Output Pin
17	DVDD	-	Digital Power Supply Pin, 4.75 ~ 5.25V
18	DVSS	-	Digital Ground Pin
19	TVDD	-	Output Buffer Power Supply Pin, 2.7 ~ 5.25V
20	XTO	O	X'tal Output Pin
21	XTI	I	X'tal Input Pin
	MCKI	I	External Master Clock Input Pin
22	DMCK	I	MCKO1 Disable Pin "H" : MCKO1 "L" output, "L" : MCKO1 output

23	MCKO1	O	Master Clock Output 1 Pin
24	MCKO2	O	Master Clock Output 2 Pin
25	SDTO	O	Audio Serial Data Output Pin
26	SDTI	I	Audio Serial Data Input Pin
27	BICK	I/O	Audio Serial Data Clock Pin
28	LRCK	I/O	Input / Output Channel Clock Pin
29	M/S	I	Master / Slave Mode Pin "H" : Master Mode, "L" : Slave Mode
30	DZF	O	Zero Input Detect Pin
31	VCOM	O	Common Voltage Output Pin, AVDD/2 Bias voltage of ADC inputs and DAC outputs.
32	LOUT	O	Lch Analog Output Pin
33	ROUT	O	Rch Analog Output Pin
34	AVSS	-	Analog Ground Pin
35	AVDD	-	Analog Power Supply Pin, 4.75 ~ 5.25V
36	VREF	I	Voltage Reference Input Pin, AVDD Used as a voltage reference by ADC & DAC. VREF is connected externally to filtered AVDD.
37	RIN	I	Rch Analog Input Pin
38	LIN	I	Lch Analog Input Pin
39	PVDD	-	PLL Power Supply Pin, 4.75 ~ 5.25V
40	R	-	External Resistor Pin for PLL **13kΩ ± 1% resistor to PVSS externally.**
41	PVSS	-	PLL Ground Pin
42	RX1	I	Receiver Input 1 with Amp for 0.2Vpp
43	TEST1	I	Test 1 Pin (Internal pull-down pin)
44	RX2	I	Receiver Input 2 with Amp for 0.2Vpp

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
	PLL	PVDD	–0.3	6.0	V
	Output Buffer	TVDD	–0.3	6.0	V
	|AVSS – DVSS| (Note 2)	ΔGND1	-	0.3	V
	|AVSS – PVSS| (Note 2)	ΔGND2	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (VREF, LIN, RIN pins)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage 1 (Except RX1-4, BICK, LRCK pins)		VIND1	–0.3	DVDD+0.3	V
Digital Input Voltage 2 (RX1-4 pins)		VIND2	–0.3	PVDD+0.3	V
Digital Input Voltage 3 (BICK, LRCK pins)		VIND3	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note: 1. All voltages with respect to ground.
Note: 2. AVSS, DVSS and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS, PVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	AVDD	V
	PLL	PVDD	4.75	5.0	AVDD	V
	Output Buffer	TVDD	2.7	3.0	DVDD	V
Voltage Reference (Note 4)		VREF	3.0	-	AVDD	V

Note: 1. All voltages with respect to ground.
Note: 3. The power up sequence between AVDD, DVDD, PVDD and TVDD is not critical.
Note: 4. Normally, VREF voltage is the same as AVDD voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=TVDD=5.0V; AVSS=DVSS=PVSS=0V; VREF=AVDD; fs=44.1kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=10Hz ~ 20kHz at fs=44.1kHz, 10Hz ~ 40kHz at fs=96kHz; 10Hz ~ 80kHz at fs=192kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
Input PGA Characteristics:					
Input Voltage (Note 5)	fs=44.1kHz, AIN=0.6 x AVDD	2.8	3.0	3.2	Vpp
	fs=96kHz, AIN=0.62 x AVDD	2.9	3.1	3.3	Vpp
Input Resistance		5	10	15	kΩ
Step Size		0.2	0.5	0.8	dB
Gain Control Range		0		18	dB
ADC Analog Input Characteristics: IPGA=0dB					
Resolution				24	Bits
S/(N+D) (-0.5dBFS)	fs=44.1kHz	84	90		dB
	fs=96kHz	80	88		dB
DR (-60dBFS)	fs=44.1kHz, A-weighted	94	100		dB
	fs=96kHz	88	96		dB
S/N	fs=44.1kHz, A-weighted	94	100		dB
	fs=96kHz	88	96		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Power Supply Rejection (Note 6)			50	-	dB
DAC Analog Output Characteristics:					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=44.1kHz	88	94		dB
	fs=96kHz	86	92		dB
	fs=192kHz	-	84		dB
DR (-60dBFS)	fs=44.1kHz, A-weighted	98	104		dB
	fs=96kHz	90	98		dB
	fs=192kHz	-	85		dB
S/N	fs=44.1kHz, A-weighted	98	104		dB
	fs=96kHz	90	98		dB
	fs=192kHz	-	85		dB
Interchannel Isolation		90	100		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			20	-	ppm/°C
Output Voltage (Note 7)		2.8	3.0	3.2	Vpp
Load Resistance		5			kΩ
Load Capacitance				25	pF
Power Supply Rejection (Note 6)			50	-	dB

Note: 5. Full scale (0dB) of the input voltage at IPGA = 0dB.
Note: 6. PSR is applied to AVDD, DVDD, PVDD and TVDD with 1kHz, 50mVpp.VREF pin is held a constant voltage.
Note: 7. This voltage is proportional to VREF. Vout = 0.6 x VREF.

Parameter		min	typ	max	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN = "H")					
AVDD			23	35	mA
PVDD	(fs=44.1kHz)		12	18	mA
DVDD+TVDD	(fs=44.1kHz)		24	36	mA
	(fs=96kHz)		36	54	mA
Power-down mode (PDN = "L")	(Note 8)				
AVDD			10	100	μA
PVDD			10	100	μA
DVDD+TVDD			10	100	μA

Note: 8. All digital input pins are held DVDD or DVSS.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V; TVDD=2.7 ~ 5.25V)

Parameter	Symbol	min	typ	Max	Unit
Input Resistance	Zin		10		kΩ
Input Voltage	VTH	200			mVpp
Input Hysteresis	VHY	-	50		mV
Input Sample Frequency	fs	32	-	192	kHz

FILTER CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V; TVDD=2.7 ~ 5.25V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	±0.005dB	PB	0		19.76	kHz
	-0.02dB		-	20.02	-	kHz
	-0.06dB		-	20.20	-	kHz
	-6.0dB		-	22.05	-	kHz
Stopband		SB	24.34			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 10)		GD		31		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	-3dB	FR		0.9		Hz
	-0.5dB			2.7		Hz
	-0.1dB			6.0		Hz
DAC Digital Filter:						
Passband (Note 9)	±0.01dB	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	75			dB
Group Delay (Note 10)		GD		30		1/fs
DAC Digital Filter + SCF + SMF:						
Frequency Response:		FR				
0 ~ 20.0kHz				−0.1		dB
~ 40kHz (Note 11)				−0.2		dB
~ 80kHz (Note 12)				−1.0		dB

Note: 9. The passband and stopband frequencies scale with fs. For example, 20.02kHz at −0.02dB is 0.454 x fs.

Note: 10. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.
For DAC, this time is from setting the 24bit data of both channels on DAC input register to the output of an analog signal.

Note: 11. fs = 96kHz.

Note: 12. fs = 192kHz.

DC CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V; TVDD=2.7 ~ 5.25V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage					
(Except XTI pin)	VIH	2.2	-	-	V
(XTI pin)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage					
(Except XTI pin)	VIL	-	-	0.8	V
(XTI pin)	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (XTI pin, Note 13)	VAC	40%DVDD	-	-	Vpp
High-Level Output Voltage					
(Except TX1-3, DZF pins : Iout=−400μA)	VOH	TVDD-0.5	-	-	V
(TX1-3 pin : Iout=−400μA)	VOH	DVDD-0.5	-	-	V
(DZF pin : Iout=−400μA)	VOH	AVDD-0.5	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.5	V
TX Output Voltage Level (Note 14)	VOH	0.4	0.5	0.6	V
Input Leakage Current	Iin	-	-	±10	μA

Note: 13. In case of connecting capacitance to XTI pin. (Refer to Figure 3)
Note: 14. Refer to Figure 7.

SWITCHING CHARACTERISTICS

(Ta=−10 ~ 70°C; AVDD=DVDD=PVDD=4.75 ~ 5.25V, TVDD=2.7 ~ 5.25V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
Master Clock Timing						
Crystal Resonator	Frequency		11.2896		24.576	MHz
External Clock	Frequency	fCLK	11.2896		36.864	MHz
	Pulse Width Low	tCLKL	0.4/fCLK			ns
	Pulse Width High	tCLKH	0.4/fCLK			ns
MCKO1 Output	Frequency	fMCK	11.2896		24.576	MHz
	Duty Cycle (Note 15)	dMCK	40	50	60	%
MCKO2 Output	Frequency	fMCK	5.6448		18.432	MHz
	Duty Cycle	dMCK	40	50	60	%
PLL Clock Recover Frequency		fPLL	32		192	kHz
LRCK Frequency						
Normal Speed Mode (DFS0="0", DFS1="0")		fsn	32		48	kHz
Double Speed Mode (DFS0="1", DFS1="0")		fsd	88.2		96	kHz
Quad Speed Mode (DFS0="0", DFS1="1")		fsq	176.4		192	kHz
Duty Cycle	Slave mode		45		55	%
	Master mode			50		%
Audio Interface Timing						
Slave mode						
BICK Period		tBCK	81			ns
BICK Pulse Width Low		tBCKL	33			ns
Pulse Width High		tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 16)		tLRB	20			ns
BICK "↑" to LRCK Edge (Note 16)		tBLR	20			ns
LRCK to SDTO (MSB) (Except I^2S mode)		tLRS			20	ns
BICK "↓" to SDTO		tBSD			20	ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
Master mode						
BICK Frequency		fBCK		64fs		Hz
BICK Duty		dBCK		50		%
BICK "↓" to LRCK		tMBLR	–20		20	ns
BICK "↓" to SDTO		tBSD	–20		20	ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns

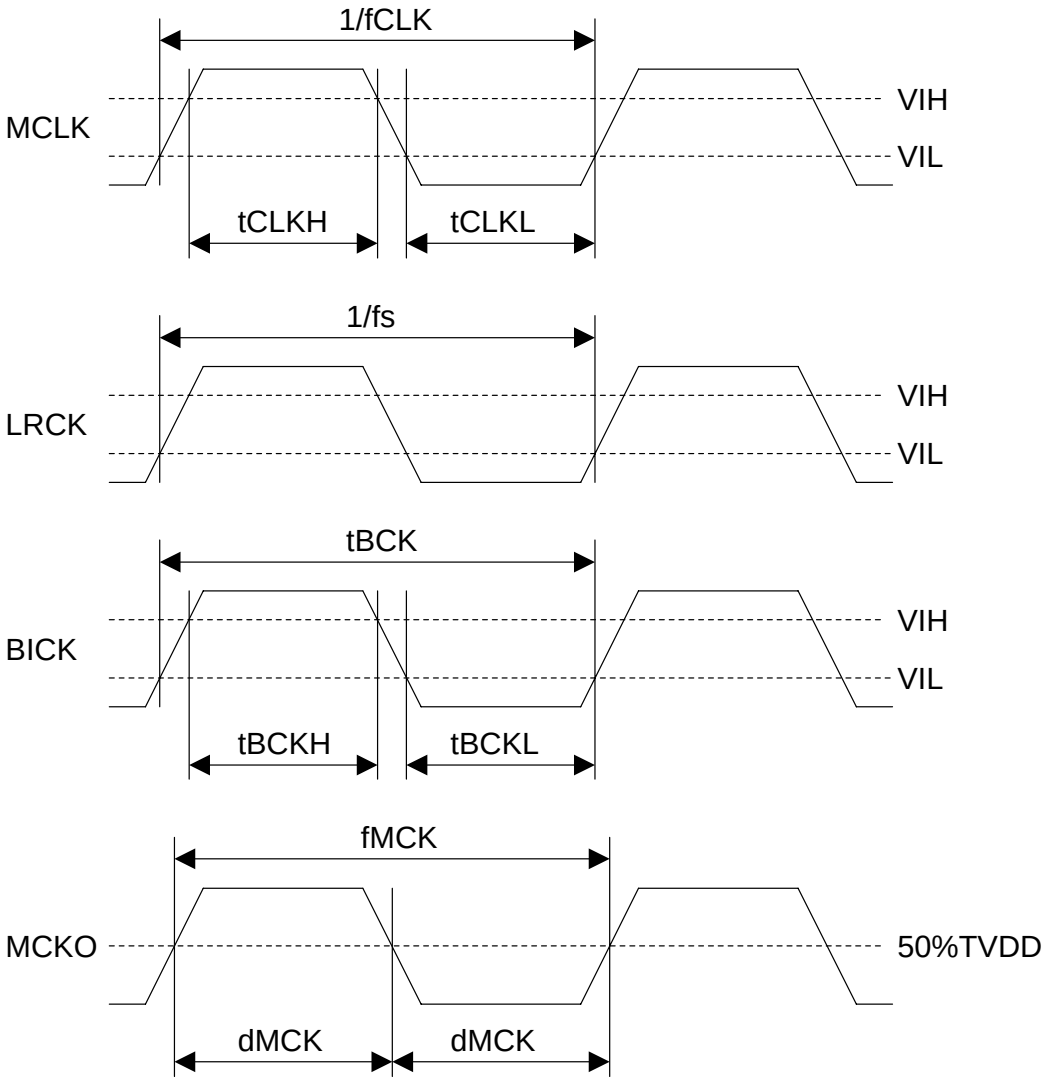
Note: 15. Duty cycle is not guaranteed when using the external clock input.

Note: 16. BICK rising edge must not occur at the same time as LRCK edge.

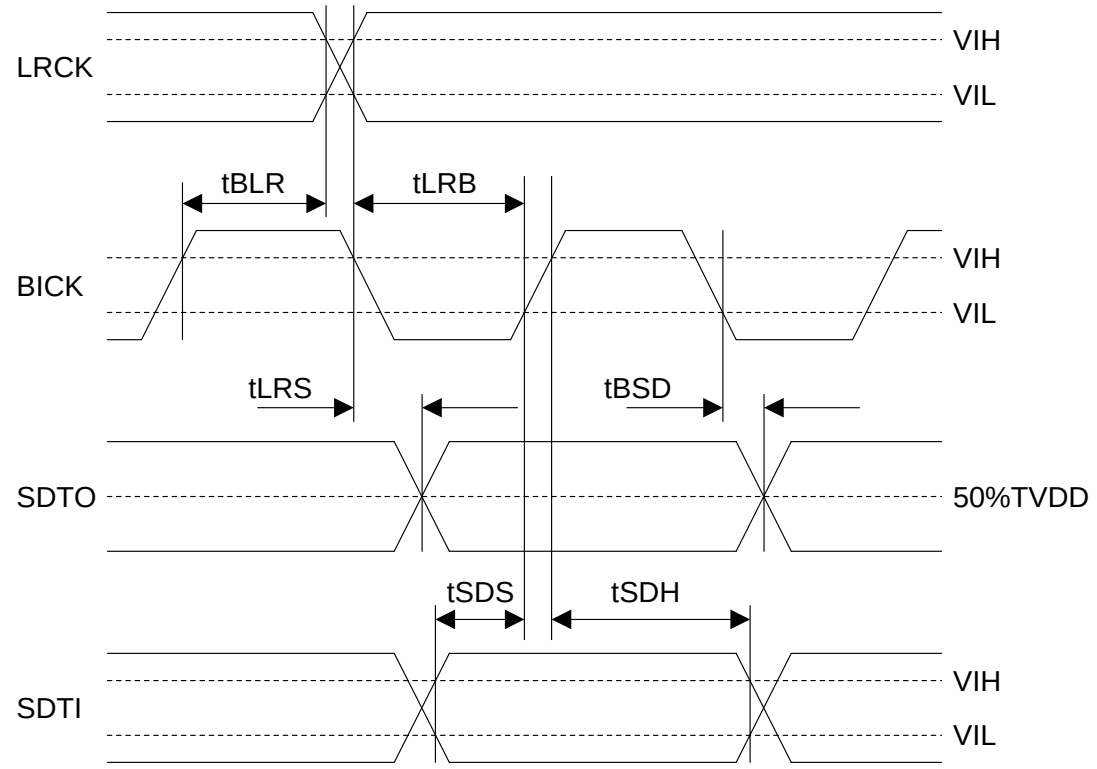
Parameter	Symbol	min	typ	max	Unit
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			45	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Reset Timing					
PDN Pulse Width (Note 17)	tPD	150			ns
RSTADN "↑" to SDTO valid (Note 18)	tPDV		516		1/fs

Note: 17. The AK4584 can be reset by bringing PDN pin = "L".
Note: 18. This cycle is the number of LRCK rising edges from the RSTADN bit.

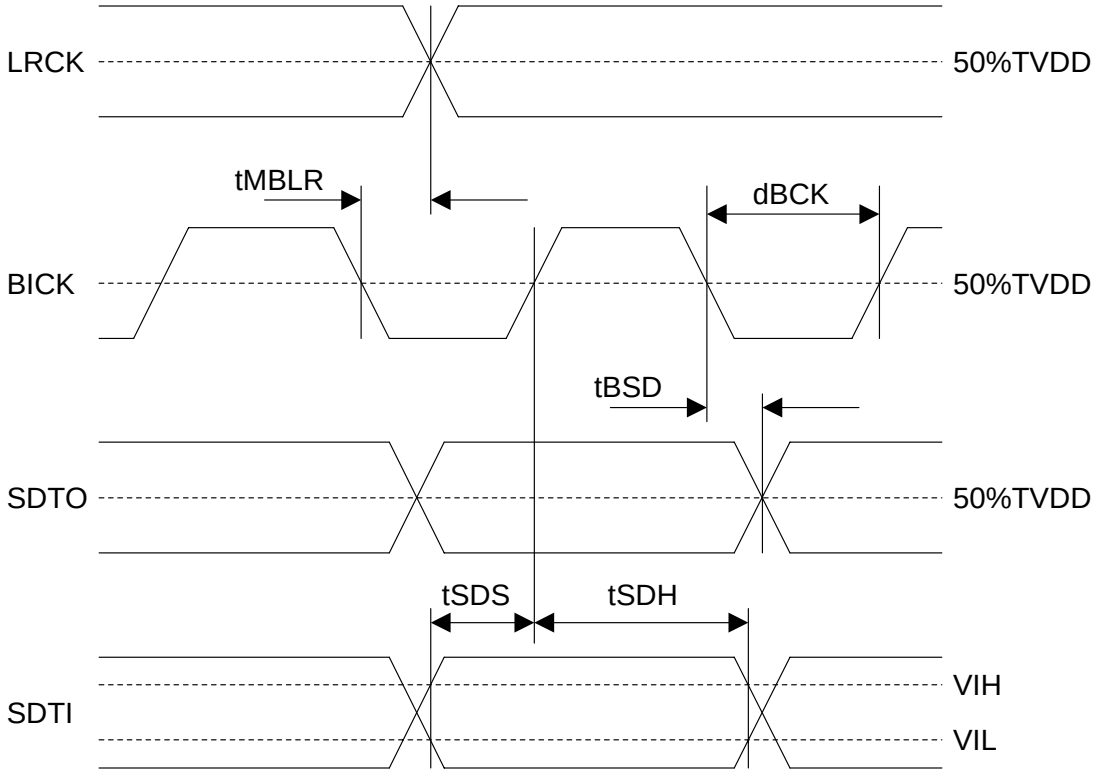
■ **Timing Diagram**



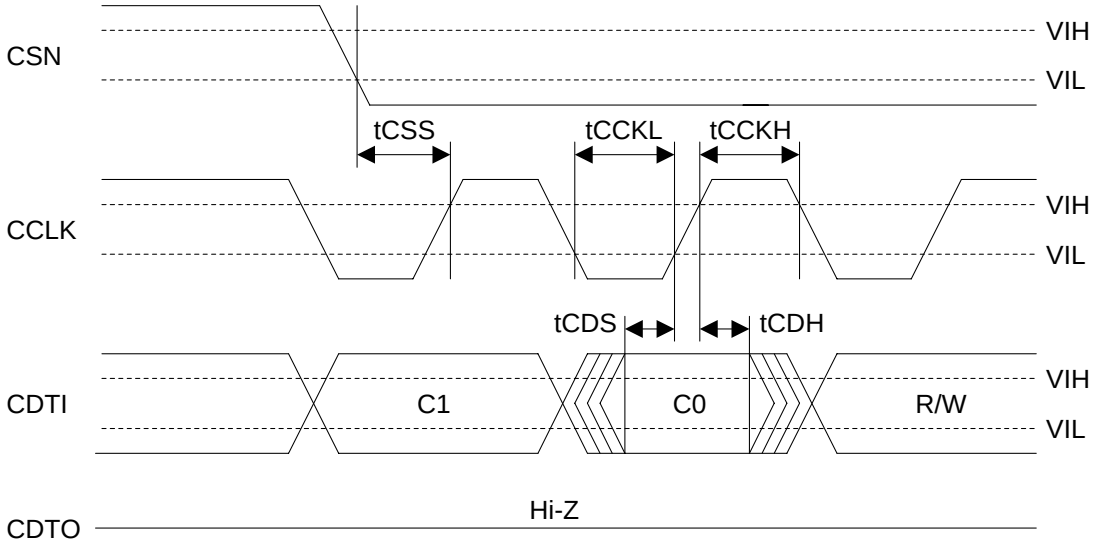
Clock Timing



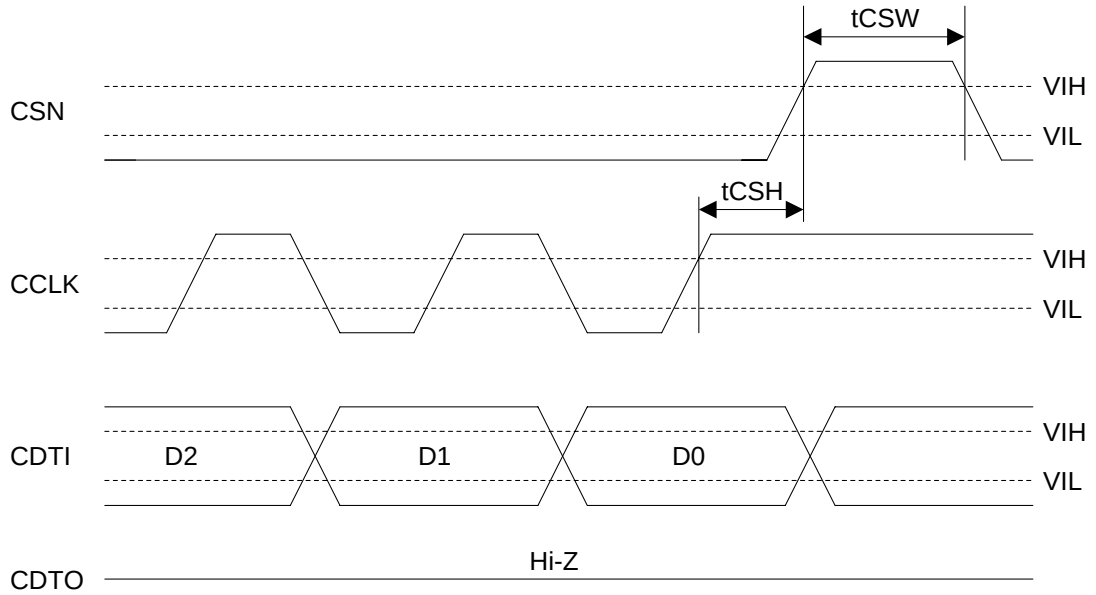
Audio Interface Timing (Slave mode)



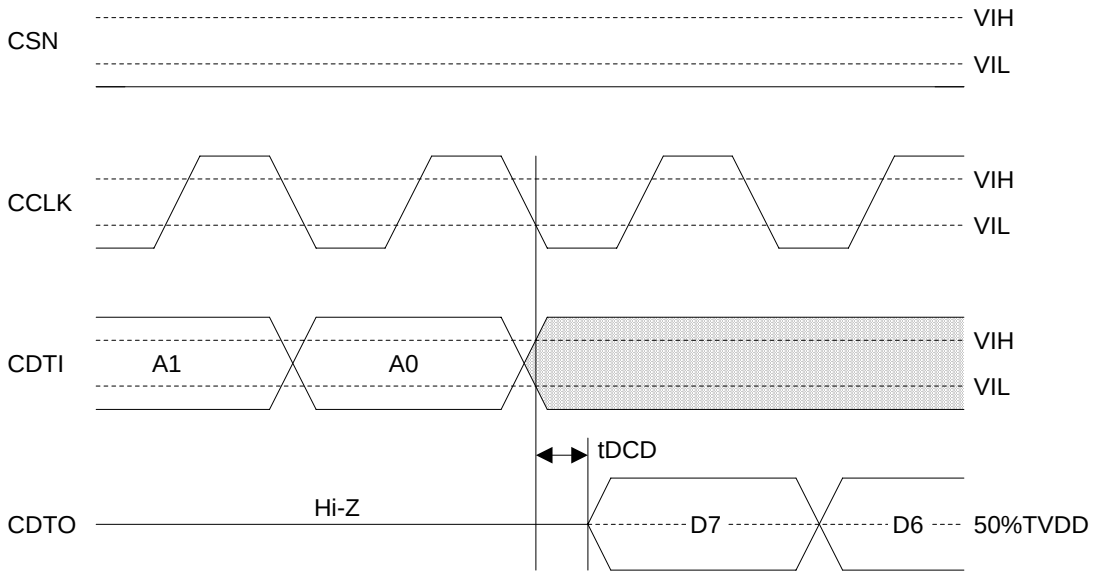
Audio Interface Timing (Master mode)



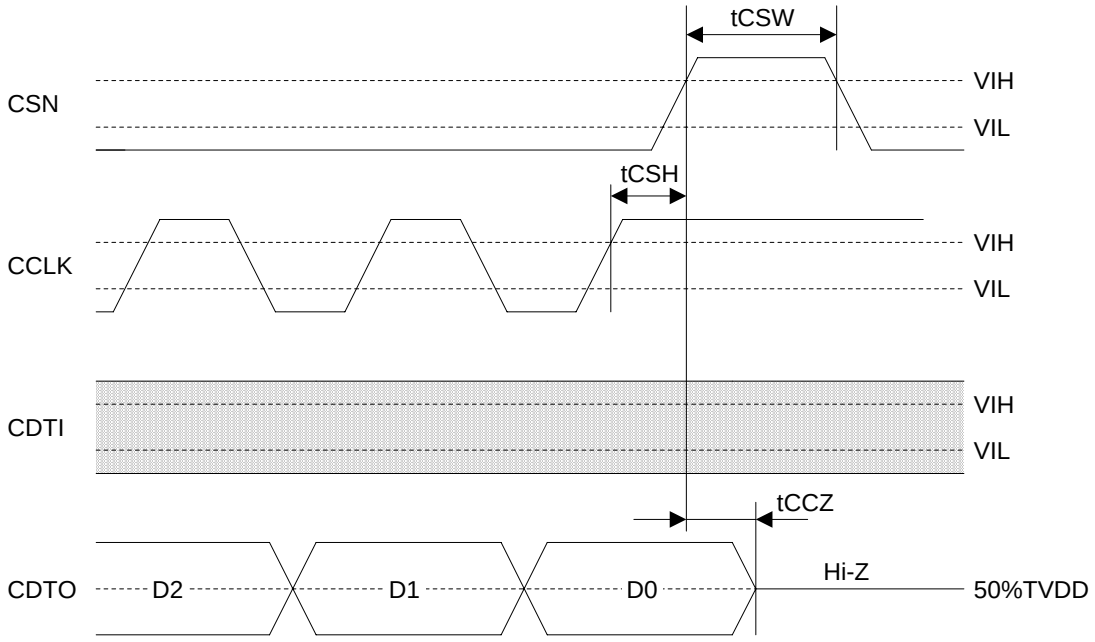
WRITE/READ Command Input Timing



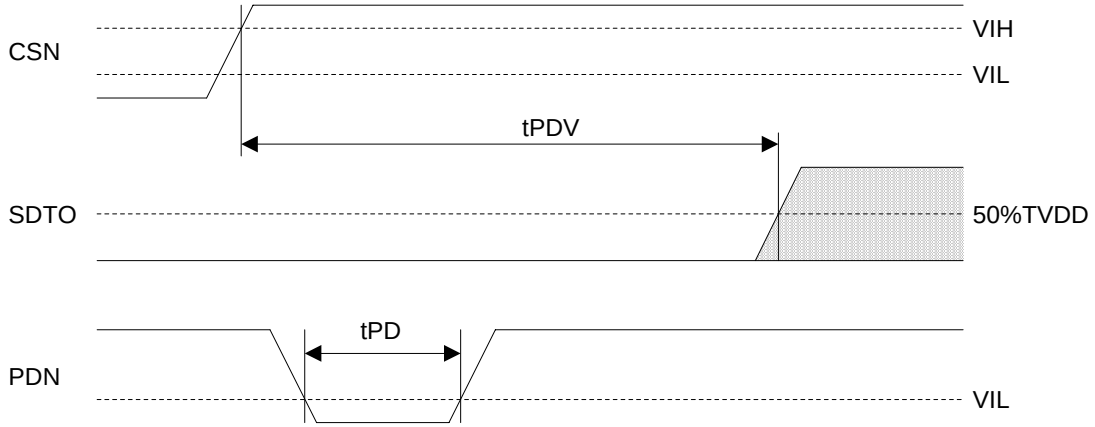
WRITE Data Input Timing



READ Data Output Timing 1



READ Data Output Timing 2



Power Down & Reset Timing

OPERATION OVERVIEW

■ Internal Signal Path

The input source of the DAC and SDTO can be switched between the outputs of the ADC, SDTI or the DIR. The input source of the DIT can be switched between the outputs of ADC or SDTI. There is also a through/bypass path from the DIR to the DIT that can be also selected. The Switch Names (DAC1-0 etc) in Figure 1 correspond to the register bits that control the switch function. Refer to "Register Definitions" (Address 08H).

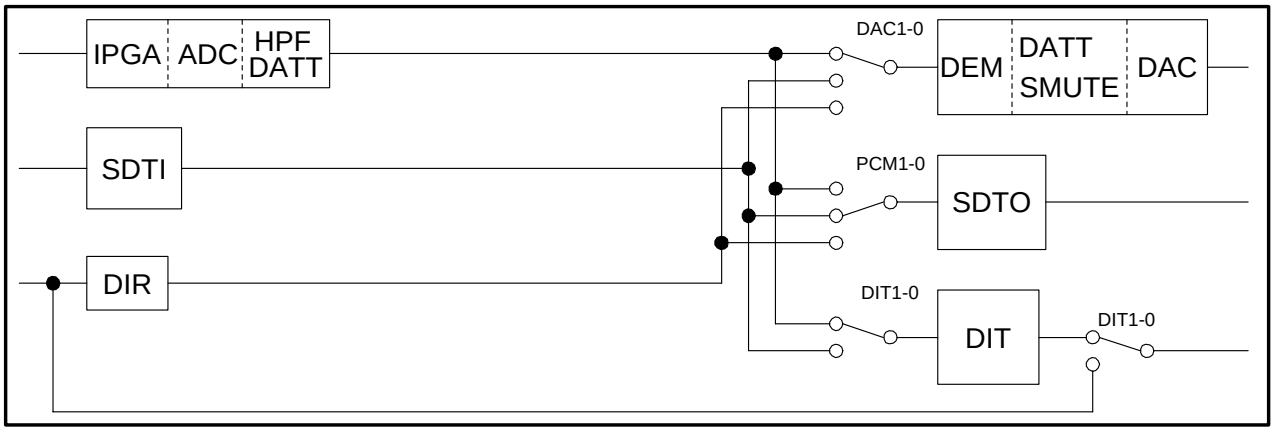


Figure 1. Connection between Input Sources & Output Sources

■ Clock Operation Mode

The CM1-0 bits determine the clock source of the AK4584; either PLL or X'tal (including external clock source, Table 1). In mode 2, the clock source is switched automatically from PLL to X'tal when the PLL loses lock. In mode 3, the clock source is fixed to the external X'tal input, however the PLL is also operating enabling the monitoring of recovered data such as C bits. For mode 2 and mode 3, the frequency of the X'tal should be different from that of the recovered frequency from PLL. When XTL1-0 bits are "11", the X'tal oscillator is stopped in mode 0. The default values are "01" for CM1-0 bits.

Since the signal path is not changed automatically when changing the CM1-0 bits, the output source should be selected by changing register 08H.

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock Source	
0	0	0	-	ON	*	PLL	
1	0	1	-	OFF	ON	X'tal	Default
2	1	0	0	ON	ON	PLL	
			1	ON	ON	X'tal	
3	1	1	-	ON	ON	X'tal	

ON: Oscillation (Power-up), OFF: STOP (Power-down)
* : OFF at XTALE pin = "L" and XTL1-0 bits = "11", ON at others
Table 1. Clock Operation Mode Select

■ Master Clock Output

The AK4584 has two clock outputs, MCKO1 and MCKO2. These clocks are derived from either the recovered clock or the X'tal oscillator. In PLL mode, the master clock output frequencies (MCKO1, MCKO2) are set by OCKS1-0 bits as shown in Table 2. In the X'tal mode or external clock mode, the frequency of MCKO1 is the same as the X'tal or external clock. MCKO2 outputs a half frequency of MCKO1 (Table 3). MCKO1 output can be disabled by the DMCK pin. MCKO1 output is "L" (Disable) when the DMCK pin = "H", MCKO1 output is normal output when the DMCK pin = "L". In PLL mode, mode 0 does not support 96kHz. The default values of OCKS1-0 bits are "01"

Mode	OCKS1	OCKS0	MCKO1	MCKO2	fs	
0	0	0	512fs	256fs	~ 48kHz	
1	0	1	256fs	128fs	~ 96kHz	Default
2	1	0	128fs	64fs	~ 192kHz	
3	1	1	64fs	32fs	~ 192kHz	

Table 2. Master Clock Output Frequency Select (PLL Mode)

X'tal	MCKO1	MCKO2
11.2896MHz	11.2896MHz	5.6448MHz
12.288MHz	12.288MHz	6.144MHz
24.576MHZ	24.576MHz	12.288MHz

Table 3. Master Clock Output Frequency Select (X'tal Mode)

Table 4 is a connection example when using AK5394 and AK4394 in slave mode.

	AK5394	AK4394
Clock Output	MCKO2	MCKO1
Normal Speed	256fs	512fs
Double Speed	128fs	256fs
Quad Speed	64fs	128fs

Table 4. Clock Select for AK5394 & AK4394

■ System Clock

The master clock (MCLK) is derived from either a X'tal oscillator or the recovered clock from the AK4584's PLL. MCLK frequency is set by ICKS1-0 bits (Table 5) for X'tal mode and external clock mode. The sampling speed (normal, double or quad speed modes) is selected by DFS1-0 bits (Table 6). The ADC is powered down during quad speed mode.

When using a X'tal oscillator, external loading capacitors between XTI/XTO pins and DVSS are required. An external clock can be input to the XTI pin with the XTO pin left floating. The input can accept both CMOS and AC coupled clock sources with 40%DVDD.

In slave mode, the LRCK clock input must be synchronized with MCLK, however the phase is not critical. All external clocks (MCLK, BICK and LRCK) must be present unless PDN pin = "L" or all parts are powered down by control register, otherwise excessive current may be produced by the internal dynamic logic. In master mode, the master clock (MCLK) must be provided by a X'tal oscillator, external clock or internal PLL unless PDN pin = "L".

			MCLK			
Mode	ICKS1	ICKS0	Normal (DFS1-0 = "00")	Double (DFS1-0 = "01")	Quad (DFS1-0 = "10")	
0	0	0	256fs	N/A	N/A	Default
1	0	1	384s	N/A	N/A	
2	1	0	512fs	256fs	128fs	
3	1	1	768fs	384fs	192fs	

Table 5. Master Clock Input Frequency Select (X'tal Mode)

DFS1	DFS0	Sampling Rate	
0	0	Normal Speed	Default
0	1	Double Speed	
1	0	Quad Speed	
1	1	N/A	

Table 6. Sampling Speed

MCLK Normal		MCLK Double		MCLK Quad	
	fs=44.1kHz		fs=88.2kHz		fs=176.4kHz
256fs	11.2896MHz	128fs	N/A	64fs	N/A
384fs	16.9344MHz	192fs	N/A	96fs	N/A
512fs	22.5792MHz	256fs	22.5792MHz	128fs	22.5792MHz
768fs	33.8688MHz	384fs	33.8688MHz	192fs	33.8688MHz

MCLK Normal		MCLK Double		MCLK Quad	
	fs=48kHz		fs=96kHz		fs=192kHz
256fs	12.288MHz	128fs	N/A	64fs	N/A
384fs	18.432MHz	192fs	N/A	96fs	N/A
512fs	24.576MHz	256fs	24.576MHz	128fs	24.576MHz
768fs	36.864MHz	384fs	36.864MHz	192fs	36.864MHz

Table 7. Master Clock Frequencies example

* X'tal mode supports from 11.2896MHz to 24.576MHz.
* Frequencies over 24.576MHz are supported in external clock mode only.

■ Clock Source

(1) Using X'tal

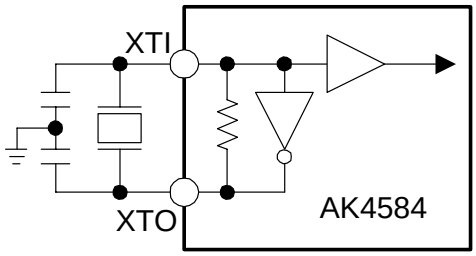


Figure 2. X'tal mode
- Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

(2) Using external clock

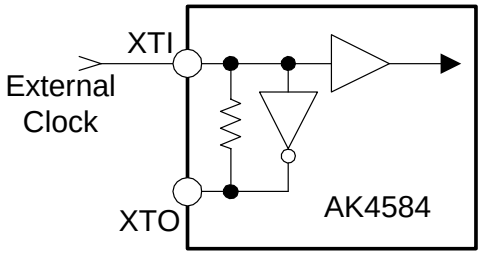


Figure 3. (a) External Clock mode
(Input : CMOS Level)

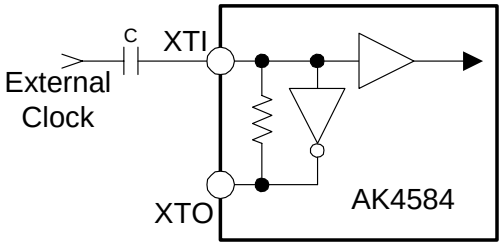


Figure 3. (b) External Clock Mode
(Input : ≥ 40%DVDD)

- Note: Input clock must not exceed DVDD.

(3) Clock Operation Mode 0

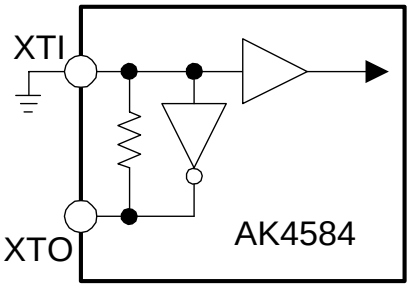


Figure 4. Off mode

■ 192kHz Clock Recovery

The on chip low jitter PLL has a wide lock range from 32kHz to 192kHz and a lock time of less than 20ms. The AK4584 also has a sampling frequency detect function that works by performing either a clock comparison against the X'tal oscillator or by using the channel status. The AK4584 detects the following sampling frequencies : 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz. The PLL loses lock when the incoming sync interval is incorrect.

■ Biphase Input

Four receiver inputs (RX1-4 pins) are available. Each input includes an unbalanced input amplifier and can accept input signals of 200mV or more.

IPS1	IPS0	Input Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 8. Recovery Data Select

■ Biphase Output

The AK4584 can output the through data from the digital receiver inputs (RX1-4) to the TX1/2 pins. The TX3 pin can output transmitter data (SDTI data, A/D converted data and through output from the DIR). The OPS1-0 bits can select the source of the output from the TX1-2 pins and the DIT1-0 bits can select the source of the TX3 pin.

The first 5 bytes of C-bit (Channel Status) can be controlled by CT39-CT0 bits in the control registers. When CT0 bit = "0" (consumer mode), bits20-23 (Audio channel) cannot be controlled directly. When the TCH bit is "1", the AK4584 outputs "1000" as CT20-23 bits for left channel and outputs "0100" at CT20-23 bits for right channel automatically. When TCH bit is "0", the AK4584 outputs "0000".

The U bit (User Data) output has two formats. When the UDIT bit is "0", the U bit is always "L". When UDIT bit is "1", the recovered U bits are passed through the DIT (DIR-DIT loop mode of U bit). This mode is only available when the PLL is locked. When PLL is unlocked, the U bit is set to "L".

OPS1	OPS0	Output Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 9. Output Data Select for TX1/2

DIT1	DIT0	Input Source	
0	0	ADC	Default
0	1	SDTI	
1	0	DIR	
1	1	N/A	

Table 10. Output Data Select for TX3

Note: When the PLL loses lock, the V bit (Validity) data in the block immediately following loss-of-lock may not be accurate. Disregard this data and use the following data blocks.

■ Biphase signal input/output circuit

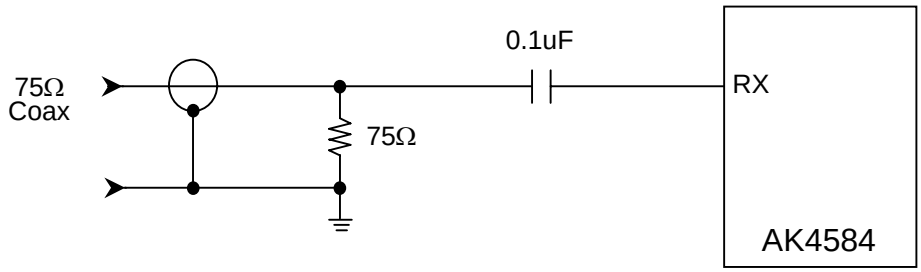


Figure 5. Consumer Input Circuit (Coaxial Input)

Note 1: Coax input only : if a coupling level to this input from the next RX input line pattern exceeds 50mV, an incorrect operation may occur. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.
Note 2: Ground of the RCA connector and terminator should be connected to PVSS of the AK4584 with low impedance on PC board.

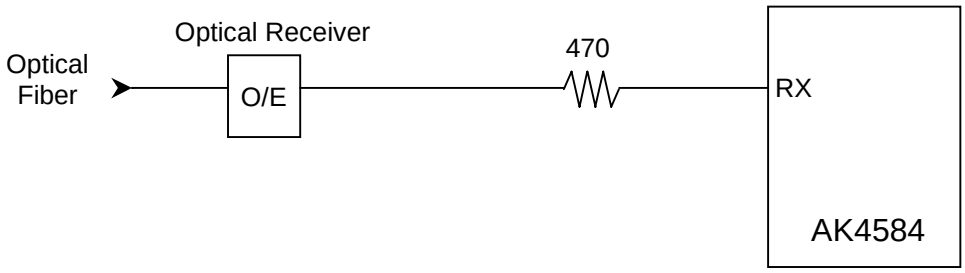


Figure 6. Consumer Input Circuit (Optical Input)

When using coaxial input, the input level of the RX line is small. Care must be taken to reduce, crosstalk among RX input lines by inserting a shield pattern between them.

The AK4584 includes a TX output buffer. The output level is 0.5V, +/–20% using the external resistor network shown below. The T1 in Figure 7 is a 1:1 transformer.

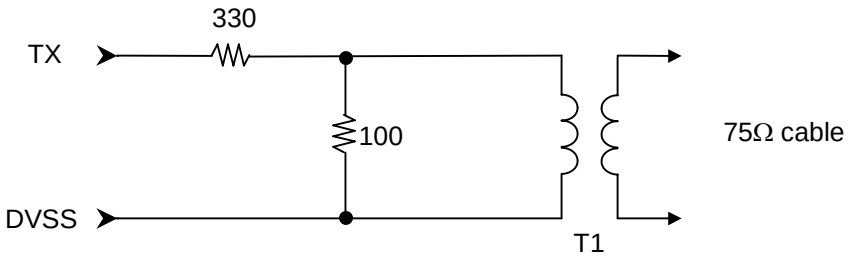


Figure 7. TX External Resistor Network

■ Sampling Frequency and Pre-emphasis Detection

The AK4584 has two methods for detecting the sampling frequency. The sampling frequency is detected by comparing the recovered clock to the X'tal oscillator, and the detected frequency is reported on FS3-0 bits. XTL1-0 bits can select reference X'tal frequency (Table 11). When XTL1-0 bits = "11" and XTALE pin = "L", X'tal oscillator is stopped and the sampling frequency is detected by the channel status sampling frequency information. The detected frequency is reported on FS3-0 bits. The default values of FS3-0 bits are "0000".

XTL1	XTL0	X'tal Frequency	
0	0	11.2896MHz	Default
0	1	12.288MHz	
1	0	24.576MHz	
1	1	Use channel status	

Table 11. Reference X'tal Frequency

Register Output				fs	Except XTL1-0 bits="11"	XTL1-0 bits="11"		
					Clock comparison	Consumer Mode (Note 1)	Pro Mode	
FS3	FS2	FS1	FS0			Byte3 Bit3,2,1,0	Byte0 Bit7,6	Byte4 Bit6,5,4,3
0	0	0	0	44.1kHz	± 3%	0000	01	0000
0	0	0	1	Reserved	-	0001	(others)	0000
0	0	1	0	48kHz	± 3%	0010	10	0000
0	0	1	1	32kHz	± 3%	0011	11	0000
1	0	0	0	88.2kHz	± 3%	(1000)	00	1010
1	0	1	0	96kHz	± 3%	(1010)	00	0010
1	1	0	0	176.4kHz	± 3%	(1100)	00	1011
1	1	1	0	192kHz	± 3%	(1110)	00	0011

Table 12. fs Information

Note 1. In consumer mode, Byte3 Bit3-0 are copied to FS3-0.

The pre-emphasis information is detected and reported on the PEM bit. This information is extracted from channel 1 (default). It can be switched to channel 2 via the CS12 bit in the control register.

PEM bit	Pre-emphasis	Byte0 Bit3,4,5
0	OFF	≠ 0X100
1	ON	0X100

Table 13. PEM in Consumer Mode

PEM bit	Pre-emphasis	Byte0 Bit2,3,4
0	OFF	≠ 100
1	ON	100

Table 14. PEM in Pro Mode

■ Error Handling

The following eight events will cause the INT1-0 pins go to "H".

(1) UNOCK: "1" when PLL goes to an UNLOCK state.
The AK4584 loses lock when the distance between two preambles is not correct or when those preambles are not correct.

(2) PAR: "1" when parity error or biphase coding error is detected.
Updated every sub-frame cycle. Reading this register resets it.

(3) AUTO: "1" when Non-Linear PCM Bit Stream is detected.

(4) DTSCD: "1" when DTS-CD Bit Stream is detected.

(5) AUDION: "1" when the "AUDIO" bit in recovered channel status indicates "1".

(6) PEM: "1" when "PEM" in recovered channel status indicates "1".
Updated every block cycle.

(7) V: "1" when validity flag is detected.

(8) FS: "1" when FS3-0 bits change.
FS3-0 bits are changed, FS bit is "H" during 1 sub-frame.
The contents of FS3-0 bits are the frequency detection result by fs-bit of C-bit or X'tal (refer to Table 12), this is compared last data every one block. Reading this register resets it.

INT1-0 pins output the OR'ed signal among those eight factors. However, each mask bit can mask each factor. When a bit masks a factor, the factor does not affect INT1-0 pins operation (those masks do not affect those registers (UNLOCK, PAR, etc.) themselves). Once INT0 pin goes to "H", it maintains "H" for 1024 cycles (this value can be changed by EFH1-0 bits) after the all factors are removed. Once the PAR bit and the FS bit go to "1", it holds "1" until reading the register.

While the AK4584 loses lock, the channel status bits are not updated and hold the previous data. In its initial state, INT0 pin outputs the OR'ed signal between UNLOCK and PAR bits. INT1 pin outputs the OR'ed signal among AUTO, DTSCD, AUDION and VDIR bits.

INT1-0 pins are "L" when the PLL is OFF.

Register								Pin	
UNLOCK	PAR	AUTO	DTSCD	AUDION	PEM	VDIR	FS	SDTO	TX
1	x	x	x	x	x	x	x	"L"	Output
0	1	x	x	x	x	x	x	Previous Data	Output
0	0	1	x	x	x	x	x	Output	Output
0	0	x	1	x	x	x	x	Output	Output
0	0	x	x	1	x	x	x	Output	Output
0	0	x	x	x	1	x	x	Output	Output
0	0	x	x	x	x	1	x	Output	Output
0	0	x	x	x	x	x	1	Output	Output

Table 15. Error Handling (x : Don't Care)

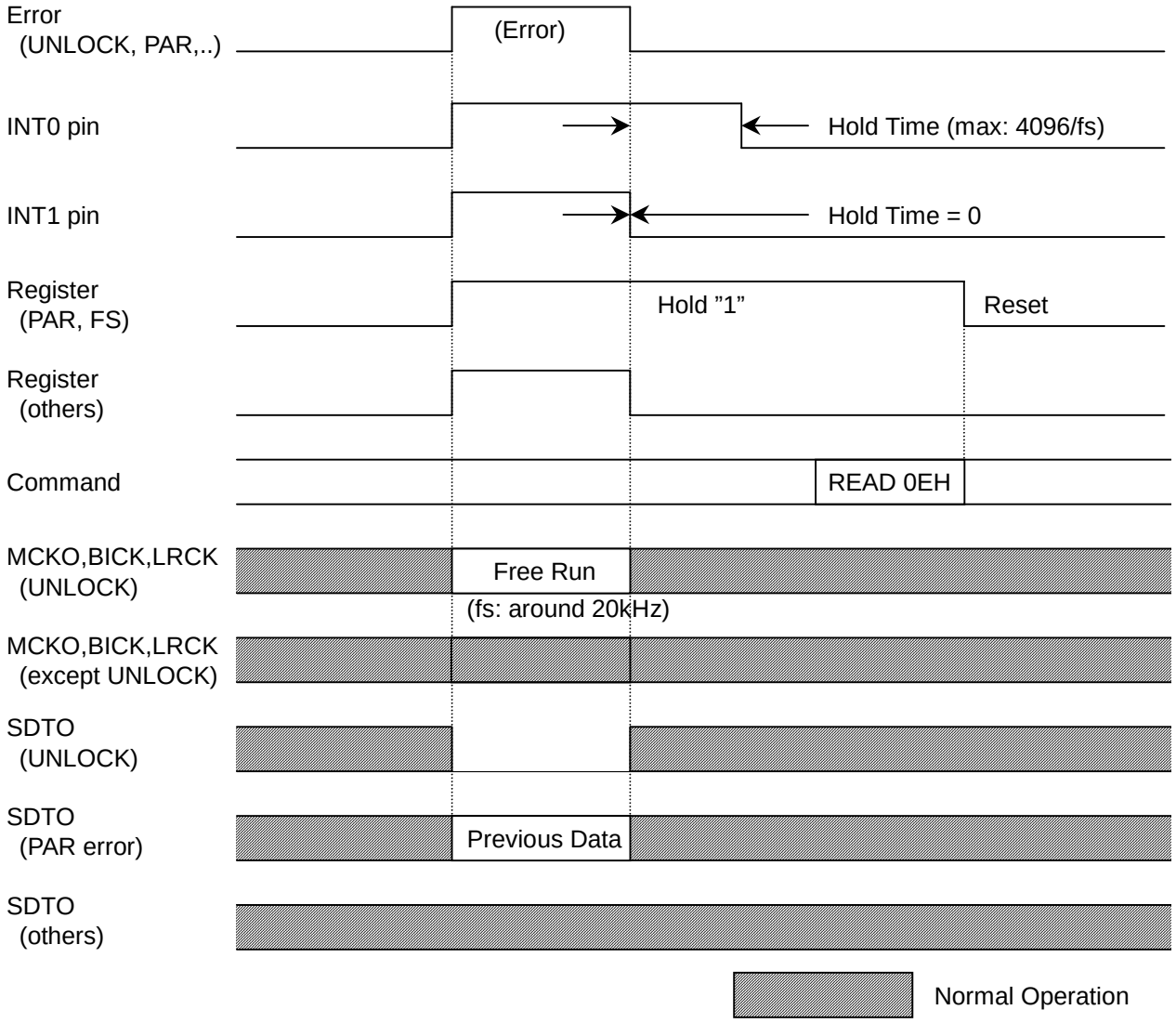


Figure 8. INT0/1 pin Timing

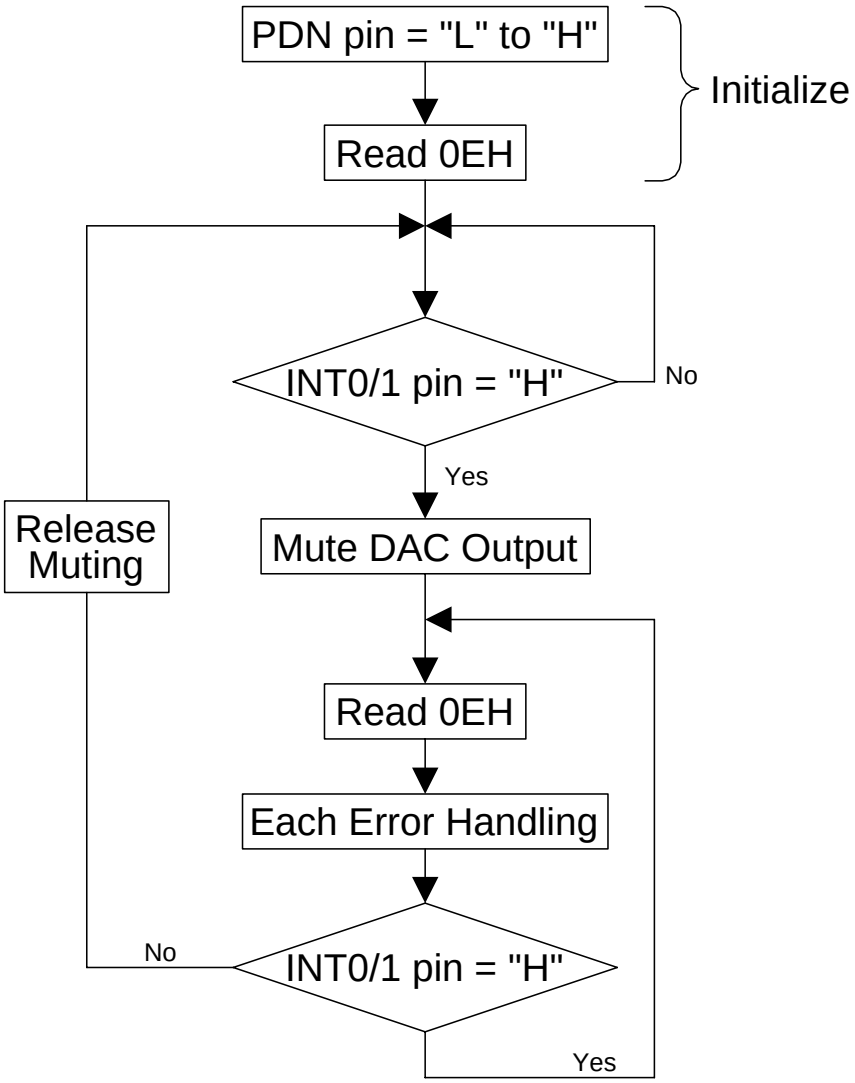


Figure 9. Error Handling Sequence Example

■ Non-PCM (AC-3, MPEG, etc.) and DTS-CD Bitstream Detection

The AK4584 has a Non-PCM steam auto-detect function. When the 32-bit mode Non-PCM preamble based on Dolby's "AC-3 Data Stream in IEC60958 Interface" is detected, the AUTO bit goes to "1". The 96-bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the AUTO to "1". Once the AUTO is set "1", it will remain "1" until 4096 frames pass through the chip without an additional sync pattern being detected. When those preambles are detected, the burst preambles Pc and Pd that follow the sync codes are stored to registers. The AK4584 also has DTS-CD bit stream auto-detection. When the AK4584 detects DTS-CD bit streams, the DTSCD bit goes to "1". If the next sync code does not appear within 4096 flames, the DTSCD bit goes to "0" until when the AK4584 detects the stream again.

■ Audio Interface Format

Five serial modes are supported as shown in Table 16, and are selected by the DIF2-0 bits. In all modes, the serial data is in MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. The audio interface supports both master and slave modes. In master mode, BICK and LRCK are output with the BICK frequency fixed to 64fs and the LRCK frequency fixed to fs.

When the format is equal or less than 20-bit (mode 0-1), LSBs in the sub-frame are truncated. In mode 2-4, the last 4LSBs are auxiliary data (see Figure 10).

Mode 2, 3, 4 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

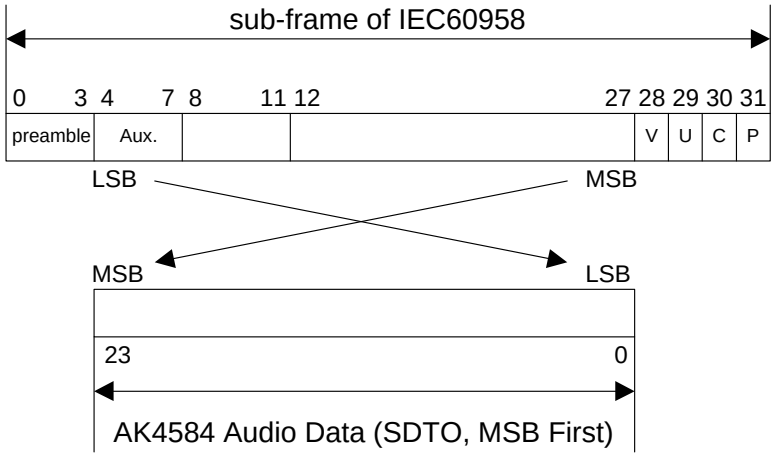


Figure 10. Bit Structure

Mode	DIF2	DIF1	DIF0	SDTO	SDTI	LRCK	BICK	
0	0	0	0	24bit, MSB justified	16bit, LSB justified	H/L	≥ 32fs	
1	0	0	1	24bit, MSB justified	20bit, LSB justified	H/L	≥ 40fs	
2	0	1	0	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	Default
3	0	1	1	24bit, I^2S Compatible	24bit, I^2S Compatible	L/H	≥ 48fs	
4	1	0	0	24bit, MSB justified	24bit, LSB justified	H/L	≥ 48fs	

Table 16. Audio Data Format

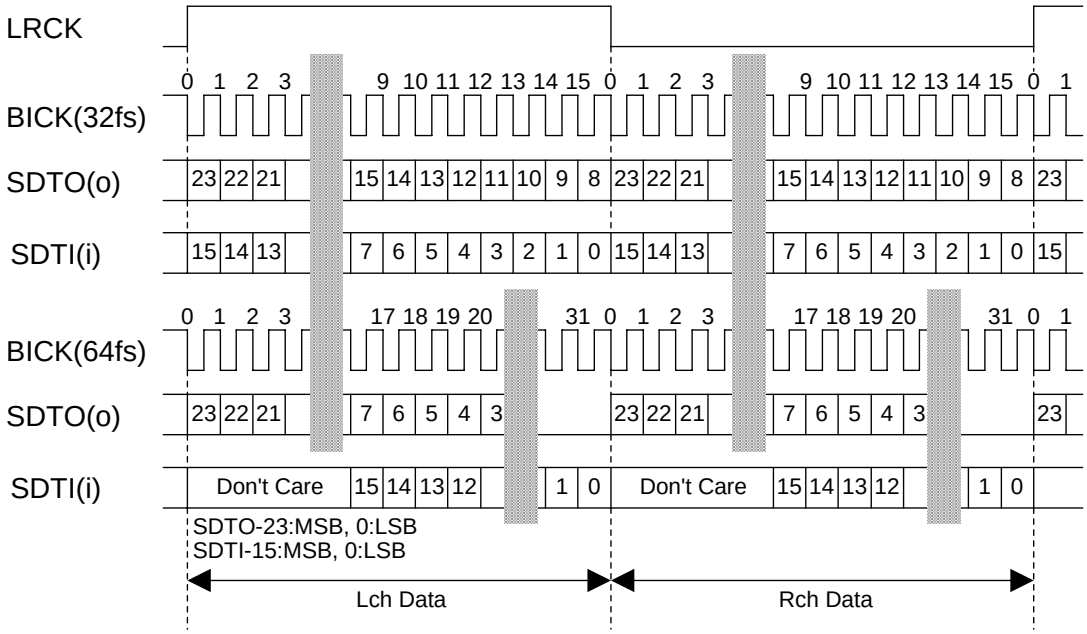


Figure 11. Mode 0 Timing

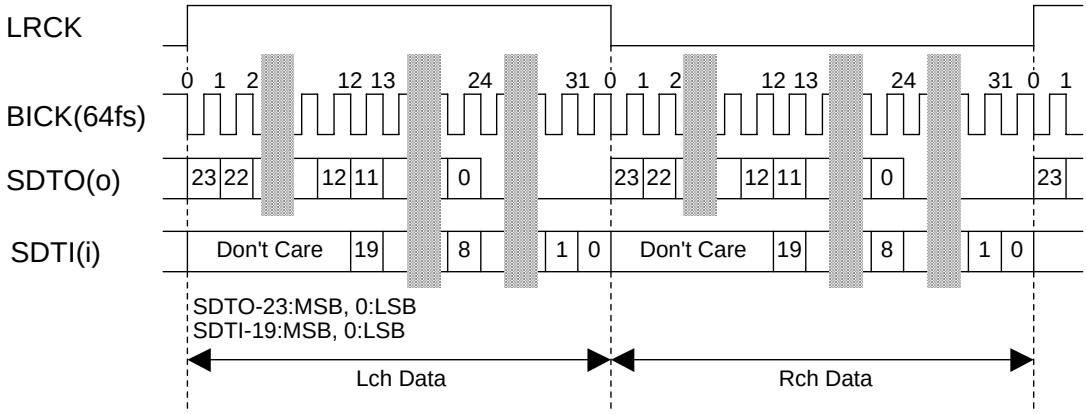


Figure 12. Mode 1 Timing

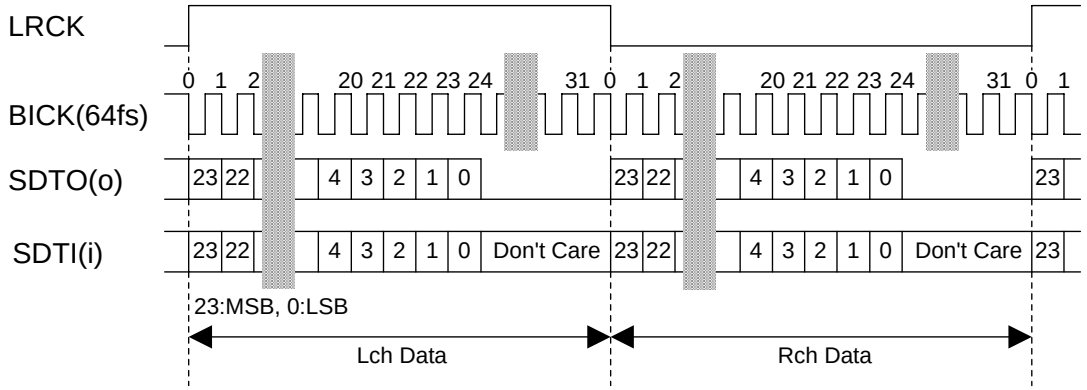


Figure 13. Mode 2 Timing

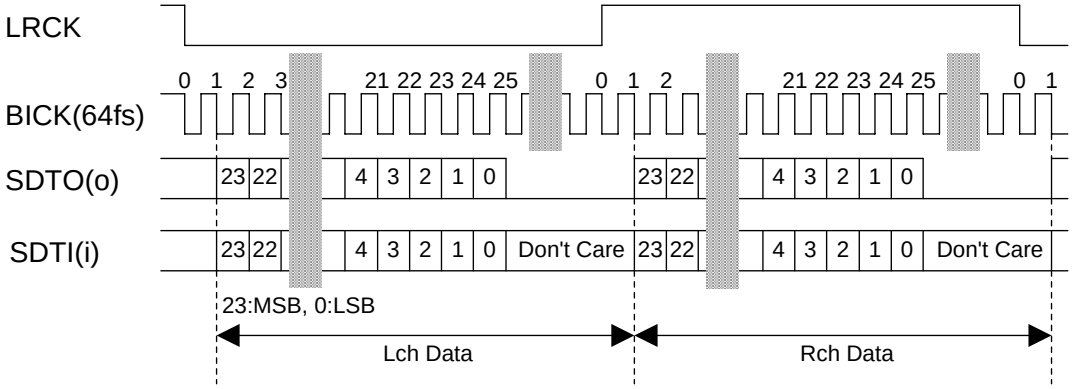


Figure 14. Mode 3 Timing

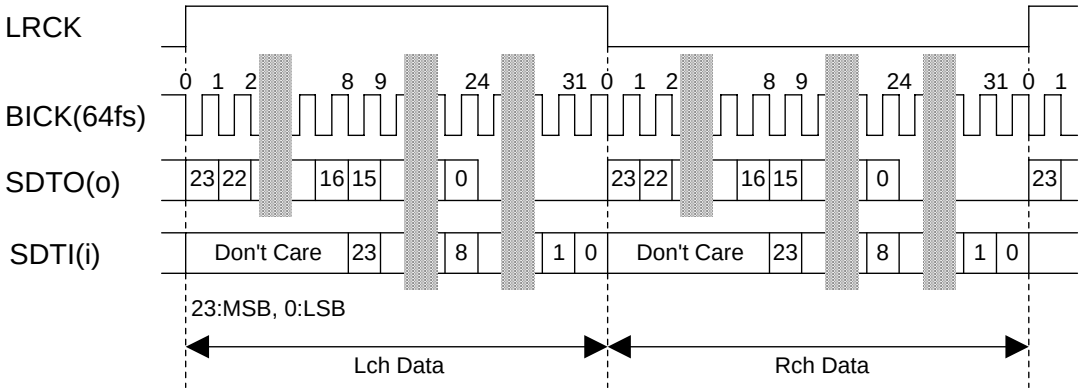


Figure 15. Mode 4 Timing

■ Master Mode and Slave Mode

The M/S pin selects between master and slave modes. M/S pin = "H" is master mode, M/S pin = "L" is slave mode. In master mode, MCKO, BICK and LRCK are output. In slave mode, only MCKO is output from the AK4584 and dividing MCKO externally provides BICK and LRCK.

	MCKO1/2	BICK, LRCK
Slave Mode	MCKO1 = Output MCKO2 = Output	BICK = Input LRCK = Input
Master Mode	MCKO1 = Output MCKO2 = Output	BICK = Output LRCK = Output

Table 17. Master mode/Slave mode

■ Relationship Clock operation and Power down

When the AK4584 is powered down, the XTALE pin controls the master clock output. The DMCK pin disables the MCKO1 output.

PDN pin	M/S pin	XTALE pin	CM1-0 bit	MCKO1/2	BICK, LRCK	DIR, DIT, CODEC
L	L	L	Default Fixed to "01"	MCKO1 = L MCKO2 = L	BICK = Input LRCK = Input	Power Down
		H		MCKO1 = Output[1)] MCKO2 = Output[1)]		
	H	L		MCKO1 = L MCKO2 = L	BICK = L LRCK = L	Power Down
		H		MCKO1 = Output[1)] MCKO2 = Output[1)]		
H	L	Don't Care	Available	MCKO1 = Output[2)] MCKO2 = Output[2)]	BICK = Input LRCK = Input	Normal Operation
	H				BICK = Output LRCK = Output	

Table 18. Clock Operation

Note 1) : Since the DIR is powered down, a X'tal oscillator or the external clock can be selected for the clock source.
Note 2) : CM1-0 bits select the clock source. When changing between modes, there is a possibility that the master clock output (MCKO) stops momentarily.
Note 3) : When PDN pin = "L", XTI pin is fixed to "L" when XTALE pin = "L" and the external clock is not AC coupled.

■ Digital High Pass Filter

The ADC has a digital high-pass filter for DC offset cancellation. The cut-off frequency of the HPF is 0.9Hz at fs = 44.1kHz and also scales with sampling rate (fs).

■ Input Volume

The AK4584 includes two channel-independent analog volumes (IPGA), each with 37 levels in 0.5dB increments. These are located in front of the ADCs while digital volume controls (IATT) with 128 levels (including MUTE) are located after the ADCs. Control of both of these volumes setting is handled the same register address. When the MSB of the register is "1", the IPGA changes and when the MSB = "0" the IATT changes.

The IPGA is an analog volume control that improves the S/N ratio compared with digital volume controls (Table 19). Level changes only occur during zero-crossings to minimize switching noise. Channel independent zero-crossing detection is used. If there is no zero-crossings, then the level will change after a time-out. The time-out period scales with fs. The periods of 256/fs, 512/fs, 1024/fs and 2048/fs are selected by ZTM1-0 bits in normal speed mode. If new value is written to the IPGA register before IPGA changes at the zero crossing or time-out, the previous value becomes invalid. The timer (channel independent) for time-out is reset and the timer restarts for new IPGA value. The ZCEI bit in the control register enable zero-crossing detection.

The IATT is a pseudo-log volume that is linear-interpolated internally. When changing the level, the transition between ATT values has 8031 levels and is done by soft changes (zero crossings), eliminating any switching noise.

	Input Gain Setting		
	0dB	+6dB	+18dB
fs=44.1kHz, A-weight	100dB	98dB	90dB

Table 19. PGA+ADC S/N

ZTM1	ZTM0	Normal Speed	Double Speed	
0	0	256/fs	512/fs	
0	1	512/fs	1024/fs	
1	0	1024/fs	2048/fs	Default
1	1	2048/fs	4096/fs	

Table 20. Zero Crossing Timeout

■ De-emphasis Control

The DAC includes the digital de-emphasis filter (tc=50/15μs) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). This setting is done via control register (DEM1-0 bits). This filter is always OFF at double speed and quad speed modes.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 21. De-emphasis Control

■ Output Volume

The AK4584 includes channel independent digital output volumes (ATT) with 256 levels at 0.5dB steps including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to −127dB and mute. When changing the level, the transitions are executed by soft changes (zero crossings), eliminating any switching noise.

■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the DAC input. When the SMUTE bit goes to "1", the output signal is attenuated by –∞ during 1024 LRCK cycles. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

Soft mute function is independent of the output volume and cascade connected between both functions.

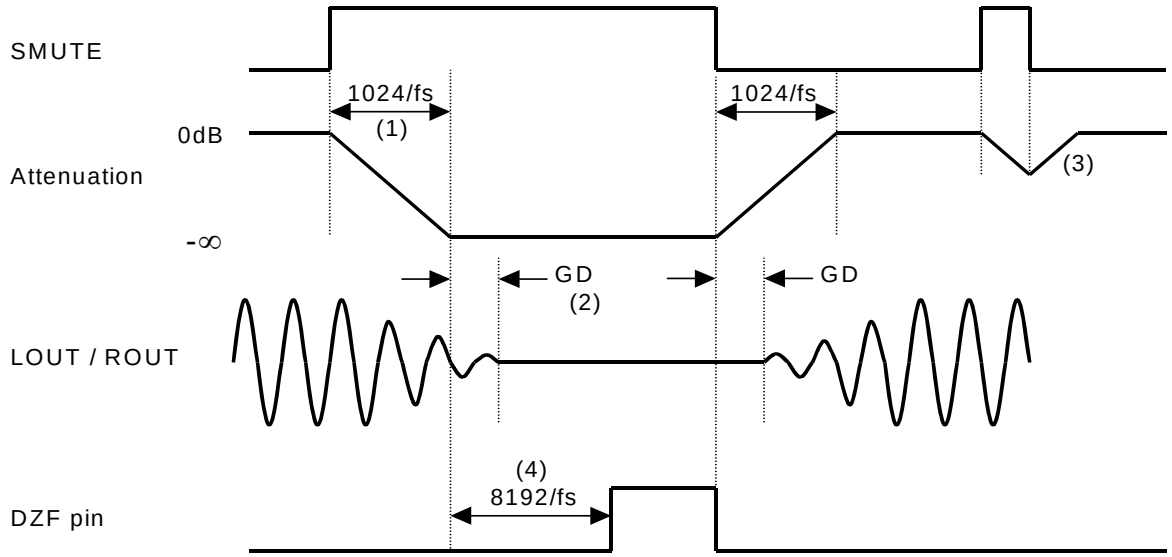


Figure 16. Soft mute function and Zero detection function

(1) The output signal is attenuated by –∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output delay from the digital input is called the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.
(4) When the input data of both channels is continuously zeros for 8192 LRCK cycles, DZF pin goes to "H". DZF pin immediately goes to "L" if input data of any channel is not zero after going DZF pin = "H".

■ Zero Detection Function

The AK4584 DAC has a L/R channel-dependent zeros detect function. When the input data at both channels is continuously zero for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately goes to "L" if the input data of each channel is not zero after DZF pin = "H". Zero detect function can be disabled by the DZFE bit. In this case, the DZF pin is always "L".

When the PDN pin is "L", the DZF pin is always "L". If PDN pin = "L" → "H", DZF pin goes from "L" → "H". When the PWVRN bit is "0", the DZF pin is "L".

If the DZF pin goes to "H" when the RSTDAN bit becomes "0", then the AK4584 is reset after 4~5/fs and goes to "L" at 6~7/fs after the RSTDAN bit becomes "1". If after the RSTDAN bit becomes "0" and within 5/fs, the RSTDAN bit becomes "1", then the AK4584 will not be properly reset.

If the DZF pin goes to "H" when the PWDAN bit becomes "0", then the AK4584 is reset after 4~5/fs and goes to "L" at 6~7/fs after the PWDAN bit becomes "1". If the PWDAN bit becomes "0", and the PWDAN bit becomes "1" within 5/fs, then the AK4584 will not be properly reset.

When PDN pin becomes "H" and the PWDAN bit becomes "1" and the RSTDAN bit becomes "1", 8192 counts start after 1/fs for the zero detect function.

■ Reset and Power Down

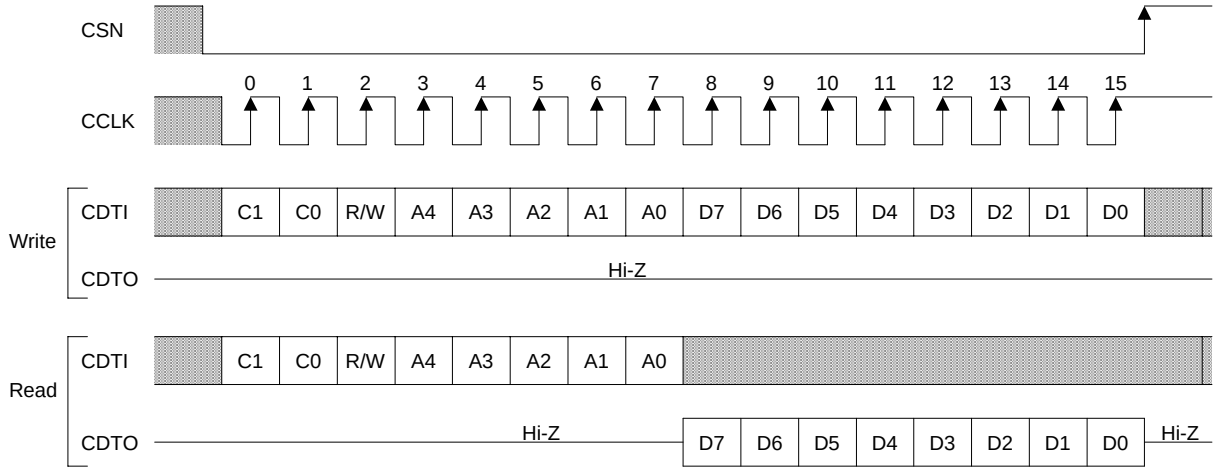
The AK4584 has both a power-down mode for all circuits by pulling the PDN pin or a partial power-down mode that is enabled via an internal register (see Table 22). The AK4584 should be reset once by bringing PDN pin = "L" upon power-up.

PDN pin	PWDITN	PWVRN	PWADN	PWDAN	CM1-0	Function	Register Initialization
L	x	x	x	x	x	All Power-down	Yes
H	0	x	x	x	x	DIT Power-down	No
	x	0	x	x	x	VREF Power-down	No
	x	x	0	x	x	ADC Power-down	No
	x	x	x	0	x	DAC Power-down	No
	x	x	x	x	00	X'tal Power-down	No
	x	x	x	x	01	PLL Power-down	No

Table 22. Reset & Power Down

■ Serial Control Interface

The internal registers may be either written or read by the 4-wire µP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C1/0 are fixed to "00"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes to high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. The chip address is fixed to "00". The access to the chip address except for "00" is invalid. PDN pin = "L" resets the registers to their default values.



C1 - C0 : Chip Address (Fixed to "00")
R/W : READ / WRITE ("1" : WRITE, "0" : READ)
A4 - A0 : Register Address
D7 - D0 : Control Data

Figure 17. Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	0	0	0	TEST	PWDITN	PWVRN	PWADN	PWDAN
01H	Reset Control	0	0	0	0	0	0	RSTADN	RSTDAN
02H	Clock & Format Control	0	0	0	DIF2	DIF1	DIF0	DFS1	DFS0
03H	Deem & Volume Control	MSDTO	SMUTE	DZFE	ZCEI	ZTM1	ZTM0	DEM1	DEM0
04H	Lch IPGA Control	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
05H	Rch IPGA Control	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
06H	Lch OATT Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
07H	Rch OATT Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
08H	In/Out Source Control	0	0	DAC1	DAC0	PCM1	PCM0	DIT1	DIT0
09H	Clock Mode Control	OCKS1	OCKS0	ICKS1	ICKS0	CM1	CM0	XTL1	XTL0
0AH	DIR Control	0	CS12	OPS1	OPS0	IPS1	IPS0	EFH1	EFH0
0BH	DIT Control	0	0	TX3E	TX2E	TX1E	UDIT	VDIT	TCH
0CH	INT0 Mask	MAT0	MDTS0	MAN0	MV0	MPE0	MUL0	MPR0	MFS0
0DH	INT1 Mask	MAT1	MDTS1	MAN1	MV1	MPE1	MUL1	MPR1	MFS1
0EH	Receiver Status 0	AUTO	DTSCD	AUDION	VDIR	PEM	UNLOCK	PAR	FS
0FH	Receiver Status 1	0	0	0	0	FS3	FS2	FS1	FS0
10H	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
11H	RX Channel Status Byte 1	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
12H	RX Channel Status Byte 2	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
13H	RX Channel Status Byte 3	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
14H	RX Channel Status Byte 4	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
15H	TX Channel Status Byte 0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
16H	TX Channel Status Byte 1	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
17H	TX Channel Status Byte 2	CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
18H	TX Channel Status Byte 3	CT31	CT30	CT29	CT28	CT27	CT26	CT25	CT24
19H	TX Channel Status Byte 4	CT39	CT38	CT37	CT36	CT35	CT34	CT33	CT32
1AH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
1BH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
1CH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
1DH	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8

PDN = “L” resets the registers to their default values.

■ Control Register Setup Sequence

When the PDN pin goes from “L” to “H” upon power-up etc., the AK4584 will be ready for normal operation by the next sequence. In this case, all control registers are set to initial values and the AK4584 is in the reset state.

(1) Set the clock mode and the audio data interface mode.
(2) Cancel the reset state by setting RSTADN bit or RSTDAN bit to “1”. Refer to Control Register (01H).
(3) ADC output and DAC output should be muted externally until canceling each reset state, since in master mode there is a possibility that the frequency and duty cycle of LRCK and BICK outputs may become distorted.

The clock mode should be changed after setting RSTADN bit and RSTDAN bit to “0”. At that time, the ADC and DAC outputs should be muted externally since in master mode, there is a possibility that the frequency and duty of LRCK and BICK outputs may become distorted.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Down Control	0	0	0	TEST	PWDITN	PWVRN	PWADN	PWDAN
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	1	1	1

PWDAN: DAC Power Down

0: Power down

1: Power up

"0" powers down only the DAC section and then places LOUT and ROUT immediately to a high-Z state. The OATTs also go to "FFH". But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the OATTs fade in the setting value of the control register (06H & 07H). The analog output should be muted externally as some pop noise may occur when entering to and exiting from this mode.

PWADN: ADC Power Down

0: Power down

1: Power up

"0" powers down only the ADC section and then the SDTO goes "L" immediately. The IPGAs also go "00H". But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the IPGAs fade in the setting value of the control register (04H & 05H). At that time, ADC output "0" during first 516 LRCK cycles.

PWVRN: VREF Power Down

0: Power down

1: Power up

"0" powers down all sections and then both ADC and DAC do not operate. The contents of all register are not initialized and enabled to write to the registers. When PWADN bit and PWDAN bit go "0" and PWVRN bit goes "1", only VREF section can be powered up.

PWDITN: DIT Power Down

0: Power down

1: Power up

"0" powers down only the DIT section. Therefore, TX3 pin output is disabled . TX1 pin and TX2 pin can output the biphase signal. The contents of all register are not initialized and enabled to write to the registers.

TEST: TEST bit

Must be fixed to "1"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Reset Control	0	0	0	0	0	0	RSTADN	RSTDAN
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

RSTDAN: DAC Reset

0: Reset

1: Normal Operation

"0" resets the internal timing and immediately drives the LOUT and ROUT to the VCOM voltage. The OATTs go to "FFH". The contents of all registers are unaffected but are write-enabled. After exiting the power down mode, the OATTs fade in based on the values of the control registers (06H & 07H). The analog outputs should be muted externally as some pop noise may occur when entering to and exiting from this mode.

RSTADN: ADC Reset

0: Reset

1: Normal Operation

"0" resets the internal timing and SDTO immediately goes to "L". The IPGAs go to "00H". The contents of all registers are unaffected but are write-enabled. After exiting the power down mode, the IPGAs fade in based on the values of the control registers (04H & 05H). At that time, ADC output is "0" during first 516 LRCK cycles.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Clock and Format Control	0	0	0	DIF2	DIF1	DIF0	DFS1	DFS0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

DFS1-0: Sampling Speed Control (see Table 6)

Initial values are "00".

DIF2-0: Audio Data Interface Modes (see Table 16)

Initial values are "010" (24bit MSB justified for both ADC and DAC).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Deem and Volume Control	MSDTO	SMUTE	DZFE	ZCEI	ZTM1	ZTM0	DEM1	DEM0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	1

DEM1-0: De-emphasis Response (see Table 21)
Initial values are “01” (OFF).

ZTM1-0: Zero Crossing Time-out Period Select (see Table 20)
Initial values are “10” (1024/fs).

ZCEI: ADC IPGA Zero Crossing Enable
0: Input PGA gain changes occur immediately
1: Input PGA gain changes occur only on zero-crossing or after timeout.
Initial value is “1” (Enable).

DZFE: Data Zero Detect Enable
0: Disable
1: Enable
Zero detect function can be disabled by the DZFE bit. In this case, DZF pin is always “L”.
Initial value is “0” (Disable).

SMUTE: DAC Input Soft Mute Control
0: Normal operation
1: DAC outputs soft-muted
The soft mute is independent of the output ATT and performed digitally.

MSDTO: SDTO Mute Control
0: Disable
1: Enable
When MSDTO bit is “1”, SDTO outputs “L”. Initial value is “0” (Disable).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch IPGA Control	IPGL7	IPGL6	IPGL5	IPGL4	IPGL3	IPGL2	IPGL1	IPGL0
05H	Rch IPGA Control	IPGR7	IPGR6	IPGR5	IPGR4	IPGR3	IPGR2	IPGR1	IPGR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	1	1	1	1	1

IPGL/R7-0: ADC Input Gain Level (see Table 23)

Initial value is “7FH” (0dB).

Digital ATT with 128 levels operates when writing data of less than 7FH. This ATT is a linear ATT with 8032 levels internally and these levels are assigned to pseudo-log data with 128 levels. The transition between ATT values has 8032 levels and is done by soft changes. For example, when ATT changes from 127 to 126, the internal ATT value decreases from 8031 to 7775, one by one every fs cycle. It takes 8031 cycles (182ms@fs=44.1kHz) from 127 to 0 (Mute).

The IPGAs are set to “00H” when PDN pin goes “L”. After returning to “H”, the IPGAs fade into the initial value, “7FH” in 8031 cycles.

The IPGAs are set to “00H” when PWADN bit goes “0”. After returning to “1”, the IPGAs fade into the current value. The ADC output is “0” during the first 516 cycles.

The IPGAs are set to “00H” when RSTADN bit goes to “0”. After returning to “1”, the IPGAs fade into the current value. The ADC output is “0” during the first 516 cycles.

Data	Internal (DATT)	Gain (dB)	Step width (dB)	
255 - 165	-	+18	-	**IPGA** Analog volume with 0.5dB step
164	-	+18	-	
163	-	+17.5	0.5	
162	-	+17	0.5	
:	-	:	0.5	
130	-	+1.0	0.5	
129	-	+0.5	0.5	
128	-	0	0.5	
127	8031	0	-	**IATT** External 128 levels are converted to internal 8032 linear levels of DATT. Internal DATT soft-changes between data. DATT=2^m x (2 x l + 33) – 33 m: MSB 3-bits of data l: LSB 4-bits of data
126	7775	–0.28	0.28	
125	7519	–0.57	0.29	
:	:	:	:	
112	4191	–5.65	0.51	
111	3999	–6.06	0.41	
110	3871	–6.34	0.28	
:	:	:	:	
96	2079	–11.74	0.52	
95	1983	–12.15	0.41	
94	1919	–12.43	0.28	
:	:	:	:	
80	1023	–17.90	0.53	
79	975	–18.32	0.42	
78	943	–18.61	0.29	
:	:	:	:	
64	495	–24.20	0.54	
63	471	–24.64	0.43	
62	455	–24.94	0.30	
:	:	:	:	
48	231	–30.82	0.58	
47	219	–31.29	0.46	
46	211	–31.61	0.32	
:	:	:	:	
32	99	–38.18	0.67	
31	93	–38.73	0.54	
30	89	–39.11	0.38	
:	:	:	:	
16	33	–47.73	0.99	
15	30	–48.55	0.83	
14	28	–49.15	0.60	
:	:	:	:	
5	10	–58.10	1.58	
4	8	–60.03	1.94	
3	6	–62.53	2.50	
2	4	–66.05	3.52	
1	2	–72.07	6.02	
0	0	MUTE		

Table 23. IPGA Code Table

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Lch OATT Control	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
07H	Rch OATT Control	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL/R7-0: DAC OATT Level (see Table 24)

Initial value is “FFH” (0dB).

The transition from initial to final levels has 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). If PDN pin goes to “L”, the ATTs are initialized to FFH.

The ATTs are FFH when PWDAN bit = “0”. When PWDAN bit returns to “1”, the ATTs fade to their current value.

The ATTs are FFH when RSTDAN bit = “0”. When RSTDAN bit returns to “1”, the ATTs fade to their current value.

Digital attenuation is independent of the soft mute function.

ATTL/R7-0	Attenuation
FFH	0dB
FEH	–0.5dB
FDH	–1.0dB
FCH	–1.5dB
:	:
:	:
02H	–126.5dB
01H	–127dB
00H	MUTE (–∞)

Table 24. OATT Code Table

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	In/Out Source Control	0	0	DAC1	DAC0	PCM1	PCM0	DIT1	DIT0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DIT1-0: Input Selector for DIT (see Table 10)
Initial values are “00”. When DIT1-0 bits are “10”, the selected input is sent to the TX3 output.

PCM1-0: Input Selector for SDTO (see Table 25)
Initial values are “00”.

PCM1	PCM0	Input Source	
0	0	ADC	Default
0	1	SDTI	
1	0	DIR	
1	1	N/A	

Table 25. Input Selector for SDTO

DAC1-0: Input Selector for DAC (see Table 26)
Initial values are “00”.

DAC1	DAC0	Input Source	
0	0	ADC	Default
0	1	SDTI	
1	0	DIR	
1	1	N/A	

Table 26. Input Selector for DAC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Clock Mode Control	OCKS1	OCKS0	ICKS1	ICKS0	CM1	CM0	XTL1	XTL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	1	0	0

XTL1-0: X’tal Frequency Select (see Table 11)
Initial values are “00”.

CM1-0: Master Clock Operation Mode Select (see Table 1)
Initial values are “01”.

ICKS1-0: Master Clock Input Frequency Select in X’tal Mode (see Table 5)
Initial values are “00”.
* 768fs is supported external clock mode.

OCKS1-0: Master Clock Output Frequency Select in PLL Mode (see Table 2)
Initial values are “01”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	DIR Control	0	CS12	OPS1	OPS0	IPS1	IPS0	EFH1	EFH0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

EFH1-0: Interrupt 0 Pin Hold Count Select (Table 27)
Initial values are “01”.
LRCK of Table 27 is DIR’s LRCK, the hold time scales with 1/fs.

EFH1	EFH0	Hold Count	
0	0	512LRCK	
0	1	1024LRCK	Default
1	0	2048LRCK	
1	1	4096LRCK	

Table 27. Hold Count Select

IPS1-0: Input Recovery Data Select (see Table 8)
Initial values are “00”.

OPS1-0: Output Through Data Select for TX1/2 (see Table 9)
Initial values are “00”.

CS12: Channel Status Select
0: Channel 1
1: Channel 2
Selects which channel status is used to derive C-bit buffers, AUDION, PEM, FS.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	DIT Control	0	0	TX3E	TX2E	TX1E	UDIT	VDIT	TCH
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	1	0	0

TCH: Channel Number Select for DIT
0: Don't care (bit20-23 = 0000)
1: Stereo (bit20-23 = 1000 : L channel, bit20-23 = 0100 : R channel)
Automatically sets the channel number of the DIT (bit20-23 of C-bit). Initial value is "0".
For consumer mode (CT0 bit = "0"), CT20-23 bits of address 17H cannot be controlled directly.

VDIT: V-bit Control for DIT
0: Valid
1: Invalid
Initial value is "0".

UDIT: U-bit Control for DIT
0: U-bit is fixed to "0".
1: Recovered U-bit is used for DIT. (Loop mode for U-bit)
When DIR is unlocked , U-bit is "0". Initial value is "1".

TX1E: TX1 Output Enable
0: Disable, TX1 outputs "L".
1: Enable
Initial value is "1".

TX2E: TX2 Output Enable
0: Disable, TX2 outputs "L".
1: Enable
Initial value is "1".

TX3E: TX3 Output Enable
0: Disable, TX3 outputs "L".
1: Enable
Initial value is "1".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	INT0 Mask	MAT0	MDTS0	MAN0	MV0	MPE0	MUL0	MPR0	MFS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	0	0	1

MFS0: Mask Enable for FS Bit
0: Mask disable
1: Mask enable

MPR0: Mask Enable for PAR Bit
0: Mask disable
1: Mask enable

MUL0: Mask Enable for UNLOCK Bit
0: Mask disable
1: Mask enable

MPE0: Mask Enable for PEM Bit
0: Mask disable
1: Mask enable

MV0: Mask Enable for VDIR Bit
0: Mask disable
1: Mask enable

MAN0: Mask Enable for AUDION Bit
0: Mask disable
1: Mask enable

MDTS0: Mask Enable for DTSCD Bit
0: Mask disable
1: Mask enable

MAT0: Mask Enable for AUTO Bit
0: Mask disable
1: Mask enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	INT1 Mask	MAT1	MDTS1	MAN1	MV1	MPE1	MUL1	MPR1	MFS1
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

MFS1: Mask Enable for FS Bit
0: Mask disable
1: Mask enable

MPR1: Mask Enable for PAR Bit
0: Mask disable
1: Mask enable

MUL1: Mask Enable for UNLOCK Bit
0: Mask disable
1: Mask enable

MPE1: Mask Enable for PEM Bit
0: Mask disable
1: Mask enable

MV1: Mask Enable for VDIR Bit
0: Mask disable
1: Mask enable

MAN1: Mask Enable for AUDION Bit
0: Mask disable
1: Mask enable

MDTS1: Mask Enable for DTSCD Bit
0: Mask disable
1: Mask enable

MAT1: Mask Enable for AUTO Bit
0: Mask disable
1: Mask enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Receiver Status 0	AUTO	DTSCD	AUDION	VDIR	PEM	UNLOCK	PAR	FS
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

FS: Sampling Frequency Status
0: No change
1: Change
This bit is “1” when FS3-0 bits are changed. When this address is read, this bit is reset.

PAR: Parity Error or Bi-phase Error Status
0: No error
1: Error
This bit is “1” if a Parity Error or Biphase Error is detected in the sub-frame.
When this address is read, this bit is reset.

UNLOCK: PLL Lock Status
0: Lock
1: Unlock
When this address is read, this bit is not reset.

PEM: Pre-emphasis Bit Output
0: OFF
1: ON
This bit is made by encoding the channel status bits.
When this address is read, this bit is not reset.

VDIR: Validity Bit
0: Valid
1: Invalid
When this address is read, this bit is not reset.

AUDION: Audio Bit Output
0: Audio
1: Non audio
This bit is made by encoding channel status bits.
When this address is read, this bit is not reset.

DTSCD: DTS-CD Auto Detect
0: No detect
1: Detect
When this address is read, this bit is not reset.

AUTO: Non-PCM Auto Detect
0: No detect
1: Detect
When this address is read, this bit is not reset.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	Receiver Status 1	0	0	0	0	FS3	FS2	FS1	FS0
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

FS3-0: Sampling Frequency Detection (see Table 12)
Initial values are “0000”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	RX Channel Status Byte 0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
11H	RX Channel Status Byte 1	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
12H	RX Channel Status Byte 2	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
13H	RX Channel Status Byte 3	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
14H	RX Channel Status Byte 4	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
R/W		RD							
Default		Not Initialized							

CR39-0: Receiver Channel Status Byte 4-0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	TX Channel Status Byte 0	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
16H	TX Channel Status Byte 1	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8
17H	TX Channel Status Byte 2	CT23	CT22	CT21	CT20	CT19	CT18	CT17	CT16
18H	TX Channel Status Byte 3	CT31	CT30	CT29	CT28	CT27	CT26	CT25	CT24
19H	TX Channel Status Byte 4	CT39	CT38	CT37	CT36	CT35	CT34	CT33	CT32
R/W		R/W							
Default		0							

CT39-0: Transmitter Channel Status Byte 4-0
In consumer mode (CT0 bit = “0”), bit20-23 (Audio channel) cannot be controlled directly.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
1BH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
1CH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
1DH	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
R/W		RD							
Default		Not Initialized							

PC15-0: Burst Preamble Pc Byte 1-0

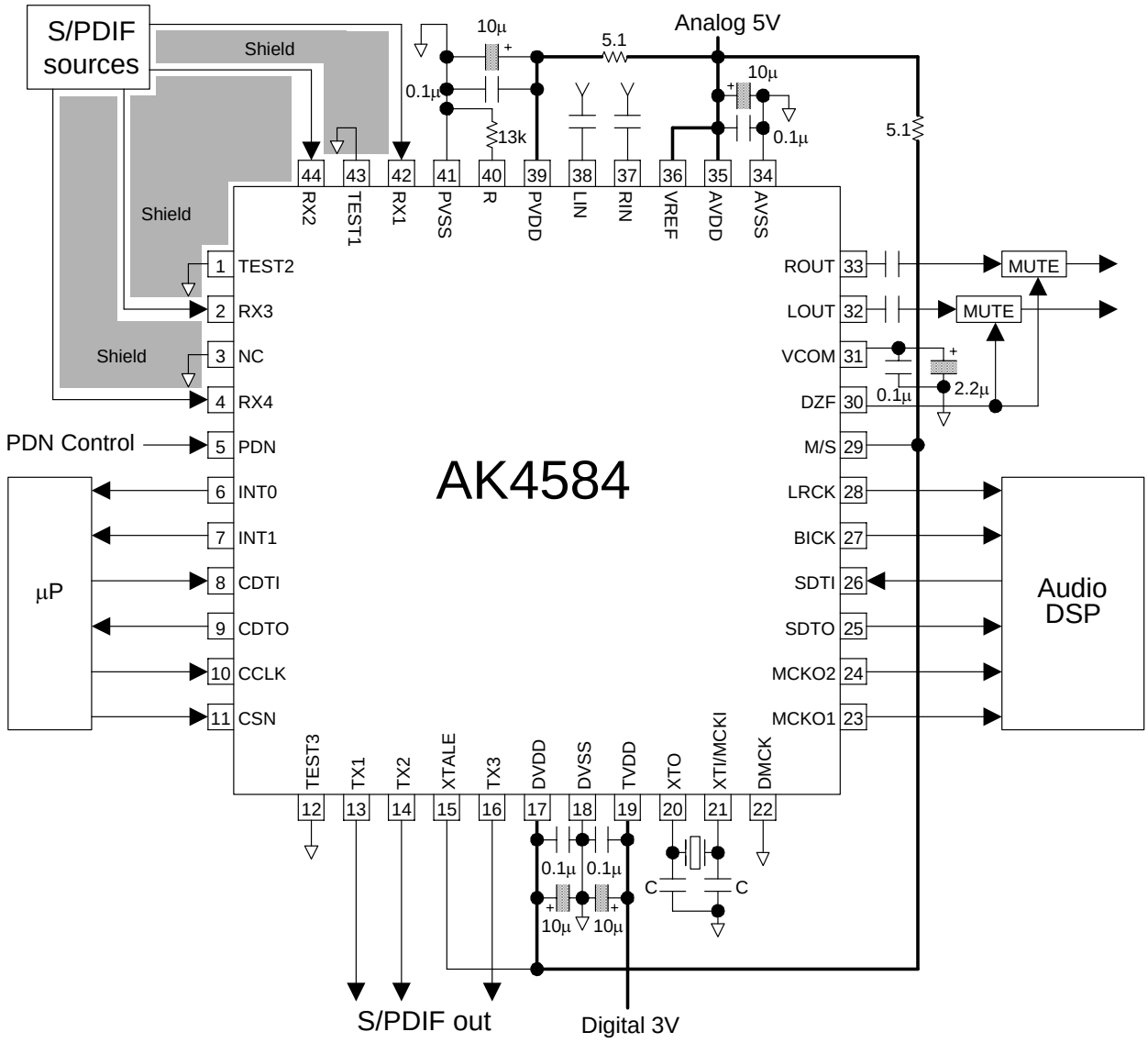
PD15-0: Burst Preamble Pd Byte 1-0

SYSTEM DESIGN

Figure 18 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

[Measurement Condition]

- TVDD = 3.0V, Master mode, XTALE = “H”, DMCK = “L”



Note:

- X’tal Oscillation circuit is specified from 11.2896MHz to 24.576MHz. Capacitors “C” depend on the X’tal.
- AGND and DGND of the AK4584 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- When LOUT/ROUT drives a capacitive load, resistors should be added in series between LOUT/ROUT and capacitive load.
- All input pins except pull-down pin (TEST1,2 pins) should not be left floating.
- To prevent coupling of TEST1, TEST2 and the RX signals, NC pins are connected PVSS.

Figure 18. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4584 requires careful attention to power supply and grounding arrangements. AVDD, DVDD and PVDD are usually supplied from the analog supply in the system. Alternatively if AVDD, DVDD and PVDD are supplied separately, the power up sequence is not critical. TVDD is a power supply pin to interface with external ICs and is supplied from the digital supply in the system. **AVSS, DVSS and PVSS of the AK4584 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4584 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The differential voltage between VREF and AVSS sets the analog input/output range. VREF pin is normally connected to AVDD with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 2.2µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4584.

3. Analog Inputs

ADC inputs are single-ended and the input resistance is 10kΩ (typ). The input signal range scales with the supply voltage and nominally 0.6 x VREF Vpp (typ). Usually the input signal is AC coupled with capacitor. The cut-off frequency is fc = 1/(2πRC). The AK4584 can accept input voltages from AVSS to AVDD. The ADC output data format 2's compliment. The internal HPF removes the DC offset.

The AK4584 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4584 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

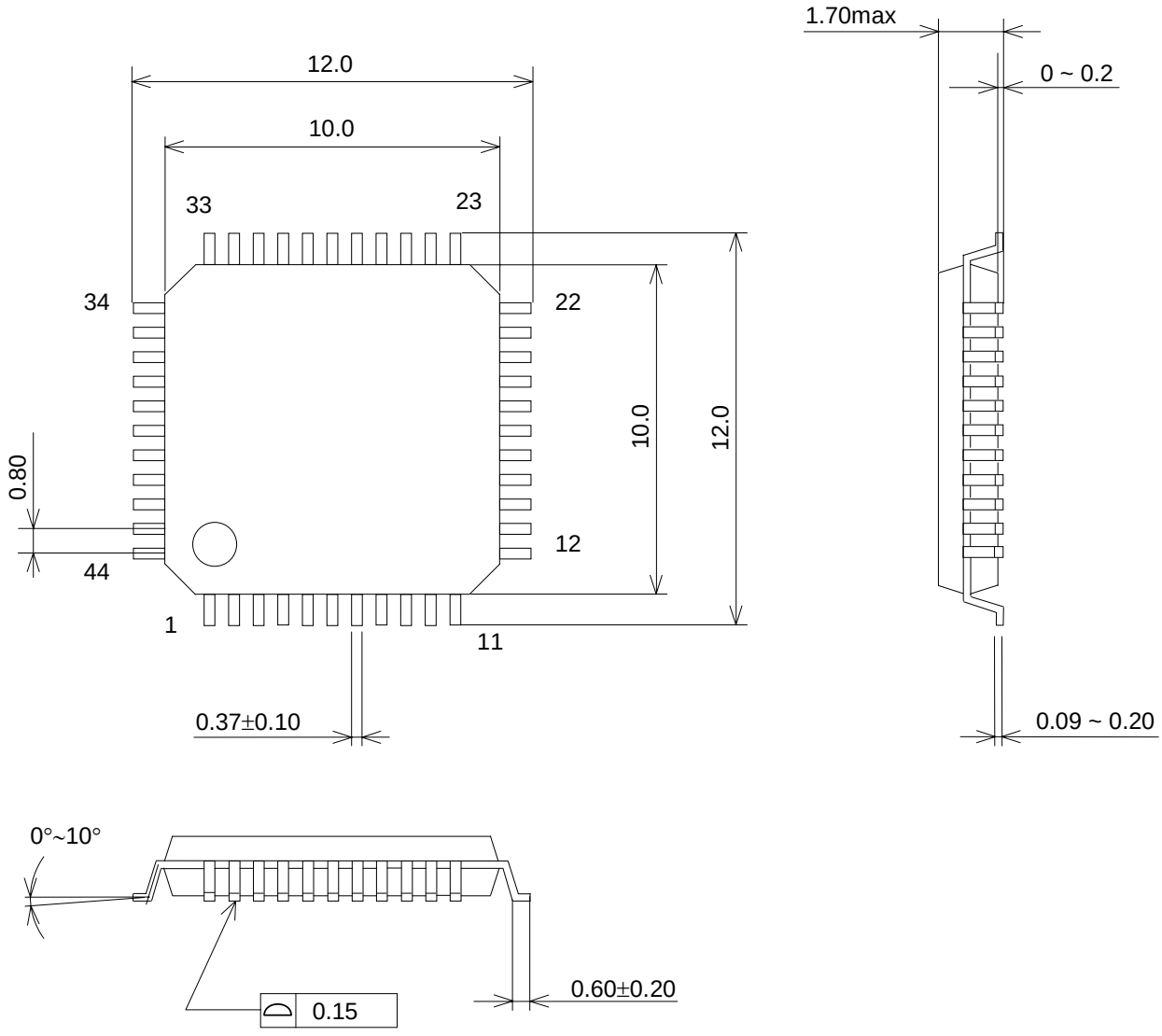
The analog outputs are single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage, nominally 0.6 x VREF Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is 0V for 000000H(@24bit). The internal analog filters remove most of the out-of-band noise generated by the DAC's delta-sigma modulator.

5. XTI pin and XTO pin

(1) C depends on the X'tal (typ. 10 ~ 40pF).
(2) When an external clock is supplied, the XTO pin is left floating and the clock source is connected to the XTI pin. The input voltage should not exceed DVDD. When applying a CMOS level signal to the XTI pin, when XTALE pin = "L" and PDN pin = "L", the XTI pin is fixed to "L". The means that the XTI pin can accept a CMOS level clock as well as TTL level clock. The only restriction to this is the clock high level must be equal to or greater than 40% DVDD, not to exceed DVDD. The low value of the clock must be 30% DVDD or lower, not to drop below DGND.
(3) When the XTI and the XTO pins are not used, leave the XTO pin floating and connect the XTI pin to DVSS.

PACKAGE

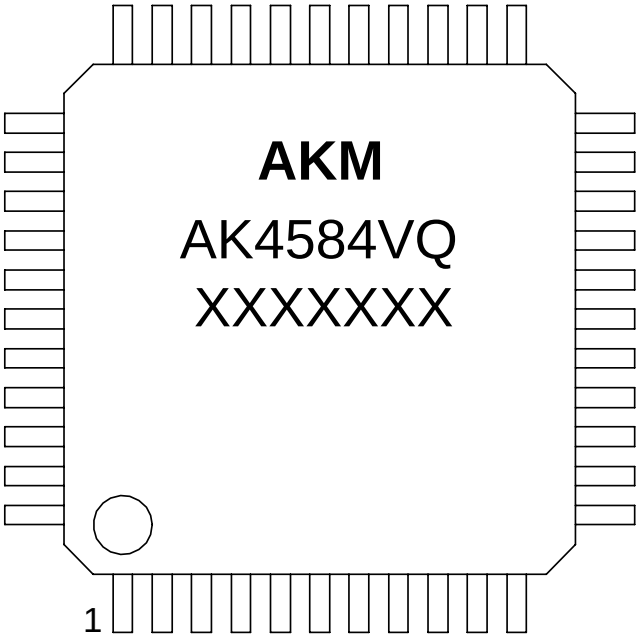
44pin LQFP (Unit: mm)



■ **Material & Lead finish**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXX : Date Code Identifier (7 digits)

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
01/11/21	00	First Edition		
12/11/20	01	Specification Change	52	PACKAGE Package dimensions were changed.

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