

# MC74VHCT157A

## Quad 2-Channel Multiplexer

The MC74VHCT157A is an advanced high speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select (S) and enable ( $\bar{E}$ ) inputs. When  $\bar{E}$  is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5 V CMOS level output swings.

The VHCT157A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed:  $t_{PD} = 4.1\text{ns}$  (Typ) at  $V_{CC} = 5$  V
- Low Power Dissipation:  $I_{CC} = 4\mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- TTL-Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise:  $VO_{LP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 82 FETs or 20 Equivalent Gates



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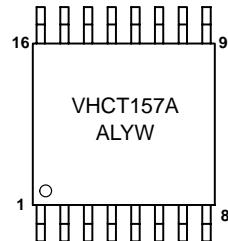
### MARKING DIAGRAMS



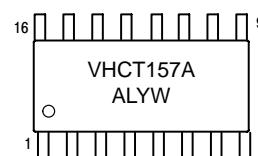
SO-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



EIAJ SO-16  
M SUFFIX  
CASE 966



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT157AD	SO-16	48 Units/Rail
MC74VHCT157ADR2	SO-16	2500 Tape & Reel
MC74VHCT157ADT	TSSOP-16	96 Units/Rail
MC74VHCT157ADTR2	TSSOP-16	2500 Tape & Reel
MC74VHCT157AM	EIAJ-SO-16	50 Units/Rail
MC74VHCT157AMEL	EIAJ-SO-16	2000 Tape & Reel

# MC74VHCT157A

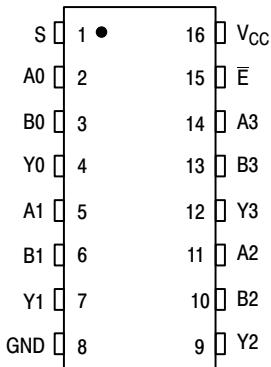


Figure 1. Pin Assignment

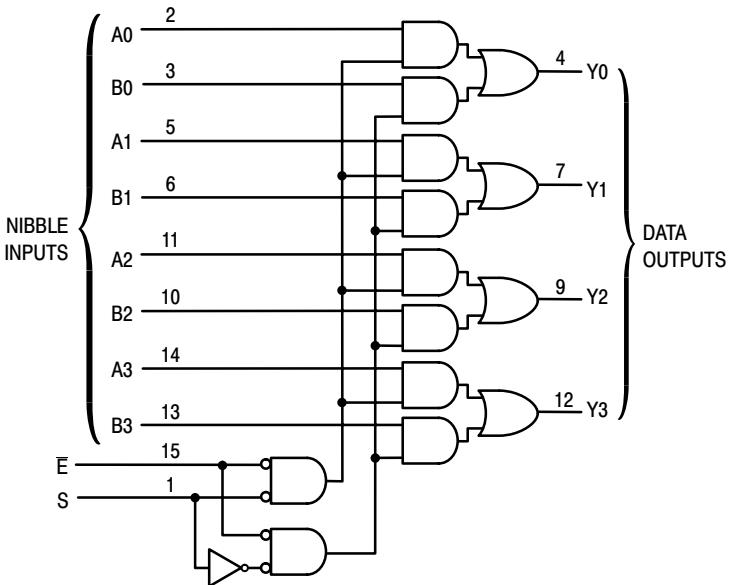


Figure 2. Expanded Logic Diagram

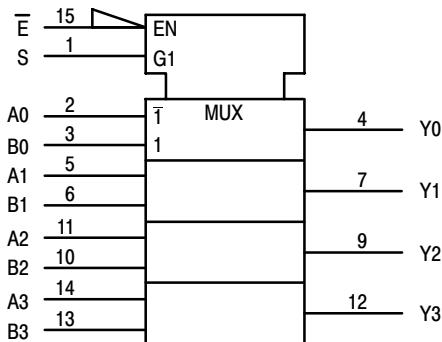


Figure 3. IEC Logic Symbol

## FUNCTION TABLE

Inputs		Outputs
$\bar{E}$	S	$Y_0 - Y_3$
H	X	L
L	L	$A_0 - A_3$
L	H	$B_0 - B_3$

$A_0 - A_3, B_0 - B_3$  = the levels of the respective Data-Word Inputs.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

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## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage	-0.5 to +7.0	V
$V_{IN}$	Digital Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	DC Output Voltage Output in 3-State High or Low State	-0.5 to +7.0 -0.5 to $V_{CC}$ +0.5	V
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current	$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air SOIC Package TSSOP	200 180	mW
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 2.) Machine Model (Note 3.) Charged Device Model (Note 4.)	>2000 >200 >2000	V
$I_{LATCH-UP}$	Latch-Up Performance Above $V_{CC}$ and Below GND at 125°C (Note 5.)	$\pm 300$	mA
$\theta_{JA}$	Thermal Resistance, Junction to Ambient SOIC Package TSSOP	143 164	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	4.5	5.5	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage Output in 3-State High or Low State	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, all Package Types	-55	125	°C
$t_r, t_f$	Input Rise or Fall Time $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	20	ns/V

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

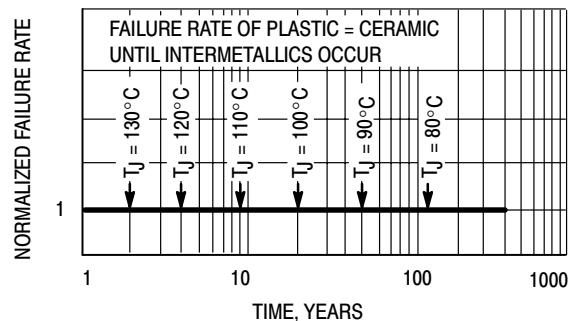


Figure 4. Failure Rate vs. Time Junction Temperature

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## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2			2	0.8	2		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8		0.8	V
V <sub>OH</sub>	Maximum High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	4.5	4.4	4.5		4.4		4.4		V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -8 mA	4.5	3.94			3.8		3.66		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	4.5		0.0	0.1		0.1		0.1	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = 8 mA	4.5			0.36		0.44		0.52	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0		40.0	μA
I <sub>CCT</sub>	Additional Quiescent Supply Current (per Pin)	Any one input: V <sub>IN</sub> = 3.4 V All other inputs: V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.35		1.5		1.5	μA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0			0.5		5		5	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay A to B to Y	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.6 8.0	7.0 10.0	1.0 1.0	7.7 11.0	1.0 1.0	7.7 11.0	ns	
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		4.1 5.6	6.4 8.4	1.0 1.0	7.5 9.5	1.0 1.0	7.5 9.5		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay S to Y	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.1 8.5	7.5 10.5	1.0 1.0	8.2 11.5	1.0 1.0	8.2 11.5	ns	
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.3 6.8	8.1 10.1	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5		
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay $\bar{E}$ to Y	V <sub>CC</sub> = 3.3 ± 0.3 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.1 8.5	7.5 10.5	1.0 1.0	8.2 11.5	1.0 1.0	8.2 11.5	ns	
		V <sub>CC</sub> = 5.0 ± 0.5 V C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.6 7.1	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0		
C <sub>IN</sub>	Maximum Input Capacitance				4	10		10		10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 6.)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V				pF
		20				

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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**NOISE CHARACTERISTICS** (Input  $t_r = t_f = 3.0\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $V_{CC} = 5.0\text{ V}$ )

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.8	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.8	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

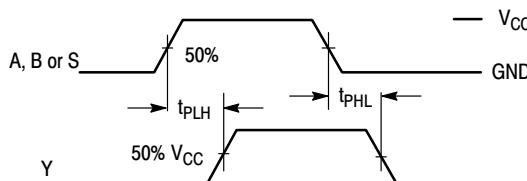


Figure 5. Switching Waveform

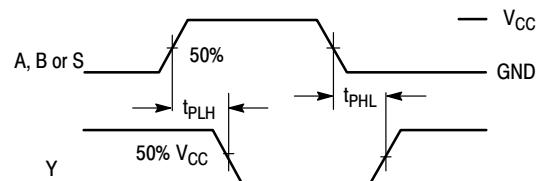
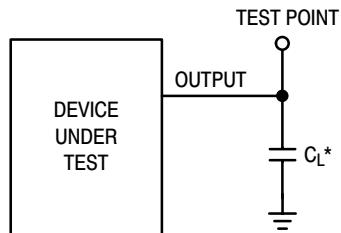


Figure 6. Inverting Switching



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

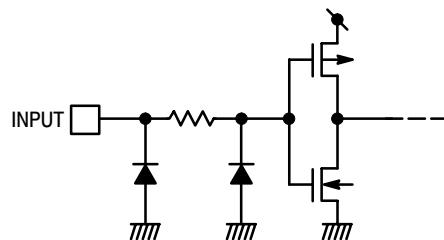
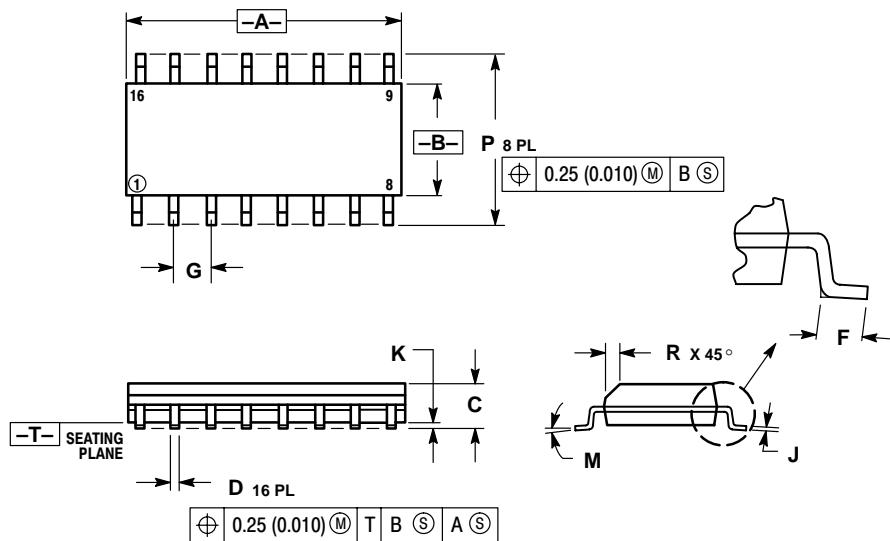


Figure 8. Input Equivalent Circuit

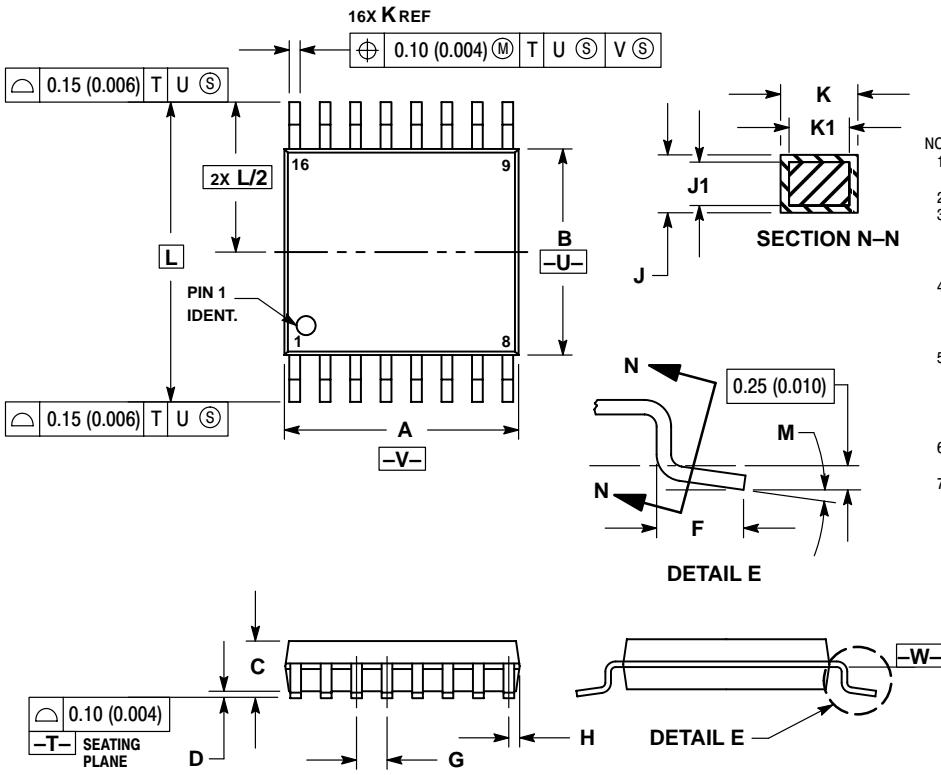
# MC74VHCT157A

## PACKAGE DIMENSIONS

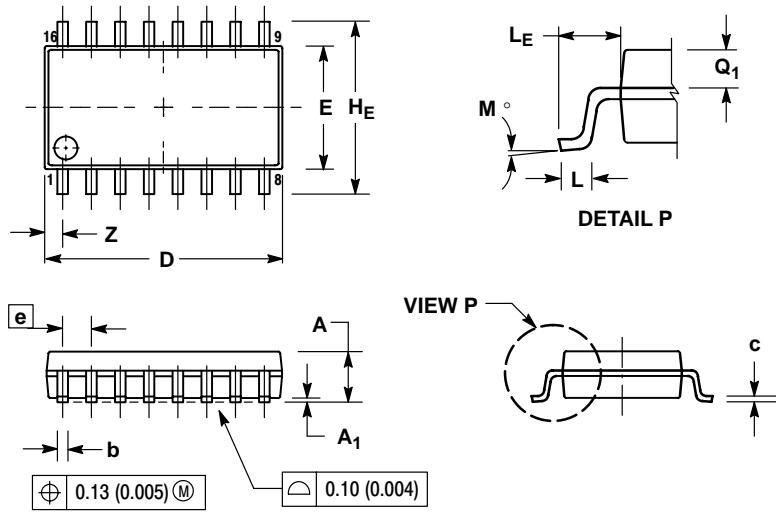
SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



## PACKAGE DIMENSIONS

SOIC EIAJ-16  
M SUFFIX  
CASE 966-01  
ISSUE O

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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