FEMTOCLOCKS™ 680MHZ, CRYSTAL-TO-3.3V DIFFERENTIAL LVPECL FREQUENCY SYNTHESIZER

ICS843202I

General Description

The ICS843202I is a 2 output LVPECL Synthesizer optimized to generate Gigabit Ethernet and SONET reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. Using a 19.44MHz and 25MHz, 18pF parallel resonant crystal, 155.52MHz and 156.25MHz frequencies can be generated. The part also allows the use of a recovered clock at QB output. The ICS843202I uses IDT's FemtoClock™ low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter. The ICS843202I is packaged in a 32-pin LQFP package.

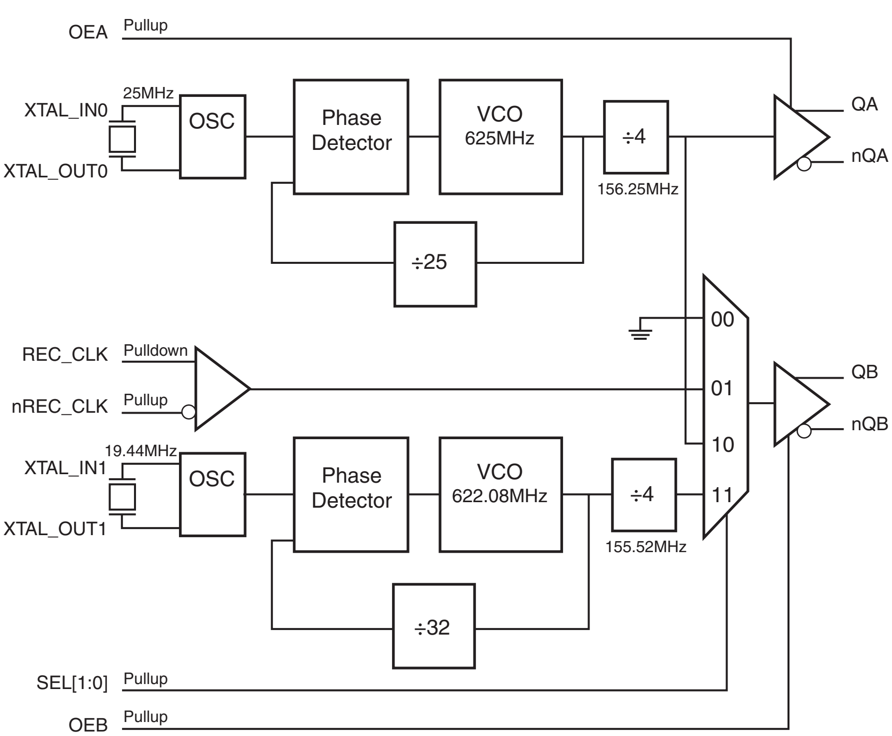
SELBx Function Table

Control Inputs	Outputs
SEL[1:0]	**nQB, QB**
00	High, Low
01	REC_CLK
10	156.25MHz driven by XTAL_0
11	155.52MHz driven by XTAL_1

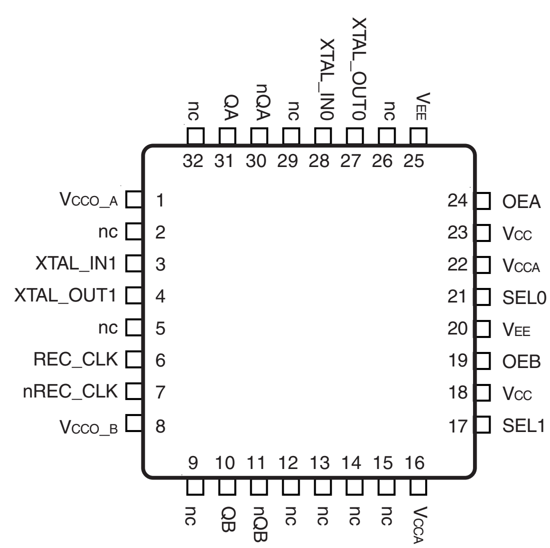
Features

- Two 3.3V LVPECL outputs
- Selectable crystal oscillator interface or one differential recovered clock inputs
- Supports the following output frequencies: 155.52MHz and 156.25MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz – 1.3MHz): 0.86ps (typical)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz –- 20MHz): 0.56ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS843202I
32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCO_A}	Power		Output supply pin for Bank A output.
2, 5, 9, 12, 13, 14, 15, 26, 29, 32	nc	Unused		No connect.
3, 4	XTAL_IN1, XTAL_OUT1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
6	REC_CLK	Input	Pulldown	Non-inverting differential recovered clock inputs.
7	nREC_CLK	Input	Pullup	Inverting differential recovered clock inputs.
8	V_{CCO_B}	Power		Output supply pin for Bank B output.
10, 11	QB, nQB	Ouput		Differential output pair. LVPECL interface levels.
16, 22	V_{CCA}	Power		Analog supply pins.
17, 21	SEL1, SEL0	Input	Pullup	Select pins. See SELx Function Table. LVCMOS/LVTTL interface levels.
18, 23	V_{CC}	Power		Core supply pins.
19	OEB	Input	Pullup	Output enable pin. QB/nQB output is enabled. LVCMOS/LVTTL interface levels.
20, 25	V_{EE}	Power		Negative supply pins.
24	OEA	Input	Pullup	Output enable pin. QA/nQA output is enabled. LVCMOS/LVTTL interface levels.
27, 28	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
30, 31	nQA, QA	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	80.8°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.22	3.3	V_{CC}	V
V_{CCO_A}, V_{CCO_B}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				138	mA
I_{CCA}	Analog Supply Current				22	mA

Table 3B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OEA, OEB, SEL0, SEL1	$V_{CC} = V_{IN}$ = 3.63V			5	µA
I_{IL}	Input Low Current	OEA, OEB, SEL0, SEL1	V_{CC} = 3.63V, V_{IN} = 0V	-150			µA

Table 3C. Differential DC Characteristics, $V_{CC} = V_{CCO\_A} = V_{CCO\_B}$ = 3.3V±10%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	REC_CLK	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		nREC_CLK	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REC_CLK	V_{CC} = 3.63V, V_{IN} = 0V	-5			µA
		nREC_CLK	V_{CC} = 3.63V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.

TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 10\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_A,\ \_B}$ - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		19.44		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

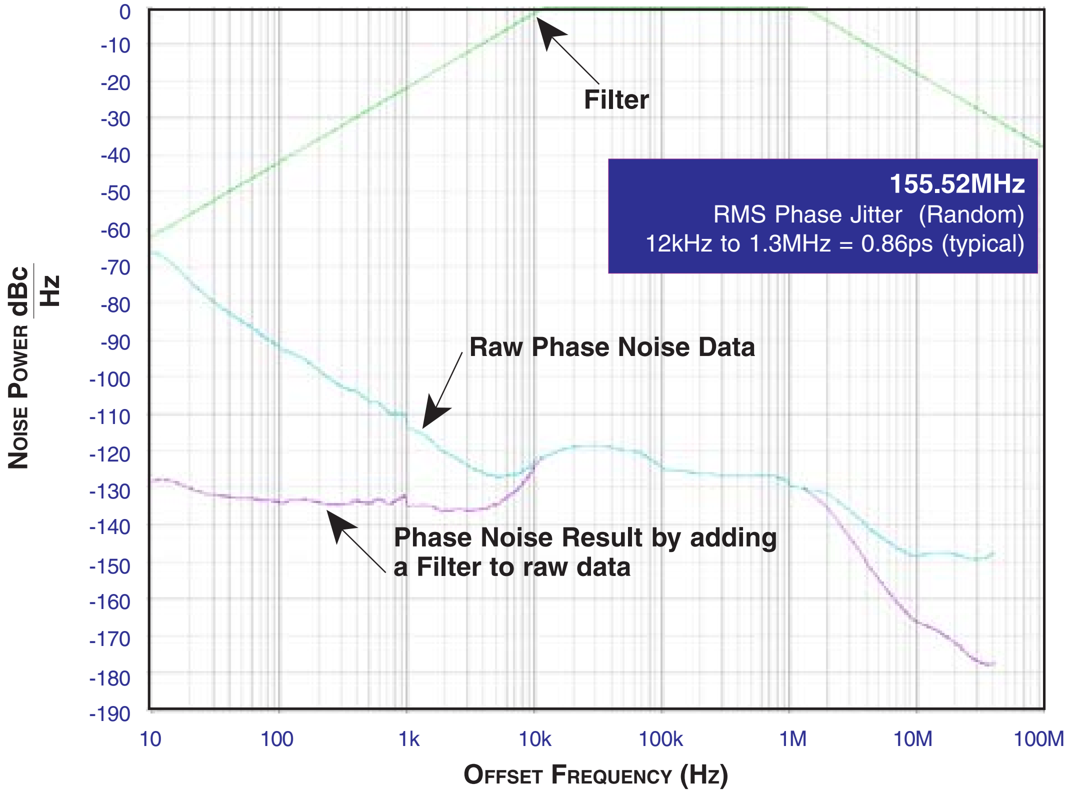
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO\_A} = V_{CCO\_B} = 3.3V \pm 10\%$, TA = -40°C TO 85°C

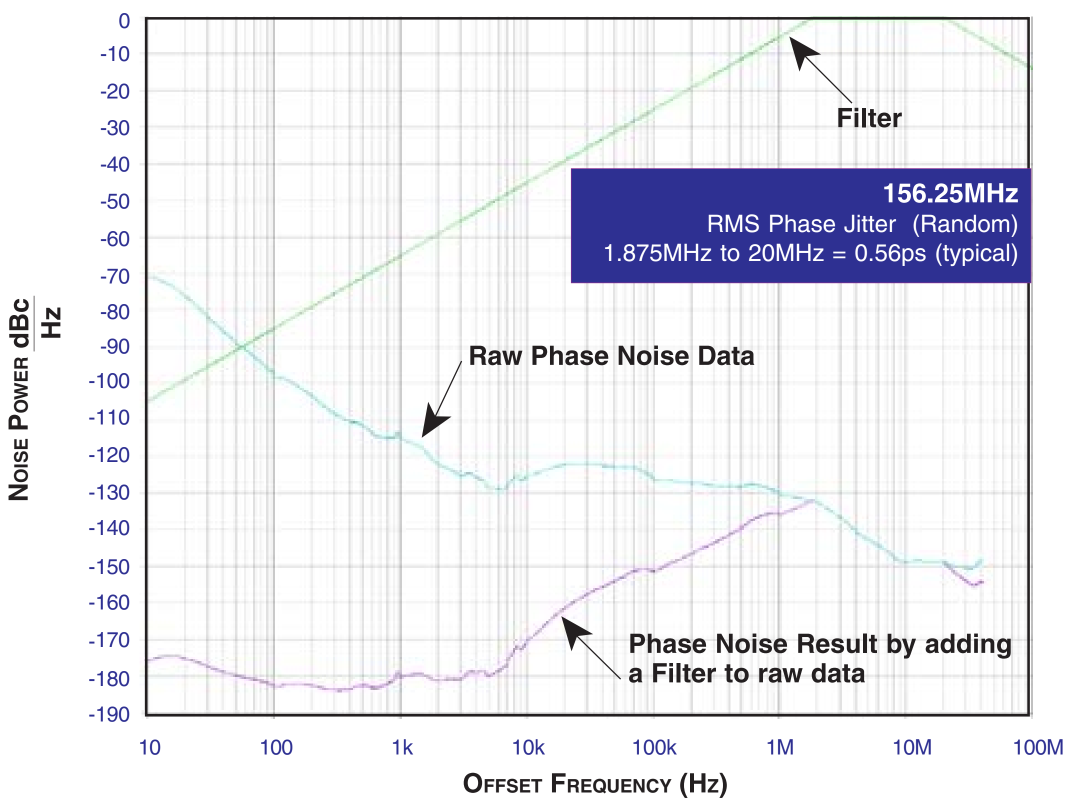
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QB/nQB	PLL Mode	140	155.52	170	MHz
		QA/nQA		140	156.25	170	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1		155.52MHz, (12kHz - 1.3MHz)		0.86		ps
			156.25MHz, (1.875MHz - 20MHz)		0.56		ps
t_R / t_F	Output Rise/Fall Time		PLL Mode, 20% to 80%	300		550	ps
odc	Output Duty Cycle		PLL Mode	49		51	%

All parameters measured up to 170MHz unless otherwise specified.
NOTE 1: See Phase Noise plots.

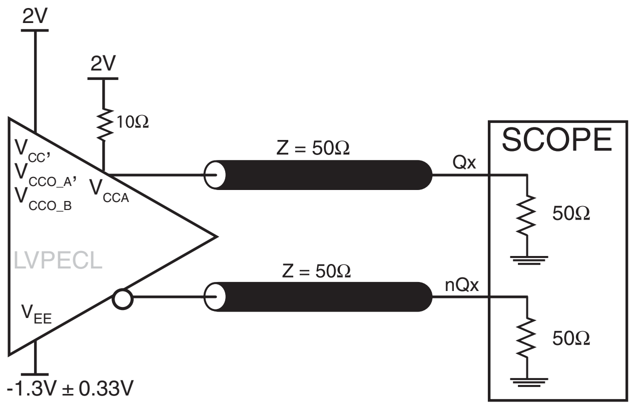
Typical Phase Noise at 155.52MHz



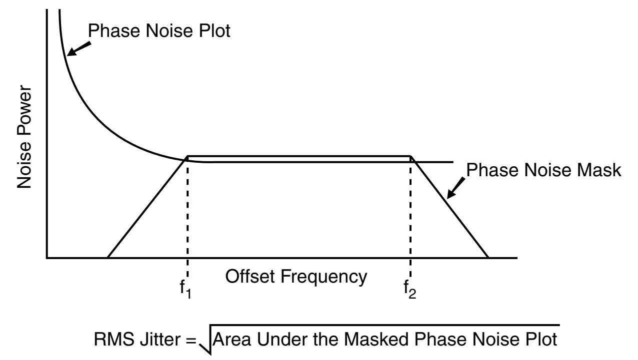
Typical Phase Noise at 156.25MHz



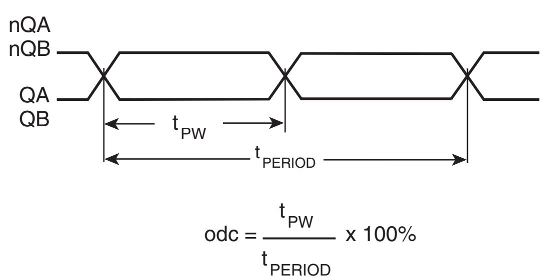
Parameter Measurement Information



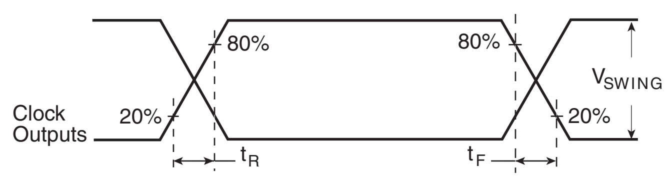
3.3V Core/3.3V Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843202I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO_x} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA}.

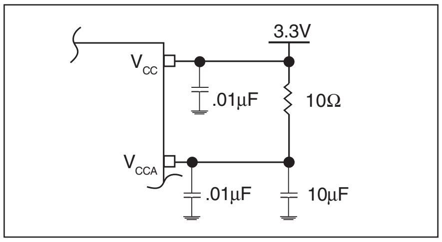


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS843202I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

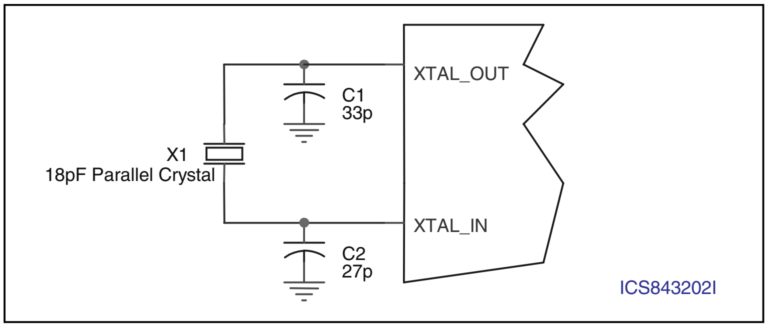


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

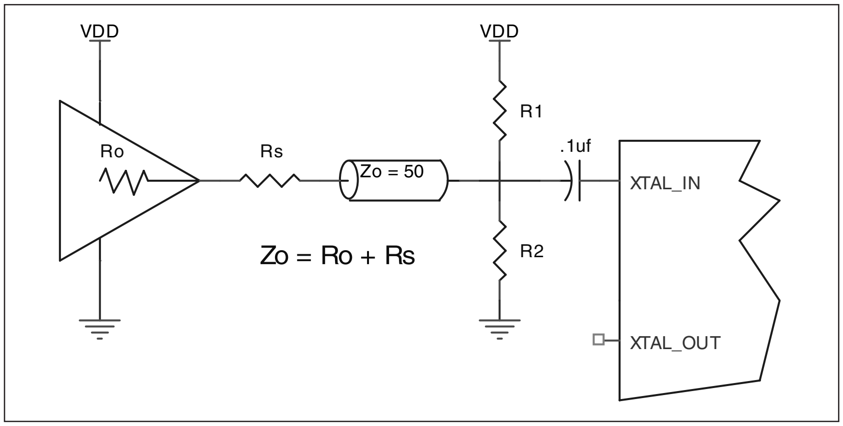


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REC_CLK/nREC_CLK Input:
For applications not requiring the use of the differential input, both REC_CLK and nREC_CLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from REC_CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

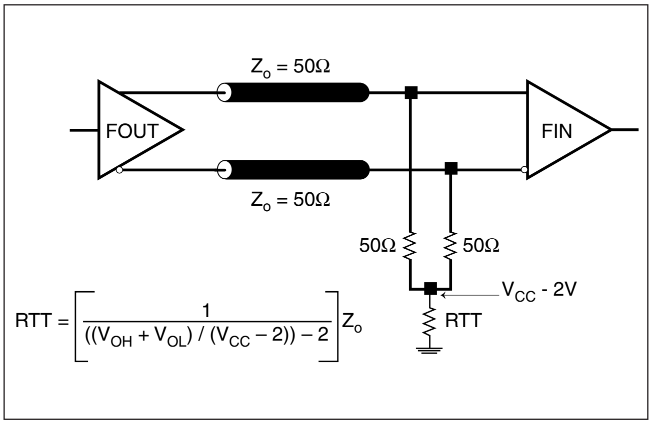


FIGURE 4A. LVPECL OUTPUT TERMINATION

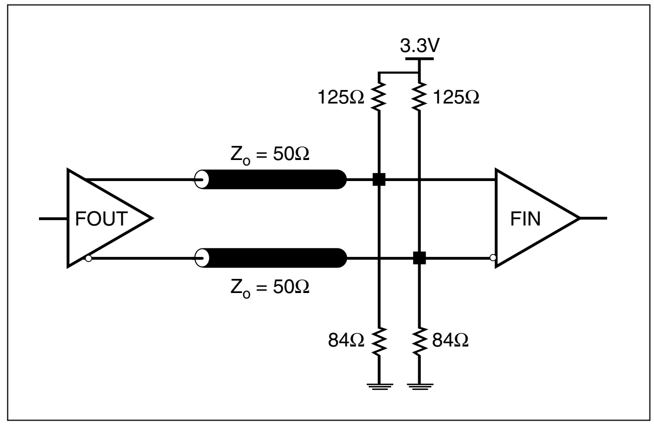


FIGURE 4B. LVPECL OUTPUT TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843202I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843202I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 138mA = **500.9mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

  Total Power $_{\_MAX}$ (3.63V, with all outputs switching) = 500.9mW + 60mW = **560.9mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A
Tj = Junction Temperature
θ_{JA} = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 71.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.561W * 71.2°C/W = 124.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Meter per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	80.8°C/W	71.2°C/W	67.6°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

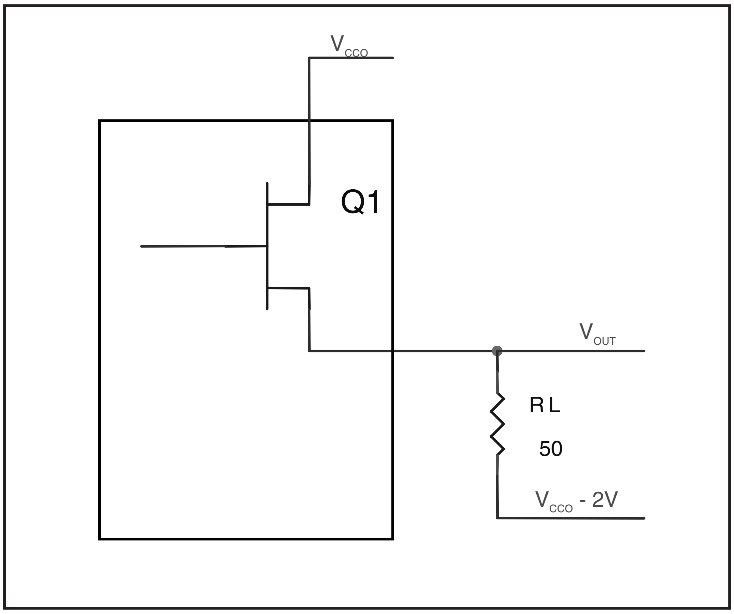


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 32 Lead LQFP

θ_{JA} by Velocity (Meter per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	80.8°C/W	71.2°C/W	67.6°C/W

Transistor Count

The transistor count for ICS843202I is: 3733

Package Outline - Y Suffix for 32 Lead LQFP

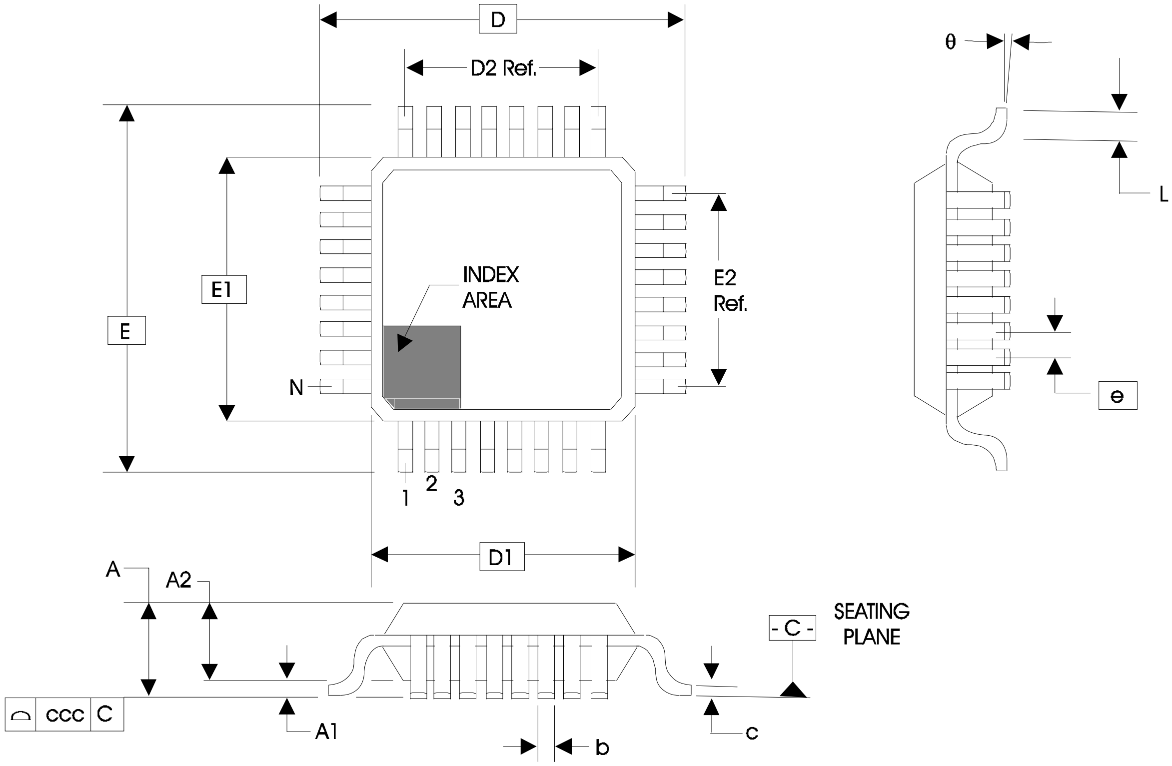


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS843202AYI	ICS843202AYI	32 Lead LQFP	tray	-40°C to 85°C
ICS843202AYIT	ICS843202AYI	32 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS843202AYILF	ICS843202AIL	32 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS843202AYILFT	ICS843202AIL	32 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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