

SN54ALS37A, SN74ALS37A QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

SDAS195A – APRIL 1982 – REVISED DECEMBER 1994

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

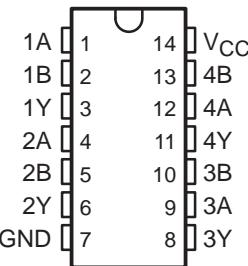
description

These devices contain four independent 2-input positive-NAND buffers. They perform the Boolean functions $Y = A \bullet B$ or $Y = \bar{A} + \bar{B}$ in positive logic.

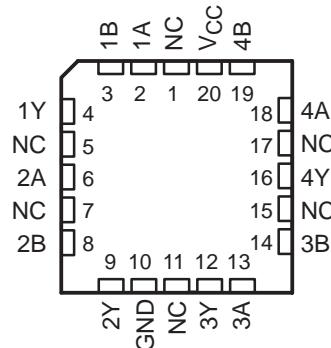
The SN54ALS37A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS37A is characterized for operation from 0°C to 70°C .

FUNCTION TABLE (each gate)		
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SN54ALS37A . . . J PACKAGE
SN74ALS37A . . . D OR N PACKAGE
(TOP VIEW)

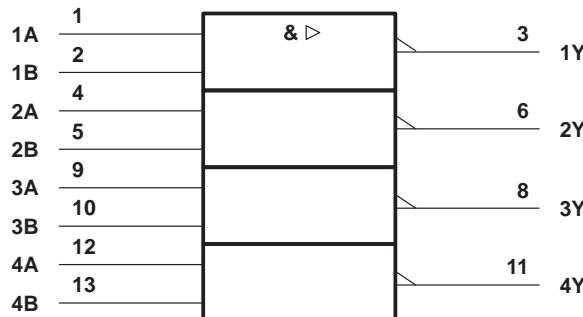


SN54ALS37A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

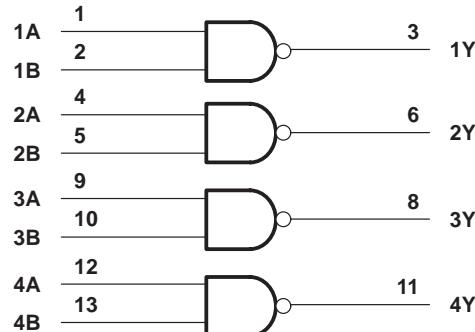
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS37A SN74ALS37A	-55°C to 125°C 0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS37A			SN74ALS37A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS37A			SN74ALS37A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA		-1.5			-1.5		V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V, $I_{OH} = -0.4$ mA		$V_{CC} - 2$		$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA	2.4	3.3		2.4	3.3	
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4	0.25	0.4	V
		$I_{OL} = 24$ mA				0.35	0.5	
I_I	$V_{CC} = 5.5$ V, $V_I = 7$ V		0.1			0.1		mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20		20		μA
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.1		-0.1		mA
$I_O\$$	$V_{CC} = 5.5$ V, $V_O = 2.25$ V	-20	-112		-30	-112		mA
I_{CCH}	$V_{CC} = 5.5$ V, $V_I = 0$		0.86	1.6	0.86	1.6		mA
I_{CCL}	$V_{CC} = 5.5$ V, $V_I = 4.5$ V		4.8	7.8	4.8	7.8		mA

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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switching characteristics (see Figure 1)

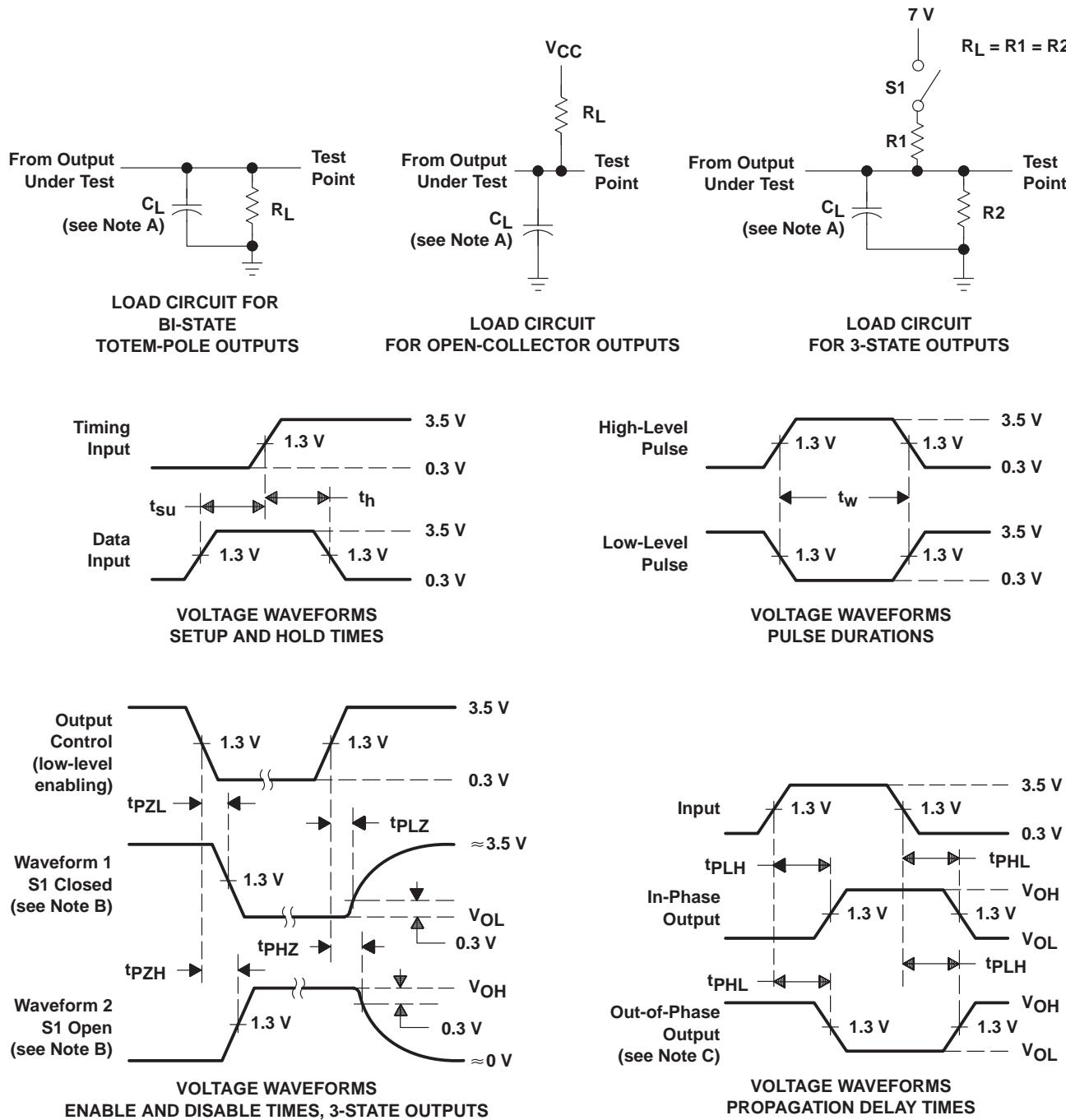
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\text{ }\Omega$, $T_A = \text{MIN to MAX}^\dagger$				UNIT	
			SN54ALS37A		SN74ALS37A			
			MIN	MAX	MIN	MAX		
t_{PLH}	A or B	Y	2	17	2	8	ns	
			2	9	2	7		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS37AN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS37AN
SN74ALS37AN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS37AN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

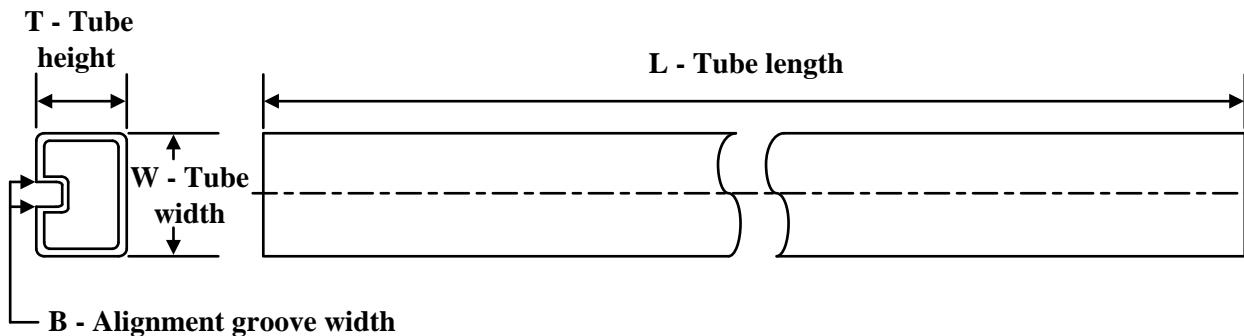
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


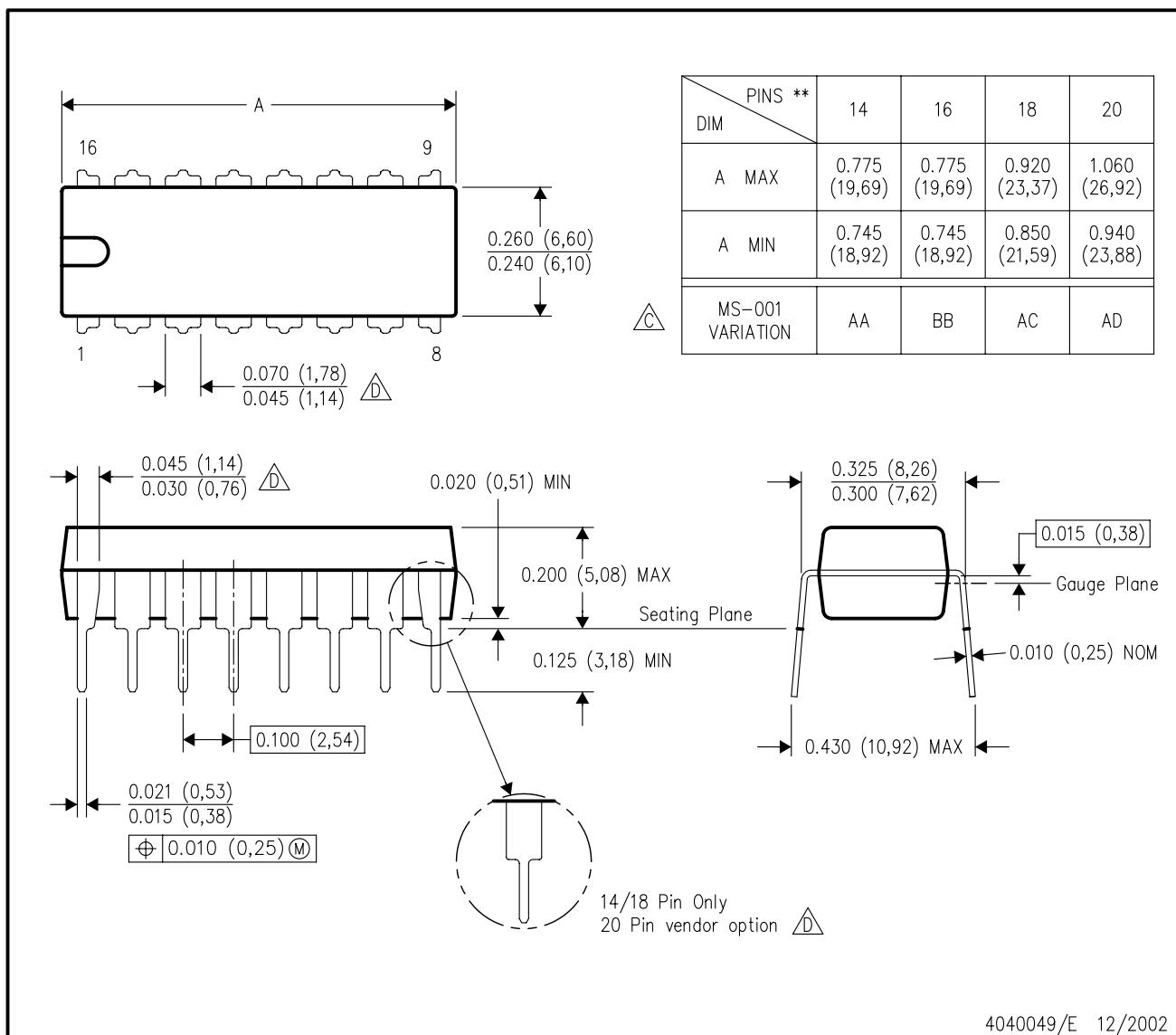
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74ALS37AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS37AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS37AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS37AN.A	N	PDIP	14	25	506	13.97	11230	4.32

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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