LM3551 /LM3552 1A White LED Driver with Flash Timeout Protection

Check for Samples: LM3551, LM3552

FEATURES

- **Up to 1A Total Drive Current**
- **Flash Timeout Protection**
- **Independent Torch/Flash/Shutdown Modes**
- **LED Disconnect in Shutdown**
- **Programmable Soft-Start Limits Inrush Current**
- **Over-Voltage Protection**
- **Wide Voltage Range 2.7 to 5.5V**
- **1.25MHz Constant Switching Frequency**
- **Small, Low Profile Package, Non-Pullback WSON(4mm x 4mm)**

APPLICATIONS

- **White LED Camera Flash**
- **White LED Torch (Flashlight)**
- **DSC (Digital Still Camera) Flash**
- **Cellular Camera Phone Flash**
- **PDA Camera Flash**
- **Camcorder Torch (Flashlight) Lamp**

DESCRIPTION

The LM3551 and LM3552 are fixed frequency, current mode step-up DC/DC converters with two integrated NFETs that can be used for precision LED brightness control. The devices are capable of driving loads up to 1A from a single-cell Li-Ion battery.

The LM3551 and LM3552 can drive one or more high current flash LEDs either in a high power Flash mode or a lower power Torch mode using the TORCH/FLASH pin. A programmable Timeout function on the FTO pin forces the internal NFETs to turn off after a certain user defined time. An external SD pin (LM3551) or EN pin (LM3552) is available to put the device into low power shutdown mode. During shutdown, the feedback resistors and the load are disconnected from the input to avoid leakage current paths to ground.

User programmable soft-start circuitry has been integrated to eliminate large inrush currents at start-up. Over-voltage protection circuitry and a 1.25MHz switching frequency allow for the use of small, low-cost output capacitors with lower voltage ratings. The LM3551 and LM3552 are available in a low profile 14-pin WSON package.

Typical Application Circuits
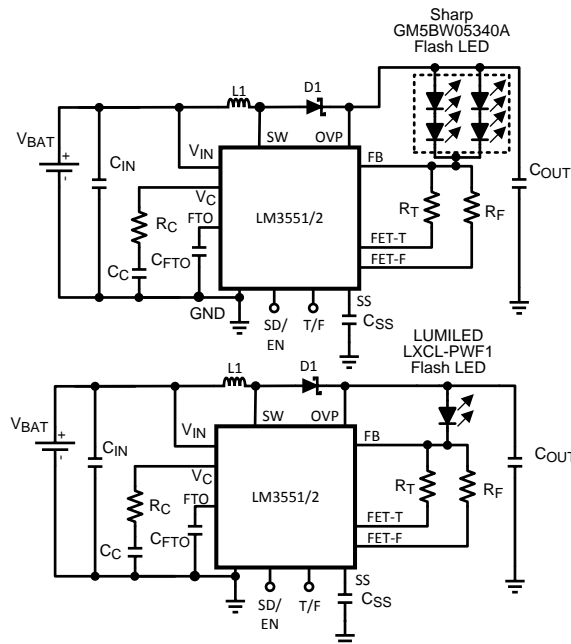
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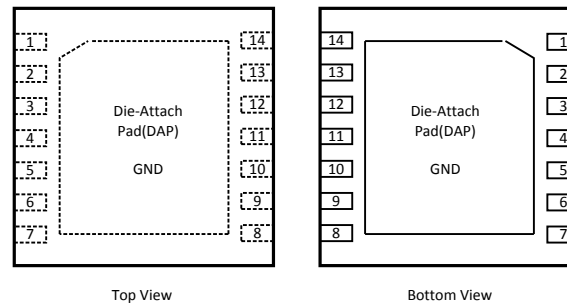
LM3551, LM3552

Connection Diagram

14-Pin WSON Package

Figure 1. Package Number NHL0014B

PIN DESCRIPTIONS

Pin	Name	Function
9	V_{IN}	Input Voltage. Input range: 2.7V to 5.5V.
13	T/F	TORCH/FLASH Pin. Low = Torch Mode, High = Flash Mode
8	SW	Switch Pin
10	OVP	Over Voltage Protection Pin
3	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
5	SD(LM3551) EN(LM3552)	Shutdown pin logic input. High = Shutdown, Low = Enabled Enable pin logic input. High = Enabled, Low = Shutdown
12	FTO	Flash Timeout. External capacitor determines max. duration allowed flash pulse
11	SS	Soft Start Pin
4	FB	Feedback Pin
14	FET-T	Torch FET Drain
2	FET-F	Flash FET Drain
1,7,DAP	GND	Ground
6	AGND	Analog Ground. Connect the ground of the compensation components, C_{FTO} and soft start cap to AGND. AGND must be connected to the GND pin through a low impedance connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)(3)]

V_{IN} pin: Voltage to GND	7.5V
SW pin: Voltage to GND	21V
FB pin: Voltage to GND	7V
V_C pin: Voltage to GND	1.26V ± 0.3V
SD,T/F pins: Voltage to GND	7.5V
FET-T, FET-F: Voltage to GND	6V
Continuous Power Dissipation[(4)]	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to +150
ESD Rating[(5)]	Human Body Model	2.0kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=140ºC (typ.) and disengages at T_J=120ºC (typ.).
(5) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7)

Operating Ratings[(1)(2)]

Input Voltage Range	2.7V to 5.5V
SW Voltage Max.[(3)]	20V
Junction Temperature (T_J) Range	-40°C to +110°C
Ambient Temperature (T_A) Range[(4)]	-40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Maximum recommended SW pin voltage when the OVP pin is grounded.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 110ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), NHL0014B Package[(1)]	37.3°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics[1][2]

Limits in standard typeface are for T_J = +25° C. Limits in boldface type apply over the full operating junction temperature range (-40°C ≤ T_J ≤ +110°C). Unless otherwise noted, specifications apply to the LM3551 and LM3552 Typical Application Circuit (pg. 1) with: V_{IN} = 3.6V, V(SD) = 0V for LM3551 and V(EN) = V_{IN} for LM3552, I_{LOAD} = 0A[3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_Q	Quiescent Current	FB = V_{IN} (Not Switching)		1.47	**2.0**	mA
I_{SD}	Shutdown Current	V(SD) = V_{IN}, LM3551		2.55	**5.0**	μA
		V(EN) = 0V, LM3552		0.1	**2.3**	
I_{CL}[4]	Switch Current Limit	V_{IN} = 3.0V[5]		2.1		A
V_{FB}	Feedback Voltage		**1.2285**	1.265	**1.2915**	V
I_{FB}[6]	Feedback Pin Bias Current			50		nA
g_m	Error Amp Transconductance	ΔI = 5μA		135		μmho
A_V	Error Amp Voltage Gain			135		V/V
D_{MAX}	Maximum Duty Cycle			92.5		%
f_{sw}	Switching Frequency		**0.9**	1.25	**1.6**	MHz
I_{SDPIN}	Shutdown Pin Current (LM3551)	V_{SD} = 0V		3.0	**6**	μA
I_{ENPIN}	Enable Pin Current (LM3552)	V_{EN} = 3.6V		3.0	**6**	μA
$I_{T/FPIN}$	T/F Pin Current	$V_{T/F}$ = 0V		26		nA
		$V_{T/F}$ = V_{IN}		22		
I_{L-SW}	SW Pin Leakage Current	V_{L-SW} = 20V		0.07	**8**	μA
$R_{DSON-SW}$	SW Pin R_{DSON}	I_{SW} = 0.5A		0.165		Ω
I_{L-T}	FET-T Leakage Current			0.1		μA
R_{DSON-T}	FET-T R_{DSON}			0.98		Ω
I_{L-F}	FET-F Leakage Current			0.1		μA
R_{DSON-F}	FET-F R_{DSON}			0.36		Ω
$Th_{SD/EN}$	Shutdown/Enable Pin Threshold	Output High	**1.2**			V
		Output Low			**0.3**	
$Th_{T/F}$	T/F Pin Threshold	Output High	**1.2**			V
		Output Low			**0.3**	
UVP	Under Voltage Protection Thresholds	On Threshold	**2.25**	2.48	**2.70**	V
		Off Threshold	**2.43**	2.58	**2.77**	
OVP	Over Voltage Protection Thresholds	On Threshold	**11.3**	12.4	**14**	V
		Off Threshold	**9.2**	10.6	**12**	
V_{FTO}	Flash Timeout trip-point		**0.99**	1.16	**1.32**	V
I_{FTO}	Flash Timeout Current		**1.12**	1.4	**1.68**	μA
V_{SS}	Soft-Start Voltage		**1.18**	1.25	**1.32**	V
I_{SS}	Soft-Start Current		**10**	11.5	**13**	μA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers represent the most likely norm. Unless otherwise specified, conditions for Typ specifications are: V_{IN} = 3.6V and T_A = 25ᵒC.
(3) C_{IN} and C_{OUT},: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics
(4) Duty cycle affects current limit due to ramp generator.
(5) Current limit at 0% duty cycle. See TYPICAL PERFORMANCE section for Switch Current Limit vs. V_{IN}
(6) Bias current flows into FB pin.

Product Folder Links: *LM3551 LM3552*

Typical Performance Characteristics

Unless otherwise specified: T_A = +25°C; V_{IN} = 3.6V; L = 4.7µH, (R_C = 10kΩ, C_C = 4.7nF, C_{IN} = C_{OUT} = 10µF for Lumiled LED), (R_C = 27kΩ, C_C = 10nF, C_{IN} = 10µF, C_{OUT} = 4.7µF for Sharp LED), C_{FTO} = 1µF, C_{SS}= 0.1µF.

I_{CL} measure when V_{OUT} = 95% × V_{OUT} (nominal)

Current Limit vs. Input Voltage
V_{OUT} = 5V

Figure 2.

Current Limit vs. Input Voltage
V_{OUT} = 10V
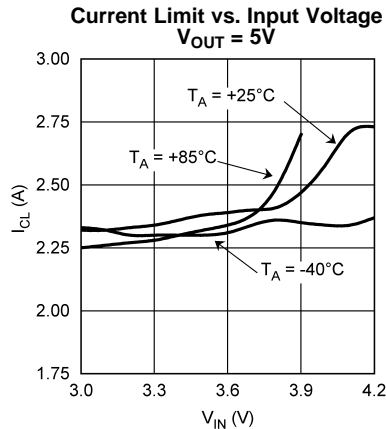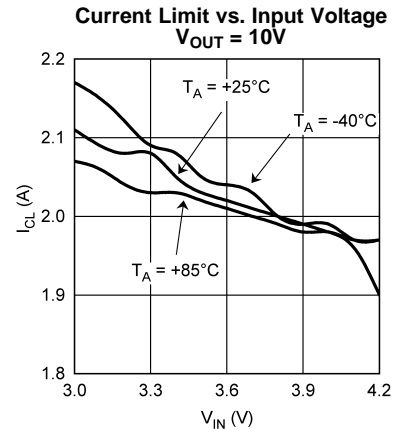
Figure 3.

I_{CL} measure when V_{OUT} = 95% × V_{OUT} (nominal)

Converter Efficiency vs. Input Voltage
Lumiled Flash LED

Figure 4.

Converter Efficiency vs. Input Voltage
Sharp Flash LED
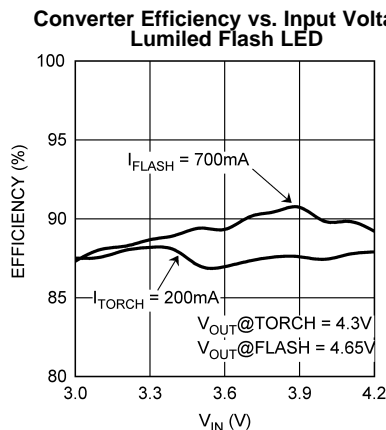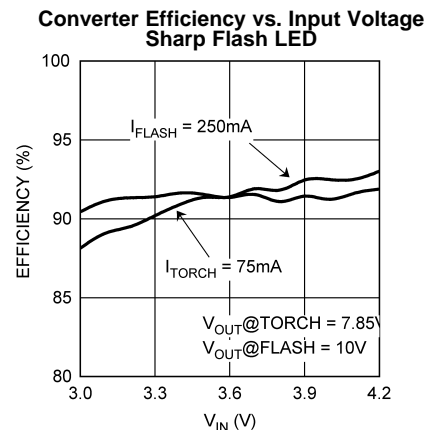
Figure 5.

I_{OUT} measured at 95%× V_{OUT} (nominal)

Maximum I_{OUT} vs. Input Voltage
V_{OUT} = 5V

Figure 6.

Maximum I_{OUT} vs. Input Voltage
V_{OUT} = 10V
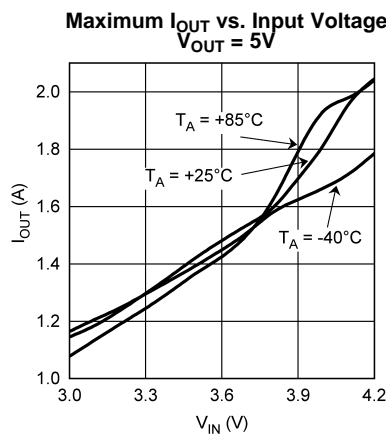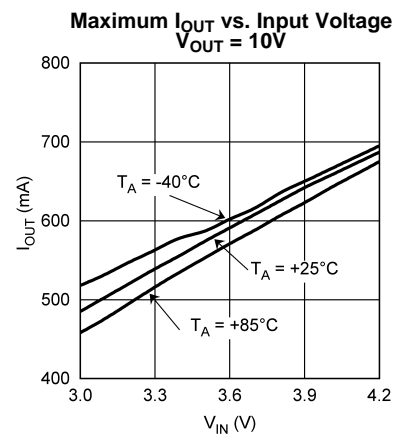
Figure 7.

I_{OUT} measured at 95%× V_{OUT} (nominal)

Product Folder Links: *LM3551 LM3552*

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = +25°C; V_{IN} = 3.6V; L = 4.7µH, (R_C = 10kΩ, C_C = 4.7nF, C_{IN} = C_{OUT} = 10µF for Lumiled LED), (R_C = 27kΩ, C_C = 10nF, C_{IN} = 10µF, C_{OUT} = 4.7µF for Sharp LED), C_{FTO} = 1µF, C_{SS}= 0.1µF.

**LED Torch Current
vs.
Input Voltage
Lumiled Flash LED**

Figure 8.

**LED Flash Current
vs.
Input Voltage
Lumiled Flash LED**

Figure 9.

**OVP Trip Voltage
vs.
Input Voltage**

Figure 10.

**Switching Frequency
vs.
Input Voltage**

Figure 11.

**Start-Up Waveform
Sharp LED**
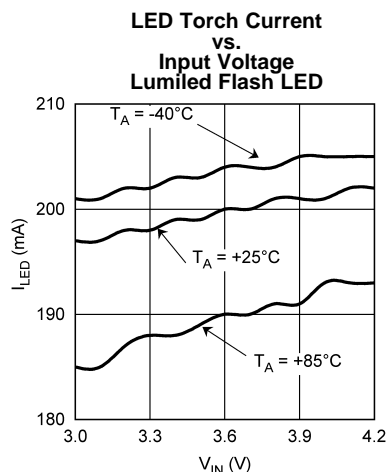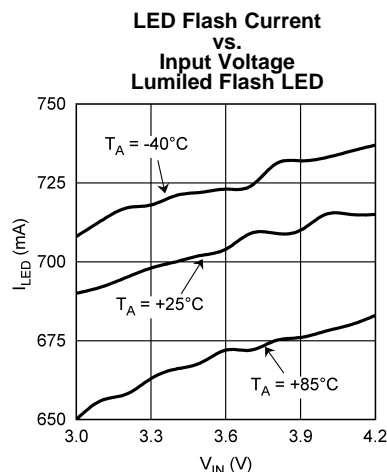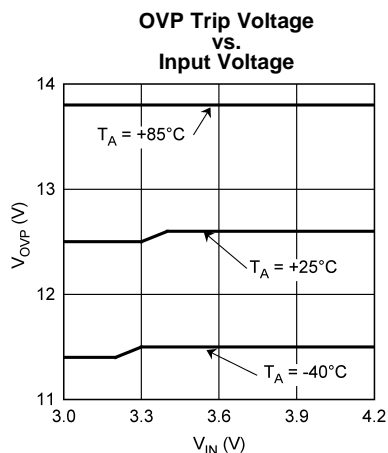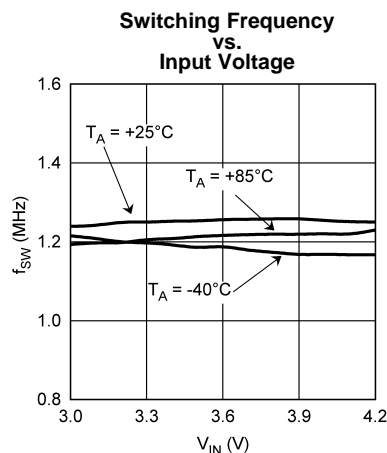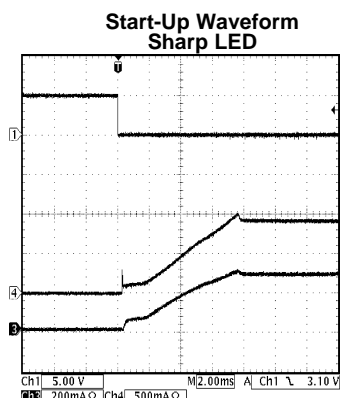
Figure 12. Ch1 = V_{SD}, Ch3 = I_{LED}, Ch4 = I_{IN}

**Start-Up Waveform
Lumiled LED**
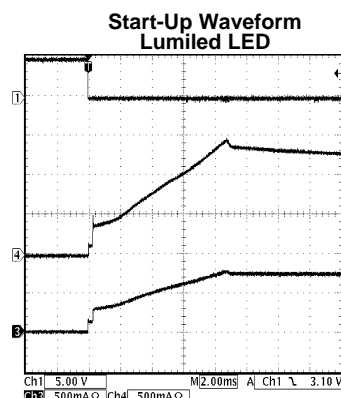
Figure 13. Ch1 = V_{SD}, Ch3 = I_{LED}, Ch4 = I_{IN}

Product Folder Links: *LM3551 LM3552*

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = +25°C; V_{IN} = 3.6V; L = 4.7µH, (R_C = 10kΩ, C_C = 4.7nF, C_{IN} = C_{OUT} = 10µF for Lumiled LED), (R_C = 27kΩ, C_C = 10nF, C_{IN} = 10µF, C_{OUT} = 4.7µF for Sharp LED), C_{FTO} = 1µF, C_{SS}= 0.1µF.

Typical Switching Waveform
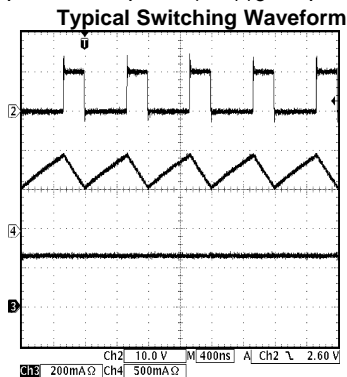
Figure 14. Sharp LED in Flash Mode
Ch1 = V_{SW}, Ch3 = I_{LED}, Ch4 = I_L

Block Diagram

Product Folder Links: *LM3551 LM3552*
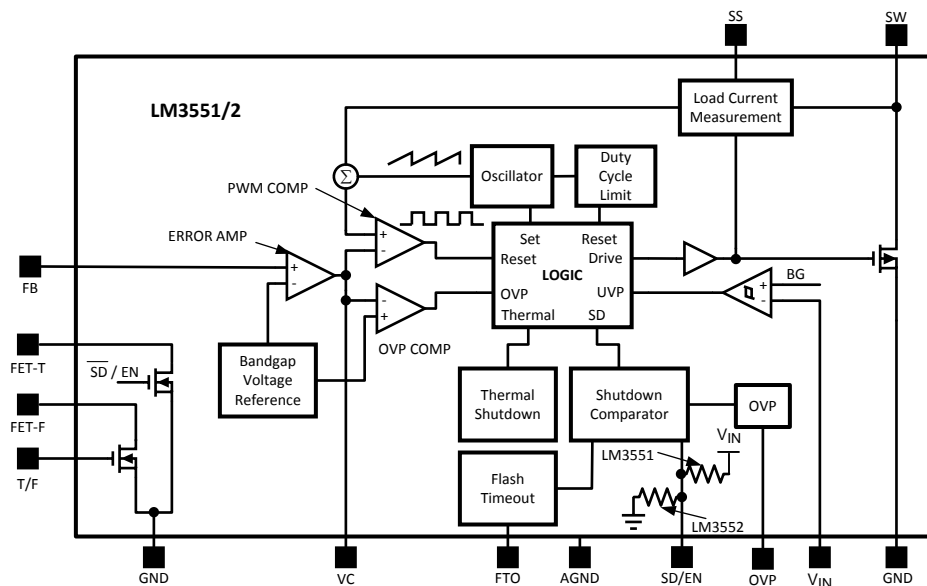
Circuit Description

OVERVIEW

The LM3551/2 are high power white LED flash drivers capable of delivering up to 1A of output current. The devices utilize a highly efficient inductive DC/DC boost converter to achieve the required output voltage. A current-mode PWM control scheme regulates the output current over a wide input voltage range. Both the LM3551 and the LM3552 have two low-side load disconnect FET's allowing for a continuous low-power Torch-mode and a high-power, short duration Flash-mode.

Several application specific safety features are integrated into the LM3551/2 design. A flash timeout circuit is present on-chip to prevent a failure in the flash LED caused by a timing violation. Over-Voltage Protection protects the output capacitor, inductor and main power switch in the event of an open circuit condition. Other safety features include inductor current limit, thermal shutdown, and an undervoltage lockout.

CIRCUIT COMPONENTS

Inductive DC/DC Boost Converter

In order to achieve the output voltages required to power high power white LEDs, the LM3551 and LM3552 utilize a highly efficient inductive DC/DC converter. The boost converter utilizes a current-mode controlled, constant frequency (1.25MHz.), PWM architecture. This architecture creates a predictable noise spectrum that allows for easy filtering and low noise. A very low on-resistance power NFET(R_{DSON} = 0.165Ω) and high value current limit (2.2A typ.) help efficiently provide a high power output (700mA@5V) over the entire lithium-ion voltage range. The feedback voltage for both the LM3551 and LM3552 is tightly regulated to 1.265V.

SD/EN Pin

The LM3551 and LM3552 provide two different options in regards to turn-on control logic. The LM3551 utilizes a shutdown pin (SD) that turns on the part when a voltage less than 0.3V is applied. An internal 1.2MΩ pull-up to V_{IN} is provided to place the LM3551 into shutdown when no control signal is provided. The LM3552 utilizes a enable pin (EN) that turns on the part when a voltage greater than 1.2V is applied. An internal 1.2MΩ pull-down to GND is provided to place the LM3552 into shutdown when no control signal is provided.

Low-side Load Disconnect FETs

The LM3551 and LM3552 have two low-side load disconnect NFETs (FET-T and FET-F) that provide the physical mechanism of Torch Mode and Flash Mode. In Torch Mode, FET-T is enabled allowing current to flow through it. FET-T has an on-resistance of 0.98Ω and is capable of handling currents up to 200mA. In Flash Mode, both FET-T and FET-F are enabled. FET-F has an on-resistance of 0.36Ω and is capable of handling currents up to 500mA. The total Flash current is equal to the sum total of the current flowing through FET-T and FET-F. See the CURRENT SET EQUATIONS in the Application Informations section for more information regarding setting LED current .

In shutdown mode, the LM3551/2 provide a true load disconnect helping to keep the total shutdown current to a minimum.

Over-Voltage Protection (OVP)

The over voltage protection (OVP) is engaged when a failure mode occurs (FB pin grounded, Flash LED becomes open or disconnected, etc.). In the event of a failure, OVP prevents the output voltage from exceeding 12.4V (typ). When the OVP level is reached, the switch FET shuts off preventing the output voltage from climbing higher. Once the FET has shut off, the output will droop at a rate determined by the value of the output capacitor and current leakage through the OVP pin and any other leakage path. When the output voltage drops to 10.6V(typ), switching will resume. The LM3551 and LM3552 will go back into OVP if the failure is still present resulting in a pulsed output condition.

NOTE
To disable OVP, ground to OVP pin. **CAUTION: The LM3551 and LM3552 may be damaged if an OVP condition occurs and OVP is disabled.**

Under-Voltage Protection (UVP)

Both the LM3551 and LM3552 have under-voltage protection circuitry (UVP). This protects the NMOS power device during startup and shutdown by preventing operation at voltages less than the minimum input voltage. The UVP protection is enabled at 2.48V(typ.) and will not disable until the input voltage rises above 2.58V(typ.) .

Torch/Flash Pin (T/F)

The TORCH/FLASH pin (T/F) controls whether the LM3551/2 is in continuous torch mode, or in flash mode. A logic '0' places the part into torch mode and a logic '1' places the part into flash mode. There are no pull-ups or pull-downs internally connected to T/F. When placed into torch mode, FET-T is enabled allowing the current set by R_T to flow. In torch mode, FET-F is not enabled. Flash mode enables both FET-T and FET-F allowing the sum total of the current set by the two external resistors, R_T and R_F, to flow.

Flash Timeout Protection (FTP)

When SD is low(LM3551) or EN is high(LM3552), and T/F is high, a current is output to an external capacitor, C_{FTO}. This causes the voltage on the capacitor to rise. If the voltage reaches Vtrip (1.16V(typ)), the timeout circuit forces the INTERNAL_EN signal to go low, which in turn shuts-off the low-side torch and flash FETs in addition to disabling the main power SW FET. At such time, the LED will be turned off. The part will remain disabled until SD is pulled high (LM3551) or EN is pulled low (LM3552) and/or T/F is pulled low. At that point, the part will return to normal operating mode. The diagram below shows a first pulse which exceeds the timeout period and internal_EN being driven low. The second FLASH pulse is shorter than the timeout period and therefore the voltage on C_{FTO} never reaches Vtrip. For information on component selection, please see the *FLASH TIMEOUT EQUATIONS* below.

$$T_{FTO} = C_{FTO} \times (\Delta V_{FTO} \div I_{FTO}) \qquad (1)$$

$$\Delta V_{FTO} = 1.16V \text{ and } I_{FTO} = 1.4\mu A \quad T_{FTO} = \text{Desired Timeout Duration} \qquad (2)$$

$$C_{FTO}(\mu F) = T_{FTO}(sec.) \times 1.21(\mu A/V) \qquad (3)$$
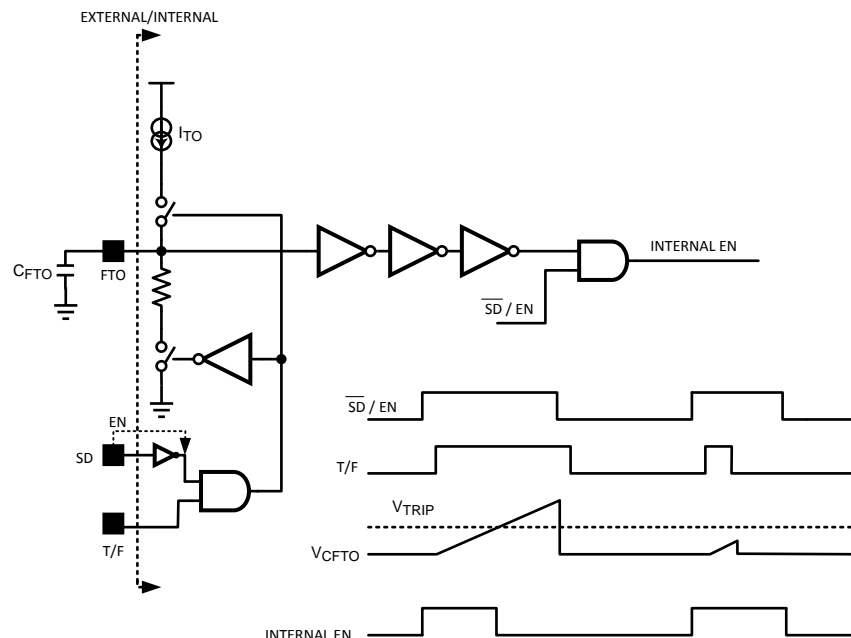
To disable the timeout function, ground the FTO pin.

Figure 15. Flash Timeout Protection Diagram

Product Folder Links: *LM3551 LM3552*

Soft-Start

The LM3551 and LM3552 have a soft-start pin that can be used to limit the inductor inrush current on start-up. The external SS pin is used to tailor the soft-start for a specific application but is not required for all applications and can be left open when not needed. When used, a current source charges the external soft-start capacitor, C_{SS}, forcing the internal reference to ramp-up at a user determined rate.

Table 1. Typical Start-Up Times V_{IN} = 3.6V, T_A = +25°C

C_{SS} (μF)	Load (mA)	Start-Up Time (msec.)
0.1	Sharp LED @ 75mA Torch	3
	Sharp LED @ 250mA Flash	8
	Lumiled LED @ 200mA Torch	1.6
	Lumiled LED @ 700mA Flash	6
0.47	Sharp LED @ 75mA Torch	12
	Sharp LED @ 250mA Flash	35
	Lumiled LED @ 200mA Torch	6
	Lumiled LED @ 700mA Flash	35
1.0	Sharp LED @ 75mA Torch	25
	Sharp LED @ 250mA Flash	75
	Lumiled LED @ 200mA Torch	30
	Lumiled LED @ 700mA Flash	70

Product Folder Links: *LM3551 LM3552*

APPLICATION INFORMATION

LM3551 AND LM3552 FUNCTIONALITY TRUTH TABLE

SD (LM3551) or EN (LM3552)	T/F	LM3551 Result	LM3552 Result
1	0	Shut-down	Torch Mode
1	1	Shut-down	Flash Mode
0	0	Torch Mode	Shut-down
0	1	Flash Mode	Shut-down

The LM3551 has a 1.2MΩ pull-up to V_{IN} on SD and the LM3552 has a 1.2MΩ pull-down to GND on EN.

CURRENT SET EQUATIONS

The LM3551/2 utilize inline resistors to set the Torch and Flash LED currents. The Torch-Mode current (continuous) and the Flash-Mode current (pulsed) are programmed by placing the appropriately selected resistors between the feedback pin (FB) and FET-T (torch FET) and FET-F (flash FET) pins. Torch-mode is set by utilizes the current through one resistor while Flash-mode is set by utilizes the currents though both current set resistors. The following equations are used to set the LED currents.

$$R_{TORCH} = (1.265V / I_{TORCH}) - R_{DSON-T} \tag{4}$$

$$R_{FLASH} = (1.265V / (I_{FLASH} - I_{TORCH})) - R_{DSON-F} \tag{5}$$

$$R_{DSON-T} = 0.98\Omega \text{ and } R_{DSON-F} = 0.36\Omega \tag{6}$$

NOTE
Flash LEDs from different manufacturers can have very different continuous and pulse current ratings. See the manufacturers datasheets to ensure that the proper current levels are used to avoid damaging the flash LED.

INDUCTOR SELECTION

Special care must be taken when selecting an inductor for use in LM3551/2 applications. The inductor should have a current saturation rating that is larger than the worst case peak inductor current of the application to ensure proper operation. Using an inductor with a lower saturation current rating than is required can cause a dramatic drop in the inductance and can derate the maximum output current levels severely. It is worth noting that the output voltage ripple is also affected by the total ripple current in the inductor. The following equations can help give a good approximation as to what the peak inductor current will be for a given application at room temperature (T_A = +25°C).

$$I_L(\text{average}) = [I_{LED} \times V_{OUT-MAX}] \div [V_{IN-MIN} \times \text{Eff.}] \tag{7}$$

$$\Delta I_L = [V_{IN} \times D] \div [L \times F_{SW}] \tag{8}$$

$$I_L(\text{peak}) = I_L(\text{ave}) + [\Delta I_L \div 2] \tag{9}$$

$V_{OUT-MAX}$ Maximum Output Voltage. Maximum output voltage over temperature with OVP used is 11V (12.4V typically).

V_{IN-MIN} Minimum Input Voltage. Recommended minimum input voltage is 3.0V. The LM3551/2 will work down to 2.7V however, use at lower input voltages will required an inductor with a higher saturation current rating.

Eff. Converter Efficiency (approx. 85% over input voltage range).

D Duty Cycle = 1 - [V_{IN} / V_{OUT}]

L Inductance. **Recommended inductance value is 4.7µH.**

F_{SW} Switching Frequency = 1.25MHz

Product Folder Links: *LM3551 LM3552*

DIODE SELECTION

The output diode for a boost regulator must be chosen correctly depending on the output voltage and output current. The output diode must have a reverse voltage rating equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

CAPACITOR SELECTION

Input Capacitor

An input capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used under normal operating condtions while a 10-22µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

Output Capacitor

A minimum output capacitor value of 4.7µF (Sharp LED) and 10µF (Lumiled) is recommended and may be increased to a larger value. The ESR of the output capacitor is important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2 \times \Delta I_L \times R_{ESR} \text{ (in Volts)} \tag{10}$$

After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi[R_{ESR} + (V_{OUT}/I_{LED})]C_{OUT}} \text{ Hz}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR}C_{OUT}} \text{ Hz} \tag{11}$$

The zero created by the ESR of the output capacitor is generally at a very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. The output capacitor pole information is useful in selecting the proper compensation components and is discussed in the Compensation Components section of the datasheet.

Capacitor Properties

Surface-mount multi-layer ceramic capacitors are recommended for both the input and output capacitors. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM3551/2 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM3551/2. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM3551/2. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1µF. Such deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM3551/2.

The minimum voltage rating acceptable for the input capacitor is 6.3V (10V recommended) and 16V for the output capacitor. In applications that have DC operating points near the maximum voltage rating of the ceramic capacitor, larger capacitor values may be required to compensate for capacitance loss due to capacitor voltage coefficient. See the capacitor manufacturer's datasheet for DC bias performance.

Product Folder Links: *LM3551 LM3552*

COMPENSATION

DC Gain and Open-Loop Gain

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM3551/2, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin.

To ensure a bandwidth of ½ or less of the frequency of the RHP zero, calculate the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left(\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega c Leff)// R_L]//R_L\}\right) \text{ (in dB)} \tag{12}$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)} \tag{13}$$

$$Leff = \frac{L}{(D')^2} \tag{14}$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)} \tag{15}$$

$$mc \cong 0.072 \times fs \text{ (in V/s)} \tag{16}$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \text{ (in V/s)} \tag{17}$$

where R_L is the minimum load resistance, fs is the switching frequency, V_{IN} is the minimum input voltage, g_m is the error amplifier transconductance and R_{DSON-S} is the power switch on-resistance. The value for g_m and R_{DSON-S} are found in the Electrical Characteristics table.

Right Half Plane Zero

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$RHPzero = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD}L} \text{ (in Hz)} \tag{18}$$

where I_{LOAD} is the maximum load current.

Compensation Components

The LM3551 and LM3552 provide a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in the typical application circuit. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM3551/2 circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ Hz}$$

(19)

where R_O is the output impedance of the error amplifier, approximately 900kΩ. Since R_C is generally much less than R_O, it has little effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

(20)

Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, and change each value slightly if needed to ensure both component values are in the recommended range. For both typical applications circuits shown on the front page, the **Recommended value for C_C is 4.7nF and R_C = 10kΩ for Lumiled applications. 10nF and 27kΩ are recommended for Sharp applications.**

RECOMMENDED MINIMUM COMPONENT SPECIFICATIONS

Component	Value	Ratings
L1	4.7µH	2.0A 30% I_{SAT} Rating
C_{IN}	4.7µF (Sharp)	10V X5R or X7R
	10µF (Lumiled)	
C_{OUT}	4.7µF (Sharp)	16V X5R or X7R
	10uF (Lumiled)	
C_{FTO}	User Determined	6.3V X5R or X7R
C_C	4.7nF (Lumiled)	6.3V X5R or X7R
	10nF (Sharp)	
R_C	10kΩ (Lumiled)	
	27kΩ (Sharp)	
R_{FLASH}	User Determined	Application Specific
R_{TORCH}	User Determined	Application Specific
C_{SS}	User Determined	6.3V X5R or X7R

Torch and Flash Resistor ratings are dependent upon the current through each resistor. The minimum ratings will vary depending upon the current selected on an applicaiton by application basis. Power Rating Minimum = (Desired Current)[2] × Resistor Value. See the CURRENT SET EQUATIONS section to determine torch and flash currents.

Product Folder Links: *LM3551 LM3552*

THERMAL PROTECTION

Internal thermal protection circuitry disables the LM3551/2 when the junction temperature exceeds +140°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below +120°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

PCB LAYOUT CONSIDERATIONS

The WSON is a leadframe based Chip Scale Package (CSP) with very good thermal properties. This package has an exposed DAP (die attach pad) at the center of the package measuring 2.6mm x 3.0mm. The main advantage of this exposed DAP is to offer lower thermal resistance when it is soldered to the thermal land pad on the PCB. For PCB layout, Texas Instruments highly recommends a 1:1 ratio between the package and the PCB thermal land. To further enhance thermal conductivity, the PCB thermal land may include vias to a ground plane. For more detailed instructions on mounting WSON packages, please refer to Application Note AN-1187 (SNOA401)

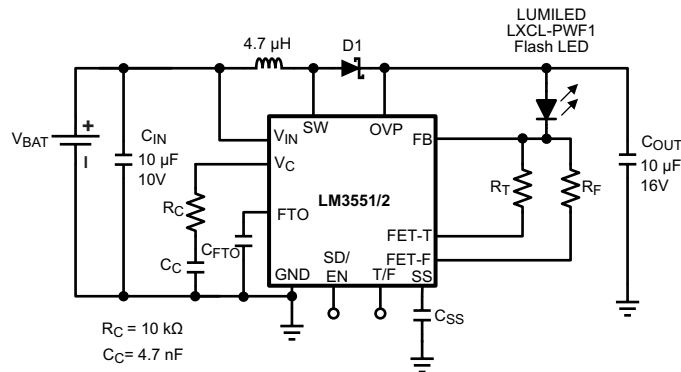## Application Examples

TYPICAL CONFIGURATIONS

Figure 16. LUMILED LXCL-PWF1
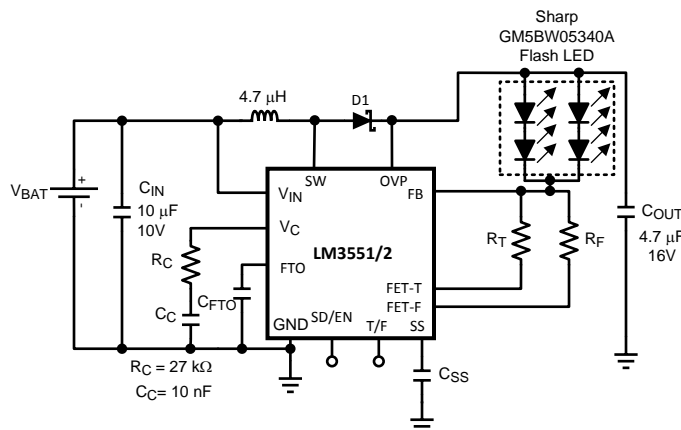$R_T = 5.6\Omega$, $R_F = 2.2\Omega$
$I_{TORCH} = 200mA$, $I_{FLASH} = 700mA$

Figure 17. SHARP GM5BW05340A
$R_T = 17\Omega$, $R_F = 6.5\Omega$
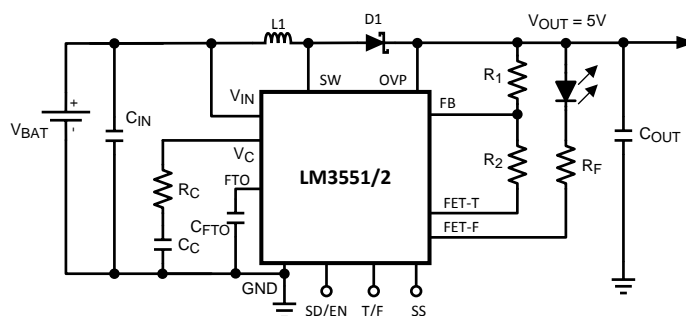$I_{TORCH} = 75mA$, $I_{FLASH} = 250mA$

Product Folder Links: *LM3551 LM3552*

DUAL-MODE CONFIGURATION[(1)]

Figure 18. R_1 = 29.5kΩ, R_2 = 10kΩ R_F = 3Ω
I_{FLASH} = 500mA

Using the Dual-Mode configuration with either the LM3551/2, a 5V, high current rail (approx. 700mA total) can be created while still allowing for a high flash with a true load disconnect. R1 and R2 setup the +5V following the equation: V_{OUT} = 1.265 × (1 + R1/R2) . When the LM3551/2 is on, and the T/F pin is low (logic '0'), the part will provide a regulated output voltage that can be used to provide a voltage rail within a system. By setting the T/F pin high, the LM3551/2 will allow the current to flow through the flash LED while still maintaining the fixed output voltage rail. The flash current is set by R_F using the equation R_F = [(V_{OUT} - V_{LED}) / I_{LED}] - 0.36Ω , and should not exceed 500mA. The total usable output current is dependent upon the output voltage selected. If the dual-mode configuration is used, the FTO pin should be grounded to prevent the voltage rail from being shutdown at an unwanted time.

(1)   Please refer to the RECOMMENDED MINIMUM COMPONENT SPECIFICATIONS section of the datasheet for more information.

Product Folder Links: *LM3551 LM3552*

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D   **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3551SD/NOPB	OBSOLETE	WSON	NHL	14		TBD	Call TI	Call TI	-40 to 85	L3551SD	
LM3552SD/NOPB	OBSOLETE	WSON	NHL	14		TBD	Call TI	Call TI	-40 to 85	L3552SD	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
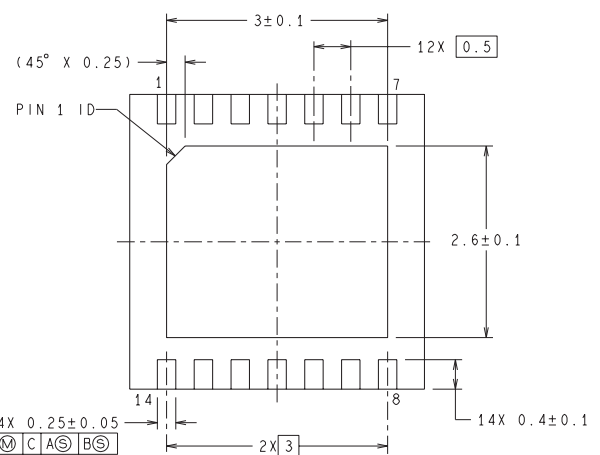
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NHL0014B

(3)

(3.8)

(2.6)

(14X 0.6)

(14X 0.25)

(12X 0.5)

RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

(0.1)

PIN 1 INDEX AREA

4±0.1

4±0.1

B

A

C

0.8 MAX

(0.2)

3±0.1

(45° X 0.25)

12X 0.5

PIN 1 ID

1

7

2.6±0.1

14

8

14X 0.25±0.05

⊕ 0.1 Ⓜ C AⓈ BⓈ

2X 3

14X 0.4±0.1

SDA14B (Rev A)

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