19-3483; Rev 0; 11/04

EVALUATION KIT AVAILABLE

Dual PCI Express, Hot-Plug Controller

General Description

The MAX5946 dual hot-plug controller is designed for PCI Express™ applications. The device provides hot-plug control for 12V, 3.3V, and 3.3V auxiliary supplies of two PCI express slots. The MAX5946's logic inputs/outputs allow interfacing directly with the system hot-plug management controller or through an SMBus™ with an external I/O expander. An integrated debounced attention switch and present-detect signals are included to simplify system design.

The MAX5946 drives four external n-channel MOSFETs to control the 12V and 3.3V main outputs. The 3.3V auxiliary outputs are controlled through internal 0.3Ω n-channel MOSFETs. Internal charge pumps provide gate drive for the 12V outputs while the gate drive of the 3.3V output is driven by the 12V input supply. The 3.3V auxiliary outputs are completely independent from the main outputs with their own charge pumps.

At power-up, the MAX5946 keeps all of the external MOSFETs off until the supplies rise above their respective undervoltage lockout (UVLO) thresholds. The device keeps the internal MOSFETs off only until the auxiliary input supply rises above its UVLO threshold. Upon a turn-on command, the MAX5946 enhances the external and internal MOSFETs slowly with a constant gate current to limit the power-supply inrush current. The MAX5946 actively limits the current of all outputs at all times and shuts down if an overcurrent condition persists for longer than a programmable overcurrent timeout. Thermal-protection circuitry also shuts down all outputs if the die temperature exceeds +150°C. After an overcurrent or overtemperature fault condition, the MAX5946L latches off while the MAX5946A automatically restarts after a restart time delay. The device is available in a 36-pin (6mm × 6mm) thin QFN package and operates over the -40°C to +85°C temperature range.

Applications

Servers

Desktop Mobile Server Platforms

Workstations

Embedded Devices

Typical Application Circuit appears at end of data sheet.

SMBus is a trademark of Intel Corp.

PCI Express is a trademark of PCI-SIG Corp.

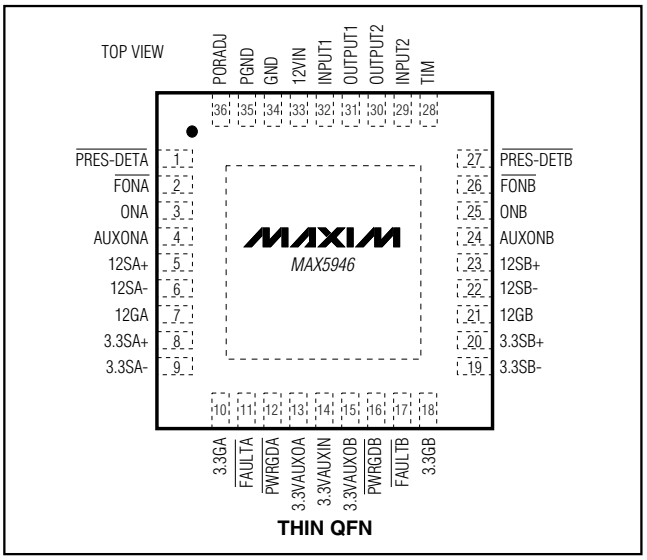
Features

- **PCI Express Compliant**
- **Hot Swaps 12V, 3.3V, and 3.3V Auxiliary for 2 PCI-E Slots**
- **Integrated Power MOSFET for Auxiliary Supply Rails**
- **Controls dI/dt and dV/dt**
- **Active Current Limiting Protects Against Overcurrent/Short-Circuit Conditions**
- **Programmable Current-Limit Timeout**
- **$\overline{\text{PWRGD}}$ Signal Outputs with Programmable Power-On Reset (POR) (160ms Default)**
- **Latched $\overline{\text{FAULT}}$ Signal Output after Overcurrent or Overtemperature Fault**
- **Attention Switch Inputs/Outputs with 4ms Debounce**
- **Present-Detect Inputs**
- **Forced-On Inputs Facilitates Testing**
- **Thermal Shutdown**
- **Allows Control through SMBus with an I/O Expander**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5946AETX	-40°C to +85°C	36 Thin QFN
MAX5946LETX	-40°C to +85°C	36 Thin QFN

Pin Configuration



Dual PCI Express, Hot-Plug Controller

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
12VIN.....-0.3V to +14V
12GA, 12GB .....-0.3V to (V_{12VIN} + 6V)
12SA+, 12SA-, 12SB+, 12SB-,
3.3GA, 3.3GB .....-0.3V to (V_{12VIN} + 0.3V)
3.3VAUXIN, ONA, ONB, $\overline{FAULTA}$, $\overline{FAULTB}$ .....-0.3V to +6V
$\overline{PWRGDA}$, $\overline{PWRGDB}$ .....-0.3V to +6V
PGND .....-0.3V to +0.3V
All Other Pins to GND.....-0.3V to ($V_{3.3VAUXIN}$ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
36-Pin Thin QFN (derate 26.3mW/°C above +70°C).....2.105W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{12VIN} = V_{12S_-} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3VAUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON}\_\_}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = 12G_ = 3.3G_ = OPEN, INPUT_ = $\overline{PRES\_DET\_}$ = PGND = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
12V SUPPLY						
12V Supply Voltage Range	V_{12VIN}		10.8	12	13.2	V
12VIN Undervoltage Lockout	V_{12UVLO}	V_{12VIN} rising	9.5	10	10.5	V
		Hysteresis		0.1		
12VIN Supply Current	I_{12VIN}	V_{12VIN} = 13.2V		0.5	1	mA
12VIN CONTROL						
12VIN Current-Limit Threshold (V_{12S_+} - V_{12S_-})	V_{12ILIM}		49	54	59	mV
12G_ Gate Charge Current	I_{12G_CHG}	$V_{12G\_}$ = GND	4	5	6	µA
12G_ Gate Discharge Current	I_{12G_DIS}	Normal turn-off, ON_ = GND, $V_{12G\_}$ = 2V	50	150	250	µA
		Output short-circuit condition, strong gate pulldown to regulation, V_{12VIN} - $V_{12S\_}$ ≥ 1V, $V_{12G\_}$ = 5V	50	120	180	mA
12G_ Gate High Voltage ($V_{12G\_}$ - V_{12VIN})	V_{12G_H}	$I_{12G\_}$ = 1µA	4.8	5.3	5.8	V
$\overline{12G\_}$ Threshold Voltage For $\overline{PWRGD\_}$ Assertion (Note 2)	V_{PGTH12}	Referred to V_{12VIN}, $I_{12G\_}$ = 1µA	-3.0	-4	-4.8	V
12S_- Input Bias Current					1	µA
12S_+ Input Bias Current				20	60	µA
3.3V SUPPLY						
3.3V Supply Voltage Range	$V_{3.3SA+}$, $V_{3.3SB+}$		3.0	3.3	3.6	V
Undervoltage Lockout (Note 3)		3.3SA+ rising	2.52	2.65	2.78	V
		Hysteresis		30		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{12VIN} = V_{12S_-} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3VAUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON}\_\_}$ = 3.3V, $\overline{PWRGD}\_$ = $\overline{FAULT}\_$ = PORADJ = TIM = OUTPUT_ = 12G_ = 3.3G_ = OPEN, INPUT_ = $\overline{PRES\_DET}\_$ = PGND = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V CONTROL						
3.3V Current-Limit Threshold ($V_{3.3S\_+}$ - $V_{3.3S\_-}$)	$V_{3.3ILIM}$		17	20	23	mV
3.3G_ Gate Charge Current	$I_{3.3G\_CHG}$	$V_{3.3G\_}$ = GND	4	5	6	µA
3.3G_ Gate Discharge Current	$I_{3.3G\_DIS}$	ON_ = GND, $V_{3.3G\_}$ = 2V	50	150	250	µA
		Output short-circuit condition, strong gate pulldown to regulation, $V_{3.3S\_+}$ - $V_{3.3S\_}$ ≥ 1V, $V_{3.3G\_}$ = 5V	100	150	220	mA
3.3G_ Gate High Voltage ($V_{3.3G\_}$ - $V_{3.3S\_+}$)	$V_{3.3G\_H}$	Sourcing 1µA	4.5	5.5	6.8	V
3.3G_ Threshold Voltage For $\overline{PWRGD}\_$ Assertion (Note 2)	$V_{PGTH3.3}$	Referred to $V_{3.3VAUXIN}$, $I_{3.3G\_}$ = 1µA	-3.0	-4	-4.5	V
3.3S_- Input Bias Current					1	µA
3.3S_+ Input Bias Current				20	60	µA
3.3V AUXILIARY SUPPLY						
3.3VAUXIN Supply Voltage Range	$V_{3.3VAUXIN}$		3.0	3.3	3.6	V
3.3VAUXIN Undervoltage Lockout	$V_{3.3VAUXUVLO}$	3.3VAUXIN rising	2.52	2.65	2.78	V
		Hysteresis		30		mV
3.3VAUXIN Supply Current		$V_{3.3VAUXIN}$ = 3.6V		1.5	3	mA
3.3VAUXIN to 3.3VAUXO_ Maximum Dropout		$I_{3.3VAUXO\_}$ = 375mA			225	mV
3.3VAUXO_ Current-Limit Threshold		3.3VAUXO_ shorted to GND	376	470	564	mA
3.3VAUXO_ Threshold For $\overline{PWRGD}\_$ Assertion ($V_{3.3VAUXIN}$ - $V_{3.3VAUXO\_}$) (Note 3)	$V_{PGTH3.3AUX}$				400	mV
LOGIC SIGNALS						
Input-Logic Threshold (ON_, $\overline{FON}\_$, AUXON_, $\overline{PRES\text{-}DET}\_$, INPUT_)		Rising edge	1.0		2.0	V
		Hysteresis		25		mV
Input Bias Current (ON_, AUXON_, INPUT_)					1	µA
$\overline{FON}\_$, $\overline{PRES\text{-}DET}\_$ Internal Pullup			25	50	75	kΩ
ON_, AUXON_ High-to-Low Deglitch Time				4		µs

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ELECTRICAL CHARACTERISTICS (continued)

(V_{12VIN} = V_{12S_-} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3VAUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON}\_\_}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = 12G_ = 3.3G_ = OPEN, INPUT_ = $\overline{PRES\_DET\_}$ = PGND = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

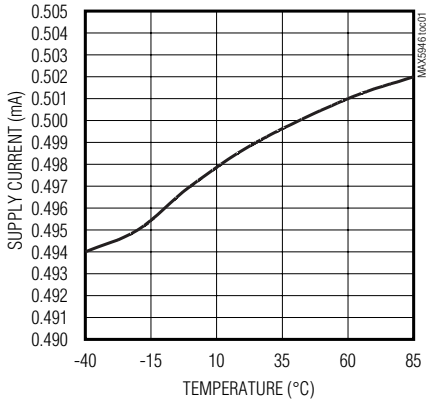
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{PRES\text{-}DET\_}$ High-to-Low Deglitch Time	t_{DEG}		3	5	7	ms
$\overline{PWRGD\_}$ Power-On Reset Time (Note 2)	t_{POR_HL}	PORADJ = open	90	160	250	ms
		R_{PORADJ} = 20kΩ	35	55	75	
		R_{PORADJ} = 100kΩ	145	265	380	
		R_{PORADJ} = 200kΩ		570		
$\overline{PWRGD\_}$ Low-to-High Deglitch Time	t_{POR_LH}			4		µs
$\overline{PWRGD\_}$, $\overline{FAULT\_}$ Output Low Voltage		Sinking 2mA			0.1	V
		Sinking 30mA			0.7	
$\overline{PWRGD\_}$, $\overline{FAULT\_}$ Output-High Leakage Current		$V_{\overline{PWRGD\_}}$ = $V_{\overline{FAULT\_}}$ = 5.5V			1	µA
$\overline{FAULT\_}$ Timeout	t_{FAULT}	TIM = open	5.5	11	17.0	ms
		R_{TIM} = 15kΩ	1.4	2.6	3.8	
		R_{TIM} = 120kΩ	12	22	32	
		R_{TIM} = 300kΩ		59		
$\overline{FAULT\_}$ Timeout During Startup	t_{SU}			2 x t_{FAULT}		ms
Autorestart Delay Time	$t_{RESTART}$			64 x t_{FAULT}		ms
Fault Reset Minimum Pulse Width (Note 4)	t_{RESET}			100		µs
Thermal-Shutdown Threshold	T_{SD}	T_J rising		+150		°C
Thermal-Shutdown Threshold Hysteresis				20		°C
OUTPUT_ Debounce Time	t_{DBC}		2.6	4.4	6.2	ms
OUTPUT_ High Voltage		Sourcing 2mA	$V_{3.3VAUXIN}$ - 0.3		$V_{3.3VAUXIN}$	V
OUTPUT_ Low Voltage		Sinking 2mA			0.4	V

Note 1: 100% production tested at T_A = +25°C. Parameters over temperature are guaranteed by design.
Note 2: $\overline{PWRGD\_}$ asserts a time t_{POR_HL} after V_{PGTH12}, $V_{PGTH3.3}$, and $V_{PGTH3.3AUX}$ conditions are met.
Note 3: The UVLO for the 3.3V supply is sensed at 3.3SA+.
Note 4: This is the time that ON_ or AUXON_ must stay low when resetting a fault condition.

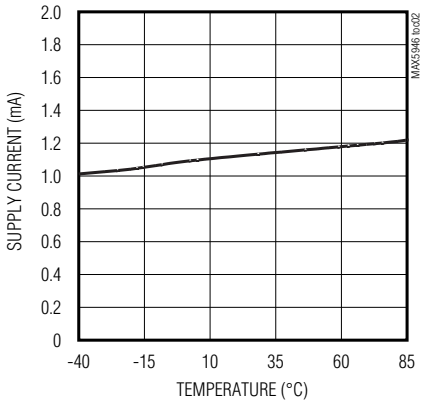
Typical Operating Characteristics

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

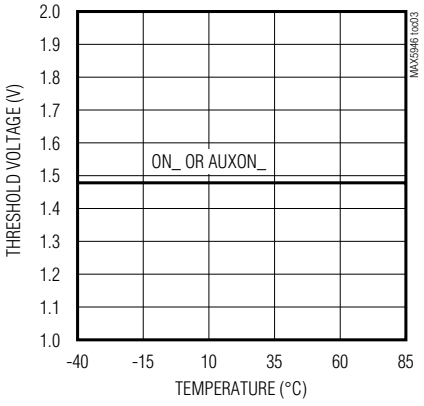
12VIN INPUT SUPPLY CURRENT vs. TEMPERATURE



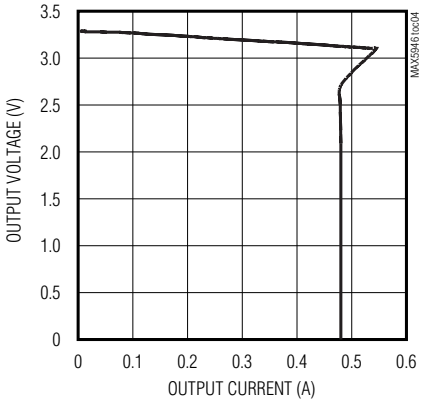
3.3VAUXIN SUPPLY CURRENT vs. TEMPERATURE



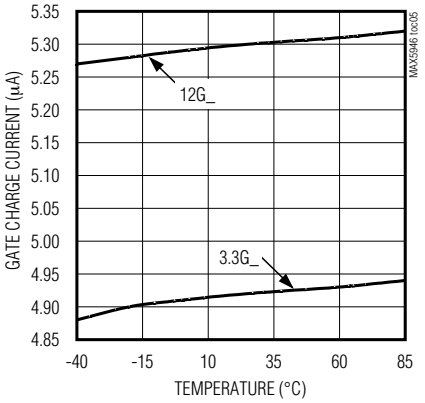
ON AND AUXON LOW-TO-HIGH THRESHOLD VOLTAGE vs. TEMPERATURE



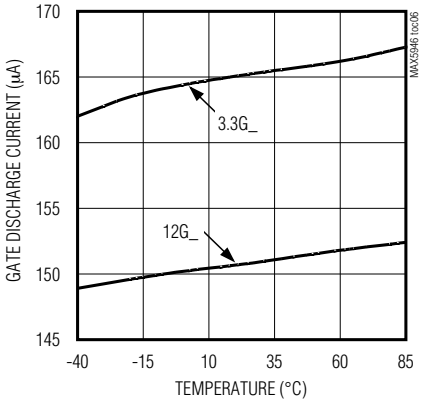
3.3VAUXO_ OUTPUT VOLTAGE vs. CURRENT



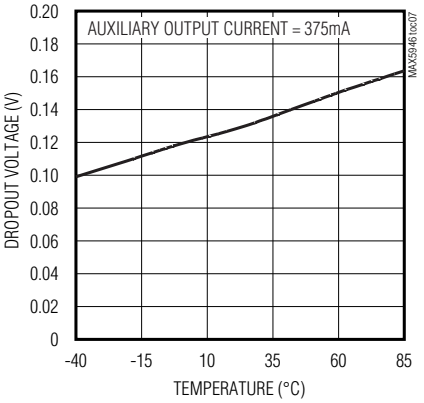
12G_ AND 3.3G_ GATE CHARGE CURRENT vs. TEMPERATURE



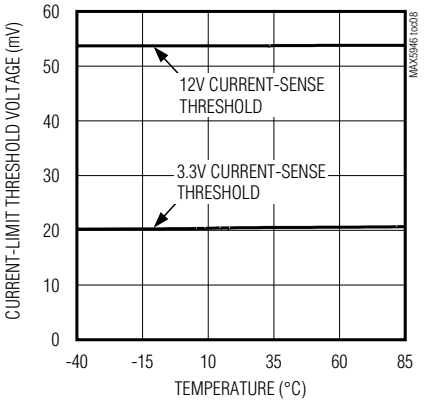
12G_ AND 3.3G_ GATE DISCHARGE CURRENT vs. TEMPERATURE



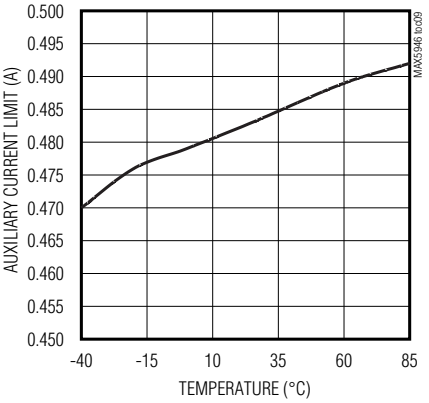
3.3VAUX INTERNAL SWITCH MAXIMUM DROPOUT vs. TEMPERATURE



12V AND 3.3V CURRENT-LIMIT THRESHOLD VOLTAGE vs. TEMPERATURE



AUXILIARY CURRENT LIMIT vs. TEMPERATURE

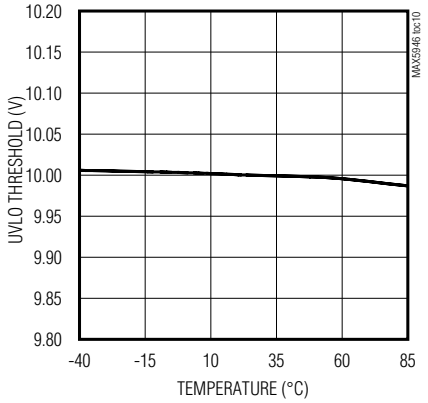


Dual PCI Express, Hot-Plug Controller

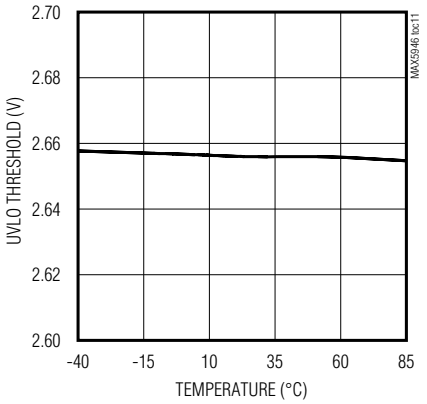
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

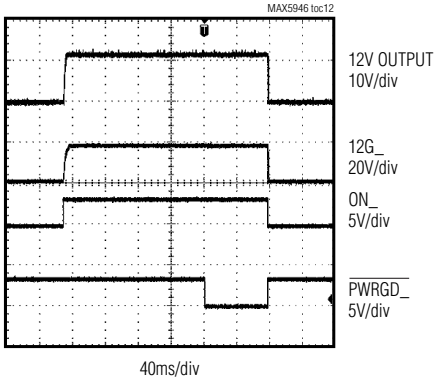
12VIN UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



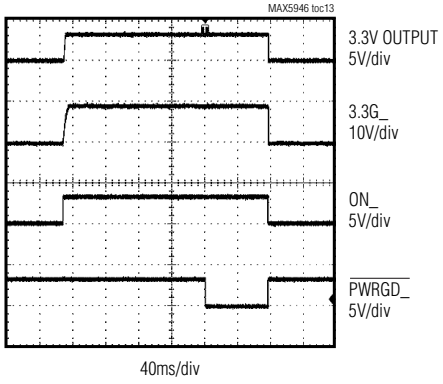
3.3VAUXIN UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



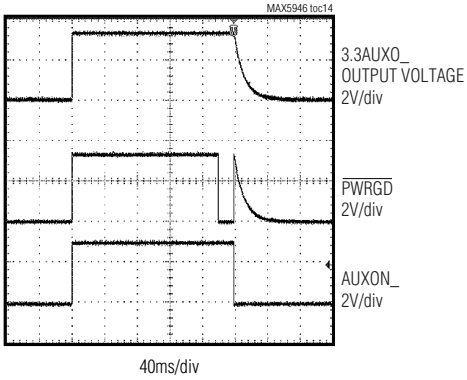
12V TURN-ON/OFF TIME



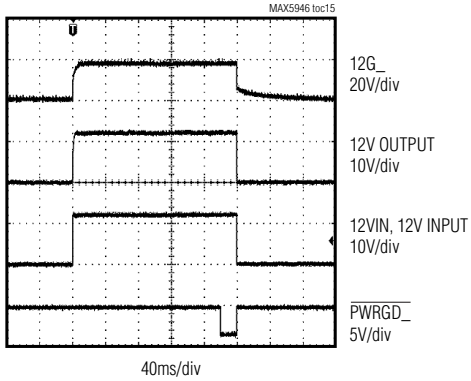
3.3V TURN-ON/OFF TIME



3.3V AUXILIARY TURN-ON/OFF TIME



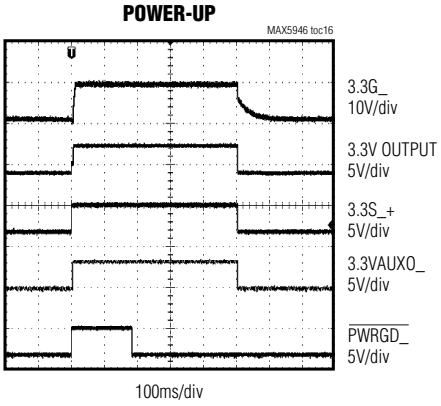
12V POWER-UP



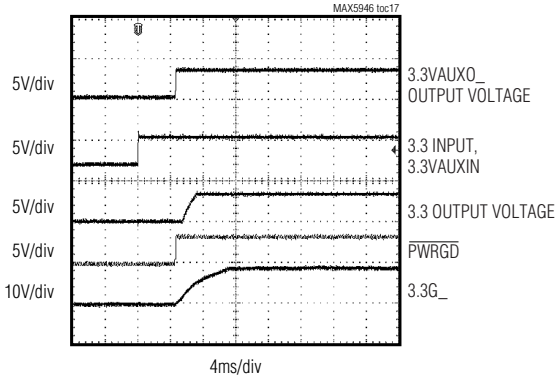
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

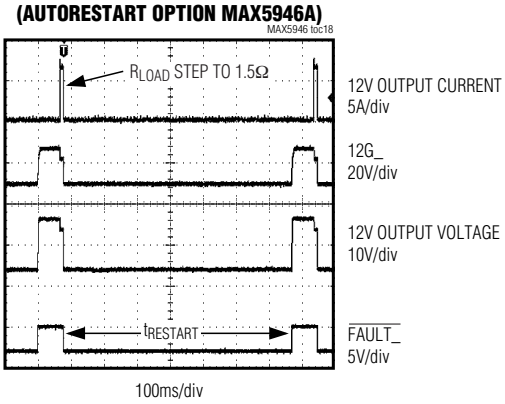
3.3V INPUT/3.3V AUXILIARY INPUT POWER-UP



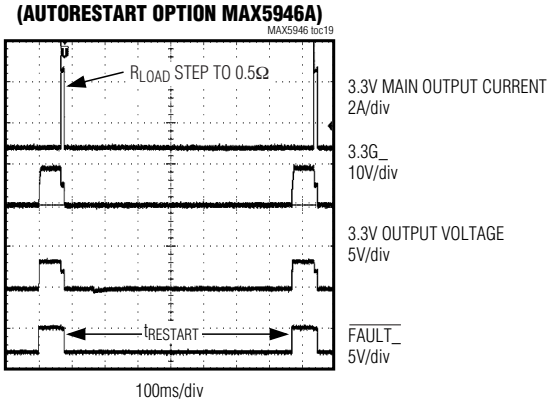
TURN-ON DELAY 3.3V OUTPUT AND 3.3V AUXILIARY OUTPUT



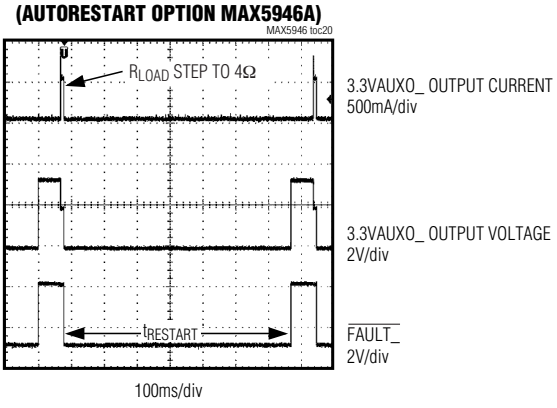
FAULT CONDITION ON 12V OUTPUT (AUTORESTART OPTION MAX5946A)



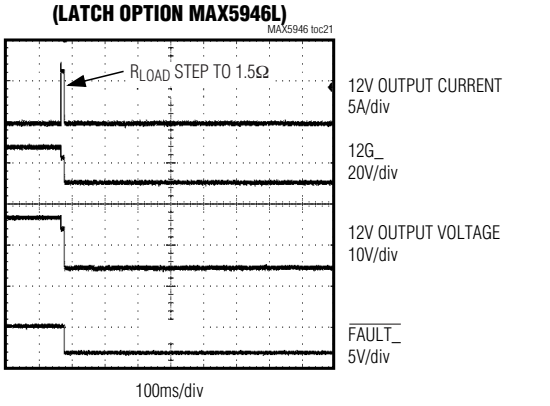
FAULT CONDITION ON 3.3V OUTPUT (AUTORESTART OPTION MAX5946A)



FAULT CONDITION ON AUXILIARY OUTPUT (AUTORESTART OPTION MAX5946A)



FAULT CONDITION ON 12V OUTPUT (LATCH OPTION MAX5946L)

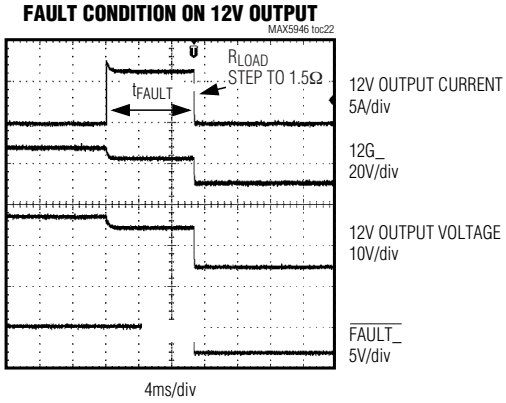


Dual PCI Express, Hot-Plug Controller

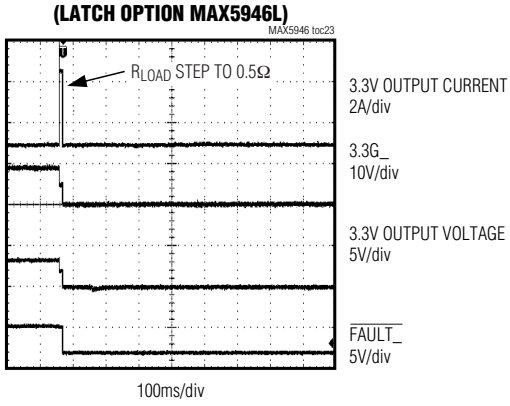
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

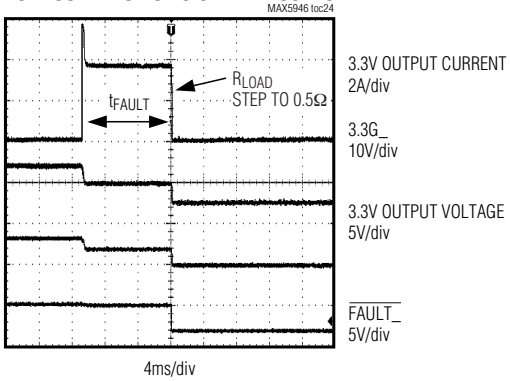
FAULT CONDITION ON 12V OUTPUT



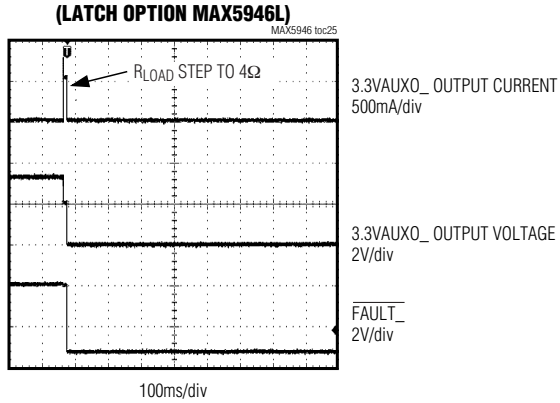
FAULT CONDITION ON 3.3V OUTPUT (LATCH OPTION MAX5946L)



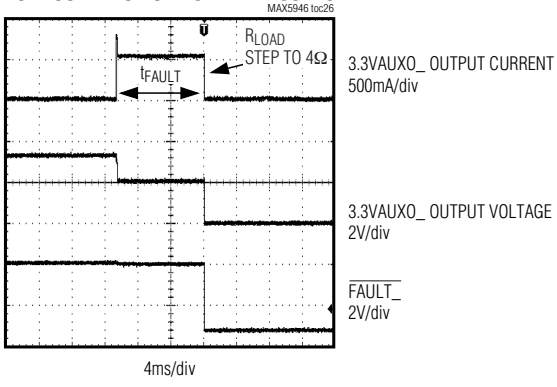
FAULT CONDITION ON 3.3V MAIN OUTPUT



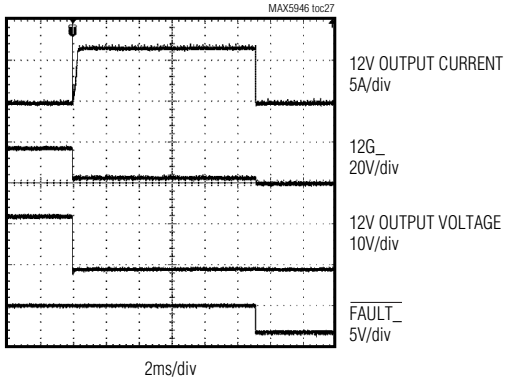
FAULT CONDITION ON AUXILIARY OUTPUT (LATCH OPTION MAX5946L)



FAULT CONDITION ON AUXILIARY OUTPUT



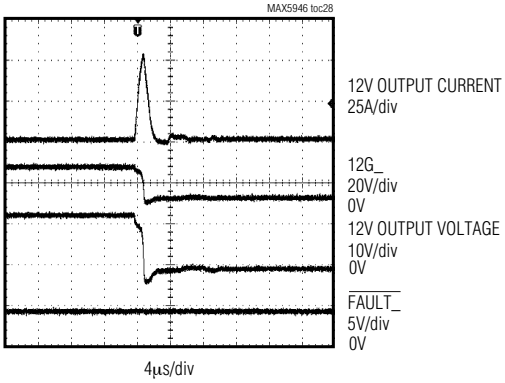
SHORT CIRCUIT ON 12V OUTPUT



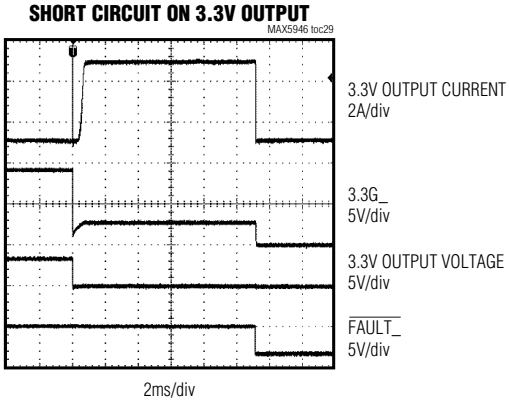
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

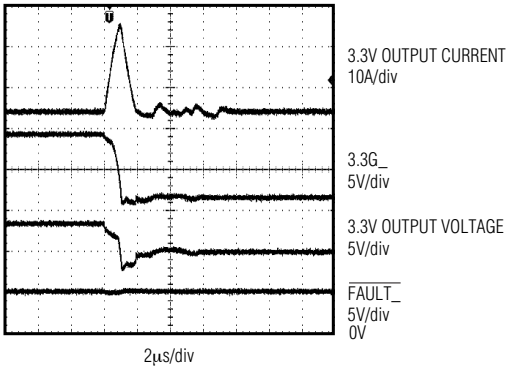
SHORT CIRCUIT ON 12V OUTPUT



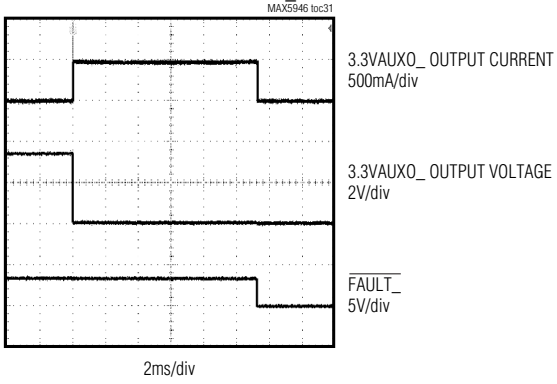
SHORT CIRCUIT ON 3.3V OUTPUT



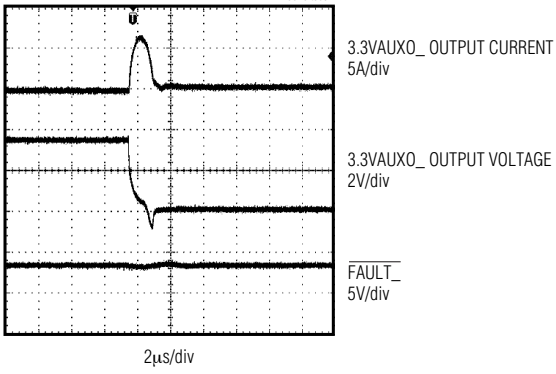
SHORT CIRCUIT ON 3.3V OUTPUT



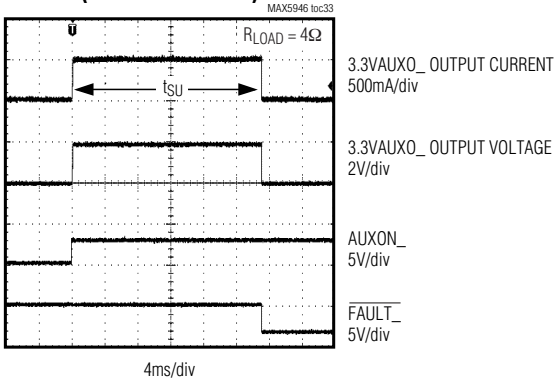
SHORT CIRCUIT ON 3.3AUXO_



SHORT CIRCUIT ON 3.3VAUXO_



POWER-UP INTO FAULT (AUXILIARY SUPPLY)

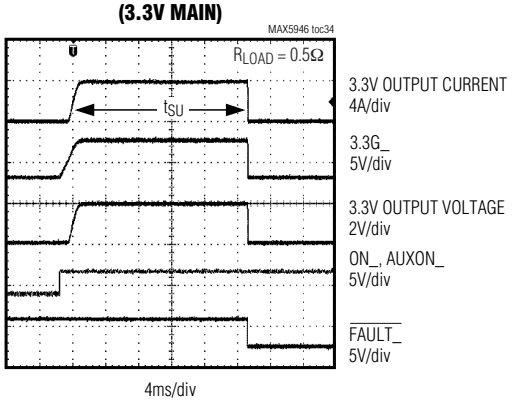


Dual PCI Express, Hot-Plug Controller

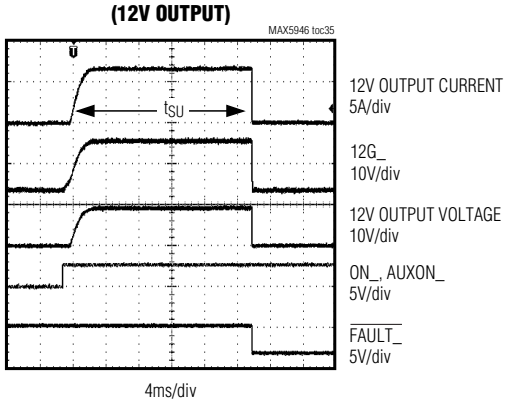
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

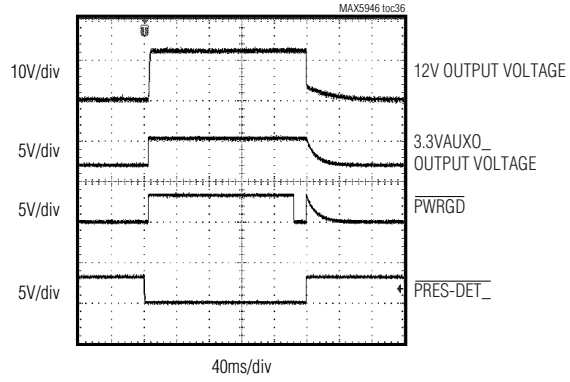
POWER-UP INTO FAULT (3.3V MAIN)



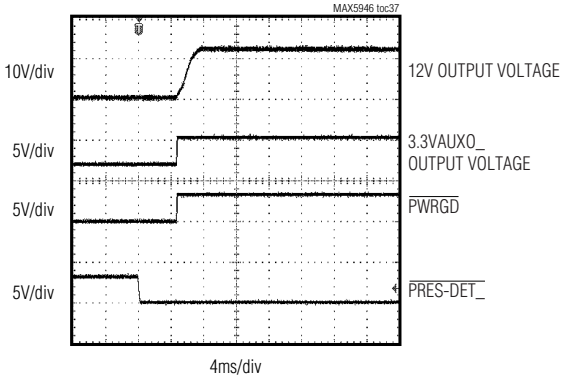
POWER-UP INTO FAULT (12V OUTPUT)



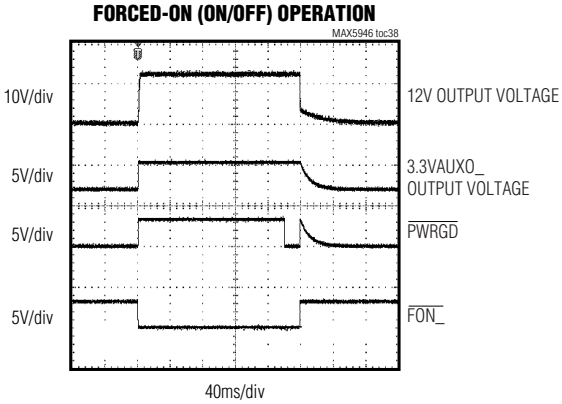
PRESENT-DETECT (ON/OFF) OPERATION



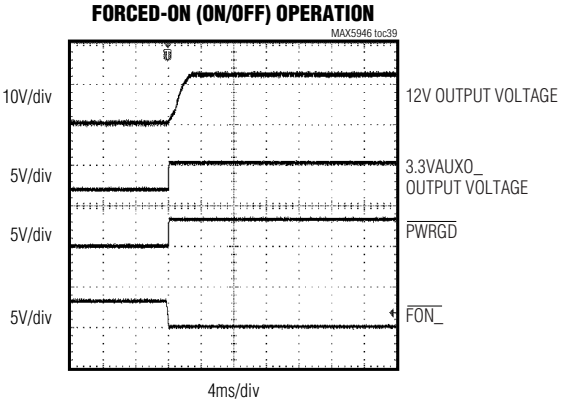
PRESENT-DETECT (ON/OFF) OPERATION



FORCED-ON (ON/OFF) OPERATION



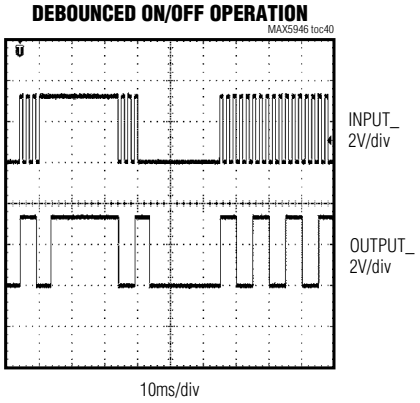
FORCED-ON (ON/OFF) OPERATION



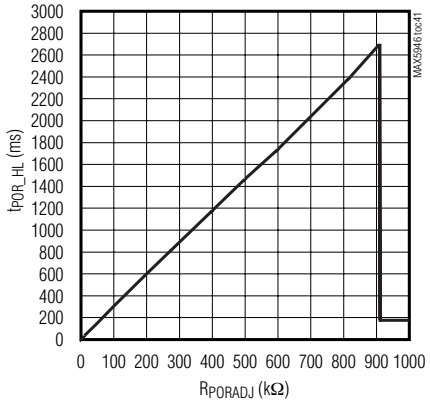
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12SA+} = 12V, $V_{3.3VAUXIN}$ = $V_{3.3S\_+}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{INPUT\_}$ = 3.3V, $\overline{PRES\text{-}DET\_}$ = GND, FON_ = PORADJ = TIM = float, $\overline{FAULT\_}$ = 10kΩ to 3.3VAUXIN, $\overline{PWRGDA}$ = 10kΩ to 3.3VAUXO_, T_A = +25°C, unless otherwise noted, see the *Typical Application Circuit*.)

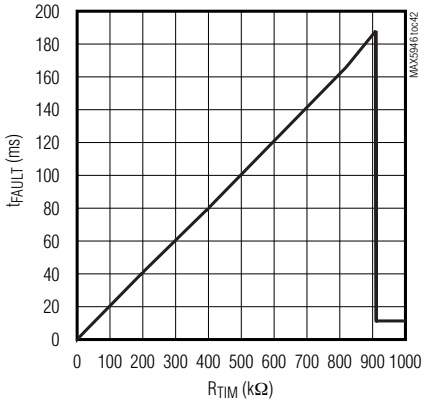
DEBOUNCED ON/OFF OPERATION



POWER-ON-RESET TIME vs. PORADJ RESISTOR



t_{FAULT} TIME DELAY vs. TIM RESISTOR



Dual PCI Express, Hot-Plug Controller

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{PRES-DETA}}$	Present-Detect Input A. $\overline{\text{PRES-DETA}}$ accepts inputs from the PRSNT#2 pin on a PCI express connector. $\overline{\text{PRES-DETA}}$ has an internal pullup to 3.3VAUXIN. When $\overline{\text{PRES-DETA}}$ is low, the outputs follow the command from ONA and AUXONA after a 4ms debounced time. When $\overline{\text{PRES-DETA}}$ goes from low to high, all outputs of the respective slot shut down with no delay (see Table 2).
2	$\overline{\text{FONA}}$	Forced-On Input A. $\overline{\text{FONA}}$ has a 50kΩ internal pullup to 3.3VAUXIN. A logic-low on $\overline{\text{FONA}}$ turns on all slot A outputs as long as the power inputs are within their operating range, regardless of the status of the other input signals. Leave $\overline{\text{FONA}}$ open for normal operation (see Table 2).
3	ONA	Slot A 12V And 3.3V Outputs Enable. A logic-high at ONA turns on the 12V and 3.3V outputs of slot A (see Table 2).
4	AUXONA	Slot A 3.3V Auxiliary Output Enable. A logic-high at AUXONA turns on the slot A auxiliary output (3.3VAUXOA), see Table 2.
5	12SA+	Slot A 12V Positive Current-Sense Input. Connect the positive terminal of the current-sense resistor to 12SA+ using the Kelvin-sensing technique to assure accurate current sensing.
6	12SA-	Slot A 12V Negative Current-Sense Input. Connect 12SA- to the negative side of the current-sense resistor using the Kelvin-sensing technique to assure accurate current sensing.
7	12GA	Slot A 12V Gate-Drive Output. Connect 12GA to the gate of slot A's 12V MOSFET. At power-up, V_{12GA} is raised to the internal charge-pump voltage level by a constant current.
8	3.3SA+	Slot A 3.3V Positive Current-Sense Input. Connect the positive side of the current-sense resistor to 3.3SA+ using the Kelvin-sensing technique to assure accurate current sensing. This input is also used for the 3.3V supply's UVLO function.
9	3.3SA-	Slot A 3.3V Negative Current-Sense Input. Connect to the negative side of the sense resistor using the Kelvin-sensing technique to assure accurate current sensing.
10	3.3GA	Slot A 3.3V Gate-Drive Output. Connect 3.3GA to the gate of slot A's 3.3V MOSFET. At power-up, $V_{3.3GA}$ is charged to 5.5V above the 3.3V supply by a constant current derived from V_{12VIN}.
11	$\overline{\text{FAULTA}}$	Open-Drain Fault Output Signal. $\overline{\text{FAULTA}}$ latches active low whenever the slot A outputs are shut down due to a fault. A fault is either of: • An overcurrent condition lasting longer than the overcurrent timeout. • A device over temperature condition. If the fault is detected in the main outputs, $\overline{\text{FAULTA}}$ must be reset by toggling the ONA input. If the fault is in the auxiliary output, $\overline{\text{FAULTA}}$ must be reset by toggling both ONA and AUXONA. For the auto-restart version, $\overline{\text{FAULTA}}$ is reset when the part initiates the next power-on cycle.
12	$\overline{\text{PWRGDA}}$	Open-Drain Power-Good Output. $\overline{\text{PWRGDA}}$ goes low t_{POR_HL} after all outputs of slot A reach their final value and the power MOSFETs are fully enhanced.
13	3.3VAUXOA	Slot A 3.3V Auxiliary Power-Supply Output
14	3.3VAUXIN	3.3V Auxiliary Supply Input. 3.3VAUXIN is the input to a charge pump that drives the internal MOSFETs connecting 3.3VAUXIN to 3.3VAUXOA and 3.3VAUXOB. $V_{3.3VAUXIN}$ is also used to power the internal control logic and analog references of the MAX5946.
15	3.3VAUXOB	Slot B 3.3V Auxiliary Power Output
16	$\overline{\text{PWRGDB}}$	Slot B Power-Good Output. See $\overline{\text{PWRGDA}}$ function.
17	$\overline{\text{FAULTB}}$	Slot B Open-Drain Fault Output. See $\overline{\text{FAULTA}}$ function.
18	3.3GB	Slot B 3.3V Gate-Drive Output. See 3.3GA function.

Pin Description (continued)

PIN	NAME	FUNCTION
19	3.3SB-	Slot B 3.3V Negative Current-Sense Input. See 3.3SA- function.
20	3.3SB+	Slot B 3.3V Positive Current-Sense Input. Connect the positive side of the current-sense resistor to 3.3SB+ using the Kelvin-sensing technique to assure accurate current sensing.
21	12GB	Slot B 12V Gate-Drive Output. See 12GA function.
22	12SB-	Slot B 12V Negative Current-Sense Input. See 12SA- function.
23	12SB+	Slot B 12V Positive Current-Sense Input. See 12SA+ function.
24	AUXONB	Slot B 3.3V Auxiliary Output Enable. See AUXONA function.
25	ONB	Slot B 12V And 3.3V Outputs Enable. See ONA function.
26	$\overline{FONB}$	Slot B Forced-On Input. See $\overline{FONA}$ function.
27	$\overline{PRES\text{-}DETB}$	Slot B Present-Detect Input. See $\overline{PRES\text{-}DETA}$ function.
28	TIM	Overcurrent Timeout Programming Input. Connect a resistor between 500Ω and 500kΩ from TIM to GND to program t_{FAULT}. Leave TIM floating for a default timeout of 11ms.
29	INPUT2	Digital Logic Gate Input
30	OUTPUT2	Digital Output. 4ms debounced digital output of INPUT2.
31	OUTPUT1	Digital Output. 4ms debounced digital output of INPUT1.
32	INPUT1	Digital Logic Gate Input
33	12VIN	12V Supply Input. V_{12VIN} drives the gates of the MOSFETs connected to 3.3GA and 3.3GB. 12VIN powers an internal charge pump that drives the gates of the MOSFETs connected to 12GA and 12GB.
34	GND	Ground
35	PGND	Power Ground. Connect externally to GND.
36	PORADJ	Power-On-Reset Programming Input. Connect a resistor between 500Ω and 500kΩ from PORADJ to GND to program the POR timing. Leave floating for a default value of 160ms.

Detailed Description

The MAX5946 dual hot-plug controller is designed for PCI express applications. The device provides hot-plug control for 12V, 3.3V, and 3.3V auxiliary supplies of two PCI express slots. The MAX5946's logic inputs/outputs allow interfacing directly with the system hot-plug-management controller or through an SMBus with an external I/O expander. An integrated debounced attention switch and present-detect signals are included to simplify system design.

The MAX5946 drives four external n-channel MOSFETs to control the 12V and 3.3V main outputs. The 3.3V auxiliary outputs are controlled through internal 0.24Ω n-channel MOSFETs. Internal charge pumps provide a gate drive for the 12V outputs while the gate drive of the 3.3V output is driven by the 12V input supply. The 3.3V auxiliary outputs are completely independent from the main outputs with their own charge pumps.

At power-up, the MAX5946 keeps all of the external MOSFETs off until all supplies rise above their respective UVLO thresholds. The device keeps the internal MOSFETs off only until the 3.3VAUXIN supply rises above its UVLO threshold. Upon a turn-on command, the MAX5946 enhances the external and internal MOSFETs slowly with a constant gate current to limit the power-supply inrush current. The MAX5946 actively limits the current of all outputs at all times and shuts down if an overcurrent condition persists for longer than a programmable overcurrent timeout. Thermal-protection circuitry also shuts down all outputs if the die temperature exceeds +150°C. After an overcurrent or overtemperature fault condition, the MAX5946L latches off while the MAX5946A automatically restarts after a restart time delay.

The power requirement for PCI express connectors is defined by the PCI express card specification and summarized in Table 1.

Dual PCI Express, Hot-Plug Controller

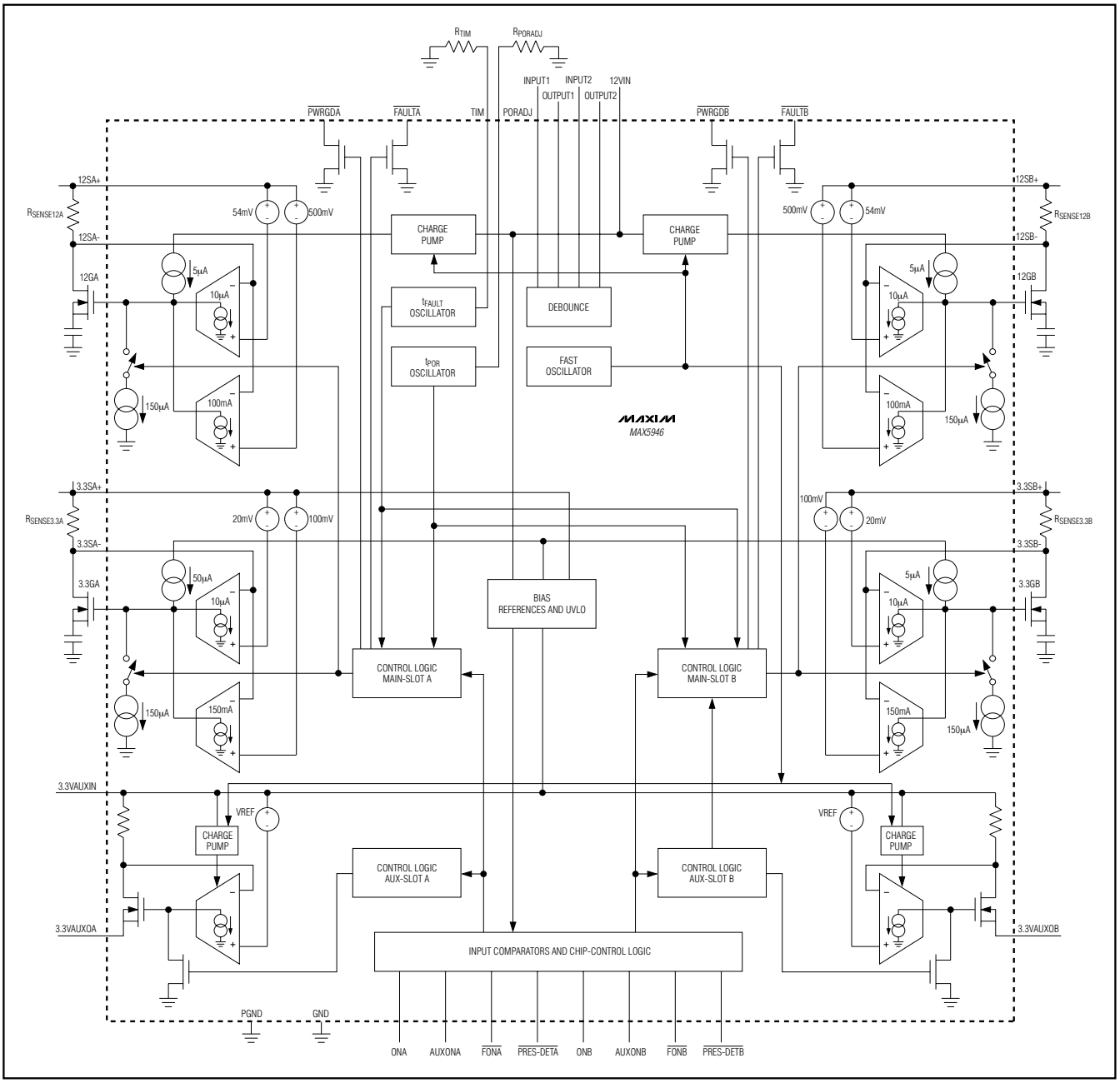


Figure 1. Functional Diagram

Table 1. Power Requirements for PCI Express Connectors

POWER RAIL	X1 CONNECTOR	X4/8 CONNECTOR	X16 CONNECTOR
3.3V			
Voltage Tolerance	±9% (max)	±9% (max)	±9% (max)
Supply Current	3.0A (max)	3.0A (max)	3.0A (max)
Capacitive Load	1000µF (max)	1000µF (max)	1000µF (max)
12V			
Voltage Tolerance	±8% (max)	±8% (max)	±8% (max)
Supply Current	0.5A (max)	2.1A (max)	5.5A (max)
Capacitive Load	300µF (max)	1000µF (max)	2000µF (max)
3.3V AUXILIARY			
Voltage Tolerance			
Supply Current	±9% (max)	±9% (max)	±9% (max)
Wake Enabled	375mA (max)	375mA (max)	375mA (max)
375mA (max)	20mA (max)	20mA (max)	20mA (max)
Non-Wake Enabled, Capacitive Load	150µF (max)	150µF (max)	150µF (max)

Table 2. Control Logic Truth Table

ON_	AUXON_	$\overline{FON\_}$	$\overline{PRES\text{-}DET\_}$	12V_ AND 3.3V_ OUTPUTS	3.3VAUXO_ AUXILIARY OUTPUTS
X	X	Low	X	On	On
X	X	High	High	Off	Off
Low	Low	High	Low*	Off	Off
High	Low	High	Low*	On	Off
Low	High	High	Low*	Off	On
High	High	High	Low*	On	On

*$\overline{PRES\text{-}DET\_}$ high-to-low transition has a 4ms delay (t_{DEG}).

Startup

The main supply outputs can become active only after all the following events have occurred:

- $V_{3.3VAUXIN}$ is above its UVLO threshold
- V_{12VIN} and $V_{3.3SA+}$ are both above their UVLO threshold
- ON_ is driven high
- $\overline{PRES\text{-}DET\_}$ is low for more than 4ms

The auxiliary supply output is made available only after the following events have occurred:

- $V_{3.3VAUXIN}$ is above its UVLO threshold
- AUXON_ is driven high
- $\overline{PRES\text{-}DET\_}$ is low for more than 4ms

The $\overline{FON\_}$ input overrides all other control signals and turns on the respective slot when driven low, as long as the UVLO thresholds have been reached. Table 2 summarizes the logic conditions required for startup.

The auxiliary supply input powers the internal control logic and analog references of the MAX5946, so the main supplies cannot be enabled if $V_{3.3VAUXIN}$ is not present.

When an output is enabled, a programmable startup timer (t_{SU}) begins to count the startup time duration. The value of t_{SU} is set to 2x the fault timeout period (t_{FAULT}). R_{TIM} externally connected from TIM to GND sets the duration of t_{FAULT}.

Dual PCI Express, Hot-Plug Controller

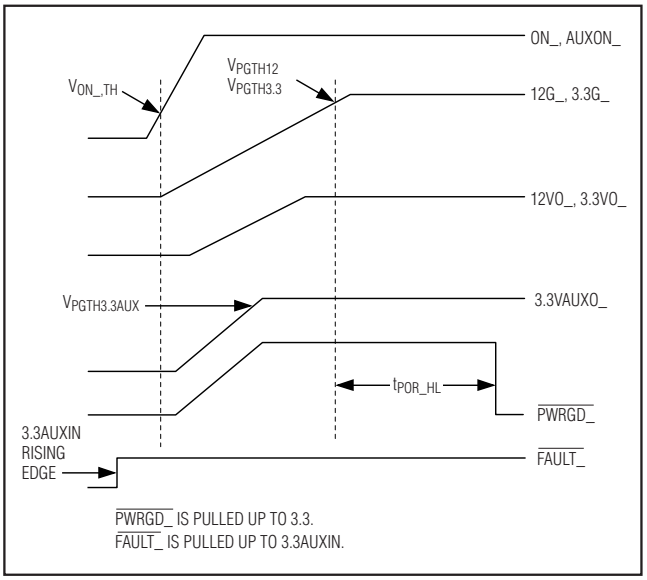


Figure 2. Power-Up Timing, No Fault

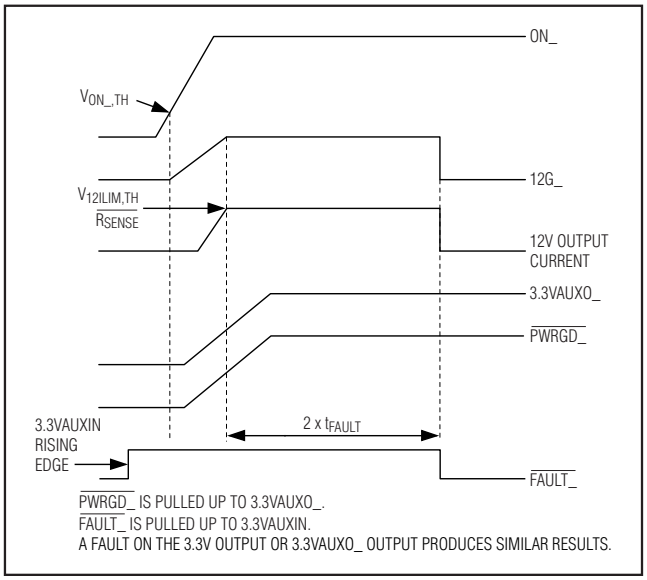


Figure 3. 12V Power-Up Timing (Turn-On into Output Overcurrent/Short Circuit)

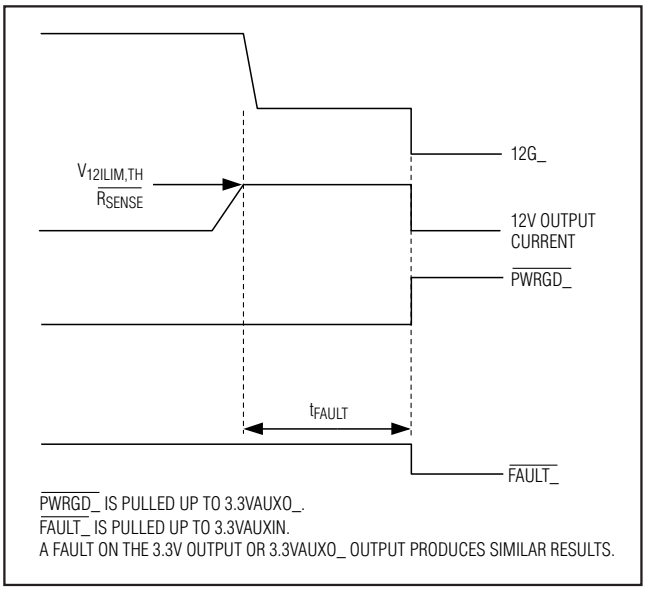


Figure 4. 12 Output Overcurrent/Short Circuit During Normal Operation

12V and 3.3V Outputs Normal Operation

The MAX5946 monitors and actively limits the current of the 12V and 3.3V outputs after the startup period. Each output has its own overcurrent threshold. If any of the monitored output currents rise above the overcurrent threshold for a period t_{FAULT}, $\overline{FAULT\_}$ asserts and the controller disengages both the 12V and 3.3V outputs for the particular slot (see the *Fault Management* section).

3.3V Auxiliary Output Normal Operation

The auxiliary output current is internally monitored and actively limited to the maximum current-limit value. An overcurrent fault condition occurs when the output current exceeds the overcurrent threshold for longer then $t_{\overline{FAULT}}$. A fault on an auxiliary channel causes all supplies of the affected channel to be disabled after a programmable time period t_{FAULT} (see the *Fault Management* section).

Power-Good ($\overline{PWRGD\_}$)

Power-good ($\overline{PWRGD\_}$) is an open-drain output that pulls low a time (t_{POR_HL}) after all of the outputs of the respective slot are fully on. All outputs are considered fully on when 3.3G_ has risen to $V_{PGTH3.3}$, 12G_ has risen to V_{PGTH12}, and $V_{3.3AUXO\_}$ is less then $V_{PGTH3.3AUX}$. t_{POR_HL} is adjustable from 2.5ms to 1.5s by connecting a resistor from PORADJ to GND. See the *Setting the Power-On-Reset Timeout Period (t_{POR})* section.

Thermal Shutdown

When the die temperature goes above (T_{SD}) +150°C, an overtemperature fault occurs and the MAX5946 shuts down all outputs. The device waits for the junction temperature to decrease below T_{SD} - Hysteresis before entering fault management (see the *Fault Management* section).

FAULT Management

A fault occurs when an overcurrent lasts longer then $t_{\overline{FAULT}}$ or when the device experiences an overtemperature condition.

- A fault on a main output (12V or 3.3V) shuts down both main outputs of the respective slot. The 3.3V auxiliary is not affected.
- A fault on the 3.3V auxiliary output shuts down all three outputs of the respective slot.

The MAX5946A automatically restarts from a fault shutdown after the $t_{RESTART}$ period, while the MAX5946L latches off. If an overcurrent fault occurred on a main output, bring ON_ low for at least t_{RESET} (100µs) and high again to reset the fault and restart the outputs. If the overcurrent fault occurred on an auxiliary output or an overtemperature fault occurred, bring both ON_ and AUXON_ low for a minimum of t_{RESET} to reset the fault. Bring ON_ and/or AUXON_ high again to restart the respective outputs. As an extra protection, the MAX5946L waits a minimum of $t_{RESTART}$ before it can be restarted.

Debounced Logic Gate (Input_ and Output_)

INPUT1 and INPUT2 accept inputs from mechanical switches. The corresponding outputs are OUTPUT1 and OUTPUT2. OUTPUT_ is debounced for 4ms. When INPUT_ goes from high to low, OUTPUT_ goes low right away and stays low for at least 4ms. After the debounce time OUTPUT_ follows INPUT_. If INPUT_ goes from low to high, OUTPUT_ goes high right away and stays high for at least 4ms. After the debounce time, OUTPUT_ follows INPUT_. Figure 5 shows the timing diagram describing the INPUT_/OUTPUT_ debounced feature.

Present-Detect and Forced-On Inputs ($\overline{PRES\text{-}DET\_}$, $\overline{FON\_}$)

$\overline{PRES\text{-}DETA}$ and $\overline{PRES\text{-}DETB}$ inputs detect the PRSNT#2 pin on a PCI express connector. When the card is plugged in, $\overline{PRES\text{-}DET\_}$ goes low and allows the turn-on of the outputs of the respective slot after a 4ms debounced time. When the card is removed, an internal 50kΩ pullup forces $\overline{PRES\text{-}DET\_}$ high and the respective slot is shut down with no delay. $\overline{PRES\text{-}DET\_}$ works in conjunction with ON_ and VAUXON_ and only enables the device when ON_ and VAUXON_ are high.

A logic-low on $\overline{FON\_}$ forces the respective slot (main supplies and auxiliary) to turn on regardless of the status of the other logic inputs provided the UVLO thresholds are exceeded on all of the inputs.

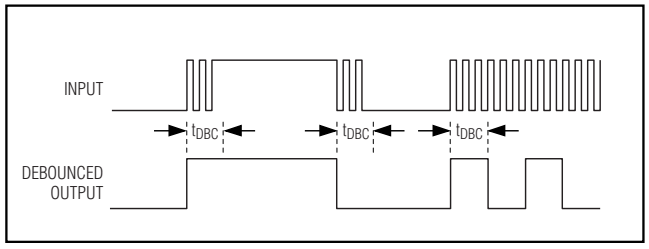


Figure 5. INPUT_ and OUTPUT_ Debounced Feature

Active Current Limits

Active current limits are provided for all three outputs of slot A and slot B. Connect a current-sense resistor between 12S_+ and 12S_- to set the current limit for the 12V outputs. The current limit is set to 54mV/$R_{SENSE12}$. $R_{SENSE12}$ is either R1 or R3 in the *Typical Application Circuit*. Connect a current-sense resistor between 3.3S_+ and 3.3S_- to set the current limit for the 3.3V main outputs to 20mV/$R_{SENSE3.3}$. $R_{SENSE3.3}$ is either R2 or R4 in the *Typical Application Circuit*. For the auxiliary output ($3.3V_{AUXO\_}$) the current limit is fixed at 470mA.

When the voltage across $R_{SENSE12}$ or $R_{SENSE3.3}$ reaches the current-limit threshold voltage, the MAX5946 regulates the gate voltage to maintain the current-limit threshold voltage across the sense resistor. If the current limit lasts for t_{FAULT} then an overcurrent fault occurs. The MAX5946_ shuts down both the 12V and 3.3V outputs and asserts the $\overline{FAULT\_}$ output of the respective slot.

When the auxiliary output reaches the current limit (470mA) for longer then t_{FAULT}, a fault occurs and the device shuts down all outputs and asserts $\overline{FAULT}$ of the respective slot.

Undervoltage Lockout Threshold

The UVLO thresholds prevent the internal auxiliary MOSFETs and the external main channel MOSFETs (Q1–Q4 in the *Typical Application Circuit*) from turning on if V_{12VIN}, $V_{3.3VIN}$, and $V_{3.3VAUXIN}$ are not present. Internal comparators monitor the main supplies and the auxiliary supply and keep the gate-drive outputs (12GA, 12GB, 3.3GA, and 3.3GB) low until the supplies rise above their UVLO threshold. The 12V main supply is monitored at 12VIN and has a UVLO threshold of 10V. The 3.3V main supply is monitored at 3.3SA+ and has a UVLO threshold of 2.65V. The auxiliary supply is monitored at 3.3VAUXIN and has a 2.65V UVLO threshold. For either main channel to operate, $V_{3.3VAUXIN}$ must be above its UVLO threshold.

Dual PCI Express, Hot-Plug Controller

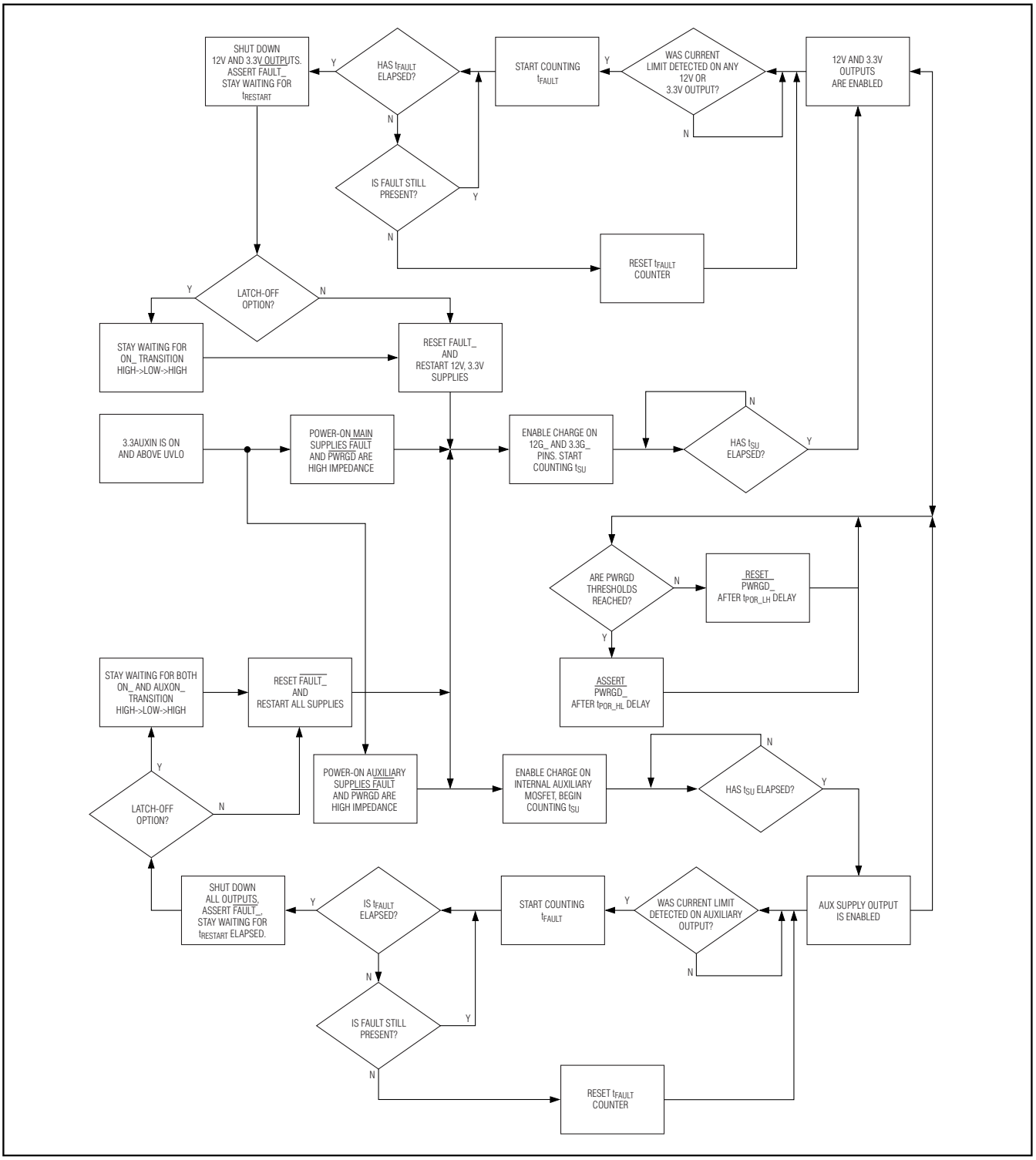


Figure 6. Fault Management Flow Chart

External MOSFET Gate Drivers (12GA, 12GB, 3.3GA, and 3.3GB)

The gate drive for the external MOSFETs is provided at 12GA, 12GB, 3.3GA, and 3.3GB. 12G_ is the gate drive for the 12V main supply and is boosted to 5.3V above V_{12VIN} by an internal charge pump. During turn-on, 12G_ sources 5µA into the external gate capacitance to control the turn-on time of the external MOSFET. During turn-off, 12G_ sinks 150µA from the external gate capacitance to quickly turn off the external MOSFET. During short-circuit events, an internal 100mA current activates to rapidly bring the load current into the regulation limits.

3.3G_ is the gate drive for the 3.3V main supply's MOSFET and is driven to 5.5V above the 3.3V main supply. The power for 3.3G_ is supplied from 12VIN and has no internal charge pump. During turn-on, 3.3G_ sources 5µA into the external gate capacitance to control the turn-on time of the external MOSFET. During turn-off, 3.3G_ sinks 150µA to quickly turn off the external MOSFET. During short-circuit events, an internal 150mA current activates to rapidly turn off the appropriate external MOSFET.

Auxiliary Supply (3.3VAUXIN)

3.3VAUXIN provides power to the auxiliary outputs as well as the internal logic and references. The drains of the internal auxiliary MOSFETs connect to 3.3VAUXIN through internal sense resistors and the sources connect to the auxiliary outputs (3.3VAUXOA and 3.3VAUXOB). Both MOSFETs have typical on-resistance of 0.3Ω. An internal charge pump boosts the gate-drive voltage to fully turn on the internal n-channel MOSFETs. The auxiliary supplies have an internal current limit set to 470mA.

Applications Information

Setting the Fault Timeout Period (t_{FAULT})

t_{FAULT} is the time an overcurrent or overtemperature fault must remain for the MAX5946 to disable the main or auxiliary channels of a particular slot. Program the fault timeout period (t_{FAULT}) by connecting a resistor (R_{TIM}) from TIM to GND. t_{FAULT} can be calculated by the following equation:

$$t_{FAULT} = 166ns / \Omega \times R_{TIM}$$

The t_{FAULT} programmed time duration must be chosen according to the total capacitance load connected to the 12G_ and 3.3G_ pins. To properly power-up the main supply outputs, the following constraints need to be taken:

$$t_{SU} \geq \frac{V_{GATE} \times C_{LOAD}}{I_{CHG}}$$

where $t_{SU} = 2 \times t_{FAULT}$ and where

1) $I_{CHG} = 5\mu A$.
2) V_{GATE} = 18.4V for 12G_ and V_{GATE} = 9.4V for 3.3G_.
3) C_{LOAD} is the total capacitance load at the gate.

Maximum and minimum values for R_{TIM} are 500Ω and 500kΩ, respectively. Leave TIM floating for a default t_{FAULT} of 11ms.

Setting the Power-On-Reset Timeout Period (t_{POR_HL})

t_{POR_HL} is the time from when the gate voltages of all outputs of a slot reach their power-good threshold to when $\overline{PWRGD\_}$ pulls low. Program the power-on-reset timeout period (t_{POR}) by connecting a resistor (R_{PORADJ}) from PORADJ to GND. t_{POR_HL} can be calculated by the following equation:

$$t_{POR\_HL} = 2.5\mu s / \Omega \times R_{PORADJ}$$

Maximum and minimum values for R_{PORADJ} are 500Ω and 500kΩ, respectively. Leave PORADJ floating for a default t_{POR} of 160ms.

Component Selection

Select the external n-channel MOSFET according to the applications current requirement. Limit the switch power dissipation by choosing a MOSFET with an R_{DS_ON} low enough to have a minimum voltage drop at full load. High R_{DS_ON} causes larger output ripple if there are pulsed loads. High R_{DS_ON} can also trigger an external undervoltage fault at full load. Determine the MOSFETs power rating requirement to accommodate a short-circuit condition on the board during start-up. Table 3 lists MOSFETs and sense resistor manufacturers.

Additional External Gate

External capacitance can be added from the gate of the external MOSFETs to GND to slow down the dV/dt of the 12V and 3.3V outputs.

Maximum Load Capacitance

Large capacitive loads at the 12V output, the 3.3V output, and the 3.3V auxiliary output can cause a problem when inserting discharged PCI cards into live backplanes. A fault occurs if the time needed to charge the capacitance of the board is greater than the typical startup time (2 x t_{FAULT}). The MAX5946 can withstand

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Table 3. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistor	Vishay-Dale	402-564-3131	www.vishay.com
	IRC	704-264-8861	www.irctt.com
MOSFETs	Fairchild	888-522-5372	www.fairchildsemi.com
	International Rectifier	310-322-3331	www.irf.com
	Motorola	602-244-3576	www.mot-sps.com/ppd/
	Vishay-Siliconix	—	www.vishay.com

large capacitive loads due to their adjustable startup times and adjustable current-limit thresholds. Calculate the maximum load capacitance as follows:

$$C_{LOAD} < \frac{t_{SU} \times I_{LIM}}{V_{OUT}}$$

V_{OUT} is either the 3.3V output, the 12V output, or the 3.3V auxiliary output for slot A or slot B.

Input Transients

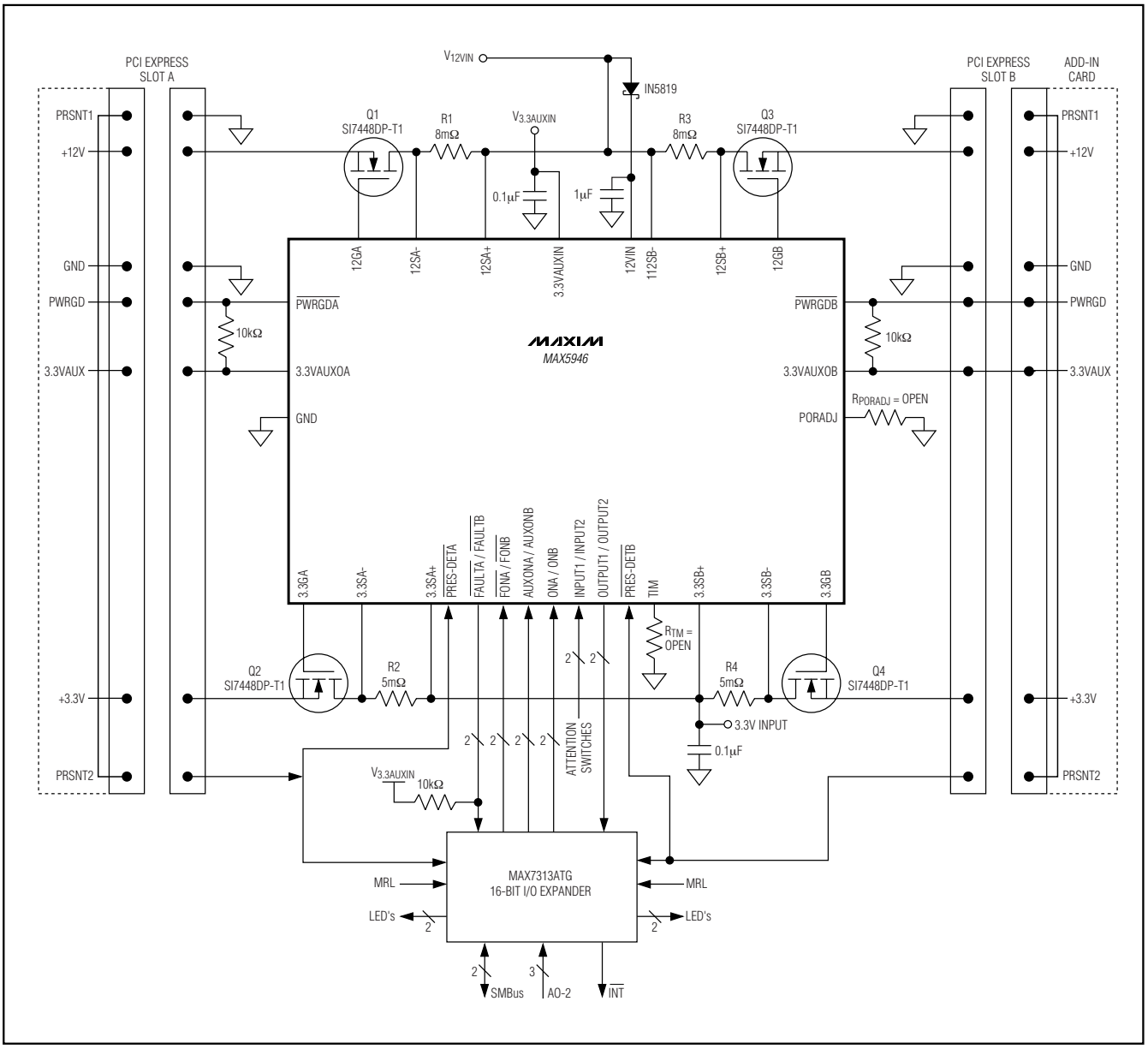
The 12V input (12VIN), the 3.3V input (3.3SA+), and the 3.3V auxiliary (3.3VAUXIN) must be above their UVLO thresholds before startup can occur. Input transients can cause the input voltage to sag below the UVLO threshold. The MAX5496 rejects transients on the input supplies that are shorter than 4µs typical.

Chip Information

TRANSISTOR COUNT: 10,487

PROCESS: BiCMOS

Typical Application Circuit



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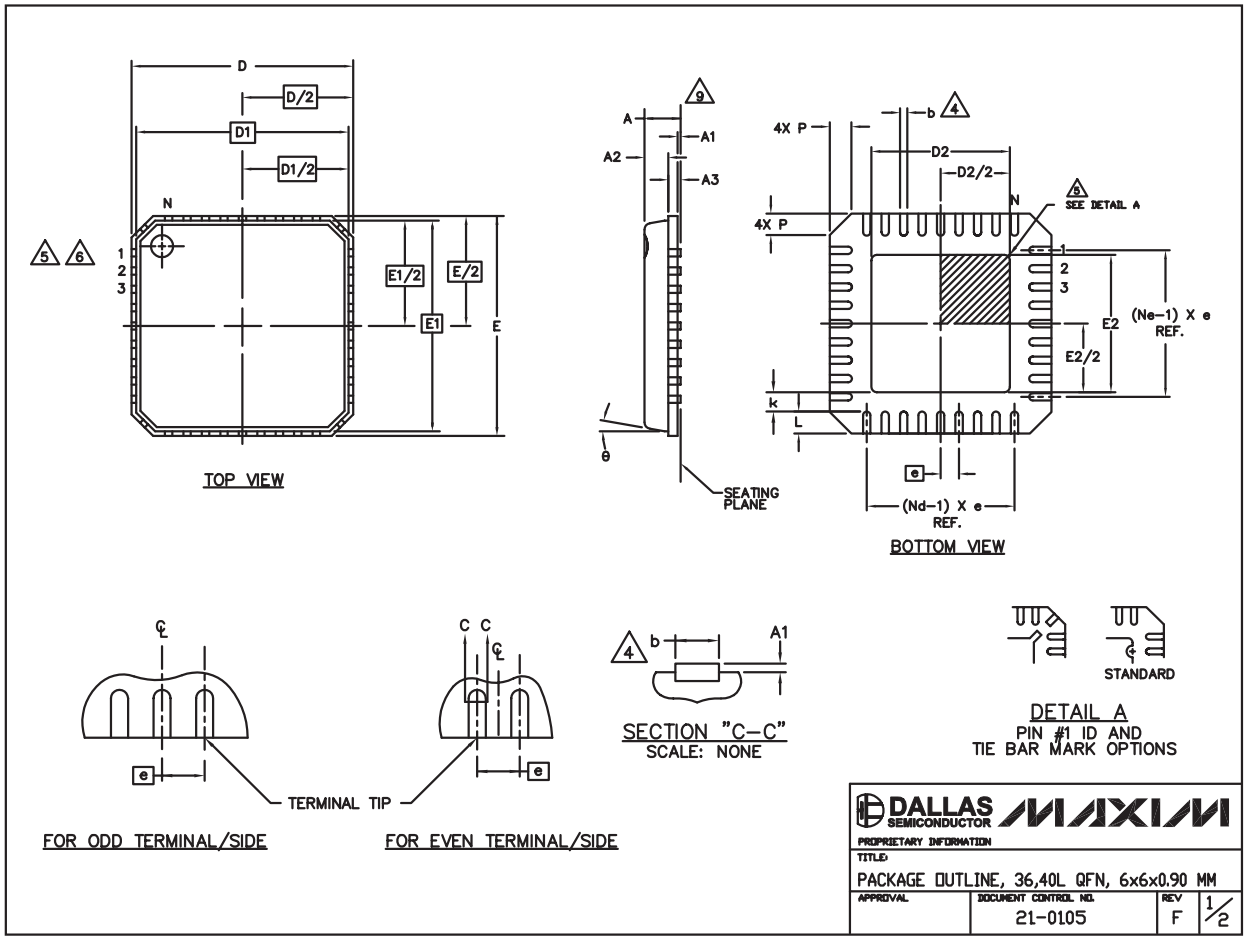
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

36L,40L, QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS						
PKG	36L 6x6			40L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.80	0.90	1.00
A1	0.00	0.01	0.05	0.00	0.01	0.05
A2	0.00	0.65	0.80	0.00	0.65	0.80
A3	0.20 REF			0.20 REF		
b	0.18	0.23	0.30	0.18	0.23	0.30
D	5.90	6.00	6.10	5.90	6.00	6.10
D1	5.75 BSC			5.75 BSC		
E	5.90	6.00	6.10	5.90	6.00	6.10
E1	5.75 BSC			5.75 BSC		
e	0.50 BSC			0.50 BSC		
k	0.25	-	-	0.25	-	-
L	0.50	0.60	0.75	0.30	0.40	0.50
N	36			40		
Nd	6			10		
Ne	6			10		
P	0.24	0.42	0.60	0.24	0.42	0.60
U	10°	11°	12°	10°	11°	12°

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G3666-1	3.55	3.70	3.85	3.55	3.70	3.85
G4066-1	3.95	4.10	4.25	3.95	4.10	4.25

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES).
12. LEADS TO BE COPLANAR 0.08 mm

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 36,40L QFN, 6x6x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0105	F	2/2