



Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

MAX5590-MAX5595

General Description

The MAX5590-MAX5595 octal, 12/10/8-bit, voltage-output digital-to-analog converters (DACs) offer buffered outputs and a 3 μ s maximum settling time at the 12-bit level. The DACs operate from a +2.7V to +5.25V analog supply and a separate +1.8V to +5.25V digital supply. The 20MHz 3-wire serial interface is compatible with SPI™, QSPI™, MICROWIRE™, and digital signal processor (DSP) protocol applications. Multiple devices can share a common serial interface in direct-access or daisy-chained configuration. The MAX5590-MAX5595 provide two multifunction, user-programmable, digital I/O ports. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale. Software-selectable FAST and SLOW settling modes decrease settling time in FAST mode, or reduce supply current in SLOW mode.

The MAX5590/MAX5591 are 12-bit DACs, the MAX5592/MAX5593 are 10-bit DACs, and the MAX5594/MAX5595 are 8-bit DACs. The MAX5590/MAX5592/MAX5594 provide unity-gain-configured output buffers, while the MAX5591/MAX5593/MAX5595 provide force-sense-configured output buffers. The MAX5590-MAX5595 are specified over the extended -40°C to +85°C temperature range, and are available in space-saving 24-pin and 28-pin TSSOP packages.

Applications

Portable Instrumentation
Automatic Test Equipment (ATE)
Digital Offset and Gain Adjustment
Automatic Tuning
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Controls
Motion Control
Microprocessor (μ P)-Controlled Systems
Power Amplifier Control
Fast Parallel-DAC to Serial-DAC Upgrades

Features

- ◆ Octal, 12/10/8-Bit Serial DACs in TSSOP Packages
- ◆ 3 μ s (max) 12-Bit Settling Time to 1/2 LSB
- ◆ Integral Nonlinearity:
 - 1 LSB (max) MAX5590/MAX5591 A-Grade (12-Bit)
 - 1 LSB (max) MAX5592/MAX5593 (10-Bit)
 - 1/2 LSB (max) MAX5594/MAX5595 (8-Bit)
- ◆ Guaranteed Monotonic, ± 1 LSB (max) DNL
- ◆ Two User-Programmable Digital I/O Ports
- ◆ Single +2.7V to +5.25V Analog Supply
- ◆ +1.8V to AVDD Digital Supply
- ◆ 20MHz, 3-Wire, SPI-/QSPI-/MICROWIRE-/DSP-Compatible Serial Interface
- ◆ Glitch-Free Outputs Power Up to Zero Scale, Midscale, or Full Scale Controlled by PU Pin
- ◆ Unity-Gain or Force-Sense-Configured Output Buffers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5590 AEUG*	-40°C to +85°C	24 TSSOP
MAX5590BEUG	-40°C to +85°C	24 TSSOP
MAX5591 AEUI*	-40°C to +85°C	28 TSSOP
MAX5591BEUI	-40°C to +85°C	28 TSSOP
MAX5592 EUG	-40°C to +85°C	24 TSSOP
MAX5593 EUI	-40°C to +85°C	28 TSSOP
MAX5594 EUG	-40°C to +85°C	24 TSSOP
MAX5595 EUI	-40°C to +85°C	28 TSSOP

*Future product—contact factory for availability. Specifications are preliminary.

Selector Guide and Pin Configurations appear at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor Corp.



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For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

AV_{DD} to DV_{DD} ±6V
 AGND to DGND ±0.3V
 AV_{DD} to AGND, DGND -0.3V to +6V
 DV_{DD} to AGND, DGND -0.3V to +6V
 FB₋, OUT₋,
 REF to AGND -0.3V to the lower of (AV_{DD} + 0.3V) or +6V
 SCLK, DIN, CS, PU,
 DSP to DGND -0.3V to the lower of (DV_{DD} + 0.3V) or +6V
 UPIO1, UPIO2
 to DGND -0.3V to the lower of (DV_{DD} + 0.3V) or +6V

Maximum Current into Any Pin ±50mA
 Continuous Power Dissipation (T_A = +70°C)
 24-Pin TSSOP (derate 12.2mW/°C above +70°C) 976mW
 28-Pin TSSOP (derate 12.8mW/°C above +70°C) 1026mW
 Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Maximum Junction Temperature +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 2.7V to 5.25V, DV_{DD} = 1.8V to AV_{DD}, AGND = 0, DGND = 0, V_{REF} = 2.5V (for AV_{DD} = 2.7V to 5.25V), V_{REF} = 4.096V (for AV_{DD} = 4.5V to 5.25V), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution	N	MAX5590/MAX5591		12			Bits
		MAX5592/MAX5593		10			
		MAX5594/MAX5595		8			
Integral Nonlinearity	INL	VREF = 2.5V at AVDD = 2.7V and VREF = 4.096V at AVDD = 5.25V (Note 2)	MAX5590A/MAX5591A (12-bit)	±1			LSB
			MAX5590B/MAX5591B (12-bit)	±2	±4		
			MAX5592/MAX5593 (10-bit)	±0.5	±1		
			MAX5594/MAX5595 (8-bit)	±0.125	±0.5		
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 2)		±1			LSB
Offset Error	VOS	MAX5590A/MAX5591A (12-bit), decimal code = 40		±5			mV
		MAX5590B/MAX5591B (12-bit), decimal code = 40		±5	±25		
		MAX5592/MAX5593 (10-bit), decimal code = 10		±5	±25		
		MAX5594/MAX5595 (8-bit), decimal code = 3		±5	±25		
Offset-Error Drift				5			ppm of FS/°C
Gain Error	GE	Full-scale output	MAX5590A/MAX5591A (12-bit)	±4			LSB
			MAX5590B/MAX5590B (12-bit)	±20	±40		
			MAX5592/MAX5593 (10-bit)	±5	±10		
			MAX5594/MAX5595 (8-bit)	±2	±3		
Gain-Error Drift				1			ppm of FS/°C

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 2.7V to 5.25V, DVDD = 1.8V to AVDD, AGND = 0, DGND = 0, VREF = 2.5V (for AVDD = 2.7V to 5.25V), VREF = 4.096V (for AVDD = 4.5V to 5.25V), RL = 10kΩ, CL = 100pF, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	Full-scale output, AVDD = 2.7V to 5.25V		200		μV/V
REFERENCE INPUT						
Reference Input Range	VREF		0.25		AVDD	V
Reference Input Resistance	RREF	Normal operation (no code dependence)	145	200		kΩ
Reference Leakage Current		Shutdown mode		0.5	1	μA
DAC OUTPUT CHARACTERISTICS						
Output Voltage Noise		SLOW mode, full scale	Unity gain		85	μVRMS
			Force sense		67	
		FAST mode, full scale	Unity gain		140	
			Force sense		110	
Output Voltage Range (Note 3)		Unity-gain output	0		AVDD	V
		Force-sense output	0		AVDD / 2	
DC Output Impedance				38		Ω
Short-Circuit Current		AVDD = 5V, OUT_ to AGND, full scale, FAST mode		57		mA
		AVDD = 3V, OUT_ to AGND, full scale, FAST mode		45		
Power-Up Time		From VDD applied until interface is functional		30	60	μs
Wake-Up Time		Coming out of shutdown, outputs settled		40		μs
Output OUT_ and FB_ Open-Circuit Leakage Current		Programmed in shutdown mode, force-sense outputs only		0.01		μA
DIGITAL OUTPUTS (UPIO_)						
Output High Voltage	VOH	ISOURCE = 2mA		DVDD - 0.5		V
Output Low Voltage	VOL	ISINK = 2mA			0.4	V
DIGITAL INPUTS (SCLK, CS, DIN, DSP, UPIO_)						
Input High Voltage	VIH	DVDD ≥ 2.7V		2.4		V
		DVDD < 2.7V		0.7 x DVDD		
Input Low Voltage	VIL	DVDD > 3.6V			0.8	V
		2.7V ≤ DVDD ≤ 3.6V			0.6	
		DVDD < 2.7V			0.2	
Input Leakage Current	IIN			±0.1	±1	μA
Input Capacitance	CIN			10		pF

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 2.7V to 5.25V, DVDD = 1.8V to AVDD, AGND = 0, DGND = 0, VREF = 2.5V (for AVDD = 2.7V to 5.25V), VREF = 4.096V (for AVDD = 4.5V to 5.25V), RL = 10kΩ, CL = 100pF, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PU INPUT							
Input High Voltage	V _{IH-PU}			DV _{DD} - 200mV			V
Input Low Voltage	V _{IL-PU}			200			mV
Input Leakage Current	I _{IN-PU}	PU still considered floating when connected to a tri-state bus		±200			nA
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	FAST mode		3.6			V/μs
		SLOW mode		1.6			
Voltage-Output Settling Time (Note 5)		FAST mode	MAX5590/MAX5591 from code 322 to code 4095 to 1/2 LSB	2	3		μs
			MAX5592/MAX5593 from code 10 to code 1023 to 1/2 LSB	1.5	3		
			MAX5594/MAX5595 from code 3 to code 255 to 1/2 LSB	1	2		
		SLOW mode	MAX5590/MAX5591 from code 322 to code 4095 to 1/2 LSB	3	6		
			MAX5592/MAX5593 from code 10 to code 1023 1/2 LSB	2.5	6		
			MAX5594/MAX5595 from code 3 to code 255 to 1/2 LSB	2	4		
FB_ Input Voltage				0	V _{REF} / 2		V
FB_ Input Current				0.1			μA
Reference -3dB Bandwidth (Note 6)		Unity gain		200			kHz
		Force sense		150			
Digital Feedthrough		CS = DV _{DD} , code = zero scale, any digital input from 0 to DV _{DD} and DV _{DD} to 0, f = 100kHz		0.1			nV-s
Digital-to-Analog Glitch Impulse		Major carry transition		2			nV-s
DAC-to-DAC Crosstalk		(Note 4)		15			nV-s

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = 2.7V to 5.25V, DVDD = 1.8V to AVDD, AGND = 0, DGND = 0, VREF = 2.5V (for AVDD = 2.7V to 5.25V), VREF = 4.096V (for AVDD = 4.5V to 5.25V), RL = 10kΩ, CL = 100pF, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Analog Supply Voltage Range	AV _{DD}			2.70		5.25	V
Digital Supply Voltage Range	DV _{DD}			1.8		AV _{DD}	V
Operating Supply Current	I _{AVDD} + I _{DVDD}	SLOW mode, all digital inputs at DGND or DV _{DD} , no load, V _{REF} = 4.096V	Unity gain		1.5	3.2	mA
			Force sense		2.4	4.8	
		FAST mode, all digital inputs at DGND or DV _{DD} , no load, V _{REF} = 4.096V	Unity gain		2.5	8	
			Force sense		3.4	8	
Shutdown Supply Current	I _{AVDD(SHDN)} + I _{DVDD(SHDN)}	No clocks, all digital inputs at DGND or DV _{DD} , all DACs in shutdown mode			0.5	1	μA

Note 1: For the force-sense versions, FB₋ is connected to its respective OUT₋. VOUT (max) = VREF / 2, unless otherwise noted.

Note 2: Linearity guaranteed from decimal code 40 to code 4095 for the MAX5590B/MAX5591B (12-bit, B-grade), code 10 to code 1023 for the MAX5592/MAX5593 (10-bit), and code 3 to code 255 for the MAX5594/MAX5595 (8-bit).

Note 3: Represents the functional range. The linearity is guaranteed at VREF = 2.5V (for AVDD from 2.7V to 5.25V), and VREF = 4.096V (for AVDD = 4.5V to 5.25V). See the *Typical Operating Characteristics* section for linearity at other voltages.

Note 4: DC crosstalk is measured as follows: outputs of DACA–DACH are set to full scale and the output of DACH is measured. While keeping DACH unchanged, the outputs of DACA–DACG are transitioned to zero scale and the ΔVOUT of DACH is measured.

Note 5: Guaranteed by design.

Note 6: The reference -3dB bandwidth is measured with a 0.1VP-P sine wave on VREF and with full-scale input code.

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TIMING CHARACTERISTICS—DSP Mode Disabled (3V, 3.3V, 5V Logic) (Figure 1)

(DV_{DD} = 2.7V to 5.25V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f _{SCLK}	2.7V < DV _{DD} < 5.25V			20	MHz
SCLK Pulse-Width High	t _{CH}	(Note 7)	20			ns
SCLK Pulse-Width Low	t _{CL}	(Note 7)	20			ns
$\overline{\text{CS}}$ Fall to SCLK Rise Setup Time	t _{CSS}		10			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	t _{CSH}		5			ns
SCLK Rise to $\overline{\text{CS}}$ Fall Setup	t _{CS0}		10			ns
DIN to SCLK Rise Setup Time	t _{DS}		12			ns
DIN to SCLK Rise Hold Time	t _{DH}		5			ns
SCLK Rise to DOUTDC1 Valid Propagation Delay	t _{DO1}	C _L = 20pF, UPIO ₋ = DOUTDC1 mode			30	ns
SCLK Fall to DOUT ₋ Valid Propagation Delay	t _{DO2}	C _L = 20pF, UPIO ₋ = DOUTDC0 or DOUTRB mode			30	ns
$\overline{\text{CS}}$ Rise to SCLK Rise Hold Time	t _{CS1}	MICROWIRE and SPI modes 0 and 3	10			ns
$\overline{\text{CS}}$ Pulse-Width High	t _{CSW}		45			ns
UPIO₋ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t _{DOZ}	C _L = 20pF, from end of write cycle to UPIO ₋ in high impedance			100	ns
DOUTRB Tri-State Time from $\overline{\text{CS}}$ Rise	t _{DRBZ}	C _L = 20pF, from rising edge of $\overline{\text{CS}}$ to UPIO ₋ in high impedance			20	ns
DOUTRB Tri-State Enable Time from 8th SCLK Rise	t _{ZEN}	C _L = 20pF, from 8th rising edge of SCLK to UPIO ₋ driven out of tri-state			20	ns
$\overline{\text{LDAC}}$ Pulse-Width Low	t _{LDL}	Figure 5	20			ns
$\overline{\text{LDAC}}$ Effective Delay	t _{LDS}	Figure 6	100			ns
$\overline{\text{CLR}}$, $\overline{\text{MID}}$, $\overline{\text{SET}}$ Pulse-Width Low	t _{CMS}	Figure 5	20			ns
GPO Output Settling Time	t _{GP}	Figure 6			100	ns
GPO Output High-Impedance Time	t _{GPZ}				100	ns

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TIMING CHARACTERISTICS—DSP Mode Disabled (1.8V Logic) (Figure 1)

(DV_{DD} = 1.8V to 5.25V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f _{SCLK}	1.8V < DV _{DD} < 5.25V			10	MHz
SCLK Pulse-Width High	t _{CH}	(Note 7)	40			ns
SCLK Pulse-Width Low	t _{CL}	(Note 7)	40			ns
$\overline{\text{CS}}$ Fall to SCLK Rise Setup Time	t _{CSS}		20			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	t _{CSH}		0			ns
SCLK Rise to $\overline{\text{CS}}$ Fall Setup	t _{CS0}		10			ns
DIN to SCLK Rise Setup Time	t _{DS}		20			ns
DIN to SCLK Rise Hold Time	t _{DH}		5			ns
SCLK Rise to DOUTDC1 Valid Propagation Delay	t _{DO1}	C _L = 20pF, UPIO_ = DOUTDC1 mode			60	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t _{DO2}	C _L = 20pF, UPIO_ = DOUTDC0 or DOUTRB mode			60	ns
$\overline{\text{CS}}$ Rise to SCLK Rise Hold Time	t _{CS1}	MICROWIRE and SPI modes 0 and 3	20			ns
$\overline{\text{CS}}$ Pulse-Width High	t _{CSW}		90			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t _{DOZ}	C _L = 20pF, from end of write cycle to UPIO_ in high impedance			200	ns
DOUTRB Tri-State Time from $\overline{\text{CS}}$ Rise	t _{DRBZ}	C _L = 20pF, from rising edge of $\overline{\text{CS}}$ to UPIO_ in high impedance			40	ns
DOUTRB Tri-State Enable Time from 8th SCLK Rise	t _{ZEN}	C _L = 20pF, from 8th rising edge of SCLK to UPIO_ driven out of tri-state			40	ns
$\overline{\text{LDAC}}$ Pulse-Width Low	t _{LDL}	Figure 5	40			ns
$\overline{\text{LDAC}}$ Effective Delay	t _{LDS}	Figure 6	200			ns
$\overline{\text{CLR}}$, $\overline{\text{MID}}$, $\overline{\text{SET}}$ Pulse-Width Low	t _{CMS}	Figure 5	40			ns
GPO Output Settling Time	t _{GP}	Figure 6			200	ns
GPO Output High-Impedance Time	t _{GPZ}				200	ns

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TIMING CHARACTERISTICS—DSP Mode Enabled (3V, 3.3V, 5V Logic) (Figure 2)

(DVDD = 2.7V to 5.25V, GND = 0, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	fSCLK	2.7V < DVDD < 5.25V			20	MHz
SCLK Pulse-Width High	tCH	(Note 7)	20			ns
SCLK Pulse-Width Low	tCL	(Note 7)	20			ns
$\overline{\text{CS}}$ Fall to SCLK Fall Setup Time	tCSS		10			ns
$\overline{\text{DSP}}$ Fall to SCLK Fall Setup Time	tDSS		10			ns
SCLK Fall to $\overline{\text{CS}}$ Rise Hold Time	tCSH		5			ns
SCLK Fall to $\overline{\text{CS}}$ Fall Delay	tCS0		10			ns
SCLK Fall to $\overline{\text{DSP}}$ Fall Delay	tDS0		10			ns
DIN to SCLK Fall Setup Time	tDS		12			ns
DIN to SCLK Fall Hold Time	tDH		5			ns
SCLK Rise to DOUT_ Valid Propagation Delay	tDO1	CL = 20pF, UPIO_ = DOUTDC1 or DOUTRB mode			30	ns
SCLK Fall to DOUT_ Valid Propagation Delay	tDO2	CL = 20pF, UPIO_ = DOUTDC0 mode			30	ns
$\overline{\text{CS}}$ Rise to SCLK Fall Hold Time	tCS1	MICROWIRE and SPI modes 0 and 3	10			ns
$\overline{\text{CS}}$ Pulse-Width High	tCSW		45			ns
$\overline{\text{DSP}}$ Pulse-Width High	tDSW		20			ns
$\overline{\text{DSP}}$ Pulse-Width Low	tDSPWL	(Note 8)	20			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	tDOZ	CL = 20pF, from end of write cycle to UPIO_ in high impedance			100	ns
DOUTRB Tri-State Time from $\overline{\text{CS}}$ Rise	tDRBZ	CL = 20pF, from rising edge of $\overline{\text{CS}}$ to UPIO_ in high impedance			20	ns
DOUTRB Tri-State Enable Time from 8th SCLK Fall	tZEN	CL = 20pF, from 8th falling edge of SCLK to UPIO_ driven out of tri-state			20	ns
$\overline{\text{LDAC}}$ Pulse-Width Low	tLDL	Figure 5	20			ns
$\overline{\text{LDAC}}$ Effective Delay	tLDS	Figure 6	100			ns
$\overline{\text{CLR}}$, $\overline{\text{MID}}$, $\overline{\text{SET}}$ Pulse-Width Low	tCMS	Figure 5	20			ns
GPO Output Settling Time	tGP	Figure 6			100	ns
GPO Output High-Impedance Time	tGPZ				100	ns

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TIMING CHARACTERISTICS—DSP Mode Enabled (1.8V Logic) (Figure 2)

(DV_{DD} = 1.8V to 5.25V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Frequency	f _{SCLK}	1.8V < DV _{DD} < 5.25V			10	MHz
SCLK Pulse-Width High	t _{CH}	(Note 7)	40			ns
SCLK Pulse-Width Low	t _{CL}	(Note 7)	40			ns
$\overline{\text{CS}}$ Fall to SCLK Fall Setup Time	t _{CSS}		20			ns
$\overline{\text{DSP}}$ Fall to SCLK Fall Setup Time	t _{DSS}		20			ns
SCLK Fall to $\overline{\text{CS}}$ Rise Hold Time	t _{CSH}		0			ns
SCLK Fall to $\overline{\text{CS}}$ Fall Delay	t _{CS0}		10			ns
SCLK Fall to $\overline{\text{DSP}}$ Fall Delay	t _{DS0}		15			ns
DIN to SCLK Fall Setup Time	t _{DS}		20			ns
DIN to SCLK Fall Hold Time	t _{DH}		5			ns
SCLK Rise to DOUT_ Valid Propagation Delay	t _{DO1}	C _L = 20pF, UPIO_ = DOUTDC1 or DOUTRB mode			60	ns
SCLK Fall to DOUT_ Valid Propagation Delay	t _{DO2}	C _L = 20pF, UPIO_ = DOUTDC0 mode			60	ns
$\overline{\text{CS}}$ Rise to SCLK Fall Hold Time	t _{CS1}	MICROWIRE and SPI modes 0 and 3	20			ns
$\overline{\text{CS}}$ Pulse-Width High	t _{CSW}		90			ns
$\overline{\text{DSP}}$ Pulse-Width High	t _{DSW}		40			ns
$\overline{\text{DSP}}$ Pulse-Width Low	t _{DSPWL}	(Note 8)	40			ns
UPIO_ TIMING CHARACTERISTICS						
DOUT Tri-State Time when Exiting DOUTDC0, DOUTDC1, and UPIO Modes	t _{DOZ}	C _L = 20pF, from end of write cycle to UPIO_ in high impedance			200	ns
DOUTRB Tri-State Time from $\overline{\text{CS}}$ Rise	t _{DRBZ}	C _L = 20pF, from rising edge of $\overline{\text{CS}}$ to UPIO_ in high impedance			40	ns
DOUTRB Tri-State Enable Time from 8th SCLK Fall	t _{ZEN}	C _L = 20pF, from 8th falling edge of SCLK to UPIO_ driven out of tri-state			40	ns
$\overline{\text{LDAC}}$ Pulse-Width Low	t _{LDL}	Figure 5	40			ns
$\overline{\text{LDAC}}$ Effective Delay	t _{LDS}	Figure 6	200			ns
$\overline{\text{CLR}}$, $\overline{\text{MID}}$, $\overline{\text{SET}}$ Pulse-Width Low	t _{CMS}	Figure 5	40			ns
GPO Output Settling Time	t _{GP}	Figure 6			200	ns
GPO Output High-Impedance Time	t _{GPZ}				200	ns

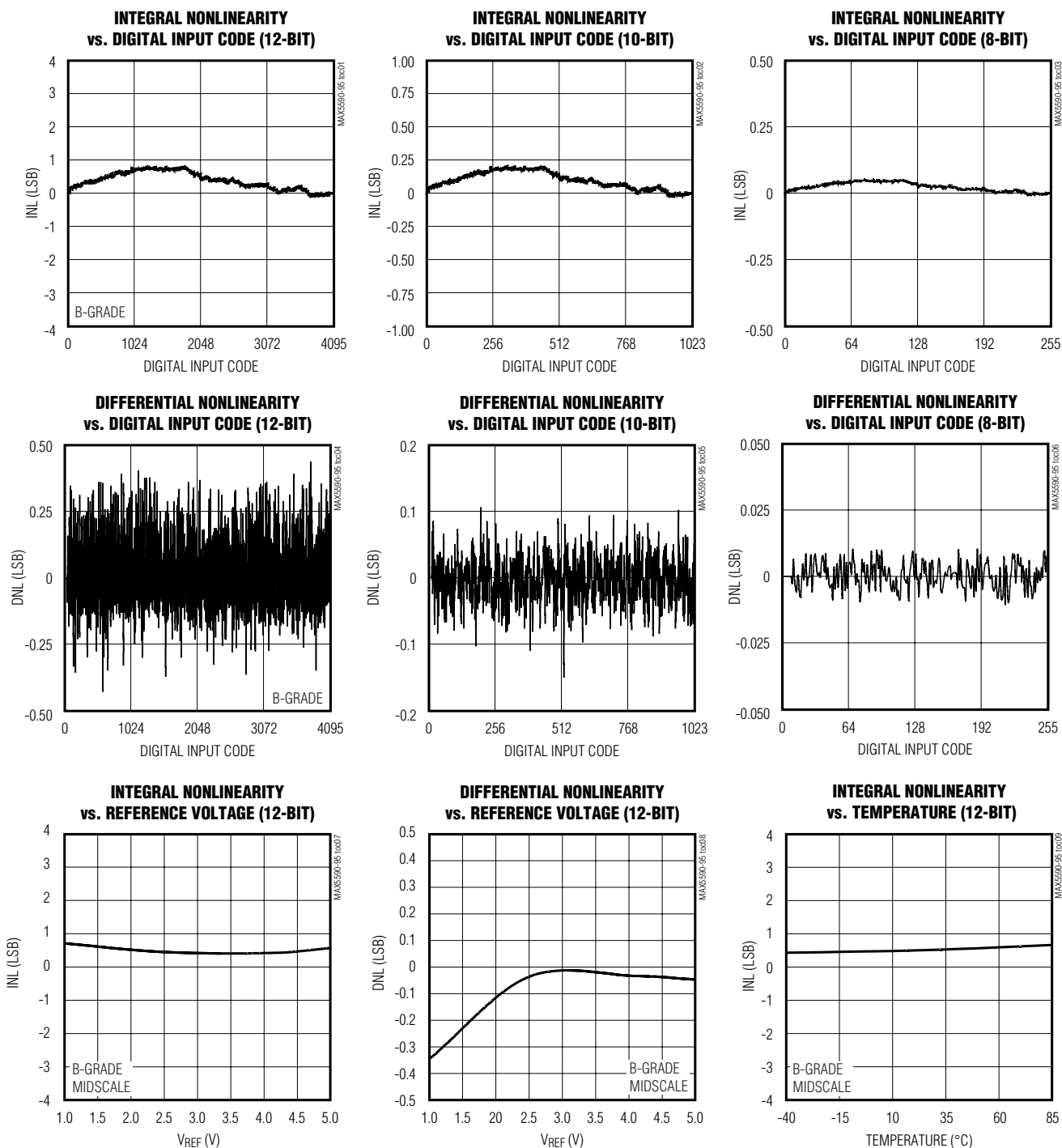
Note 7: In some daisy-chain modes, data is required to be clocked in on one clock edge and the shifted data clocked out on the following edge. In the case of a 1/2 clock-period delay, it is necessary to increase the minimum high/low clock times to 25ns (2.7V) or 50ns (1.8V).

Note 8: The falling edge of $\overline{\text{DSP}}$ starts a DSP-type bus cycle, provided that $\overline{\text{CS}}$ is also active low to select the device. $\overline{\text{DSP}}$ active low and $\overline{\text{CS}}$ active low must overlap by a minimum of 10ns (2.7V) or 20ns (1.8V). $\overline{\text{CS}}$ can be permanently low in this mode of operation.

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Typical Operating Characteristics

($AV_{DD} = DV_{DD} = 5V$, $V_{REF} = 4.096V$, $R_L = 10k\Omega$, $C_L = 100pF$, speed mode = FAST, PU = floating, $T_A = +25^\circ C$, unless otherwise noted.)

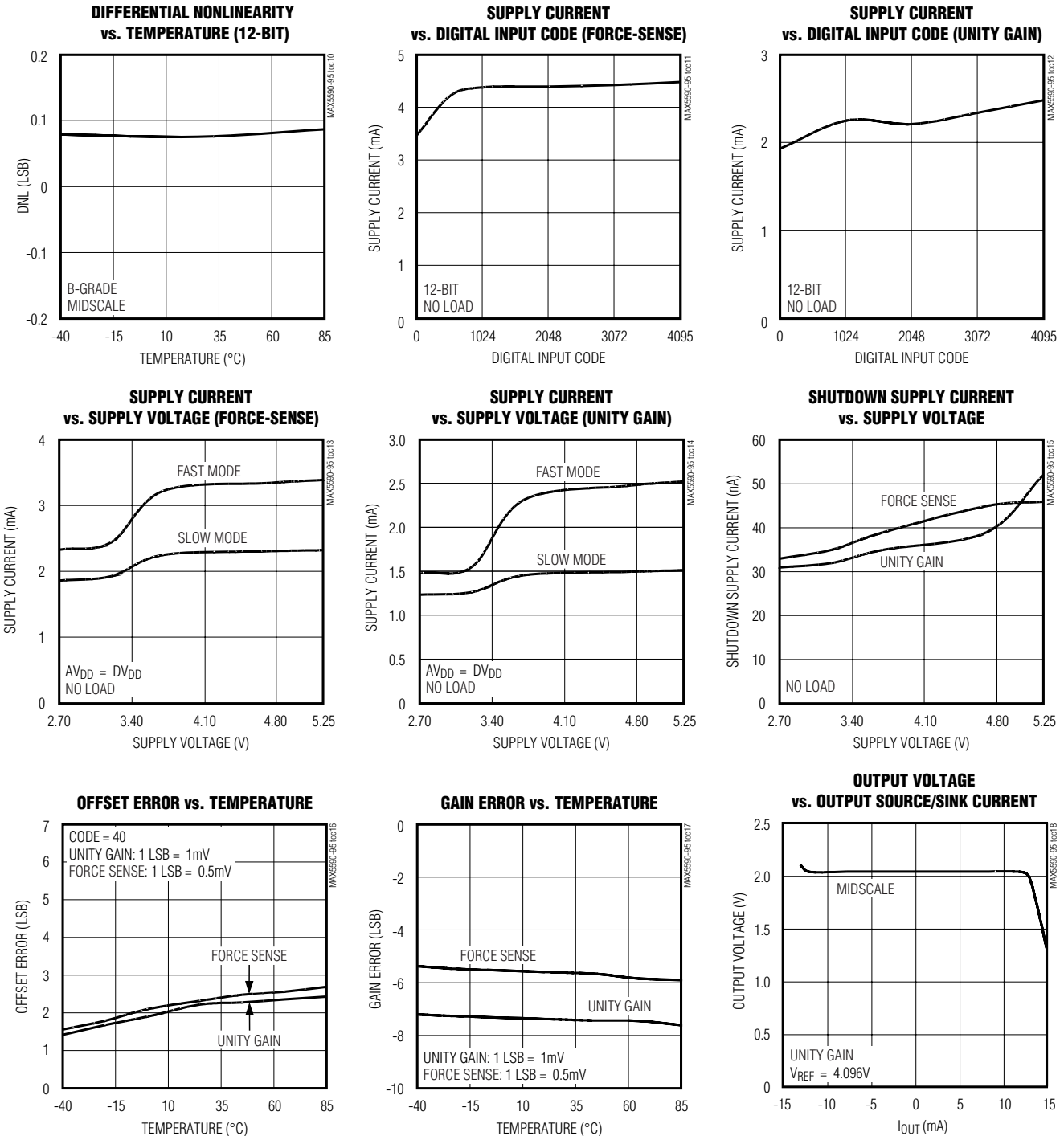


Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = 5V$, $V_{REF} = 4.096V$, $R_L = 10k\Omega$, $C_L = 100pF$, speed mode = FAST, PU = floating, $T_A = +25^\circ C$, unless otherwise noted.)

MAX5590-MAX5595

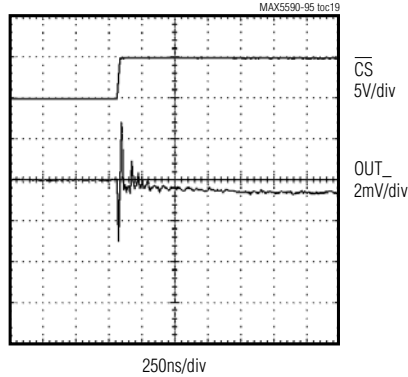


Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

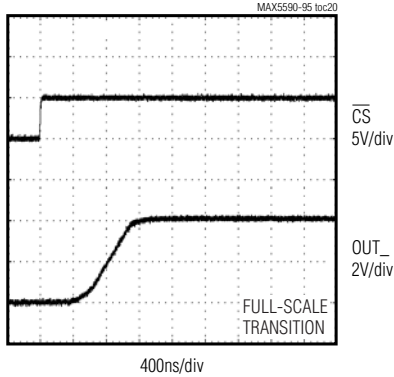
Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = 5V$, $V_{REF} = 4.096V$, $R_L = 10k\Omega$, $C_L = 100pF$, speed mode = FAST, PU = floating, $T_A = +25^\circ C$, unless otherwise noted.)

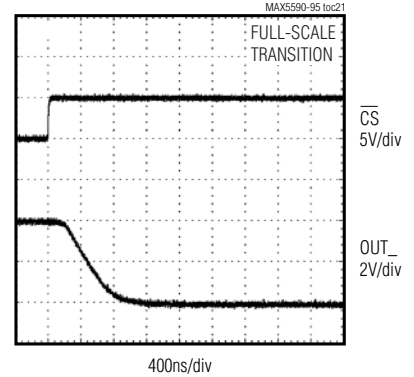
MAJOR-CARRY TRANSITION GLITCH



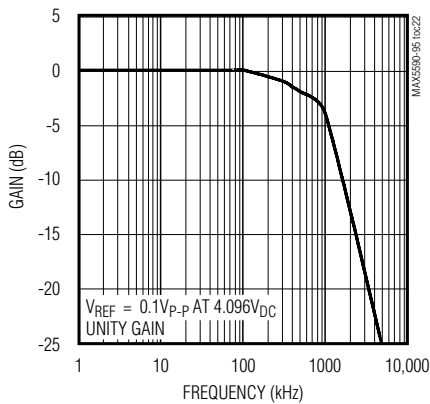
SETTLING TIME POSITIVE



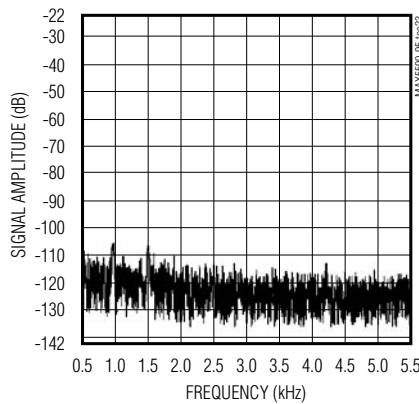
SETTLING TIME NEGATIVE



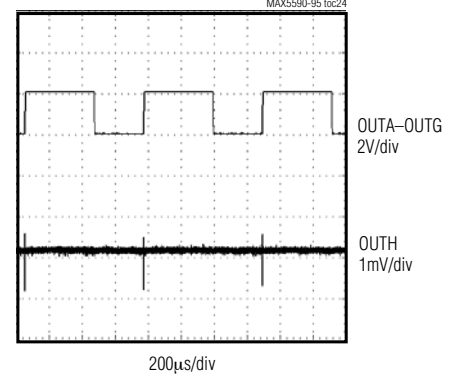
REFERENCE INPUT BANDWIDTH



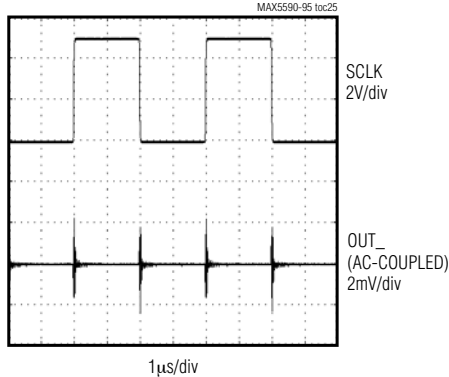
REFERENCE FEEDTHROUGH AT 1kHz



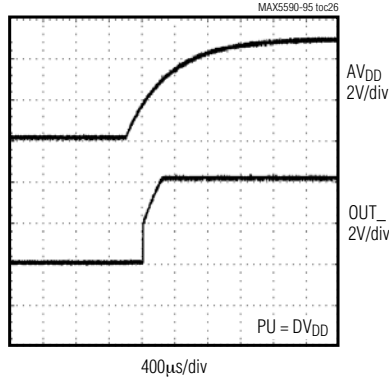
DAC-TO-DAC CROSSTALK



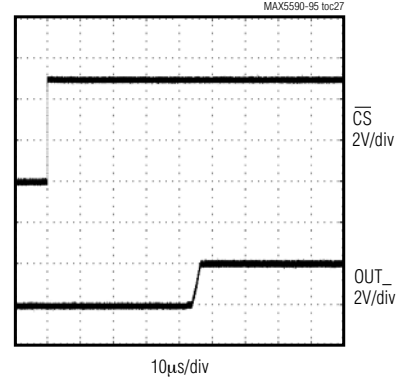
DIGITAL FEEDTHROUGH



POWER-UP GLITCH



EXITING SHUTDOWN TO MIDSACLE



Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Pin Description

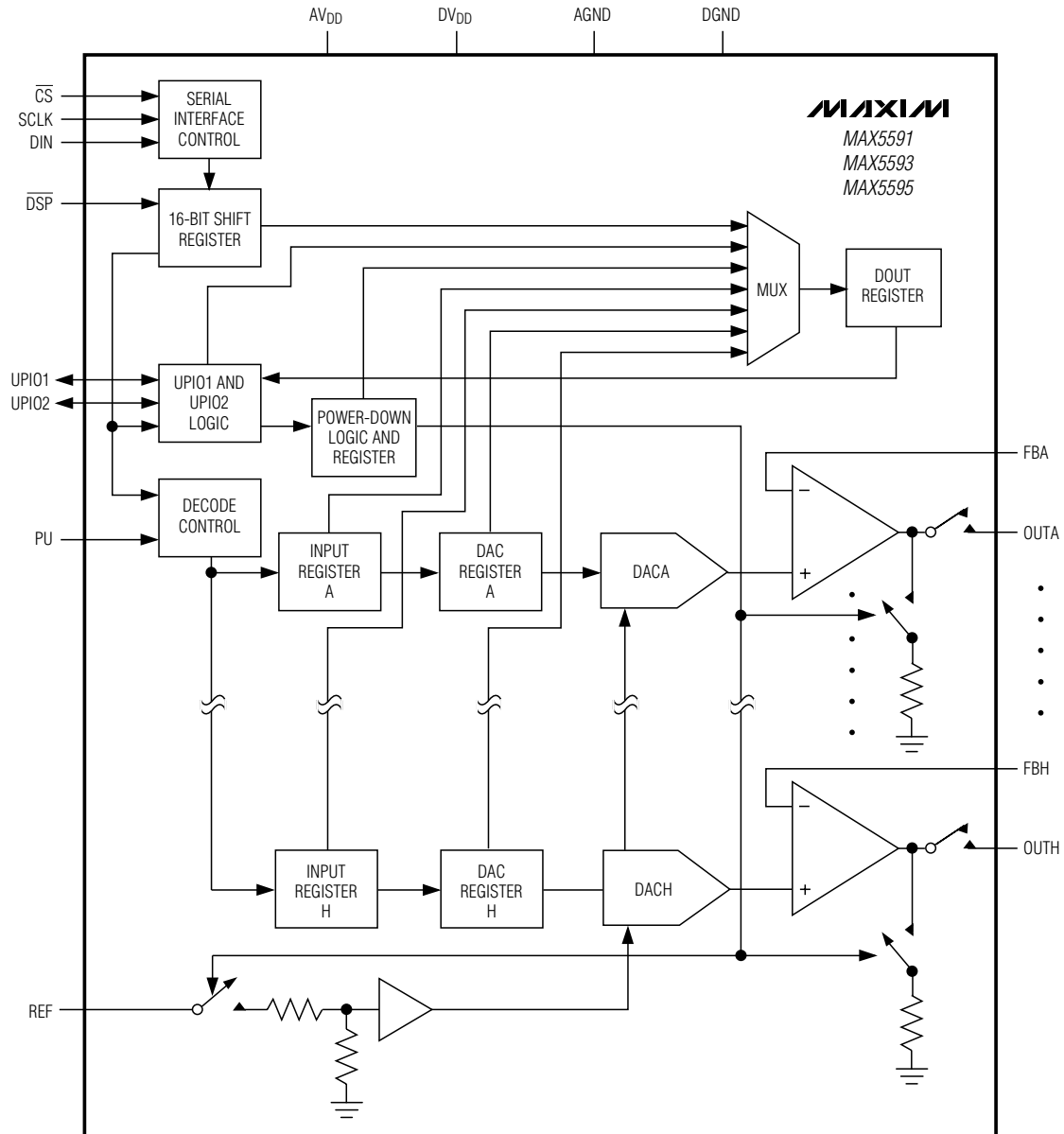
MAX5590-MAX5595

PIN		NAME	FUNCTION
MAX5590 MAX5592 MAX5594	MAX5591 MAX5593 MAX5595		
1	1	AV _{DD}	Analog Supply
2	2	AGND	Analog Ground
3	3	OUTA	DACA Output
4, 8, 17, 21	—	N.C.	No Connection. Not internally connected.
5	6	OUTB	DACB Output
6	7	OUTC	DACC Output
7	10	OUTD	DACD Output
9	11	$\overline{\text{CS}}$	Active-Low Chip-Select Input
10	12	SCLK	Serial Clock Input
11	13	DIN	Serial Data Input
12	14	$\overline{\text{DSP}}$	Clock Enable. Connect $\overline{\text{DSP}}$ to DV _{DD} at power-up to transfer data on the rising edge of SCLK. Connect $\overline{\text{DSP}}$ to GND to transfer data on the falling edge of SCLK. Connect $\overline{\text{DSP}}$ to DGND at power-up to transfer data on the falling edge of SCLK.
13	15	DV _{DD}	Digital Supply
14	16	DGND	Digital Ground
15	17	UPIO1	User-Programmable Input/Output 1
16	18	UPIO2	User-Programmable Input/Output 2
18	19	OUTE	DACE Output
19	22	OUTF	DACF Output
20	23	OUTG	DACG Output
22	26	OUTH	DACH Output
23	27	PU	Power-Up State Select Input. Connect PU to DV _{DD} to set OUTA–OUTH to full scale upon power-up. Connect PU to DGND to set OUTA–OUTH to zero upon power-up. Leave PU floating at power-up to set OUTA–OUTH to midscale.
24	28	REF	Reference Input
—	4	FBA	Feedback for DACA
—	5	FBB	Feedback for DACB
—	8	FBC	Feedback for DACC
—	9	FBD	Feedback for DACD
—	20	FBE	Feedback for DACE
—	21	FBF	Feedback for DACF
—	24	FBG	Feedback for DACG
—	25	FBH	Feedback for DACH

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Functional Diagrams (continued)

MAX5590-MAX5595



Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Detailed Description

The MAX5590–MAX5595 octal, 12/10/8-bit, voltage-output DACs offer buffered outputs and a 3μs maximum settling time at the 12-bit level. The DACs operate from a single 2.7V to 5.25V analog supply and a separate 1.8V to AVDD digital supply. The MAX5590–MAX5595 include an input register and DAC register for each channel and a 16-bit data-in/data-out shift register. The 3-wire serial interface is compatible with SPI, QSPI, MICROWIRE, and DSP applications. The MAX5590–MAX5595 provide two user-programmable digital I/O ports, which are programmed through the serial interface. The externally selectable power-up states of the DAC outputs are either zero scale, midscale, or full scale.

Reference Input

The reference input, REF, accepts both AC and DC values with a voltage range extending from analog ground (AGND) to AVDD. The voltage at REF sets the full-scale output of the DACs. Determine the output voltage using the following equations:

Unity-gain versions:

$$V_{OUT_} = (V_{REF} \times \text{CODE}) / 2^N$$

Force-sense versions (FB_ connected to OUT_):

$$V_{OUT} = 0.5 \times (V_{REF} \times \text{CODE}) / 2^N$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the MAX5590/MAX5591, N = 12 and CODE ranges from 0 to 4095. For the MAX5592/MAX5593, N = 10 and CODE ranges from 0 to 1023. For the MAX5594/MAX5595, N = 8 and CODE ranges from 0 to 255.

Output Buffers

The DACA and DACH output-buffer amplifiers of the MAX5590–MAX5595 are unity-gain stable with rail-to-rail output voltage swings and a typical slew rate of 3.6V/μs (FAST mode). The MAX5590/MAX5592/MAX5594 provide unity-gain outputs, while the MAX5591/MAX5593/MAX5595 provide force-sense outputs. For the MAX5591/MAX5593/MAX5595, access to the output amplifier's inverting input provides flexibility in output gain setting and signal conditioning (see the *Applications Information* section).

The MAX5590–MAX5595 offer FAST and SLOW settling-time modes. In the SLOW mode, the settling time is 6μs (max), and the supply current is 3.2mA (max). In the FAST mode, the settling time is 3μs (max), and the supply current is 8mA (max). See the *Digital Interface* section for settling-time mode programming details.

Use the serial interface to set the shutdown output impedance of the amplifiers to 1kΩ or 100kΩ for the MAX5590/MAX5592/MAX5594 and 1kΩ or high impedance for the MAX5591/MAX5593/MAX5595. The DAC outputs can drive a 10kΩ (typ) load and are stable with up to 500pF (typ) of capacitive load.

Power-On Reset

At power-up, all DAC outputs power up to full scale, midscale, or zero scale, depending on the configuration of the PU input. Connect PU to DVDD to set OUT_ to full scale upon power-up. Connect PU to digital ground (DGND) at power-up to set OUT_ to zero scale. Leave PU floating to set OUT_ to midscale.

Digital Interface

The MAX5590–MAX5595 use a 3-wire serial interface that is compatible with SPI, QSPI, MICROWIRE, and DSP protocol applications (Figures 1 and 2). Connect $\overline{\text{DSP}}$ to DVDD before power-up to clock data in on the rising edge of SCLK. Connect $\overline{\text{DSP}}$ to DGND before power-up to clock data in on the falling edge of SCLK. After power-up, the device enters DSP frame-sync mode on the first rising edge of $\overline{\text{DSP}}$. Refer to the *MAX5590–MAX5595 Programmer's Handbook* for details.

The MAX5590–MAX5595 include a 16-bit input shift register. The data is loaded into the input shift register through the serial interface. The 16 bits can be sent in two serial 8-bit packets or one 16-bit word (CS must remain low until all 16 bits are transferred). The data is loaded MSB first. For the MAX5590/MAX5591, the 16 bits consist of 4 control bits (C3–C0) and 12 data bits (D11–D0) (see Table 1). For the 10-bit MAX5592/MAX5593 devices, D11–D2 are the data bits and D1 and D0 are sub-bits. For the 8-bit MAX5594/MAX5595 devices, D11–D4 are the data bits and D3–D0 are sub-bits. Set all sub-bits to zero for optimum performance.

Each DAC channel includes two registers: an input register and the DAC register. At power-up, the DAC output is set according to the state of PU. The DACs are double-buffered, which allows any of the following for each channel:

- Loading the input register without updating the DAC register
- Updating the DAC register from the input register
- Updating the input and DAC registers simultaneously

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

MAX5590-MAX5595

Table 1. Serial Write Data Format

MSB				16 BITS OF SERIAL DATA												LSB
CONTROL BITS				DATA BITS												
C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	

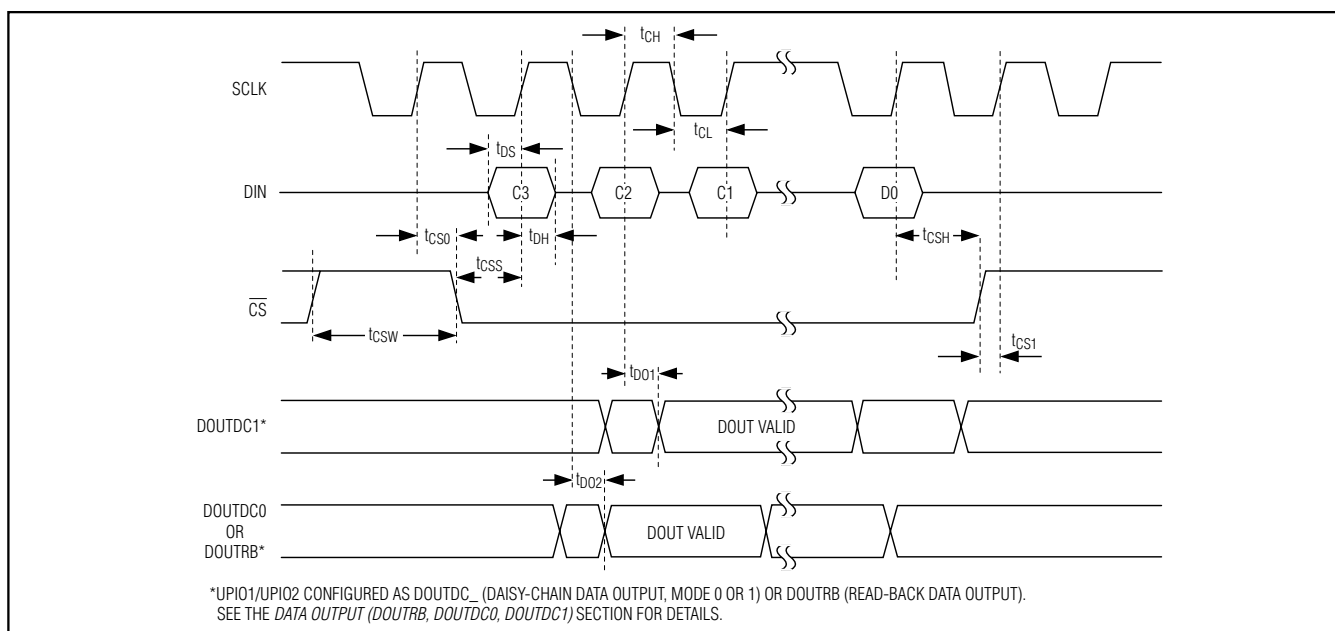


Figure 1. Serial-Interface Timing Diagram (DSP Mode Disabled)

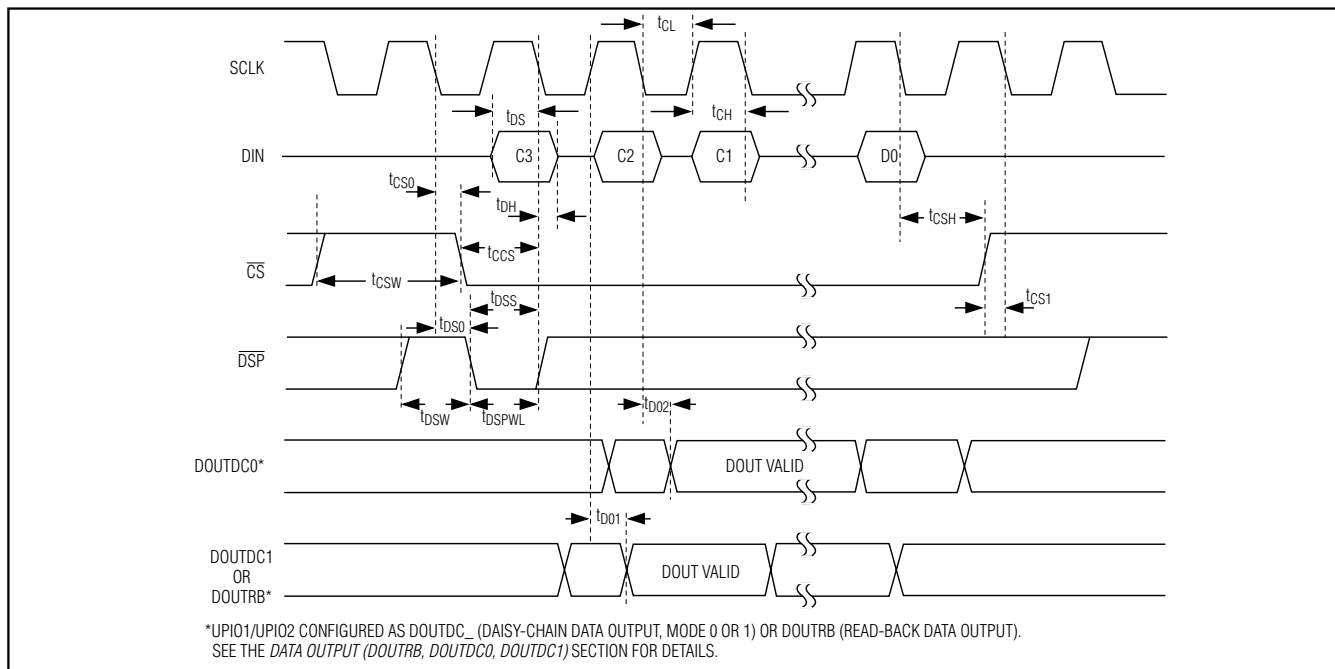


Figure 2. Serial-Interface Timing Diagram (DSP Mode Enabled)

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Serial-Interface Programming Commands

Tables 2a, 2b, and 2c provide all of the serial-interface programming commands for the MAX5590–MAX5595. Table 2a shows the basic DAC programming commands, Table 2b gives the advanced-feature programming commands, and Table 2c provides the 24-bit read commands. Figures 3 and 4 provide the serial-interface diagrams for read and write operations.

Loading Input and DAC Registers

The MAX5590–MAX5595 contain a 16-bit shift register that is followed by a 12-bit input register and a 12-bit DAC register for each channel (see the *Functional Diagrams*). Tables 3, 4, and 5 highlight a few of the commands that handle the loading of the input and DAC registers. See Table 2a for all DAC programming commands.

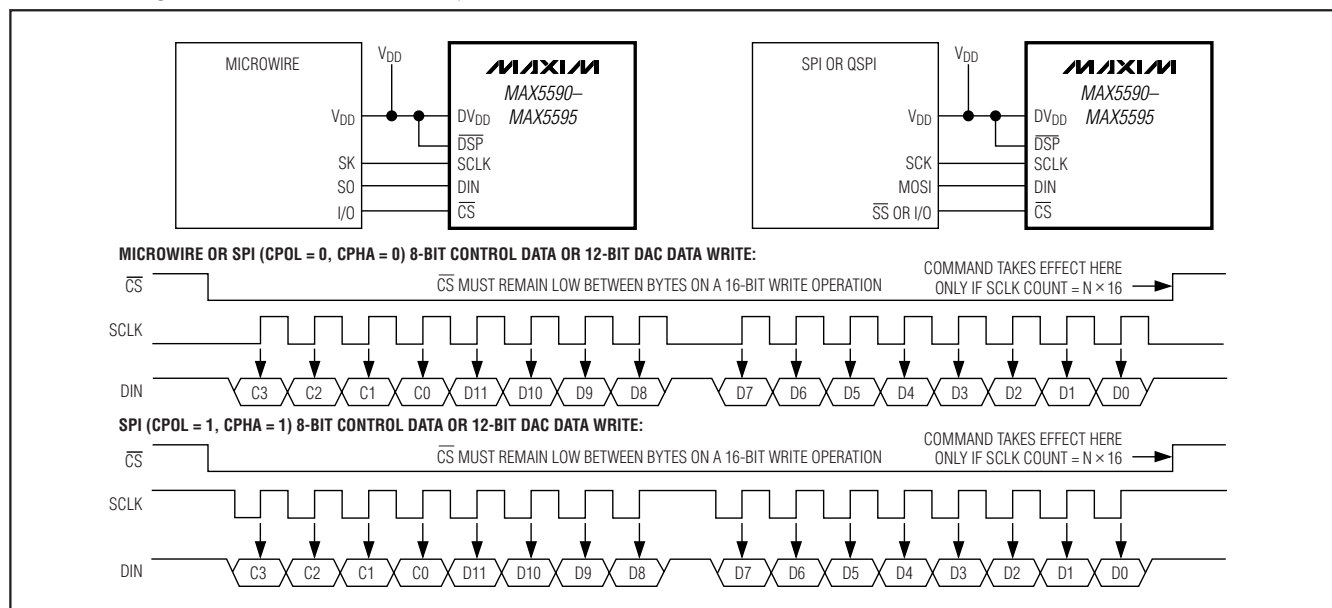


Figure 3. MICROWIRE and SPI Single DAC Writes (CPOL = 0, CPHA = 0 or CPOL = 1, CPHA = 1)

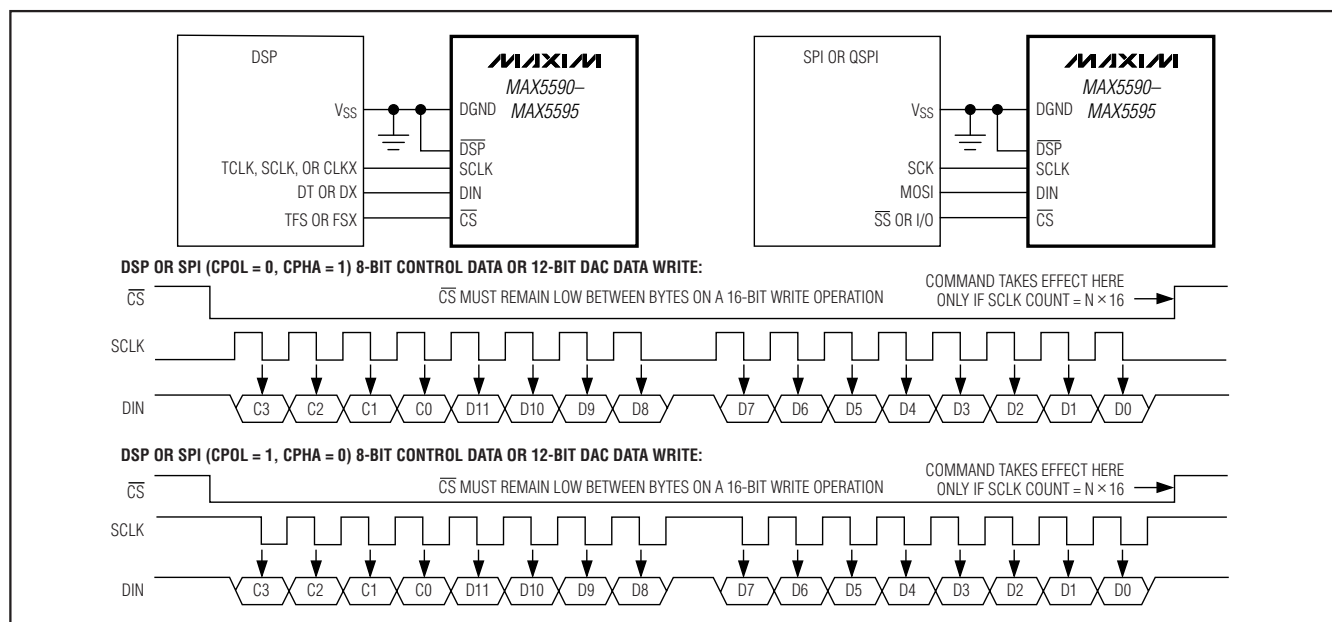


Figure 4. DSP and SPI Single DAC Writes (CPOL = 0, CPHA = 1 or CPOL = 1, CPHA = 0)

Table 2a. DAC Programming Commands

DATA	CONTROL BITS				DATA BITS													FUNCTION
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
INPUT REGISTERS (A–H)																		
DIN	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register A from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register B from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register C from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	0	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register D from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	1	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register E from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	1	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register F from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	1	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register G from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	
DIN	0	1	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0	Load input register H from shift register; DAC registers are unchanged. DAC outputs are unchanged.*	

*For the MAX5592/MAX5593 (10-bit version), D11–D2 are the significant bits and D1 and D0 are sub-bits. For the MAX5594/MAX5595 (8-bit version), D11–D4 are the significant bits and D3–D0 are sub-bits. Set all sub-bits to zero during the write commands.

Table 2b. Advanced-Feature Programming Commands

DATA	CONTROL BITS				DATA BITS								FUNCTION			
	C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SELECT BITS																
DIN	1	0	0	0	X	X	X	X	MIH	MG	MF	ME	MD	MC	MB	MA
LOADING INPUT AND DAC REGISTERS (A-H)																
DIN	1	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0
SHUTDOWN BITS																
DIN	1	0	1	1	0	0	0	0	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0
DOUTRB	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X
DIN	1	0	1	1	0	0	1	0	PDH1	PDH0	PDG1	PDG0	PDF1	PDF0	PDE1	PDE0
DOUTRB	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X
DIN	1	0	1	1	0	1	0	0	PDCH	PDCG	PDCF	PDCE	PDCD	PDCC	PDCB	PDCA
DOUTRB	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X

X = Don't care.

* For the MAX5592/MAX5593 (10-bit version), D11-D2 are the significant bits and D1 and D0 are sub-bits. For the MAX5594/MAX5595 (8-bit version), D11-D4 are the significant bits and D3-D0 are sub-bits. Set all sub-bits to zero during the write commands.

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Table 2b. Advanced-Feature Programming Commands (continued)

DATA		CONTROL BITS				DATA BITS												FUNCTION
		C3	C2	C1	C0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
UPIO CONFIGURATION BITS																		
DIN	1	0	1	1	0	1	1	0	0	UPSL2	UPSL1	UP3	UP2	UP1	UP0	X	X	Write UPIO configuration bits. See Tables 19 and 22.
DIN	1	0	1	1	0	1	1	1	1	X	X	X	X	X	X	X	X	
DOUTRB	X	X	X	X	X	X	X	X	X	UP3-2	UP2-2	UP1-2	UP0-2	UP3-1	UP2-1	UP1-1	UP0-1	Read-back UPIO configuration bits function.
SETTLING-TIME-MODE BITS																		
DIN	1	0	1	1	1	0	0	0	0	SPDH	SPDG	SPDF	SPDE	SPDD	SPDC	SPDB	SPDA	Write settling-time bits for DACA-DACH (0 = SLOW [default, 6μs], 1 = FAST [3μs]).
DIN	1	0	1	1	1	0	0	1	X	X	X	X	X	X	X	X	X	
DOUTRB	X	X	X	X	X	X	X	X	X	SPDH	SPDG	SPDF	SPDE	SPDD	SPDC	SPDB	SPDA	Read-back DAC settling-time bits.
UPIO_AS GPI (GENERAL-PURPOSE INPUT)																		
DIN	1	0	1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	Read UPIO_ inputs (valid only when UPIO1 or UPIO2 is configured as a general-purpose input.) See the GPI, GPOL, GPOH section.
DOUTRB	X	X	X	X	X	X	X	X	X	X	RTP2	LF2	LR2	RTP1	LF1	LR1		
CPOL AND CPHA CONTROL BITS																		
DIN	1	1	0	0	0	0	0	0	X	X	X	X	X	X	X	CPOL	CPHA	Write CPOL, CPHA control bits. See Table 15.
DIN	1	1	0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	
DOUTRB	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPOL	CPHA	Read CPOL, CPHA control bits.

X = Don't care.

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

DATA	CONTROL BITS

$X = \text{Don't care.}$

if During readback, all ones (code FF) must be clocked into DIN for all 24 bits. No command can be issued before all 24 bits have been clocked out. CS must be kept low while all 24 bits are being clocked out.

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

DAC Programming Examples:

To load input register A from the shift register, leaving DAC register A unchanged (DAC output unchanged), use the command in Table 3.

The MAX5590-MAX5595 can load all of the input registers (A–H) simultaneously from the shift register, leaving the DAC registers unchanged (DAC output unchanged), by using the command in Table 4.

To load all of the input registers (A–H) and all of the DAC registers (A–H) simultaneously, use the command in Table 5.

For the 10-bit and 8-bit versions, set sub-bits = 0 for best performance.

Advanced-Feature Programming Commands

Select Bits (M₇)

The select bits allow synchronous updating of any combination of channels. The select bits command the loading of the DAC register from the input register of each channel. Set the select bit M₇ = 1 to load the DAC register “_” with data from the input register “_”, where “_” is replaced with A, B, or C and so on through H, depending on the selected channel. Setting the select bit M₇ = 0 results in no action for that channel (Table 6).

Select Bits Programming Example:

To load DAC register B from input register B while keeping other channels (A, C–H) unchanged, set MB = 1 and M₇ = 0 (Table 7).

Table 3. Load Input Register A from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 4. Load Input Registers (A–H) from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	0	1	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 5. Load Input Registers (A–H) and DAC Registers (A–H) from Shift Register

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	0	D11	D10	D9	D8	D7	D6	D5	D4	D3/0	D2/0	D1/0	D0/0

Table 6. Select Bits (M₇)

DATA	CONTROL BITS								DATA BITS							
DIN	1	0	0	0	X	X	X	X	MH	MG	MF	ME	MD	MC	MB	MA

X = Don't care.

Table 7. Select Bits Programming Example

DATA	CONTROL BITS								DATA BITS							
DIN	1	0	0	0	X	X	0	0	0	0	0	0	0	0	1	0

X = Don't care.

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Shutdown-Mode Bits (PD_0, PD_1)

Use the shutdown-mode bits and control bits to shut down each DAC independently. The shutdown-mode bits determine the output state of the selected channels. The shutdown-control bits put the selected channels into shutdown-mode. To select the shutdown mode for DACA–DACH, set PD_0 and PD_1 according to Table 8 (where “_” is replaced with one of the selected channels (A–H)). The three possible states for unity-gain versions are 1) normal operation, 2) shutdown with

1k Ω output impedance, and 3) shutdown with 100k Ω output impedance. The three possible states for force-sense versions are 1) normal operation, 2) shutdown with 1k Ω output impedance, and 3) shutdown with the output in a high-impedance state. Tables 9 and 10 show the commands for writing to the shutdown-mode bits. Table 11 shows the commands for writing the shutdown-control bits. This command is required to put the selected channels into shutdown.

Always write the shutdown-mode-bits command first and then write the shutdown-control-bits command to properly shut down the selected channels. The shutdown-control-bits command can be written at any time after the shutdown-mode-bits command. It does not have to immediately follow the shutdown-mode-bits command.

Settling-Time-Mode Bits (SPD_)

The settling-time-mode bits select the settling time (FAST mode or SLOW mode) of the MAX5590–MAX5595. Set SPD_ = 1 to select FAST mode or set SPD_ = 0 to select SLOW mode, where “_” is replaced by A, B, or C and so on through H, depending on the selected channel (Table 12). FAST mode provides a 3 μ s maximum settling time, and SLOW mode provides a 6 μ s maximum settling time.

Table 8. Shutdown-Mode Bits

PD_1	PD_0	DESCRIPTIONS
0	0	Shutdown with 1k Ω termination to ground on DAC_ output.
0	1	Shutdown with 100k Ω termination to ground on DAC_ output for unity-gain versions. Shutdown with high-impedance output for force-sense versions.
1	0	Ignored.
1	1	DAC_ is powered up in its normal operating mode.

Table 9. Shutdown-Mode Write Command (DACA–DACD)

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	0	0	0	0	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0

X = Don't care.

Table 10. Shutdown-Mode Write Command (DACE–DACH)

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	0	0	1	0	PDH1	PDH0	PDG1	PDG0	PDF1	PDF0	PDE1	PDE0

X = Don't care.

Table 11. Shutdown-Control-Bits Write Command

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	0	1	0	0	PDCH	PDCG	PCDF	PDCE	PDCE	PDCE	PDCE	PDCE

X = Don't care.

Table 12. Settling-Time-Mode Write Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	0	1	1	1	0	0	0	SPDH	SPDG	SPDF	SPDE	SPDD	SPDC	SPDB	SPDA

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Settling-Time-Mode Write Example:

To configure DACA and DACD into FAST mode and DACB and DACC into SLOW mode, use the command in Table 13.

To read back the settling-time-mode bits, use the command in Table 14.

CPOL and CPHA Control Bits

The CPOL and CPHA control bits of the MAX5590–MAX5595 are defined the same as the CPOL and CPHA bits in the SPI standard. Set the DAC's CPOL and CPHA bits to CPOL = 0 and CPHA = 0 or CPOL = 1 and CPHA = 1 for MICROWIRE and SPI applications requiring the clocking of data in on the ris-

ing edge of SCLK. Set the DAC's CPOL and CPHA bits to CPOL = 0 and CPHA = 1 or CPOL = 1 and CPHA = 0 for DSP and SPI applications, requiring the clocking of data in on the falling edge of SCLK (refer to the *Programmer's Handbook* and see Table 15 for details). At power-up, if $\overline{\text{DSP}} = \text{DV}_{\text{DD}}$, the default value of CPHA is zero and if $\overline{\text{DSP}} = \text{DGND}$, the default value of CPHA is one. The default value of CPOL is zero at power-up.

To write to the CPOL and CPHA bits, use the command in Table 16.

To read back the device's CPOL and CPHA bits, use the command in Table 17.

Table 13. Settling-Time-Mode Write Example

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	1	0	0	0	X	X	X	X	1	0	0	1

X = Don't care.

Table 14. Settling-Time-Mode Read Command

DATA	CONTROL BITS								DATA BITS							
DIN	1	0	1	1	1	0	0	1	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	SPDH	SPDG	SPDF	SPDE	SPDD	SPDC	SPDB	SPDA

X = Don't care.

Table 15. CPOL and CPHA Bits

CPOL	CPHA	DESCRIPTION
0	0	Default values at power-up when $\overline{\text{DSP}}$ is connected to DV_{DD} . Data is clocked in on the rising edge of SCLK.
0	1	Default values at power-up when $\overline{\text{DSP}}$ is connected to DGND. Data is clocked in on the falling edge of SCLK.
1	0	Data is clocked in on the falling edge of SCLK.
1	1	Data is clocked in on the rising edge of SCLK.

Table 16. CPOL and CPHA Write Command

DATA	CONTROL BITS				DATA BITS											
DIN	1	1	0	0	0	0	0	0	X	X	X	X	X	X	CPOL	CPHA

X = Don't care.

Table 17. CPOL and CPHA Read Command

DATA	CONTROL BITS				DATA BITS											
DIN	1	1	0	0	0	0	0	1	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPOL	CPHA

X = Don't care.

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UPIO Bits (UPSL1, UPSL2, UP0–UP3)

The MAX5590–MAX5595 provide two user-programmable input/output (UPIO) ports: UPIO1 and UPIO2. These ports have 15 possible configurations, as shown in Table 22. UPIO1 and UPIO2 can be programmed independently or simultaneously by writing to the UPSL1, UPSL2, and UP0–UP3 bits (Table 18).

Table 19 shows how UPIO1 and UPIO2 are selected for configuration. The UP0–UP3 bits select the desired functions for UPIO1 and/or UPIO2 (Table 22).

UPIO Programming Example:

To set only UPIO1 as LDAC and leave UPIO2 unchanged, use the command in Table 20.

The UPIO selection and configuration bits can be read back from the MAX5590–MAX5595 when UPIO1 or UPIO2 is configured as a DOUTRB output. Table 21 shows the read-back data format for the UPIO bits. Writing the command in Table 21 initiates a read operation of the UPIO bits. The data is clocked out starting on the ninth clock cycle of the sequence. Bits UP3-2 through UP0-2 provide the UP3–UP0 configuration bits for UPIO2 (Table 22), and bits UP3-1 through UP0-1 provide the UP3–UP0 configuration bits for UPIO1.

Table 18. UPIO Write Command

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	0	1	1	0	UPSL2	UPSL1	UP3	UP2	UP1	UP0	X	X

X = Don't care.

Table 19. UPIO Selection Bits (UPSL1 and UPSL2)

UPSL2	UPSL1	UPIO PORT SELECTED
0	0	None selected
0	1	UPIO1 selected
1	0	UPIO2 selected
1	1	Both UPIO1 and UPIO2 selected

Table 20. UPIO Programming Example

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	0	1	1	0	0	1	0	0	0	0	X	X

X = Don't care.

Table 21. UPIO Read Command

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	0	1	1	1	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	UP3-2	UP2-2	UP1-2	UP0-2	UP3-1	UP2-1	UP1-1	UP0-1

X = Don't care.

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UPIO Configuration

Table 22 lists the possible configurations for UPIO1 and UPIO2. UPIO1 and UPIO2 use the selected function when configured by the UP3–UP0 configuration bits.

LDAC

$\overline{\text{LDAC}}$ controls the loading of the DAC registers. When $\overline{\text{LDAC}}$ is high, the DAC registers are latched, and any change in the input registers does not affect the contents of the DAC registers or the DAC outputs. When $\overline{\text{LDAC}}$ is low, the DAC registers are transparent, and the values stored in the input registers are fed directly to the DAC registers, and the DAC outputs are updated.

Drive $\overline{\text{LDAC}}$ low to asynchronously load the DAC registers from their corresponding input registers (DACs that are in shutdown remain shut down). The $\overline{\text{LDAC}}$ input does not require any activity on $\overline{\text{CS}}$, SCLK, or DIN to take effect. If $\overline{\text{LDAC}}$ is brought low coincident with a rising edge of $\overline{\text{CS}}$ (which executes a serial command modifying the value of either DAC input register), then $\overline{\text{LDAC}}$ must remain asserted for at least 120ns following the $\overline{\text{CS}}$ rising edge. This requirement applies only for serial commands that modify the value of the DAC input registers. See Figures 5 and 6 for timing details.

Table 22. UPIO Configuration Register Bits (UP3–UP0)

UPIO CONFIGURATION BITS				FUNCTION	DESCRIPTION
UP3	UP2	UP1	UP0		
0	0	0	0	$\overline{\text{LDAC}}$	Active-Low Load DAC Input. Drive low to asynchronously load all DAC registers with data from input registers.
0	0	0	1	$\overline{\text{SET}}$	Active-Low Input. Drive low to set all input and DAC registers to full scale.
0	0	1	0	$\overline{\text{MID}}$	Active-Low Input. Drive low to set all input and DAC registers to midscale.
0	0	1	1	$\overline{\text{CLR}}$	Active-Low Input. Drive low to set all input and DAC registers to zero scale.
0	1	0	0	$\overline{\text{PDL}}$	Active-Low Power-Down Lockout Input. Drive low to disable software shutdown.
0	1	0	1	Reserved	This mode is reserved. Do not use.
0	1	1	0	$\overline{\text{SHDN1K}}$	Active-Low 1k Ω Shutdown Input. Overrides PD_1 and PD_0 settings. For the MAX5590/MAX5592/MAX5594, drive $\overline{\text{SHDN1K}}$ low to pull OUTA–OUTH to AGND with 1k Ω . For the MAX5591/MAX5593/MAX5595, drive $\overline{\text{SHDN1K}}$ low to leave OUTA–OUTH high impedance.
0	1	1	1	$\overline{\text{SHDN100K}}$	Active-Low 100k Ω Shutdown Input. Overrides PD_1 and PD_0 settings. For the MAX5590/MAX5592/MAX5594, drive $\overline{\text{SHDN100K}}$ low to pull OUTA–OUTH to AGND with 100k Ω . For the MAX5591/MAX5593/MAX5595, drive low to leave OUTA–OUTH high impedance.
1	0	0	0	DOUTRB	Data Read-Back Output
1	0	0	1	DOUTDC0	Mode 0 Daisy-Chain Data Output. Data is clocked out on the falling edge of
1	0	1	0	DOUTDC1	Mode 1 Daisy-Chain Data Output. Data is clocked out on the rising edge of SCLK.
1	0	1	1	GPI	General-Purpose Logic Input
1	1	0	0	GPOL	General-Purpose Logic-Low Output
1	1	0	1	GPOH	General-Purpose Logic-High Output
1	1	1	0	TOGG	Toggle Input. Toggles DAC outputs between data in input registers and data in DAC registers. Drive low to set all DAC outputs to values stored in input registers. Drive high to set all DAC outputs to values stored in DAC registers.
1	1	1	1	$\overline{\text{FAST}}$	Fast/Slow Settling-Time-Mode Input. Drive low to select FAST (3 μ s) mode or drive high to select SLOW (6 μ s) settling mode. Overrides the SPDA–SPDH settings.

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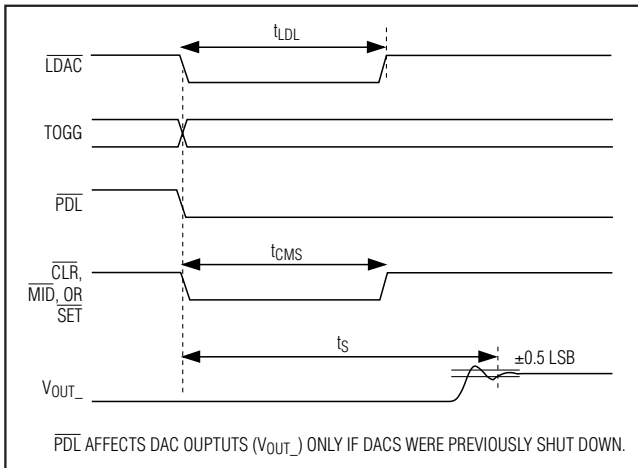


Figure 5. Asynchronous Signal Timing

SET, MID, CLR

The $\overline{\text{SET}}$, $\overline{\text{MID}}$, and $\overline{\text{CLR}}$ signals force the DAC outputs to full scale, midscale, or zero scale (Figure 5). These signals cannot be active at the same time.

The active-low $\overline{\text{SET}}$ input forces the DAC outputs to full scale when $\overline{\text{SET}}$ is low. When $\overline{\text{SET}}$ is high, the DAC outputs follow the data in the DAC registers.

The active-low $\overline{\text{MID}}$ input forces the DAC outputs to midscale when $\overline{\text{MID}}$ is low. When $\overline{\text{MID}}$ is high, the DAC outputs follow the data in the DAC registers.

The active-low $\overline{\text{CLR}}$ input forces the DAC outputs to zero scale when $\overline{\text{CLR}}$ is low. When $\overline{\text{CLR}}$ is high, the DAC outputs follow the data in the DAC registers.

If $\overline{\text{CLR}}$, $\overline{\text{MID}}$, or $\overline{\text{SET}}$ signals go low during a write command, reload the data to ensure accurate results.

Power-Down Lockout (PDL)

The $\overline{\text{PDL}}$ active-low, software-shutdown lockout input overrides (not overwrites) the PD_0 and PD_1 shutdown-mode bits. $\overline{\text{PDL}}$ cannot be active at the same time as $\overline{\text{SHDN1K}}$ or $\overline{\text{SHDN100K}}$ (see the *Shutdown Mode (SHDN1K, SHDN100K)* section).

If the PD_0 and PD_1 bits command the DAC to shut down prior to $\overline{\text{PDL}}$ going low, the DAC returns to shutdown mode immediately after $\overline{\text{PDL}}$ goes high, unless the PD_0 and PD_1 bits were modified through the serial interface in the meantime.

Shutdown Mode (SHDN1K, SHDN100K)

The $\overline{\text{SHDN1K}}$ and $\overline{\text{SHDN100K}}$ are active-low signals that override (not overwrite) the PD_1 and PD_0 bit settings. For the MAX5590/MAX5592/MAX5594, drive

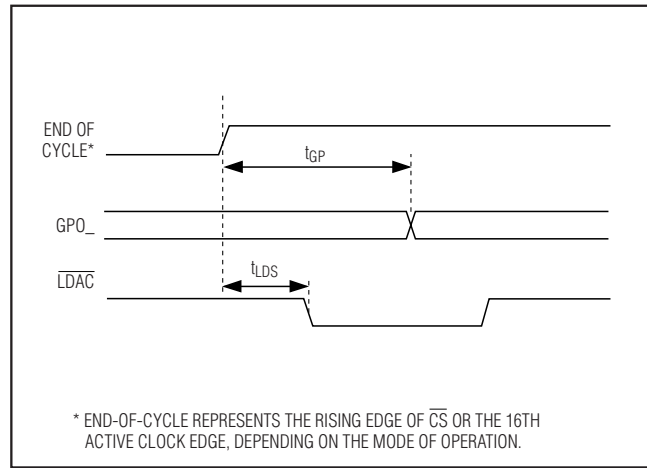


Figure 6. GPO_ and $\overline{\text{LDAC}}$ Signal Timing

$\overline{\text{SHDN1K}}$ low to select shutdown mode with OUTA–OUTH internally terminated with 1k Ω to ground, or drive $\overline{\text{SHDN100K}}$ low to select shutdown with an internal 100k Ω termination. For the MAX5591/MAX5593/MAX5595, drive $\overline{\text{SHDN1K}}$ low for shutdown with 1k Ω output termination, or drive $\overline{\text{SHDN100K}}$ low for shutdown with high-impedance outputs.

For proper shutdown, first select a shutdown mode (Table 8), then use the shutdown-control bits as listed in Table 2b.

Data Output (DOUTRB, DOUTDC0, DOUTDC1)

UPIO1 and UPIO2 can be configured as serial data outputs, DOUTRB (data out for read back), DOUTDC0 (data out for daisy-chaining, mode 0), and DOUTDC1 (data out for daisy-chaining, mode 1). The differences between DOUTRB and DOUTDC0 (or DOUTDC1) are as follows:

- The source of read-back data on DOUTRB is the DOUT register. Daisy-chain DOUTDC_ data comes directly from the shift register.
- Read-back data on DOUTRB is only present after a DAC read command. Daisy-chain data is present on DOUTDC_ for any DAC write after the first 16 bits are written.
- The DOUTRB idle state ($\overline{\text{CS}}$ = high) for read back is high impedance. Daisy-chain DOUTDC_ idles high when inactive to avoid floating the data input in the next device in the daisy-chain.

See Figures 1 and 2 for timing details.

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GPI, GPOL, GPOH

UPIO1 and UPIO2 can each be configured as a general-purpose input (GPI), a general-purpose output low (GPOL), or a general-purpose output high (GPOH).

The GPI can serve to detect interrupts from μ Ps or micro-controllers. The GPI has three functions:

- 1) Sample the signal at GPI at the time of the read (RTP1 and RTP2).
- 2) Detect whether or not a falling edge has occurred since the last read or reset (LF1 and LF2).
- 3) Detect whether or not a rising edge has occurred since the last read or reset (LR1 and LR2).

RTP1, LF1, and LR1 represent the data read from UPIO1; RTP2, LF2, and LR2 represent the data read from UPIO2.

To issue a read command for the UPIO configured as GPI, use the command in Table 23.

Once the command is issued, RTP1 and RTP2 provide the real-time status (0 or 1) of the inputs at UPIO1 or UPIO2, respectively, at the time of the read. If LF2 or LF1 is one, then a falling edge has occurred on the respective UPIO1 or UPIO2 input since the last read or reset. If LR2 or LR1 is one, then a rising edge has occurred since the last read or reset.

Table 23. GPI Read Command

DATA	CONTROL BITS				DATA BITS											
DIN	1	0	1	1	1	0	1	X	X	X	X	X	X	X	X	X
DOUTRB	X	X	X	X	X	X	X	X	X	X	RTP2	LF2	LR2	RTP1	LF1	LR1

X = Don't care.

Table 24. Unipolar Code Table (Gain = +1)

DAC CONTENTS			ANALOG OUTPUT
MSB	LSB		
1111	1111	1111	+VREF (4095 / 4096)
1000	0000	0001	+VREF (2049 / 4096)
1000	0000	0000	+VREF (2048 / 4096) = VREF / 2
0111	1111	1111	+VREF (2047 / 4096)
0000	0000	0001	+VREF (1 / 4096)
0000	0000	0000	0

GPOL outputs a constant low, and GPOH outputs a constant high. See Figure 6.

TOGG

Use the TOGG input to toggle the DAC outputs between the values in the input registers and DAC registers. A delay of greater than 100ns from the end of the previous write command is required before the TOGG signal can be correctly switched between the new value and the previously stored value. When TOGG = 0, the output follows the information in the input registers. When TOGG = 1, the output follows the information in the DAC register (Figure 5).

FAST

The MAX5590–MAX5595 have two settling-time-mode options: FAST (3 μ s max) and SLOW (6 μ s max). To select the FAST mode, drive $\overline{\text{FAST}}$ low, and to select SLOW mode, drive $\overline{\text{FAST}}$ high. This overrides (not overwrites) the SPDA–SPDH bit settings.

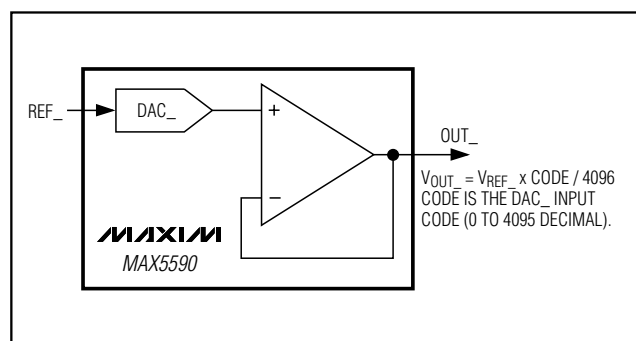


Figure 7. Unipolar Output Circuit

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Applications Information

Unipolar Output

Figure 7 shows the unity-gain MAX5590 in a unipolar output configuration. Table 24 lists the unipolar output codes.

Bipolar Output

The MAX5590 outputs can be configured for bipolar operation, as shown in Figure 8. The output voltage is given by the following equation:

$$V_{OUT_} = V_{REF} \times (\text{CODE} - 2048) / 2048$$

where CODE represents the numeric value of the DAC's binary input code (0 to 4095 decimal). Table 25 shows digital codes and the corresponding output voltage for the Figure 8 circuit.

Configurable Output Gain

The MAX5591/MAX5593/MAX5595 have force-sense outputs, which provide a direct connection to the inverting terminal of the output op amp, yielding the most flexibility. The force-sense output has the advantage that specific gains can be set externally for a given application. The gain error for the MAX5591/MAX5593/MAX5595 is specified in a unity-gain configuration (op-amp output and inverting terminals connected), and additional gain error results from external resistor tolerances. The force-sense DACs allow many useful circuits to be created with only a few simple external components.

An example of a custom, fixed gain using the MAX5591's force-sense output is shown in Figure 9. In this example, the external reference is set to 1.25V, and the gain is set to +1.1V/V with external discrete resistors to provide an approximate 0 to 1.375V DAC output voltage range.

$$V_{OUT} = [(0.5 \times V_{REF_} \times \text{CODE}) / 4096] \times [1 + (R_2 / R_1)]$$

where CODE represents the numeric value of the DAC's binary input code (0 to 4095 decimal).

In this example, $R_2 = 12\text{k}\Omega$ and $R_1 = 10\text{k}\Omega$ to set the gain = 1.1V/V.

$$V_{OUT} = [(0.5 \times 1.25\text{V} \times \text{CODE}) / 4096] \times 2.2$$

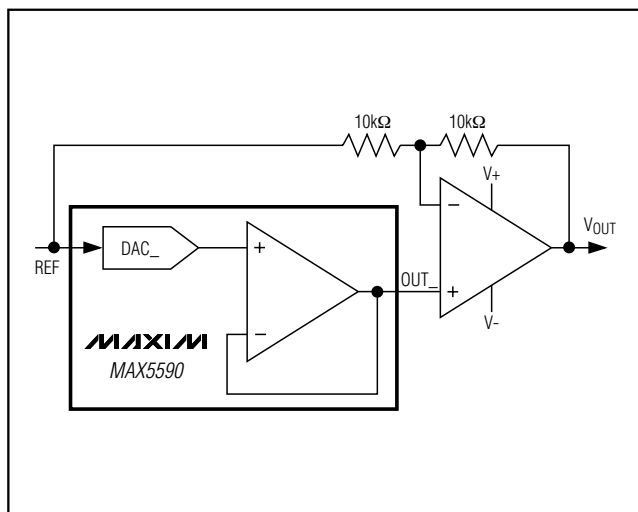


Figure 8. Bipolar Output Circuit

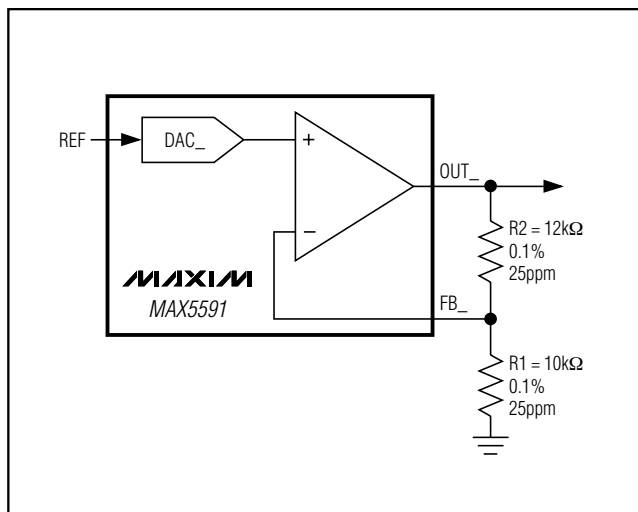


Figure 9. Configurable Output Gain

Table 25. Bipolar Code Table (Gain = +1)

DAC CONTENTS			ANALOG OUTPUT
MSB	LSB		
1111	1111	1111	+V _{REF} (2047 / 2048)
1000	0000	0001	+V _{REF} (1 / 2048)
1000	0000	0000	0
0111	1111	1111	-V _{REF} (1 / 2048)
0000	0000	0001	-V _{REF} (2047 / 2048)
0000	0000	0000	-V _{REF} (2048 / 2048) = -V _{REF}

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Power-Supply and Layout Considerations

Bypass the analog and digital power supplies by using a 10 μ F capacitor in parallel with a 0.1 μ F capacitor to AGND and DGND (Figure 10). Minimize lead lengths to reduce lead inductance. Use shielding and/or ferrite beads to further increase isolation.

Digital and AC transient signals coupling to AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-

inductance ground plane. Wire-wrapped boards and sockets are not recommended. For optimum system performance, use PC boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance power-supply source.

Using separate power supplies for AVDD and DVDD improves noise immunity. Connect AGND and DGND at the low-impedance power-supply sources (Figure 11).

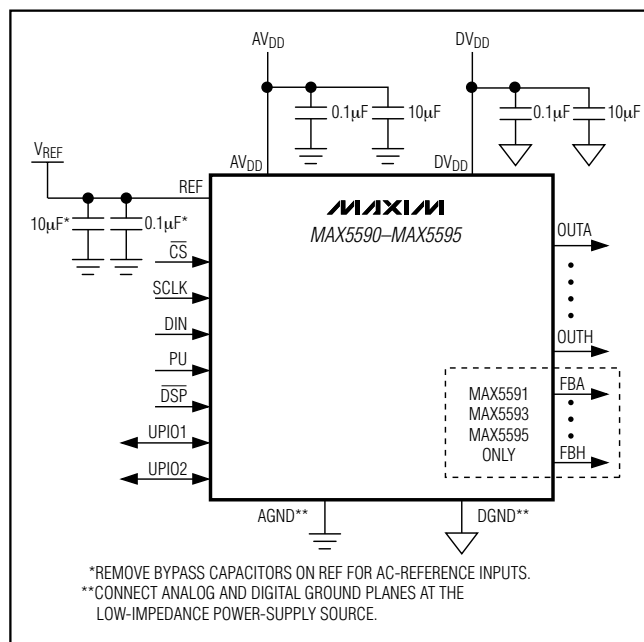


Figure 10. Bypassing Power Supplies AVDD, DVDD, and REF

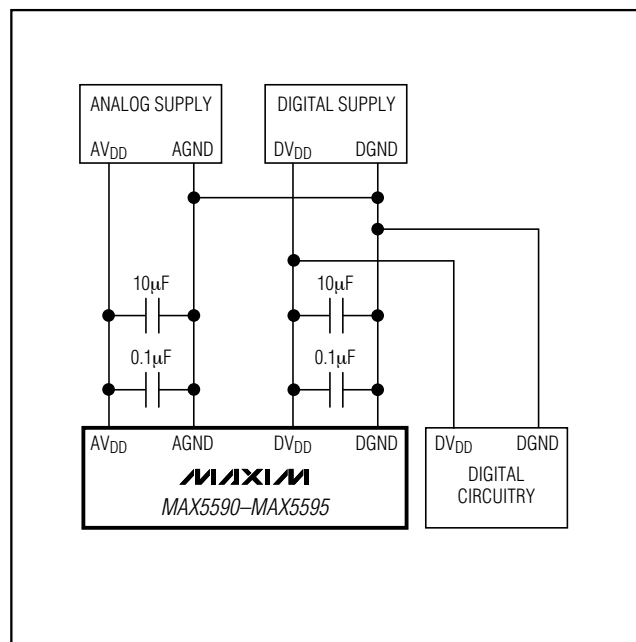
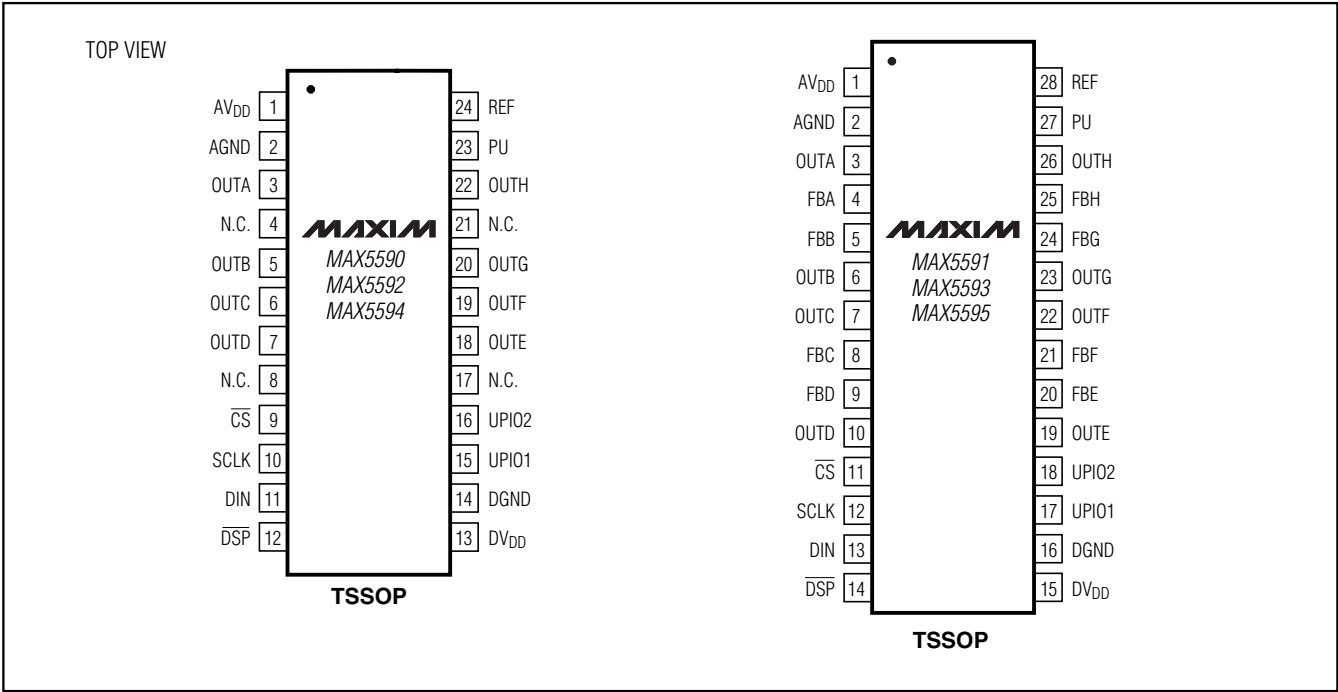


Figure 11. Separate Analog and Digital Power Supplies

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Pin Configurations



Selector Guide

PART	OUTPUT BUFFER CONFIGURATION	RESOLUTION (BITS)	INL (LSBs MAX)
MAX5590AEUG*	Unity Gain	12	±1
MAX5590BEUG	Unity Gain	12	±4
MAX5591AEUI*	Force Sense	12	±1
MAX5591BEUI	Force Sense	12	±4
MAX5592EUG	Unity Gain	10	±1
MAX5593EUI	Force Sense	10	±1
MAX5594EUG	Unity Gain	8	±0.5
MAX5595EUI	Force Sense	8	±0.5

*Future product. Contact factory for availability. Specifications are preliminary.

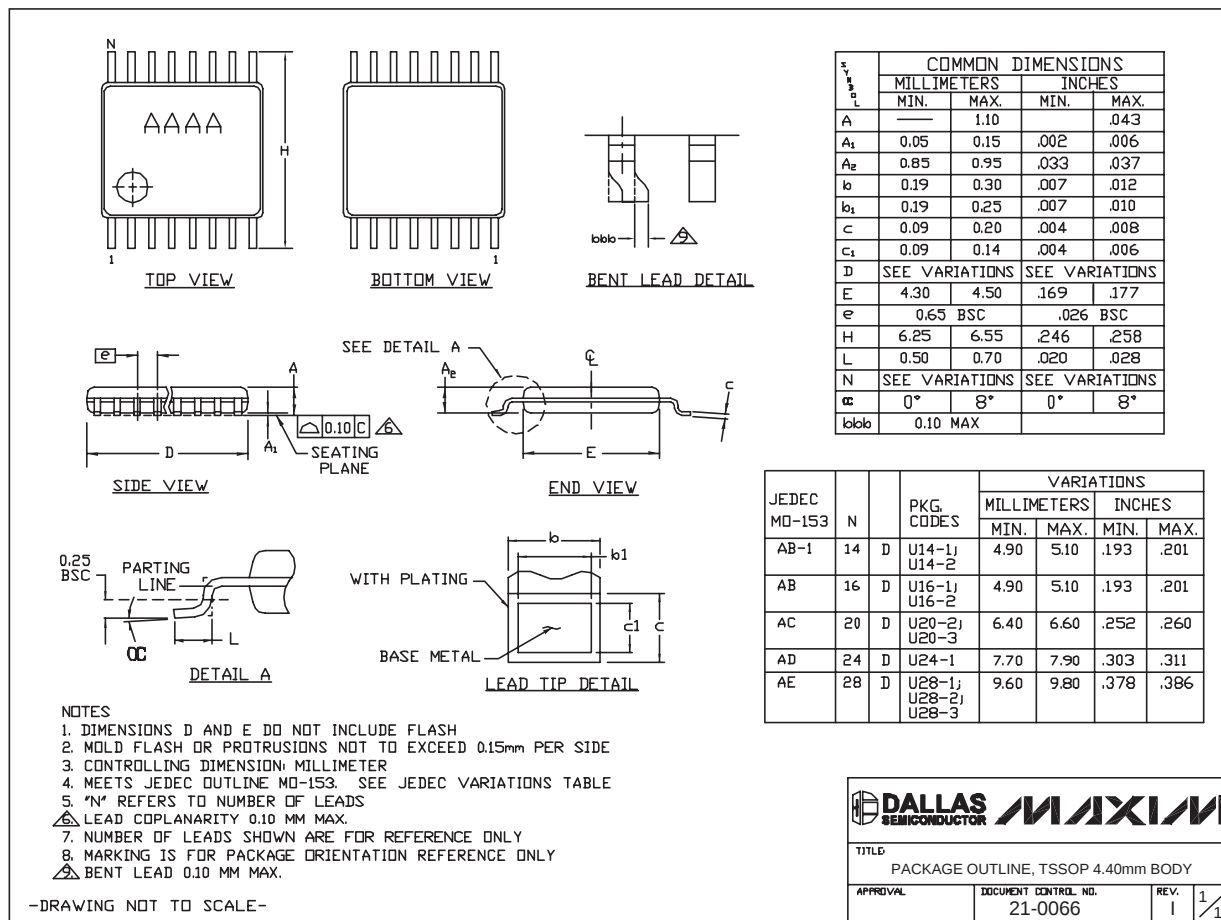
Chip Information

TRANSISTOR COUNT: 38,513
PROCESS: BiCMOS

Buffered, Fast-Settling, Octal, 12/10/8-Bit, Voltage-Output DACs

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



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MAX5590-MAX5595

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