SC1470
SYNCHRONOUS BUCK POWER SUPPLY CONTROLLER

Description

The SC1470 is a single output, constant on-time synchronous-buck, pseudo fixed frequency, PWM controller intended for use in notebook computers and other battery operated portable devices. Features include high efficiency and fast dynamic response with no minimum on time. The excellent transient response means that SC1470 based solutions will require less output capacitance than competing fixed frequency converters.

The frequency is constant until a step in load or line voltage occurs, at which time the pulse density and frequency will increase or decrease to counter the change in output or input voltage. After the transient event, the controller frequency will return to steady state operation. At light loads, Power-Save Mode enables the SC1470 to skip PWM pulses for better efficiency.

The output voltage can be adjusted from 0.5V to VCCA. The integrated gate drivers feature adaptive shoot-through protection and soft switching. Additional features include cycle-by-cycle current limit, digital soft-start, over-voltage and under-voltage protection, and a PGOOD output.

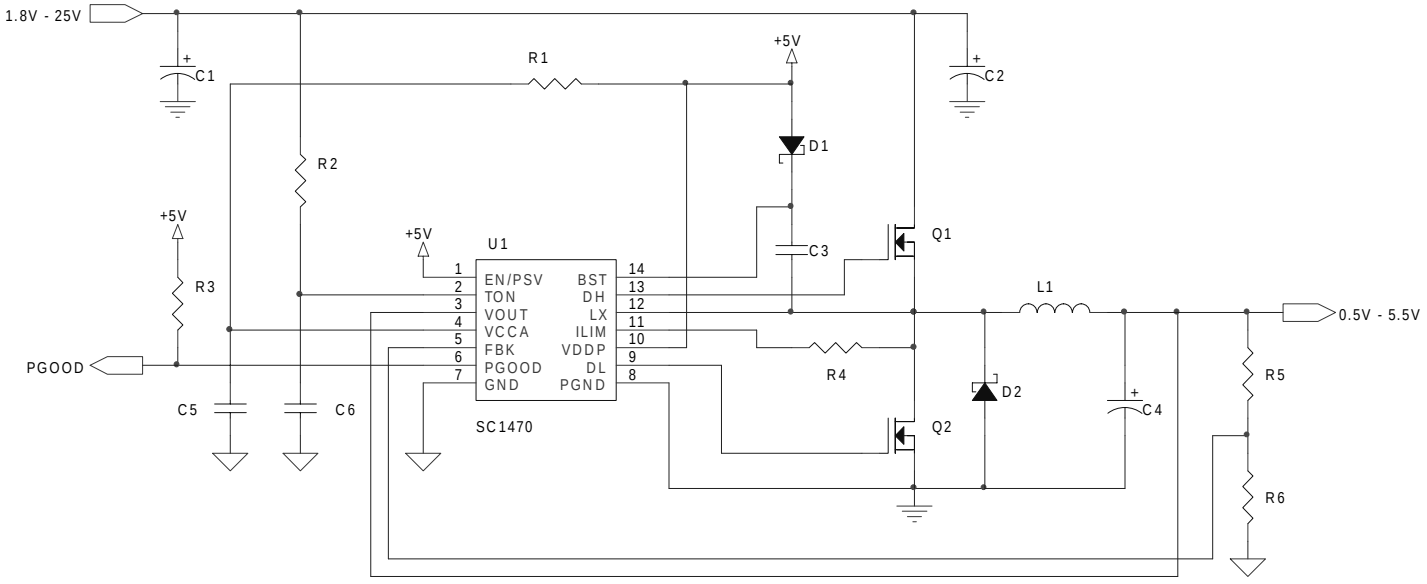
Features

- Constant On-Time for Fast Dynamic Response
- Programmable VOUT Range = 0.5 – VCCA
- VIN Range = 1.8V – 25V
- DC Current Sense Using Low-Side RDS(ON) Sensing or RSENSE in Source of Low-Side MOSFET for Greater Accuracy
- Resistor Programmable Frequency
- Cycle-by-Cycle Current Limit
- Digital Soft-Start
- Combined EN and PSAVE Functions
- Over-Voltage/Under-Voltage Fault Protection and PGOOD Output
- 5uA Typical Shutdown Current
- Low Quiescent Power Dissipation
- 14 Lead TSSOP
- Industrial Temperature Range
- 1% Internal Reference
- Integrated Gate Drivers with Soft Switching
- Efficiency > 90%

Applications

- Notebook Computers
- CPU I/O Supplies
- Handheld Terminals and PDAs
- LCD monitors
- Network power supplies

Typical Application Circuit



Absolute Maximum Ratings

Pin Combination	Absolute Maximum Ratings
TON to AGND	-0.3V to +25.0V
DH,BST to AGND	-0.3V to +30.0V
LX to AGND	-2.0V to +25.0V
AGND to PGND	-0.3V to +0.3V
BST to LX	-0.3V to +6.0V
VCCA, VDDP to AGND	-0.3V to +6.0V
FB, PGOOD, EN/PSV, ILIM, VOUT, DL to PGND	-0.3V to +6.0V
θ_{JA}	100 °C/W
Junction Temperature	+150 °C

Electrical Characteristics

Test Conditions: V_{IN} = 15V, EN/PSV = 5V, VCCA = VDDP = 5.0V, V_{OUT} = 1.8V, R_{TON} = 1M (300KHz), 0.1% Resistor Dividers

Parameter	Conditions	25C			-40C to 85C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA Input Voltage			5.0		4.5	5.5	V
VDDP Input Voltage			5.0		4.5	5.5	V
VIN Input Voltage	Vin = 1.8V - 25V Offtime > 800ns	1.8		25			V
VDDP Operating Current	FB > regulation point, ILOAD = 0A		1			5	uA
VCCA Operating Current	FB > regulation point, ILOAD = 0A		700			1100	uA
TON Operating Current	R_{TON} = 1M (300KHz)		15				uA
Shutdown Current	EN/PSV = 0V		-5			-10	uA
	VCCA		5			10	uA
	VDDP + VIN		0			1	uA
Controller							
Error Comparator Threshold (FBK Turn-on Threshold) (Note 1)	VCCA = 4.5V to 5.5V		0.500		0.495	0.505	V
Output Voltage Range	Adjust Mode				0.5	VCCA	V

Electrical Characteristics Cont.

Parameter	Conditions	25C			-40C to 85C		Units
		Min	Typ	Max	Min	Max	
On-Time	R_{TON} = 1M (300KHz) Vo = 5V		1140		969	1311	nS
	R_{TON} = 500K (600KHz) Vo = 5V		630		536	725	nS
Minimum Off Time			400			500	nS
Line Regulation Error	VCCA, VDDP = 4.5V to 5.5V Vin = 4.5V to 25V		0.04				%/V
Load Regulation Error	ILIM - PGND = 0V to OC Limit EN/PSV = Open		0.3				%
VOUT Input Resistance			500				K Ohm
FB Input Bias Current					-1.0	+1.0	uA
Over-Current Sensing							
ILIM Sink Current	DL High		10		9.0	11.0	uA
Current Comparator Offset	PGND - ILIM				-5	5	mV
PSAVE							
Zero-Crossing Threshold	PGND - LX EN/PSV = 5V		5				mV
Fault Protection							
Current Limit (Positive) (Note 2)	PGND-LX, R_{ILIM} = 5K		50		40	60	mV
	PGND-LX, R_{ILIM} = 10K		100		90	110	mV
	PGND-LX, R_{ILIM} = 20K		200		180	220	mV
Current Limit (Negative)	PGND-LX		-140		-200	-100	mV
Output Under-Voltage Fault	With respect to internal reference.		-30		-40	-25	%
Output Over-Voltage Fault	With respect to internal reference.		+10		+8	+12	%
Over-Voltage Fault Delay	FB forced above OV Vth		2.0				uS
PGOOD Low Output Voltage	Sink 1mA					0.4	V
PGOOD Leakage Current	FB in regulation, PGOOD = 5V					1	uA
PGOOD UV Threshold	With respect to internal reference.		-10		-12	-8	%

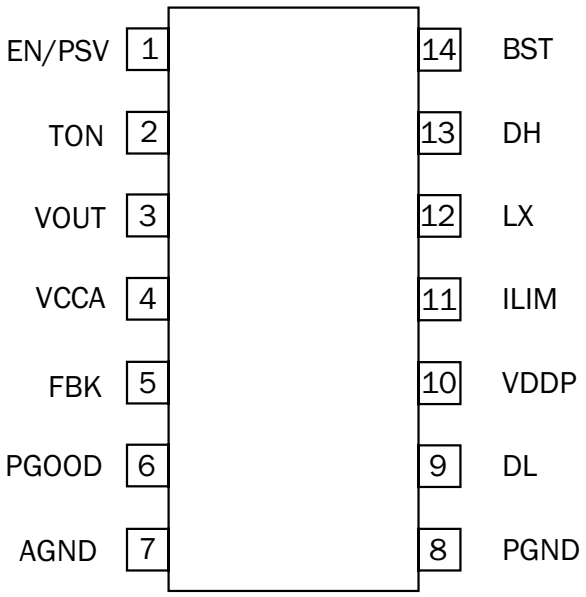
Electrical Characteristics Cont.

Parameter	Conditions	25C			-40C to 85C		Units
		Min	Typ	Max	Min	Max	
PGOOD Fault Delay	FB forced outside PGOOD window.		2.0				uS
VCCA Undervoltage Threshold	Rising Edge Hysteresis 100mv		4.0		3.7	4.3	V
Over Temperature Lockout	10°C Hysteresis		165				C
Inputs/Outputs							
Logic Input Low Voltage	EN/PSV low					1.2	V
Logic Input High Voltage	EN High, PSV low (Pin Floating)		2.0		1.2	2.4	V
Logic Input High Voltage	EN/PSV high				2.4		V
Enable/Psave Input Resistance	R Pullup to VCCA		1.5				Meg Ohm
	R Pulldown to AGND		1				Meg Ohm
Soft Start							
Soft-Start Ramp Time	EN/PSV high to full current limit.		1.6				mS
Under-Voltage Blank Time	SMPS Turn-On		2				mS
Gate Drivers							
Dead Time	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ohm
DL Pull-Up Resistance	DL high		2			4	Ohm
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ohm
DH Pull-Up Resistance	DH high, BST - LX = 5V		2			4	Ohm
DL Sink Current	DL - PGND = 2.5V		2				A
DL Source Current	VDDP - DL = 2.5V		1				A
DH Sink Current	DH - LX = 2.5V, BST - LX = 5V		1				A
DH Source Current	BST - DH = 2.5V, BST - LX = 5V		1				A

Note 1: When the inductor is in continuous and discontinuous conduction mode, the output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.
Note 2: Using a current sense resistor, this measurement relates to PGND minus the voltage of the source on the low-side MOSFET.
Note 3: This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configuration

Top View



TSSOP-14

Ordering Information

DEVICE (1)	PACKAGE	OPERATING TEMPERATURE
SC1470ITSTR	TSSOP-14	-40°C to 85°C
SC1470EVB	EVALUATION BOARD	-40°C to 85°C

Notes:
1. Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	EN/PSV	Enable/Power Save input . Tie to ground to disable SMPS. Tie to +5V to enable SMPS and activate PSAVE mode. Float to enable SMPS and activate continous conduction mode.
2	TON	On-time set input. Sets on-time of upper MOSFET via series resistor to the input supply.
3	VOUT	Output voltage sense input. Connect to the output of the SMPS.
4	VCCA	Supply voltage input for the analog supply. Connect through an RC filter to +5V.
5	FBK	Feedback input. Connect from a resistor divider at output of the SMPS to select output voltage.
6	PGOOD	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay following power up.
7	AGND	Analog ground.
8	PGND	Power ground.
9	DL	Gate drive output for the low side MOSFET switch.
10	VDDP	+5V supply voltage input for the gate drivers.
11	ILIM	Current limit input. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor. See applications section for more information.
12	LX	Switching node inductor connection.
13	DH	Gate drive output for the high side MOSFET switch.
14	BST	Boost capacitor connection for the high side gate drive.

Block Diagram

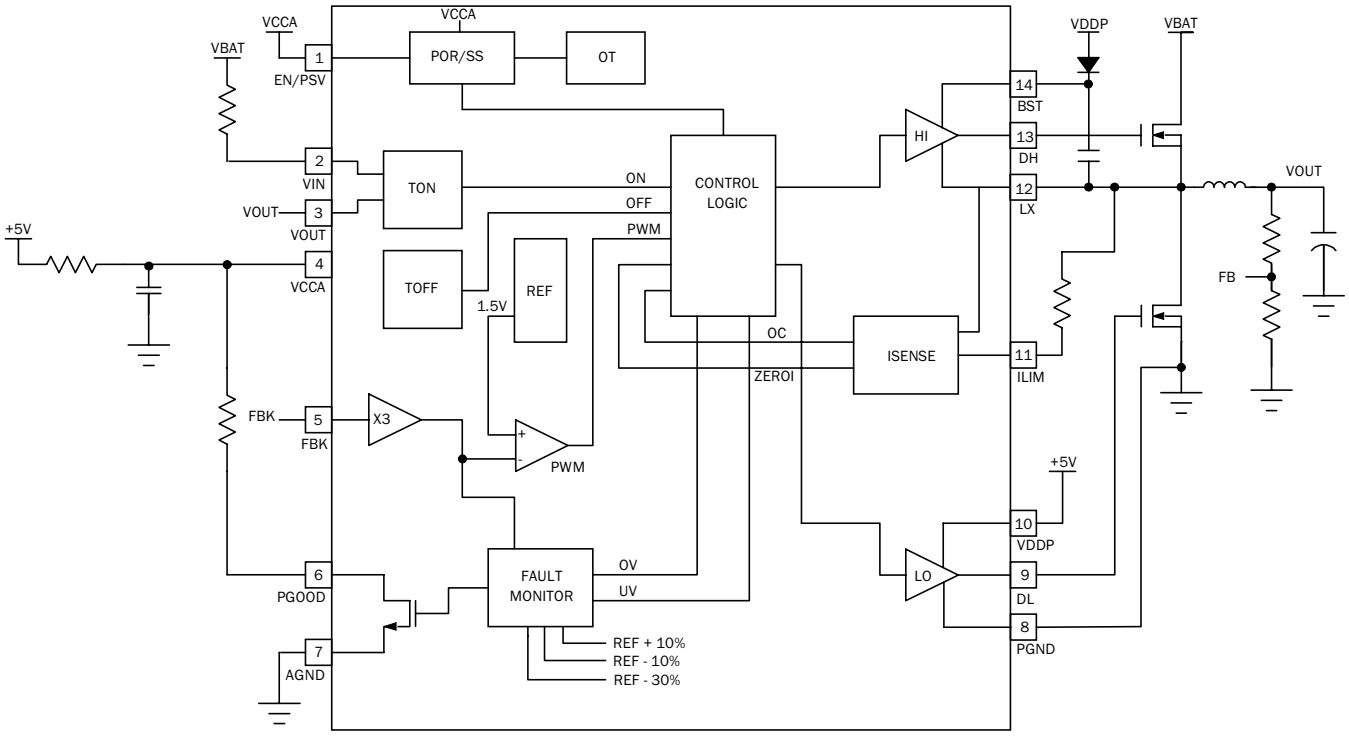


FIGURE 1

Applications Information

+5V Bias Supply

The SC1470 requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator such as the Semtech LP2951A. There are two inputs for the external +5V bias supply, VCCA & VDDP. The VCCA input powers the analog section of the SC1470 while the VDDP input provides power to the upper and lower gate drivers. VCCA will need to be decoupled from the VDDP supply through a 10 ohm resistor and the addition of a filter capacitor from VCCA to ground. The battery input VIN and the +5V inputs VCCA & VDDP can be tied together if the input voltage is fixed from +4.5V to +5.5V; however, as before, VCCA will need to be decoupled from the VDDP supply through a 10 ohm resistor and the addition of a filter capacitor from VCCA to ground.

Pseudo Fixed Frequency Constant On-Time PWM Controller

The PWM control architecture consists of a constant-on-time, pseudo fixed frequency PWM controller, (Figure 1). The output ripple voltage developed across the output filter capacitors ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time to 400ns typically.

On-Time One-Shot (T_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input proportional current is used to charge an internal on-time capacitor. The TON time is the time required for the voltage on the capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need of a clock generator.

$$T_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) + 50nS$$

R_{TON} is a resistor connected from the input supply to the TON pin. The graph on page 16 shows the relationship between R_{TON} and switching frequency.

Enable & Psave

The SC1470 combines the ENABLE and PSAVE functions into a single pin. When the pin is tied to ground the SMPS is disabled. When it is tied to +5V the SMPS is enabled and PSAVE is active. In order to enter PSAVE, the SC1470 PSAVE comparator will look for 8 consecutive inductor current reversals. When this happens, the controller will switch into PSAVE mode. At the same time, the SC1470 will increase the on-time by 1.5 times its set value. This will increase the ripple current and ripple voltage by 1.5 times their continuous conduction mode (CCM) values. This increase has two benefits. First, the reduction in switching frequency will improve efficiency. Second, hysteresis is added to the PSAVE circuit. This is important because when in PSAVE, the very first time a current reversal does not occur, the SC1470 will exit the PSAVE mode. This allows the device to rapidly respond to transient load conditions, while adding hysteresis to eliminate false PSAVE exits.

When the pin is left floating, the pin is internally pulled to 2V, enabling the SMPS in CCM.

Output Voltage Selection

Output voltage selection is set by the feedback resistors R2 & R3 of Figure 3. The internal reference is 1.5V, and the external feedback pin is multiplied by 3 to match the 1.5V reference. Therefore the output can be selected to a minimum of 0.5V. The equation for selecting the output voltage based on Figure 3 is:

$$Vout = \left(1 + \frac{R2}{R3}\right) \bullet 0.5$$

Current Limit Circuit

Current limiting of the SC1470 can be accomplished in two ways. First, the device can implement on-state resistance of the low-side MOSFET as the current sensing element (RDS_{ON} sensing). Second, the device can accept a resistive element in the low-side source ($R_{SENSE,}$ resistor sensing). The second method offers greater accuracy of the current limit threshold over RDS_{ON} sensing, at the added expense of a sense resistor and associated efficiency loss.

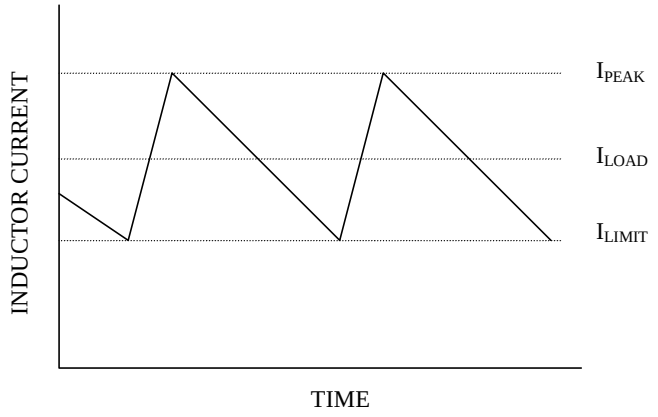
Whether RDS_{ON} sensing or R_{SENSE} resistor sensing is used, a scaling resistor between LX and ILIM is required. This

Applications Information Cont.

resistor, R_{ILIM}, is connected to a 10uA current source within the SC1470 through the ILIM pin. This sets a voltage drop equal to 10uA times R_{ILIM}. As the current increases through the lower MOSFET, the phase pin voltage will decrease until the offset voltage caused by R_{ILIM} is reached and ILIM < PGND. At this point an over-current trip signal is issued. Current limiting will prevent the firing of a DH on-pulse, thereby reducing the switching frequency. As the frequency decreases, the output voltage will drop until an under-voltage shutdown is reached. The current sensing circuit actually limits the inductor valley current (see Figure 2). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:

$$IL_{OC}(Valley) = 10\mu A \bullet \frac{R_{ILIM}}{RDS_{ON}}$$

$$IL_{OC}(Average) = IL_{OC}(Valley) + \frac{\Delta I_L}{2}$$



Valley Current-Limit Threshold Point

FIGURE 2

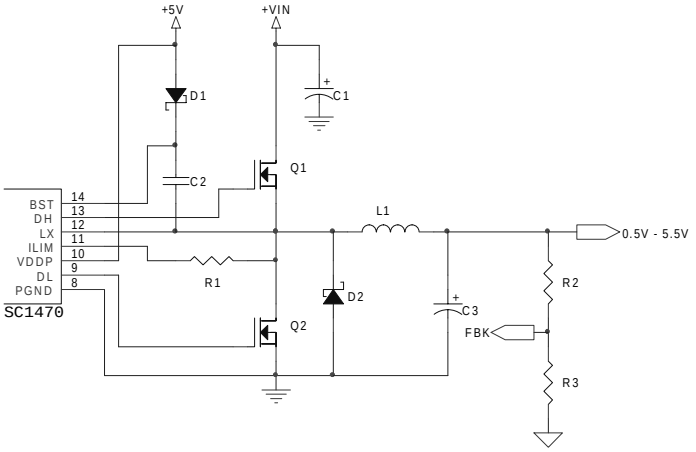


FIGURE 3

The schematic of RDS_{ON} sensing circuit is shown in Figure 3 with R_{ILIM} = R1 and RDS_{ON} of Q2.

Similarly, for resistor sensing, the current through the lower MOSFET and the source sense resistor develops a voltage that opposes the voltage developed across $R_{ILIM.}$ When the voltage developed across the R_{SENSE} resistor reaches voltage drop across $R_{ILIM,}$ an over-current will be issued. The over-current equation when using an external sense resistor is:

$$IL_{OC}(Valley) = 10\mu A \bullet \frac{R_{ILIM}}{R_{SENSE}}$$

Schematic of resistor sensing circuit is shown in Figure 4 with R_{ILIM} = R1 and R_{SENSE} = R4.

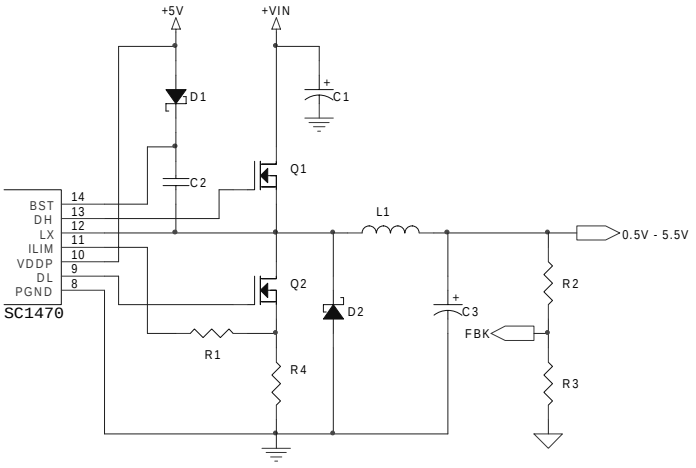


FIGURE 4

Applications Information

Power Good Output

Power good is an open-drain output and requires a pull-up resistor. When the output voltage is 10% above or below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within 10% of the output set voltage. PGOOD is also held low during start-up and will not be allowed to transition high until the output reaches 90% of its set voltage. There is a slight delay built into the PGOOD circuit to prevent false transitions.

Output Overvoltage Protection

When the output exceeds 10% of the its set voltage the low-side MOSFET is latched on. It stays latched and the SMPS is off until the enable input or POR is toggled. There is a slight delay built into the OV protection circuit to prevent false transitions.

Output Undervoltage Protection

When the output is 30% below its set voltage the output is latched in a tristated condition, and the SMPS is off until the enable input or POR is toggled. There is a slight delay built into the UV protection circuit to prevent false transitions.

POR, UVLO and Softstart

An internal power-on reset (POR) occurs when VCCA exceeds 3V, resetting the fault latch and soft-start counter, and preparing the PWM for switching. VCCA undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver high until VCCA rises above 4.1V. At this time the circuit will come out of UVLO and begin switching, and the softstart circuit being enabled, will progressively limit the output current over a predetermined time period. The ramp occurs in four steps: 25%, 50%, 75% and 100%, thereby limiting the slew rate of the output voltage. There is 100mV of hysteresis built into the UVLO circuit and when the VCCA falls to 4.0V the output drivers are shutdown and tristated.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on, until DL is fully off, and conversely, monitors the DH output and prevents the low-side MOSFET from turning on until DH is fully off. Be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

The high-side gate driver is equipped with turn-on soft switching to reduce gate drive power dissipation. When a DH turn-on is initiated the pull-up resistance is 10 ohms. This limits the peak high-side gate current before the MOSFET is conducting current. The peak gate current plays a large role in gate driver switching losses. When the high-side MOSFET begins conducting, and LX starts to rise, the pull-up resistance on DH changes to 2 ohms.

Design Procedure

Prior to any design of a switch mode power supply (SMPS) for notebook computers, determination of input voltage, load current, switching frequency and inductor ripple current must be specified.

Input Voltage Range

The maximum input voltage (VIN_{MAX}) is determined by the highest AC adaptor voltage. The minimum input voltage (VIN_{MIN}) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches.

Maximum Load Current

There are two values of load current to consider. Continuous load current and peak load current. Continuous load current has more to do with thermal stresses and therefore drives the selection of input capacitors, MOSFETs and commutation diodes. Whereas, peak load current determines instantaneous component stresses and filtering requirements such as, inductor saturation, output capacitors and design of the current limit circuit.

Switching Frequency

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up.

Inductor Ripple Current

Low inductor values create higher ripple current, resulting in smaller size, but are less efficient because of the high AC currents flowing through the inductor. Higher inductor values do reduce the ripple current and are more efficient, but are larger and more costly. The selection of the ripple current is based on the maximum output current and tends to be between 20% to 50% of the maximum load current. Again, cost, size and efficiency all play a part in the selection process.

Applications Information Cont.

Design Example

The following design example is for the evaluation board schematic shown on page 18. This design will have an input voltage from 4.5V to 19V with an output voltage of 2.5V at 6A.

Inductor Selection

The switching frequency is set to 300KHz which yields a good trade-off of size and efficiency. Using table one R_{TON} is chosen to be 1M Ohm for a switching frequency of 300KHz. Because ripple voltage is used as the feedback mechanism of this device, this leads to the choice of the ripple current being 30% of load current. This will give an nice ripple voltage waveform for ensuring proper PWM triggering for this type of controller.

$$\Delta IL = 0.3 \bullet 6 = 1.8A$$

$$L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT}) \bullet T}{V_{IN} - \Delta I_L}$$

$$L = 4\mu H$$

Setting the Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current. The valley of the inductor current occurs at:

$$ILoad(Max) - \frac{\Delta IL}{2}$$,(see Figure 2) therefore:

$$ILIM(Low) > ILoad(Max) - \frac{\Delta IL}{2}$$

The inductor must not saturate under all conditions of operation. If the current limit is set to 8.5A the maximum current through the inductor will be:

$$8.5 + \Delta IL = 10.3A$$

Setting the over current to 8.5A is calculated as follows:

$$RILIM = \frac{RDS_{ON} \bullet ILOC}{10\mu A}$$

RDSON of the MOSFET is a nominal 0.01 ohms, accounting for increased temperature effects use 0.012 ohm.

$$RILIM = \frac{0.012 \bullet 8.5}{10\mu A} = 10K$$

The inductor chosen was a Panasonic 4uH, 11A inductor.

Similarly, using a Sense resistor to obtain a more accurate current limit would make use of the valley current equation. Thus, for a 0.012 Ohm resistor the RILIM would calculate to the same 10K ohm ILIM resistor. However, the power rating of the sense resistor will be $6 \bullet 6 \bullet 0.012 = 0.432\,W$ effecting the efficiency budget.

Output Capacitor Selection

The output filter capacitor must have low effective series resistance (ESR) to meet the output ripple and load transient requirements, at the same time have high enough ESR to satisfy stability requirements. In addition, the value of output capacitance must be high enough to absorb the inductor energy going from full-load to no-load without tripping the overvoltage protection circuit. For CPU load transients, how much ESR needed depends upon output voltage variation limits under a CPU load transient. The ESR for this condition is given:

$$ESR = \frac{\Delta V_{OUT}}{I_{LOAD(MAX)}}$$

In non CPU applications, the output capacitor size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple. Under these conditions the ESR value is given:

$$ESR = \frac{\Delta V_{OUT(p-p)}}{I_{LOAD(MAX)}}$$

However, for most CPU applications the minimum capacitance required is limited by the energy absorption of the output capacitor. The equation for determining the minimum capacitance can be found by the following equation:

$$C_{MIN} = \frac{L_{OUT} \bullet I_{OUT}^2}{V_F^2 - V_I^2}$$

Where V_F is the final output voltage after release of the load and V_I is the initial voltage prior to the release of load. If no more than 100mV of output voltage variation is required between V_F and V_I, plugging in the numbers for the application circuit yields minimum output capacitance of 1400uF. As shown, a large amount of capacitance is required to absorb the energy of the inductor during a load release of 6A. In typical DDR memory applications a load release of this magnitude is not an issue and therefore the application circuit can get by with 300uF of output capacitance.

Applications Information Cont.

Stability Considerations:

Unstable operation shows up in two related but distinctly different ways: double pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is too low, causing not enough voltage ramp in the output signal. This causes the error amplifier to trigger prematurely after the 400ns minimum off-time has expired. Double-pulsing will result in higher ripple voltage at the output, but in most cases is harmless. However, in some cases double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR. One simple way to solve this problem is to add some trace resistance in the high current output path. A side effect of doing this is output voltage droop with load. Another way to eliminate doubling-pulsing is to add a capacitor across the upper feedback resistor divider network. This is shown below in Figure 5, by capacitor C4 in the schematic. This capacitance should be left out until confirmation that double-pulsing exists. Adding this capacitance will add a zero in the transfer function and should eliminate the problem. It is best to leave a spot on the PCB in case it is needed.

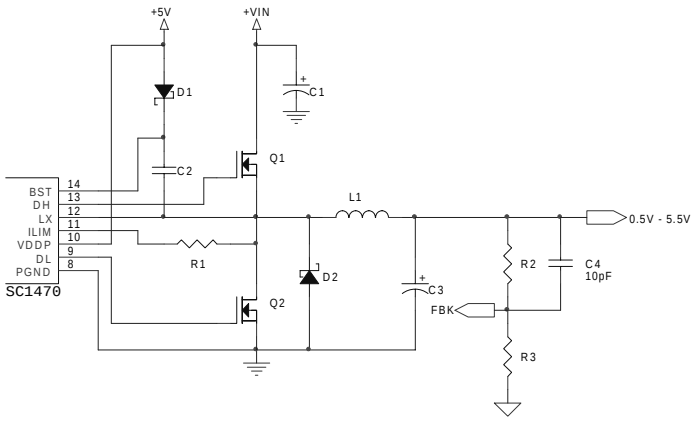


FIGURE 5

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The best way for checking stability is to apply a zero to full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is sign that the ESR should be increased.

SC1470 ESR Requirements

Constant on-time control used in the SC1470 regulates the ripple voltage at the output capacitor. This signal consists of a term generated by the output ESR of the capacitor and a term based on the increase in voltage across the capacitor due to charging and discharging during the switching cycle. The minimum ESR is set to generate the required ripple voltage for regulation. For most applications the minimum ESR ripple voltage is dominated by PCB layout and the properties of SP or POSCAP type output capacitors. For applications using ceramic output capacitors the absolute minimum ESR must be considered. Existing literature describing the ESR requirements to prevent double pulsing does not accurately predict the performance of constant on-time controllers. A time domain model of the converter was developed to generate equations for the minimum ESR empirically. If the ESR is low enough the ripple voltage is dominated by the charging of the output capacitor. This ripple voltage lags the on-time due to the LC poles and can cause double pulsing if the phase delay exceeds the off-time of the converter. Referring to Figure 5, the equation for the minimum ESR as a function of output capacitance, switching frequency and duty cycle is;

$$ESR > \left(\frac{R2+R3}{R3}\right) \bullet \left(\frac{1+3\bullet\left(\frac{Fs-200000}{Fs}\right)}{2\bullet\pi\bullet Cout\bullet Fs\bullet(1-D)^2}\right)$$

Where D = Vout/Vin. Plugging in the numbers for this design ESR > 0.023 ohms. With the capacitors chosen the total ESR of 0.025 ohms plus the board trace resistance meet the requirement.

Input Capacitor Selection

Input capacitors are selected based upon the input ripple current demand of the converter. First determine the input ripple current expected and then choose a capacitor to meet that demand.

The input RMS ripple current can be calculated as follows:

$$I_{RMS} = \sqrt{V_{OUT} \bullet (V_{IN} - V_{OUT})} \bullet \frac{I_{OUT}}{V_{IN}}$$

Therefore, for a maximum load current of 6.0A , the input capacitors should be able to safely handle 3A of ripple current. For the EVAL board, we chose two 10uF, 25V ceramic capacitors. Each capacitor has a ripple current capability of 2A.

MOSFET Switch Selection

The current selection of MOSFETs are determined by the setting of the over-current limit circuit and the maximum input voltage. The next step is to determine their power handling capability. For the EVAL board the IRF7805 & IRF7807 meet the voltage and current requirements. These are 30V, 10A & 7A FET's, respectively. Based on 85°C ambient temperature, 150°C junction temperature and thermal resistance, their power handling is calculated as follows:

Power Limit for Upper & Lower FET:

T_J = 150°C; T_A = 85°C; θ_{ja} = 50°C/W

$$P_T = \frac{T_J - T_A}{\theta_{JA}} = \frac{150 - 85}{50} = 1.3W$$

Each FET must not exceed 1.3W of power dissipation.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case conduction power dissipation occurs at minimum battery voltage:

$$P_{DUC} = \frac{V_{OUT}}{V_{IN(MIN)}} \bullet I_{LOAD}^2 \bullet R_{DS(ON)}$$

Typically, a small high-side MOSFET is selected to reduce switching losses at high input voltages. However, the RDS(ON) limits how small the MOSFET can be.

Another element of loss in the upper MOSFET is the switching loss, especially at high input voltages, those seen when the AC adaptor is applied. The upper MOSFET switching losses can be estimated as follows:

$$P_{DUS} = \frac{C_{RSS} \bullet V_{IN(MAX)}^2 \bullet f \bullet I_{LOAD}}{I_{GATE}}$$

Where CRSS is the reverse transfer capacitance of the upper MOSFET and IGATE is the peak gate-drive source/sink current which is approximately 1A for the SC1470.

For the low-side MOSFET the there are only conduction loses to be concerned about since the commutation diode is active while the lower MOSFET switches. The worst-case power dissipation occurs at maximum battery voltage:

$$P_{DLC} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \bullet I_{LOAD}^2 \bullet R_{DS(ON)}$$

Adding up the power dissipation for each MOSFET can now proceed and the total for each MOSFET should not exceed 1.3W which was calculated earlier to be the maximum power dissipation under worst-case conditions.

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 500nS (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200KHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

Layout Guidelines

As with any high frequency switching regulator, it is advisable to practice a careful layout strategy. This includes keeping loop area as small as possible. Properly decoupling lines that pull large currents in short periods of time. To keep loop area small always use a ground plane and if possible split the plane in two areas, signal GND and power GND, then tie the two together at one point. Be sure that high current paths have low inductance by making trace widths wide where possible. The SC1470 pin-outs contain digital signals on the right and analog signals on the left side of the device. This facilitates the isolation of digital and analog signals enabling effective layout of the device. In summary follow these guidelines for good PC board layout:

• Keep high-current paths short, especially at the ground terminals.

• Tie AGND and PGND together close to the IC.

• Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs 1oz) can enhance full-load efficiency by 1% or more.

• Connect the ILIMIT resistor as close to the lower MOSFET drain as possible, and keep the resistance distance from the ILIM pin to the drain short. This will improve current limit accuracy.

1470 System DC Accuracy

Three IC parameters affect system DC accuracy, the internal band gap reference, the error comparator offset voltage, and the switching frequency variation with line and load.

The internal 1% 1.5V reference contains two error components, a 0.5% DC error and a 0.5% supply and temperature error. The error comparator offset is trimmed so that it trips when the feedback pin is nominally 0.5 volts +/-1% at room temperature. The comparator offset trim compensates for any DC error in the reference. Thus, the percentage error is the sum of the reference variation over supply, temperature and the offset in the error comparator or 1.5%.

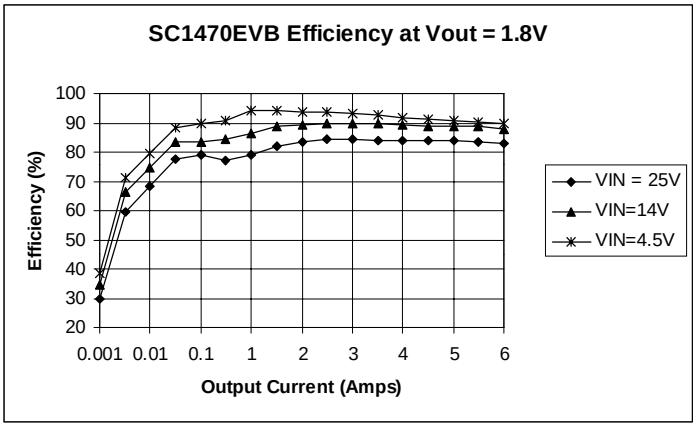
The on pulse in the SC1470 is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on-time regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the feedback resistors are chosen to divide down the output by a factor of five, the valley of the output ripple will be 2.5V. If the ripple is 50mV with VIN = 6 volts, then the measured DC output will be 2.525 volts. If the ripple increases to 80mV with VIN = 25 volts, then the measured DC output will be 2.540V. The best way to minimize this effect is to minimize the output ripple.

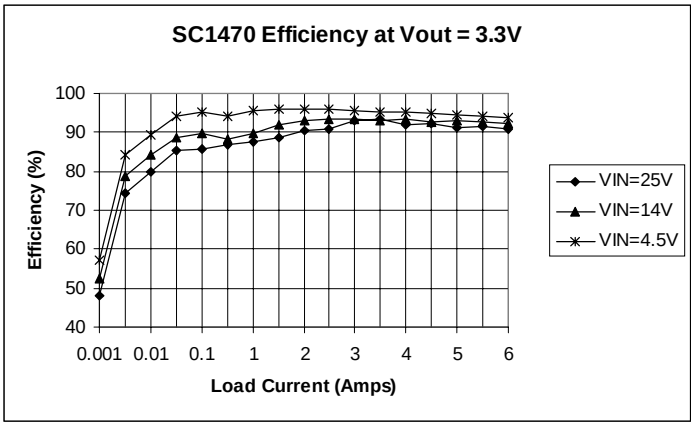
To compensate for valley regulation is usually desirable to use passive droop. Take the feedback directly from the output side of the inductor incorporating a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced.

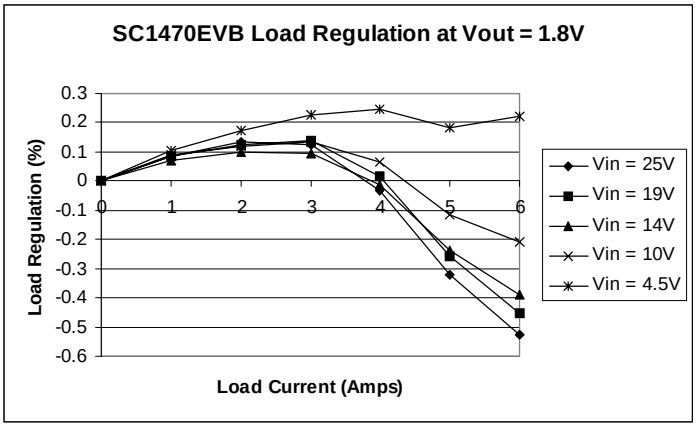
Board components and layout also influence DC accuracy. The use of 1% feedback resistors contribute 1%. If tighter DC accuracy is required use 0.1% feedback resistors.

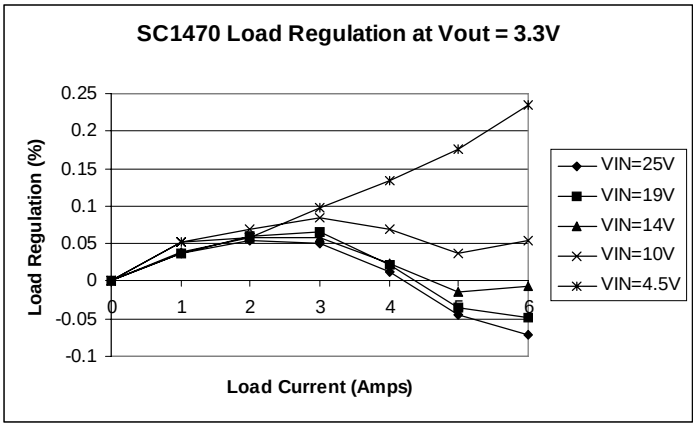
The output inductor value may change with current. This will change the output ripple and thus the DC output voltage.

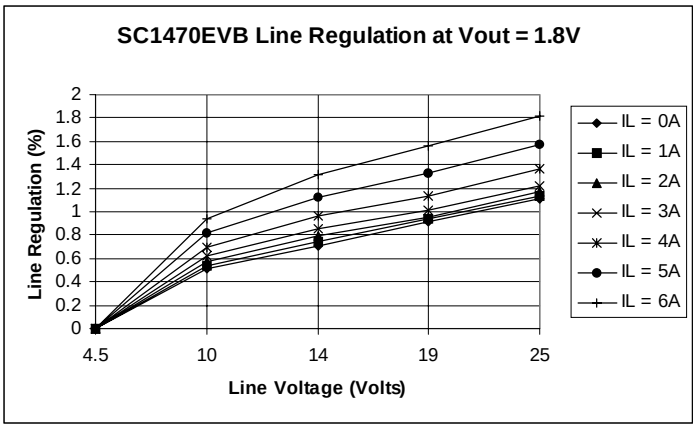
Typical Characteristics

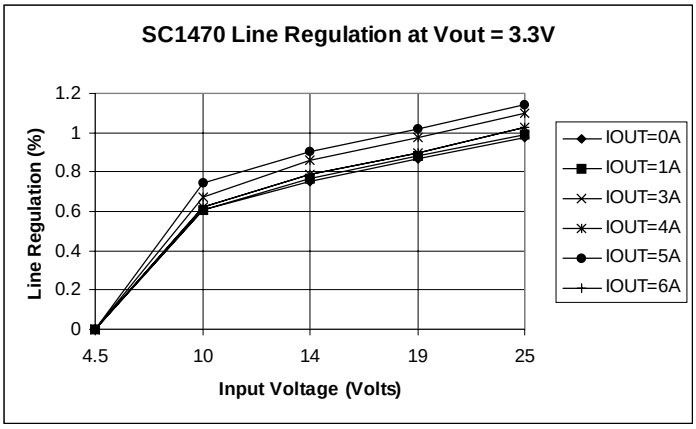






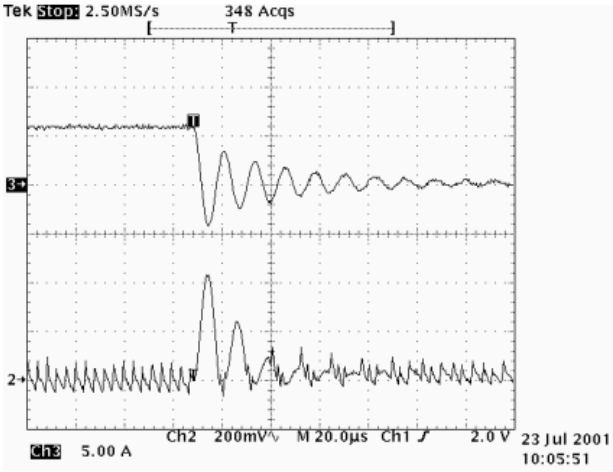




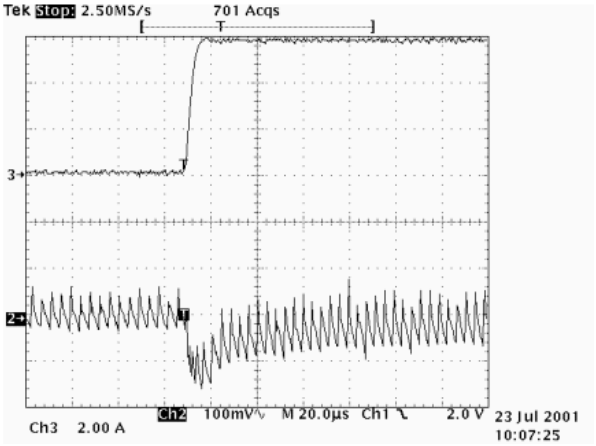


Typical Characteristics Cont.

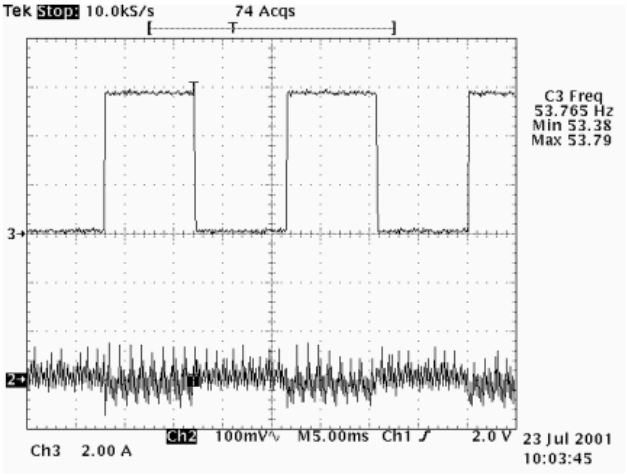
Load Release 6A - 0A, Forced Continuous Mode
L = 2uH, Cout = 600uF, Vout = 1.8V, Vin = 12V,



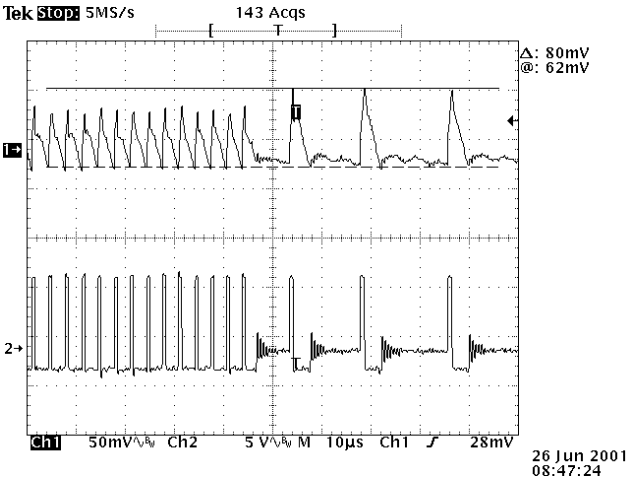
Load Applied 0A - 6A, Forced Continuous Mode
L = 2uH, Cout = 600uF, Vout = 1.8V, Vin = 12V,



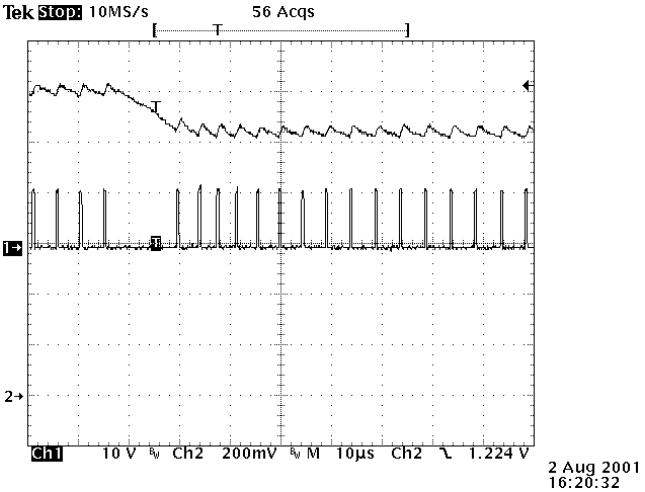
0A - 6A Transient, Forced Continuous Mode
L = 2uH, Cout = 600uF, Vout = 1.8V, Vin = 12V



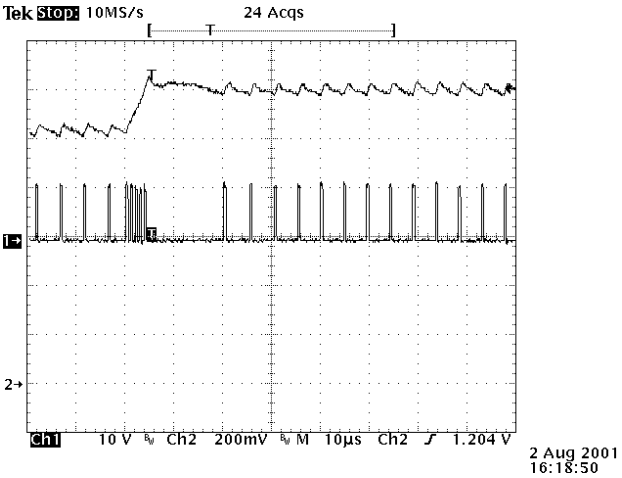
Forced Continuous Mode to PSAVE Mode



Upper Trace: Inductor Current
Lower Trace: Phase Lead

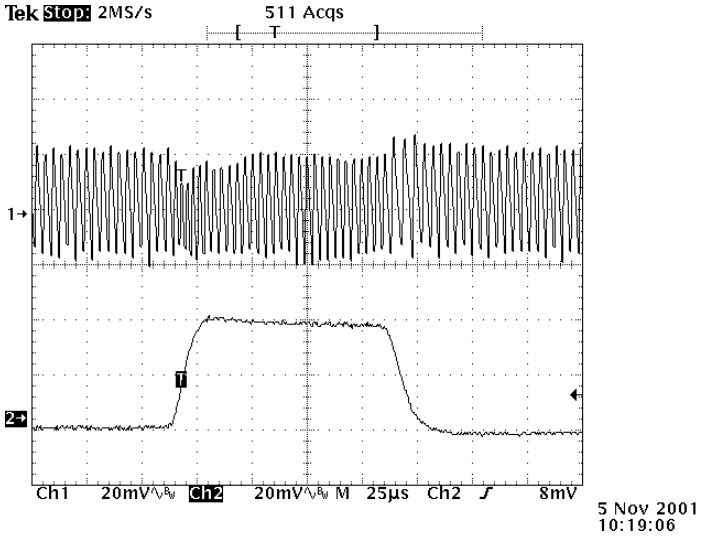


Upper Trace: Inductor Current
Lower Trace: Phase Lead

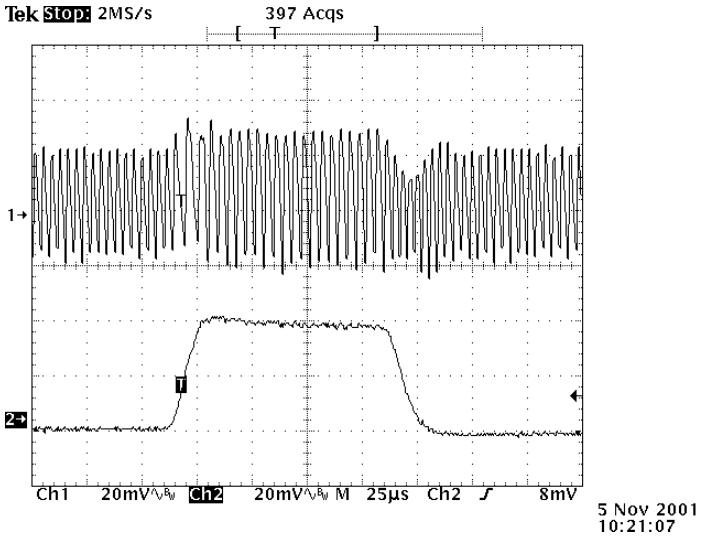


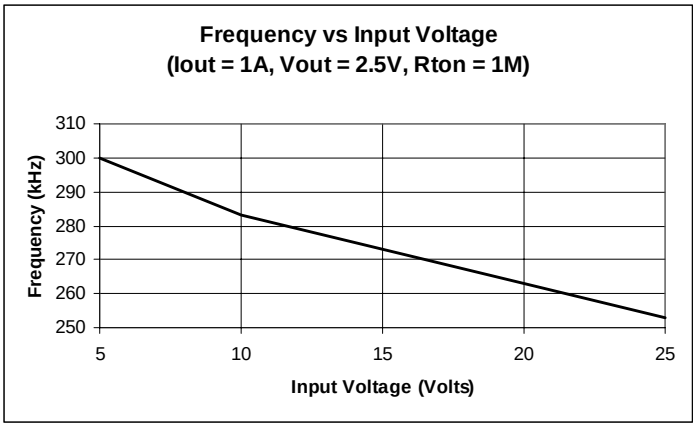
Typical Characteristics Cont.

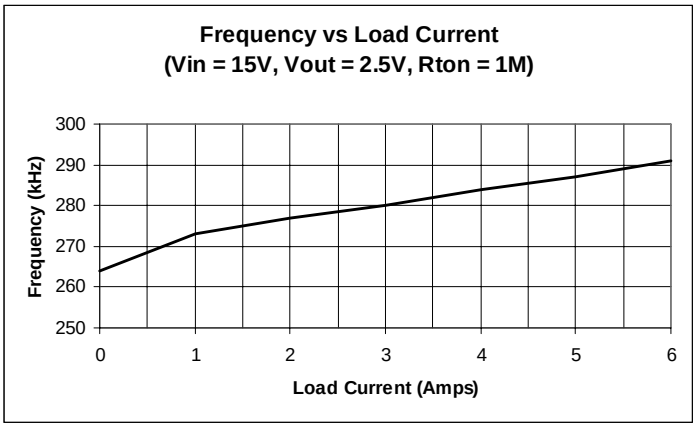
Load Step: 0A to +2A, Forced Continuous Mode
L = 4uH, Cout = 300uF, Vout = 2.5V, Vin = 15V

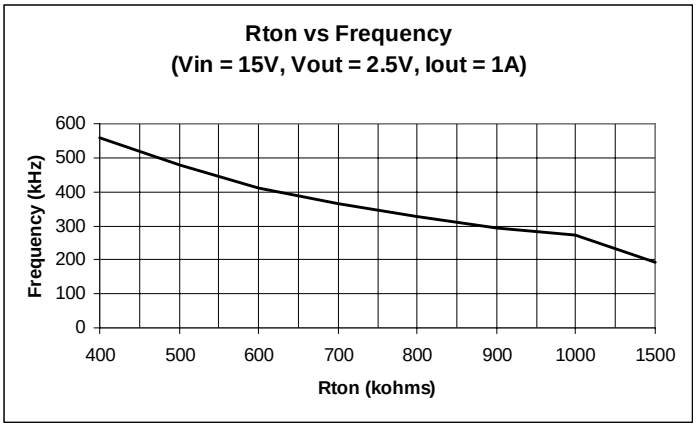


Load Step: 0A to -2A, Forced Continuous Mode
L = 4uH, Cout = 300uF, Vout = 2.5V, Vin = 15V

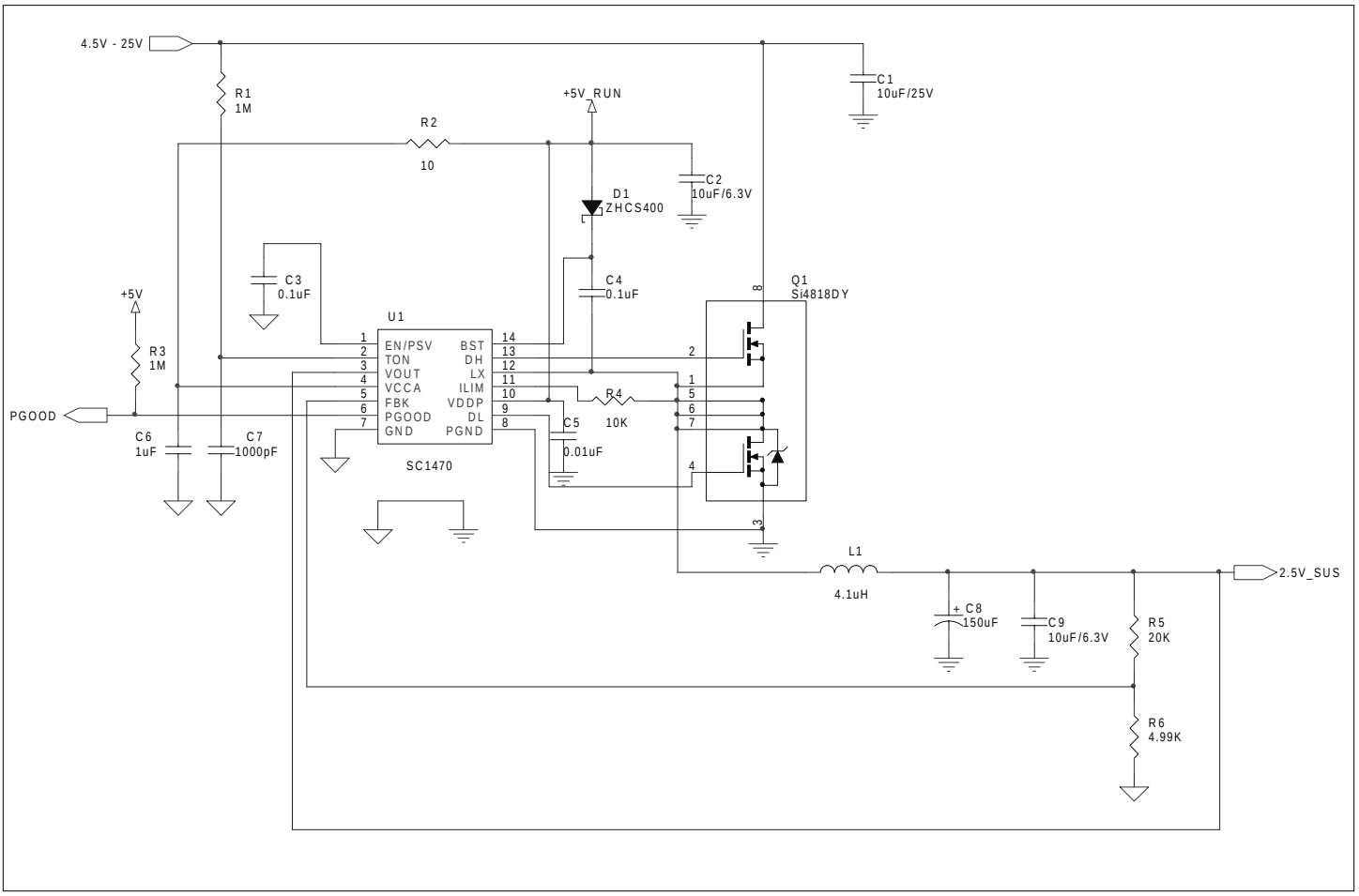








Reference Design



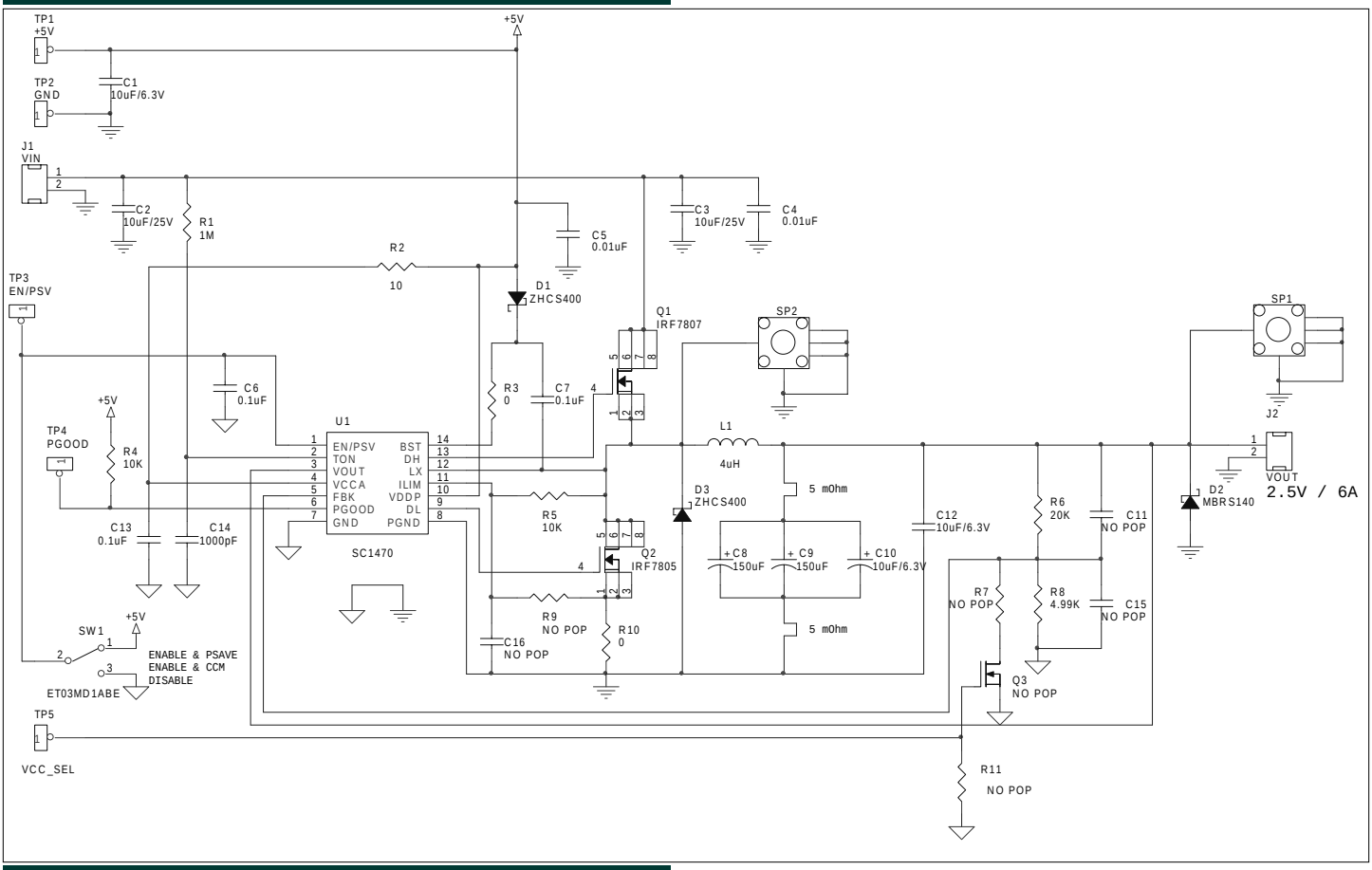
VIN = 4.5V - 25V

VOUT = 2.5V; IOUT = 3A

Bill Of Materials

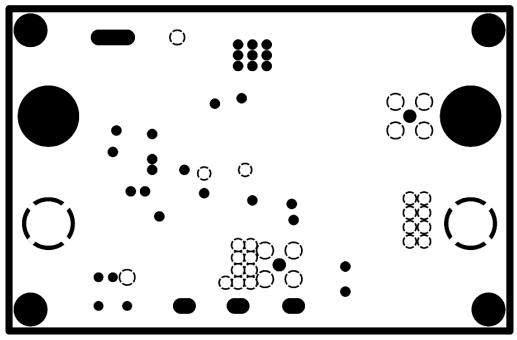
Item	Quantity	Reference	Part
1	1	C1	10uF/25V
2	2	C2,C9	10uF/6.3V
3	2	C3,C4	0.1uF
4	1	C5	0.01uF
5	1	C6	1uF
6	1	C7	1000pF
7	1	C8	150uF
8	1	D1	ZHCS400
9	1	L1	4.1uH
10	1	Q1	Si4818DY
11	2	R1,R3	1M
12	1	R2	10
13	1	R4	10K
14	1	R5	20K
15	1	R6	4.99K
16	1	U1	SC1470

Evaluation Board Schematic

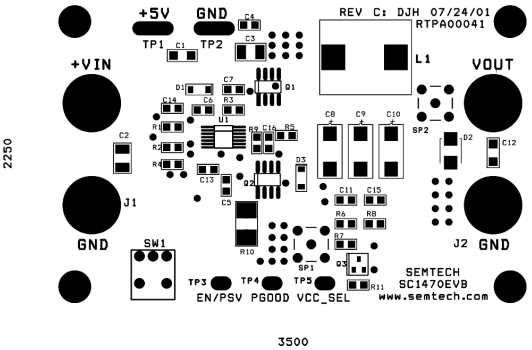


Evaluation Board Gerber Plots

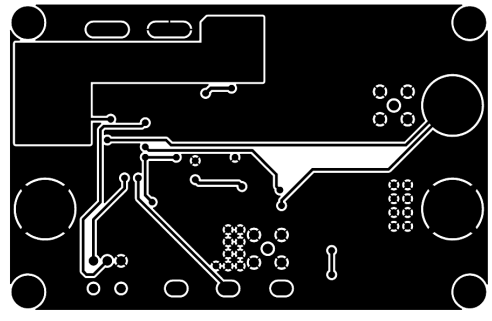
GROUND



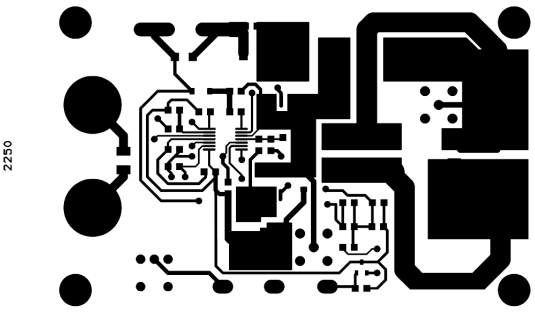
SILK SCREEN



BOTTOM



TOP



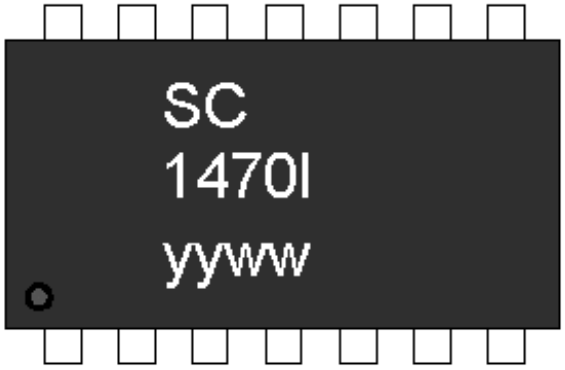
Evaluation Board Bill of Materials

Bill Of Materials

Item	Quantity	Reference	Part
1	3	C1,C10,C12	10uF/6.3V
2	2	C2,C3	10uF/25V
3	2	C4,C5	0.01uF
4	3	C6,C7,C13	0.1uF
5	2	C9,C8	150uF
6	7	Q3,R7,R9,R11,C11,C15,C16	NO POP
7	1	C14	1000pF
8	2	D3,D1	ZHCS400
9	1	D2	MBRS140
10	1	J1,J2	Banana Jack
11	1	L1	4uH
12	1	Q1	IRF7807
13	1	Q2	IRF7805
14	1	R1	1M
15	1	R2	10
16	2	R3,R10	0
17	2	R4,R5	10K
18	1	R6	20K
19	1	R8	4.99K
20	2	SP2,SP1	Probe Test Point
21	1	SW1	ET03MD1ABE
22	1	TP1,TP2,TP3,TP4,TP5	Post
23	1	U1	SC1470

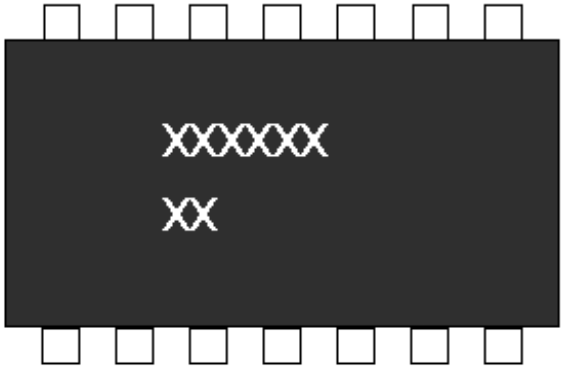
Marking Information

Top Mark



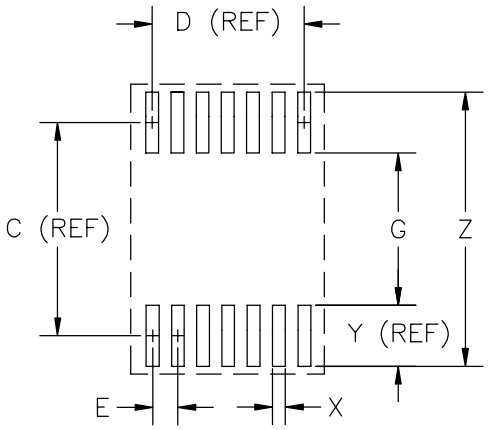
yy = two-digit year of manufacture
ww = two-digit week of manufacture

Bottom Mark



xxxxxx = Wafer Lot Number
xx = Assembly Lot Number

Land Pattern - TSSOP-14

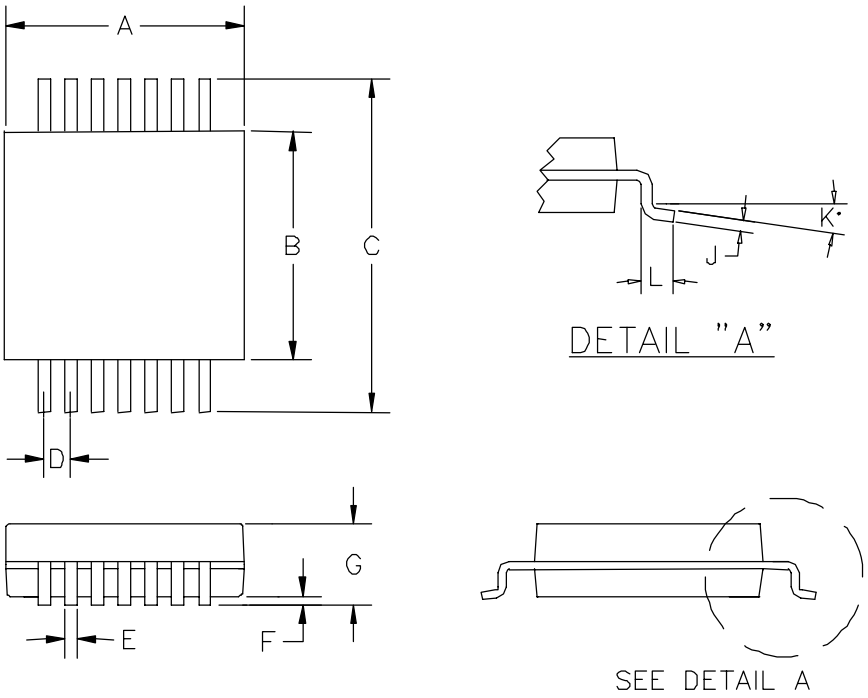


DIMENSIONS ①					
DIMⁿ	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.156	—	3.96	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	REF
Y	—	.062	—	1.583	—
Z	—	.280	—	7.113	—

② GRID PLACEMENT COURTYARD IS 10 X 15 ELEMENTS (5mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

① CONTROLLING DIMENSIONS: MILLIMETERS.

Outline Drawing



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.193	.201	4.90	5.10	(2)
B	.169	.177	4.30	4.50	(2)
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.002	.006	.05	.15	—
G		.047		1.20	—
J	.004	.008	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AB1

(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

Semtech Corporation
Power Management Products Division
652 Mitchell Rd., Newbury Park, CA 91320
Phone: (805)498-2111 FAX (805)498-3804