

## IR2153(D) (S)

### SELF-OSCILLATING HALF-BRIDGE DRIVER

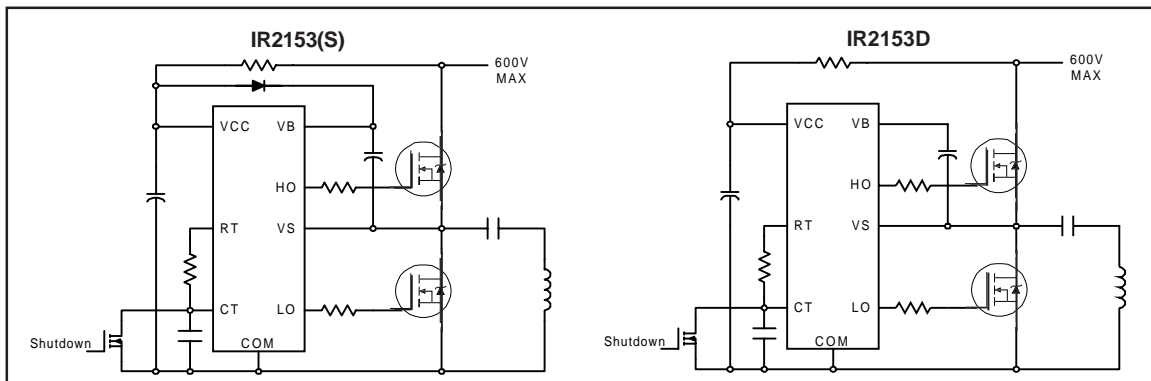
#### Features

- Integrated 600V half-bridge gate driver
- 15.6V zener clamp on V<sub>CC</sub>
- True micropower start up
- Tighter initial deadtime control
- Low temperature coefficient deadtime
- Shutdown feature (1/6th V<sub>CC</sub>) on C<sub>T</sub> pin
- Increased undervoltage lockout Hysteresis (1V)
- Lower power level-shifting circuit
- Constant LO, HO pulse widths at startup
- Lower di/dt gate driver for better noise immunity
- Low side output in phase with R<sub>T</sub>
- Internal 50nsec (typ.) bootstrap diode (IR2153D)
- Excellent latch immunity on all inputs and outputs
- ESD protection on all leads

#### Description

The IR2153(D)(S) are an improved version of the popular IR2155 and IR2151 gate driver ICs, and incorporate a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. The IR2153 provides more functionality and is easier to use than previous ICs. A shutdown feature has been designed into the C<sub>T</sub> pin, so that both gate driver outputs can be disabled using a low voltage control signal. In addition, the gate driver output pulse widths are the same once the rising undervoltage lockout threshold on V<sub>CC</sub> has been reached, resulting in a more stable profile of frequency vs time at startup. Noise immunity has been improved significantly, both by lowering the peak di/dt of the gate drivers, and by increasing the undervoltage lockout hysteresis to 1V. Finally, special attention has been paid to maximizing the latch immunity of the device, and providing comprehensive ESD protection on all pins.

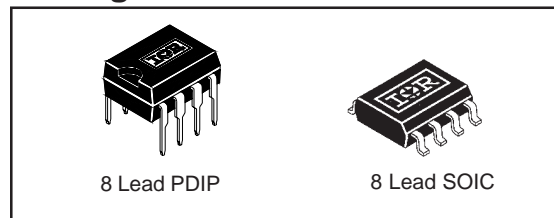
#### Typical Connections



#### Product Summary

V <sub>OFFSET</sub>	600V max.
Duty Cycle	50%
T <sub>r</sub> /T <sub>p</sub>	80/40ns
V <sub>clamp</sub>	15.6V
Deadtime (typ.)	1.2 μs

#### Packages



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## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating supply voltage	-0.3	625	V
$V_S$	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
$V_{HO}$	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{LO}$	Low side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{RT}$	$R_T$ pin voltage	-0.3	$V_{CC} + 0.3$	
$V_{CT}$	$C_T$ pin voltage	-0.3	$V_{CC} + 0.3$	
$I_{CC}$	Supply current (note 1)	—	25	mA
$I_{RT}$	$R_T$ pin current	-5	5	
$dV_S/dt$	Allowable offset voltage slew rate	-50	50	V/ns
$P_D$	Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$ (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
$R_{thJA}$	Thermal resistance, junction to ambient (8 Lead DIP)	—	125	$^\circ\text{C/W}$
	(8 Lead SOIC)	—	200	
$T_J$	Junction temperature	-55	150	$^\circ\text{C}$
$T_S$	Storage temperature	-55	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
$V_{BS}$	High side floating supply voltage	$V_{CC} - 0.7$	$V_{CLAMP}$	V
$V_S$	Steady state high side floating supply offset voltage	-3.0 (note 2)	600	
$V_{CC}$	Supply voltage	10	$V_{CLAMP}$	
$I_{CC}$	Supply current	(note 3)	5	mA
$T_J$	Junction temperature	-40	125	$^\circ\text{C}$

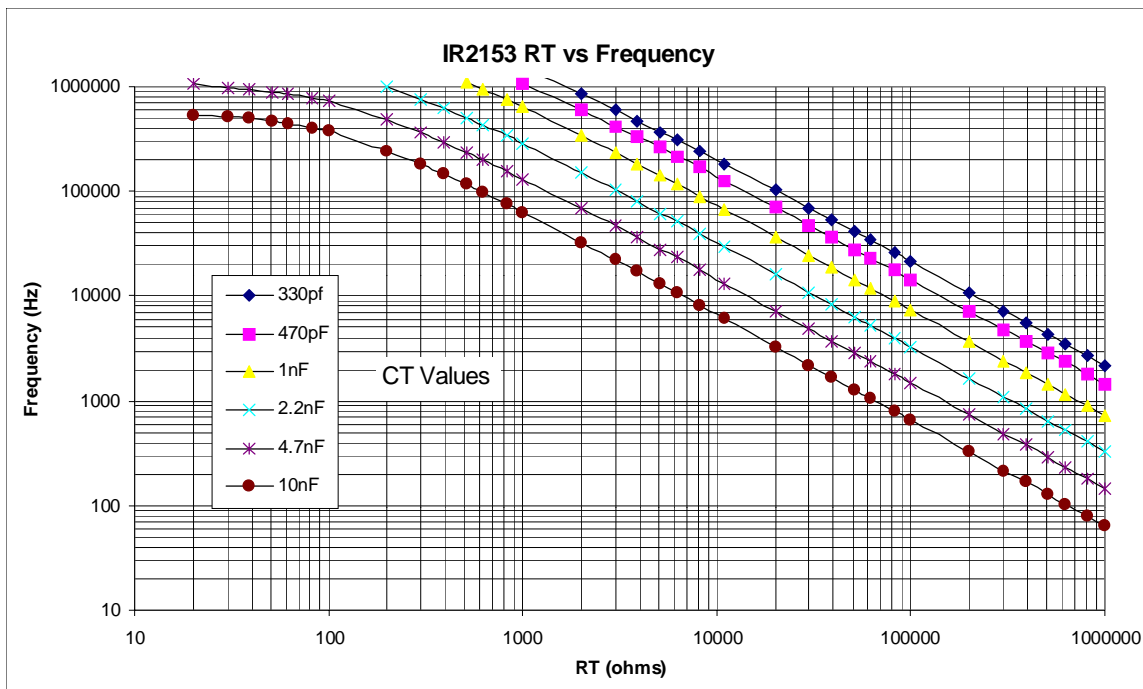
Note 1: This IC contains a zener clamp structure between the chip  $V_{CC}$  and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the  $V_{CLAMP}$  specified in the Electrical Characteristics section.

Note 2: Care should be taken to avoid output switching conditions where the  $V_S$  node flies inductively below ground by more than 5V.

Note 3: Enough current should be supplied to the  $V_{CC}$  pin of the IC to keep the internal 15.6V zener diode clamping the voltage at this pin.

## Recommended Component Values

Symbol	Component	Min.	Max.	Units
$R_T$	Timing resistor value	10	—	$k\Omega$
$C_T$	$C_T$ pin capacitor value	330	—	pF



## Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 12V,  $C_L$  = 1000 pF,  $C_T$  = 1 nF and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Low Voltage Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{CCUV+}$	Rising $V_{CC}$ undervoltage lockout threshold	8.1	9.0	9.9	V	
$V_{CCUV-}$	Falling $V_{CC}$ undervoltage lockout threshold	7.2	8.0	8.8		
$V_{CCUVH}$	$V_{CC}$ undervoltage lockout Hysteresis	0.5	1.0	1.5		
$I_{QCCUV}$	Micropower startup $V_{CC}$ supply current	—	75	150	$\mu A$	$V_{CC} \leq V_{CCUV-}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	500	950		
$V_{CLAMP}$	$V_{CC}$ zener clamp voltage	14.4	15.6	16.8	V	$I_{CC} = 5mA$
Floating Supply Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$I_{QBSUV}$	Micropower startup $V_{BS}$ supply current	—	0	10	$\mu A$	$V_{CC} \leq V_{CCUV-}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	30	50		
$V_{BSMIN}$	Minimum required $V_{BS}$ voltage for proper functionality from $R_T$ to HO	—	4.0	5.0	V	$V_{CC} = V_{CCUV+} + 0.1V$
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$V_F$	Bootstrap diode forward voltage (IR2153D)	0.5	—	1.0	V	$I_F = 250mA$
Oscillator I/O Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$f_{osc}$	Oscillator frequency	19.4	20	20.6	kHz	$R_T = 36.9k\Omega$
		94	100	106		$R_T = 7.43k\Omega$
$d$	$R_T$ pin duty cycle	48	50	52	%	$f_o < 100kHz$
$I_{CT}$	$C_T$ pin current	—	0.001	1.0	$\mu A$	
$I_{CTUV}$	UV-mode $C_T$ pin pulldown current	0.30	0.70	1.2	mA	$V_{CC} = 7V$
$V_{CT+}$	Upper $C_T$ ramp voltage threshold	—	8.0	—	V	
$V_{CT-}$	Lower $C_T$ ramp voltage threshold	—	4.0	—		
$V_{CTSD}$	$C_T$ voltage shutdown threshold	1.8	2.1	2.4		
$V_{RT+}$	High-level $R_T$ output voltage, $V_{CC} - V_{RT}$	—	10	50	mV	$I_{RT} = 100\mu A$
		—	100	300		$I_{RT} = 1mA$
$V_{RT-}$	Low-level $R_T$ output voltage	—	10	50		$I_{RT} = 100\mu A$
		—	100	300		$I_{RT} = 1mA$
$V_{RTUV}$	UV-mode $R_T$ output voltage	—	0	100		$V_{CC} \leq V_{CCUV-}$
$V_{RTSD}$	SD-Mode $R_T$ output voltage, $V_{CC} - V_{RT}$	—	10	50		$I_{RT} = 100\mu A$ , $V_{CT} = 0V$
		—	10	300		$I_{RT} = 1mA$ , $V_{CT} = 0V$

## Electrical Characteristics (cont.)

Gate Driver Output Characteristics						
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V <sub>OH</sub>	High level output voltage, V <sub>BIAS</sub> - V <sub>O</sub>	—	0	100	mV	I <sub>O</sub> = 0A
V <sub>OL</sub>	Low-level output voltage, V <sub>O</sub>	—	0	100		I <sub>O</sub> = 0A
V <sub>OL_UV</sub>	UV-mode output voltage, V <sub>O</sub>	—	0	100		I <sub>O</sub> = 0A V <sub>CC</sub> ≤ V <sub>CCUV</sub>
t <sub>r</sub>	Output rise time	—	80	150	nsec	
t <sub>f</sub>	Output fall time	—	45	100		
t <sub>sd</sub>	Shutdown propagation delay	—	660	—		
t <sub>d</sub>	Output deadtime (HO or LO)	0.75	1.20	1.65	μsec	

## Lead Definitions

Symbol	Description
V <sub>CC</sub>	Logic and internal gate drive supply voltage
R <sub>T</sub>	Oscillator timing resistor input
C <sub>T</sub>	Oscillator timing capacitor input
COM	IC power and signal ground
LO	Low side gate driver output
V <sub>S</sub>	High voltage floating supply return
HO	High side gate driver output
V <sub>B</sub>	High side gate driver floating supply

## Lead Assignments

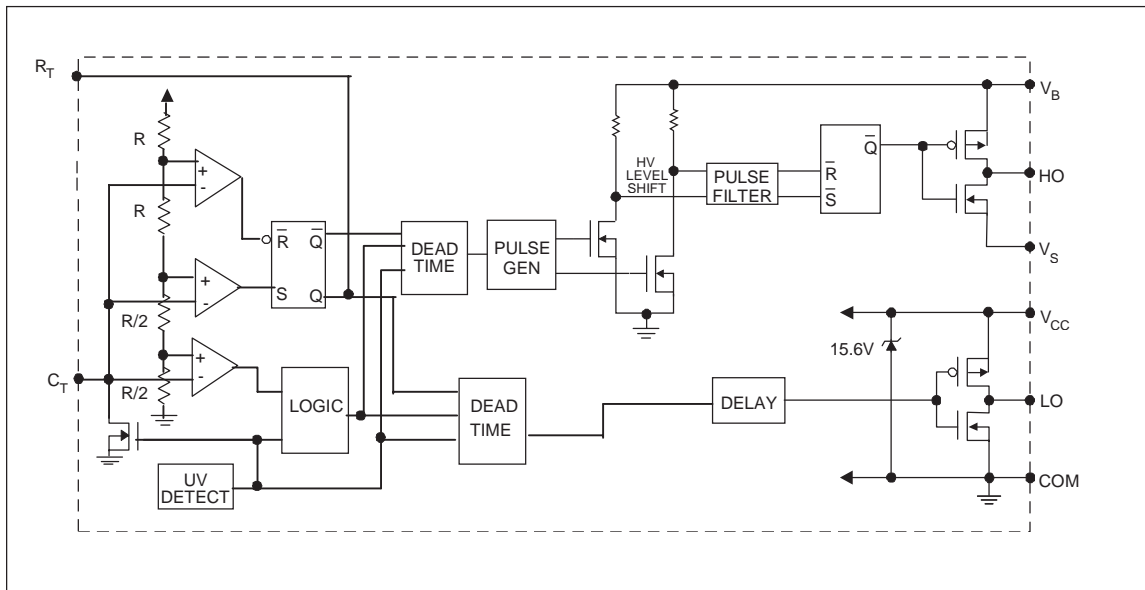
<p>8 Lead PDIP</p> <p><b>IR2153(D)</b></p>	<p>8 Lead SOIC</p> <p><b>IR2153S</b></p>
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NOTE: The IR2153D is offered in 8 lead PDIP only.

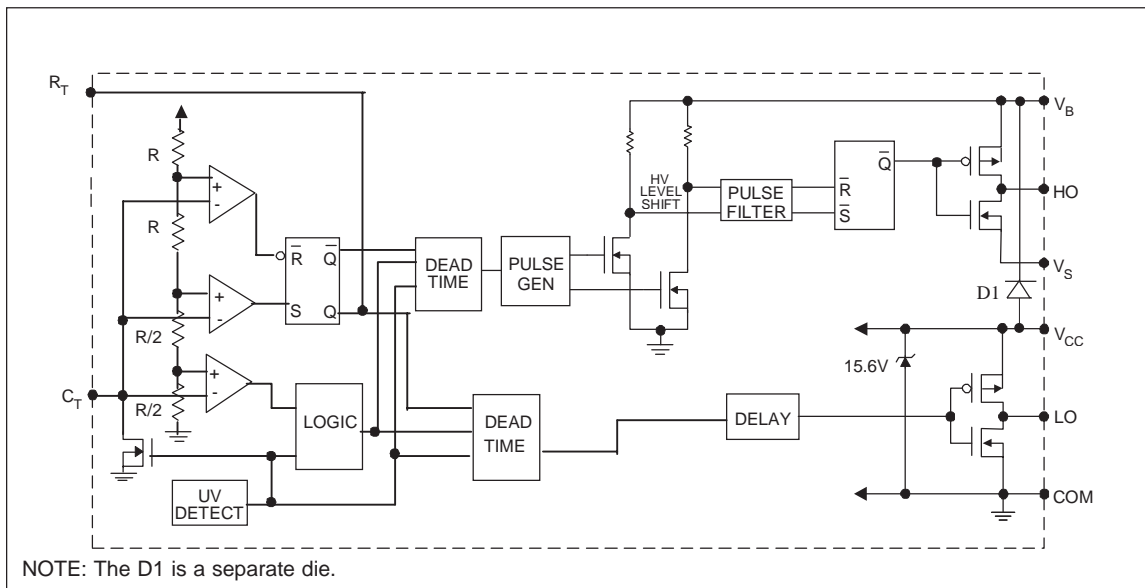
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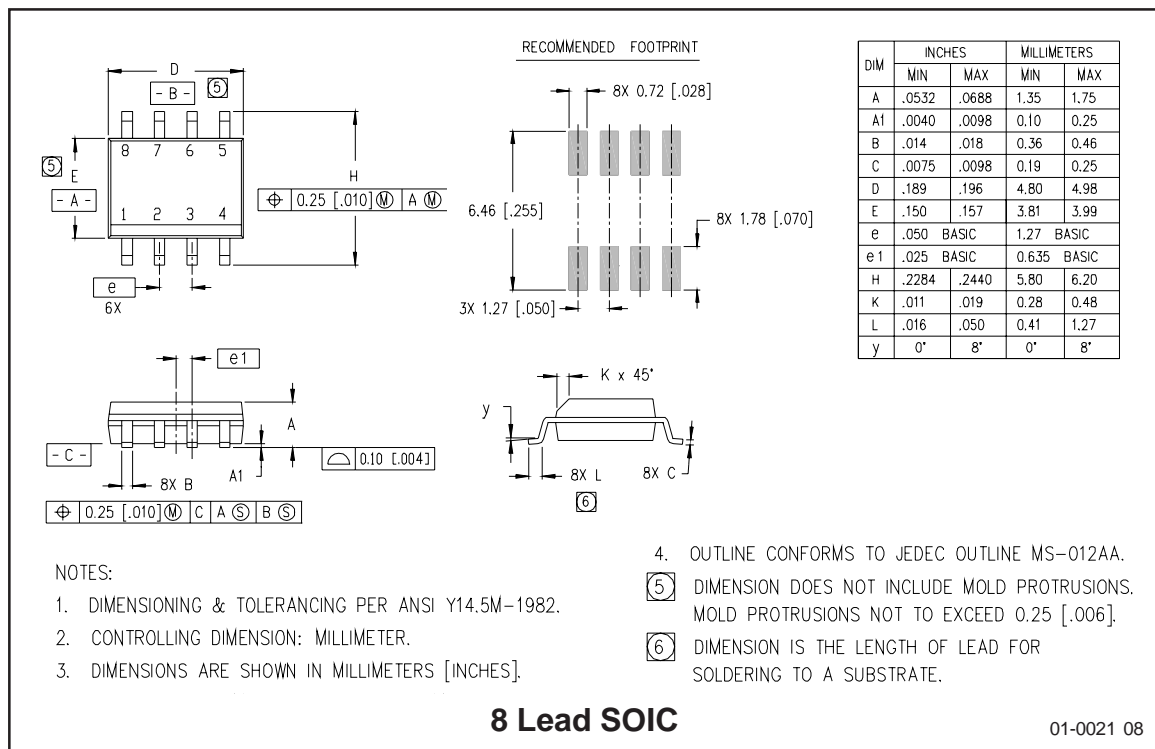
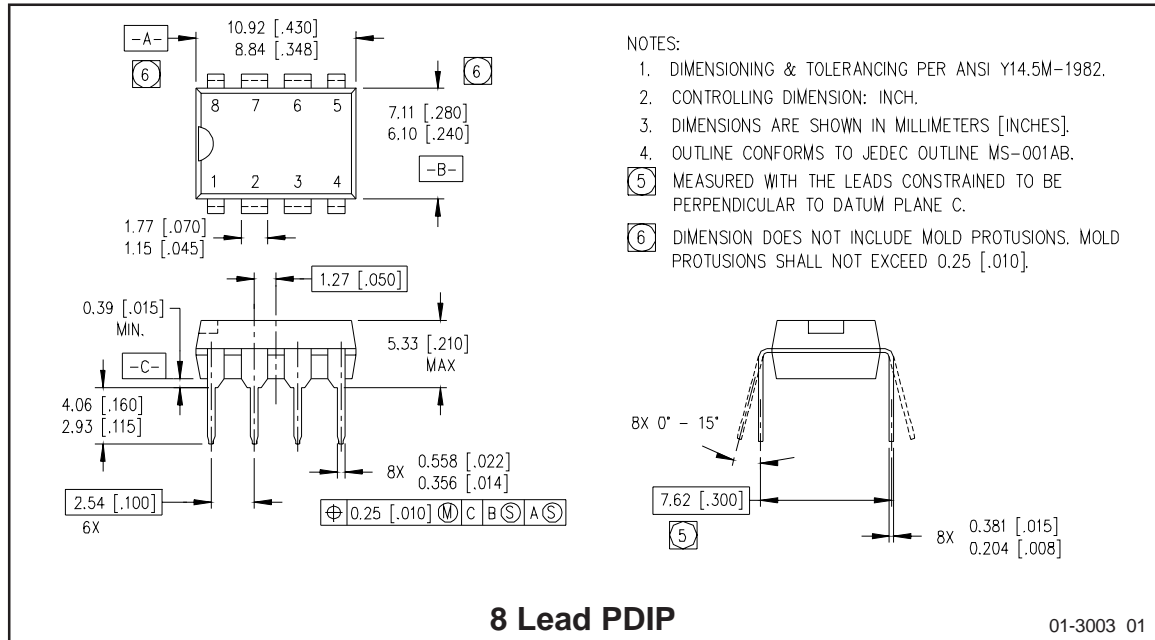
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## Functional Block Diagram for IR2153(S)



## Functional Block Diagram for IR2153D





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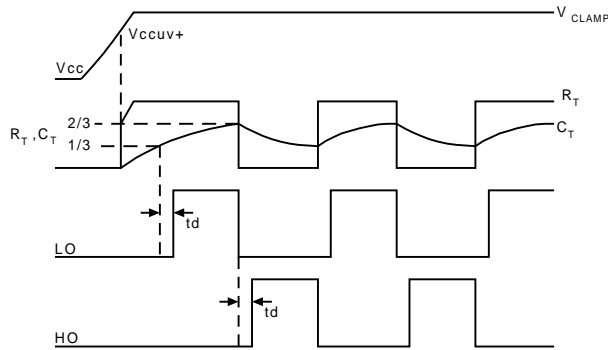


Figure 1. Input/Output Timing Diagram

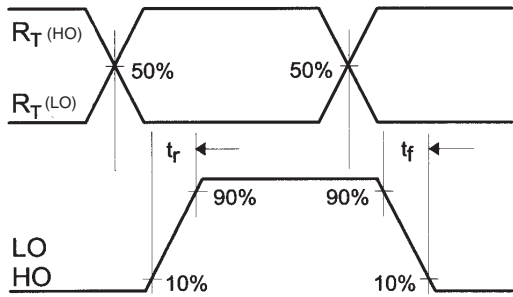


Figure 2. Switching Time Waveform Definitions

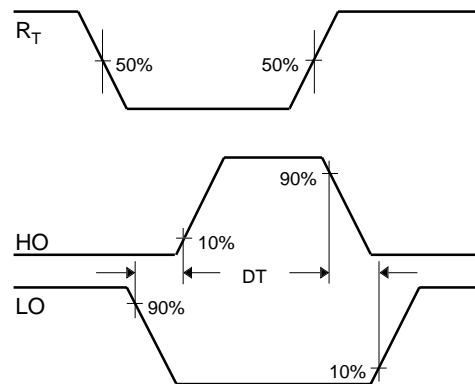


Figure 3. Deadtime Waveform Definitions

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