



# MX25L6402A

## **Macronix NBit™ Memory Family** **64M-BIT [x 1] CMOS SERIAL eLite Flash™ MEMORY**

### **FEATURES**

#### **GENERAL**

- 67,108,864 x 1 bit structure
- 128 Equal Sectors with 64K byte each
  - Any sector can be erased
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is equal to or less than 2.2V

#### **PERFORMANCE**

- High Performance
  - Fast access time: 25MHz serial clock (50pF + 1TTL Load)
  - Fast program time: 2ms/page (typical, 128-byte per page)
  - Fast erase time: 2s/sector (typical, 64K-byte per sector)
  - Acceleration mode:
    - Program time: 1.6ms/page (typical)
    - Erase time: 1.6s/sector (typical)
- Low Power Consumption
  - Low active read current: 24mA (typical) at 25MHz
  - Low active programming current: 35mA (typical)
  - Low active erase current: 35mA (typical)
  - Low standby current: 5uA (typical, CMOS)
- Minimum 100 erase/program cycle

#### **SOFTWARE FEATURES**

- Input Data Format
  - 1-byte Command code, 3-byte address, 1-byte byte address

- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
  - Provides detection of program and erase operation completion.
  - Provides auto erase/ program error report
  - Provides detection of parallel mode (for production throughputs increasing)

#### **HARDWARE FEATURES**

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO/PO7 Output
  - Serial Data Output/Parallel mode PO7 output
- ACC Pin
  - Program/erase acceleration
- RESET# Pin
  - to reset
- PO0~PO6 Output
  - for parallel mode
- PACKAGE
  - 28-pin SOP (330mil)

## GENERAL DESCRIPTION

The MX25L6402A is a CMOS 67,108,864 bit serial eLite Flash™ Memory, which is configured as 8,388,608 x 8 internally. The MX25L6402A features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input.

The MX25L6402A provide sequential read operation on whole chip. User may start to read from any byte of the array. While the end of the array is reached, the device will wrap around to the beginning of the array and continuously outputs data until CS# goes high.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (128 bytes) basis, and

erase command is executed on both chip and sector (64K bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

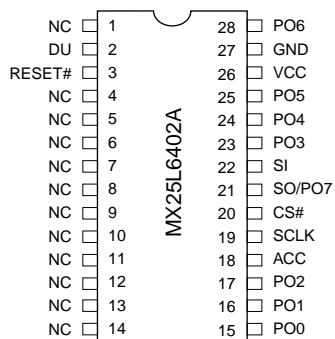
To increase user's factory throughputs, a parallel mode is provided. The performance of read/program is dramatically improved than serial mode.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 5uA DC current.

The MX25L6402A utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 100 program and erase cycles.

## PIN CONFIGURATIONS

### 28-PIN SOP (330 mil)

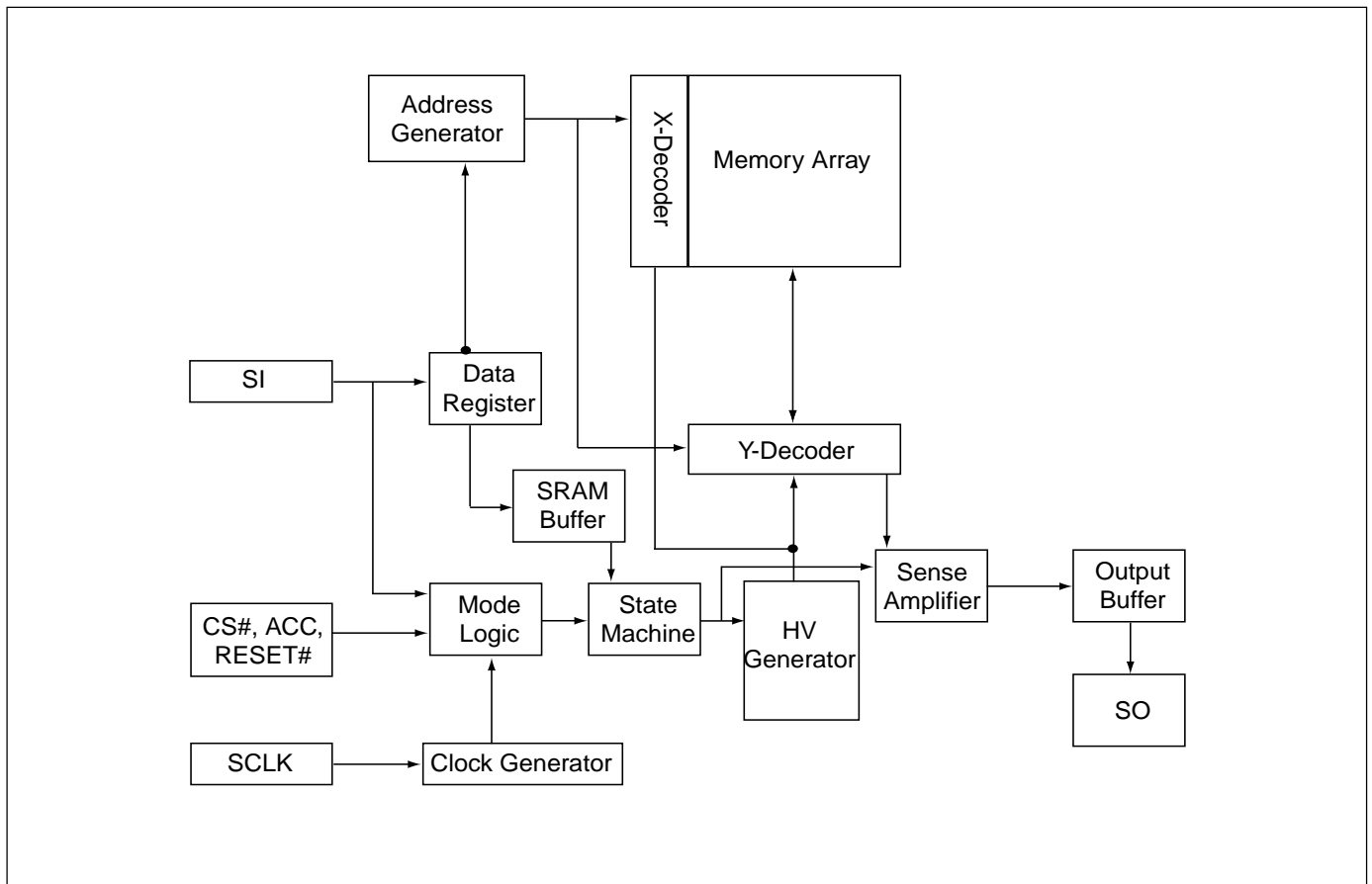


## PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI	Serial Data Input
SO/PO7	Serial Data Output/Paralled Data Output
SCLK	Clock Input
ACC	12V for program/erase acceleration
VCC	+ 3.3V Power Supply
GND	Ground
DU(1)	Do Not Use(for Test Mode only)
NC	No Internal Connection
PO0~PO6	Parallel data output (PO0~PO6 can be connected to NC in serial mode)
RESET#	Reset

### Note:

1.DU pin is used for in-house testing and can be tied to VCC, GND or open for normal operation. There is a weak pull-up resistor from VCC to DU pin.

**BLOCK DIAGRAM**

**COMMAND DEFINITION**

Com- mand (byte)	Read Array	Status Read	Clear Status	Read ID	Sector Erase	Chip Erase	Page Program	Parallel Mode
1st	52H	83H	89H	85H	F1H	F4H	F2H	55H
2nd	AD1	X		X	AD1	X	AD1	
3rd	AD2				AD2	X	AD2	
4th	AD3						AD3	
5th	BA						BA	
6th	X							
7th	X							
8th	X							
9th	X							
Action	n bytes read out until $\overline{CS}$ goes high	Output status byte until $\overline{CS}$ goes high	Clear status byte	Output vendor code until $\overline{CS}$ goes high	Start to erase at $\overline{CS}$ rising edge	Start to erase at $\overline{CS}$ rising edge	Load n bytes data to buffer until $\overline{CS}$ goes high & start to program	Enter and stay in parallel mode until power off

Note:

1.X is dummy cycle and is necessary

2.AD1 to AD3 are address input data

3.BA is byte address

**1-byte command code**

	Bit7(MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
<b>3-byte address(0 to 0FFFH)</b>								
AD1:	X	X	A22	A21	A20	A19	A18	A17
AD2:	A16	A15	A14	A13	A12	A11	A10	A9
AD3:	X	X	X	X	X	X	A8	A7
<b>1-byte byte address(0 to 7FH)</b>								
BA:	X	A6	A5	A4	A3	A2	A1	A0

Note:

A22 to A16=Sector address

## DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS falling edge. In standby mode, SO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS rising edge.

## COMMAND DESCRIPTION

### (1) Read Array

This command is sent with the 4-byte address (command included), and the byte address, followed by four dummy bytes sent to give the device time to stabilize. The device will then send out data starting at the byte address until CS goes high. The clock to clock out the data is supplied by the master SPI. The read operation is executed on whole array. If the end of the array is reached then the device will wrap around to the beginning of the array.

### (2) Read Status Register

When this command is sent, the device will continuously send out the status register contents starting at bit7. The clock to clock out the data is supplied by the master SPI.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
program/erase completion	parallel mode	NA	erase error	program error	NA	NA	ready/busy
Note1	1=in parallel 0=not in parallel mode		1=error	1=error			1=ready 0=busy

Bit 6,5,2,1 = Reserve for future use.

Bit 4 = "1" ----> There is an error occurred in last erase operation.

= "0" ----> There is no error occurred in last erase operation.

Bit 3 = "1" ----> There is an error occurred in last program operation.

= "0" ----> There is no error occurred in last program operation.

Bit 0 = "1" ----> Device is in ready mode.

= "0" ----> Device is in busy mode.

Note 1: The initial value of Bit7 is "1". Bit7 will have "1" to "0" transit only after program/erase operation is completed. Bit7 will shift from "0" to "1" only after issued program/erase/Clear status register command. Please note the Bit7=0 if program/erase fail.

Note 2: The value of Bit 0 is "1", no matter the result of program/erase is pass or fail.

### (3) Clear Status Register

This command only resets erase error bit (bit 4) and program error bit (bit 3). These two bits are set by on-chip state machine during program/erase operation, and can only be reset by issuing a clear status register command or by powering down VCC.

If status register indicates that error occurred in the last program/erase operation, any further program/erase operation will be prohibited until status register is cleared.

### (4) Read ID

This command is sent with an extra dummy byte (2-byte command). The device will clock out manufacturer code (C2H) and device code (9CH) when this command is issued. The clock to clock out the data is supplied by the master SPI.

### **(5) Sector/Chip Erase**

This command is sent with the sector address(A22~A16) when operating Sector Erase. The device will start the erase sequence after CS# goes high without any further input. A sector should be erased in a typical of 2sec. The average current is less than 26mA. The chip erase operation does not require the sector address input but two extra dummy bytes are necessary. During this operation, customer can also access Read Status & Read ID operations.

### **(6) Page Program**

This command is sent with the page number(A22~A7), and 128-byte page address(A6~A0), followed by programming data. The 128-byte page address (A6-A0) must start from 0. One to 128 bytes of data can be loaded into the buffer of the device until CS# goes high. If the end of the page is reached, then the device will wrap around to the beginning of the page. The device will program the specified page with buffered data(Until CS# goes high) without any further input. The typical page program time is 2mS. The average current is less than 26mA.

During this operation, customer can also access Read Status & Read ID operations.

### **(7) Standby Mode**

When CS# is high and there is no operation in progress, the device is put in standby mode. Typical standby current is less than 5uA.

### **(8) Parallel Mode (Highly recommended for production throughputs increasing)**

The parallel mode provides 8 bit outputs for increasing throughputs of factory production purpose. The parallel mode requires 55H command code, after writing the parallel mode command and then CS# going high, after that, the eLite Flash™ Memory can be available to accept read/program/read status/read ID command as the normal writing command procedure. The eLite Flash™ Memory will be in parallel mode until VCC power-off.

- a. Only effective for Read Array, Read Status, Read ID & Page Program write data period. (refer to page 16,18,21,23)
- b. For normal write command (by SI), No effect
- c. Under parallel mode, the fastest access clock freq. will be changed to 1.25MHz(SCLK pin clock freq.)
- d. For parallel mode, the tAA will be change to 50ns.

## **POWER-ON STATE**

After power-up, the device is placed in the standby state with following status:

The status register is reset with following status :

- Bit 7 = "1" -----> Refer to page 5 for detail.
- Bit 6 = "0" -----> Device is not in parallel mode.
- Bit 5,2,1 = Reserve for future use.
- Bit 4 = "0" -----> Erase error flag is reset.
- Bit 3 = "0" -----> Program error flag is reset.
- Bit 0="1" -----> Device is in ready state.

## RESET OPERATION

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tri-states all output pins, and ignores all commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity. Current is reduced for the duration of the RESET# pulse. When RESET# is held at VSS + 0.3V, the device draws reset current (ICC4). If RESET# is held at VIL but not within VSS + 0.3V, the reset current will be greater. The RESET# pin may be tied to system reset circuitry. A system reset would that also reset the SPI memory. Refer to the AC Characteristics tables for RESET# parameters.

## DATA SEQUENCE

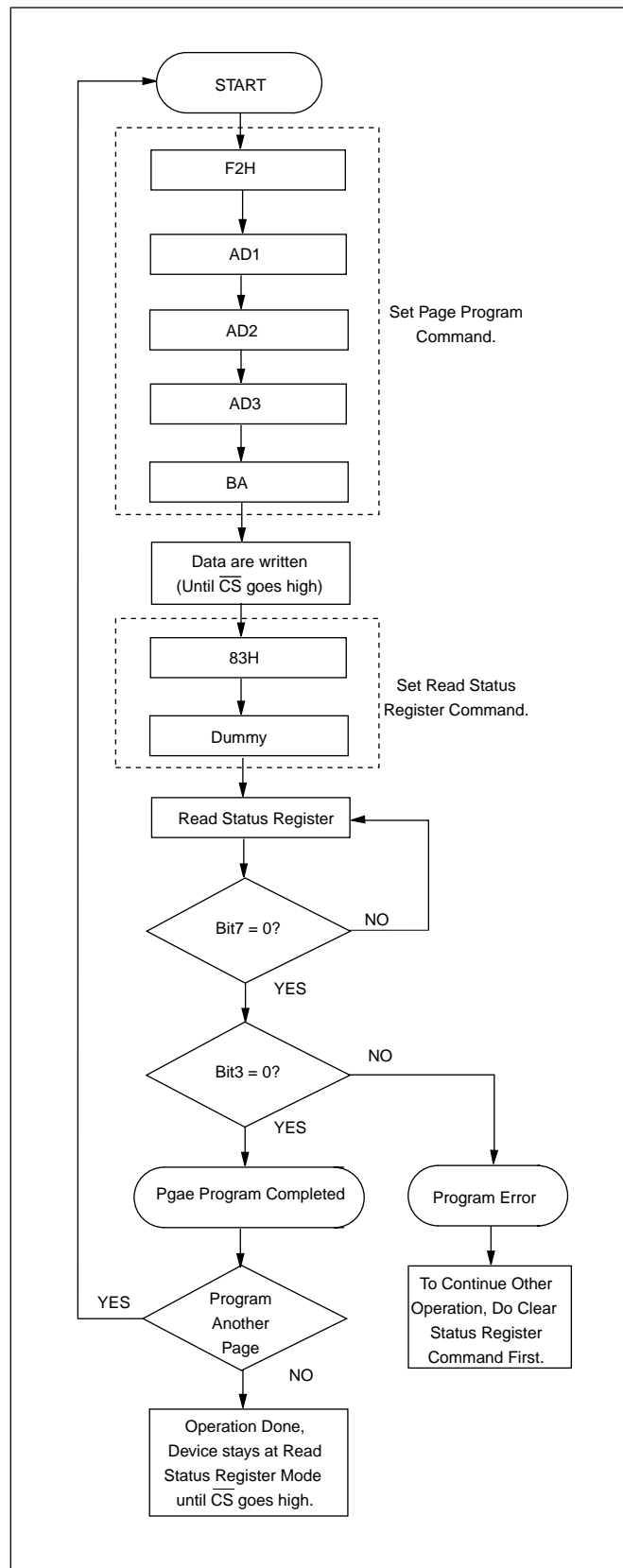
Output data is serially sent out through SO pin, synchronized with the rising edge of SCLK, whereas input data is serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data is bit 7 (MSB) first, then bit 6, bit 5, ....., and bit 0.(LSB)

## ADDRESS SEQUENCE

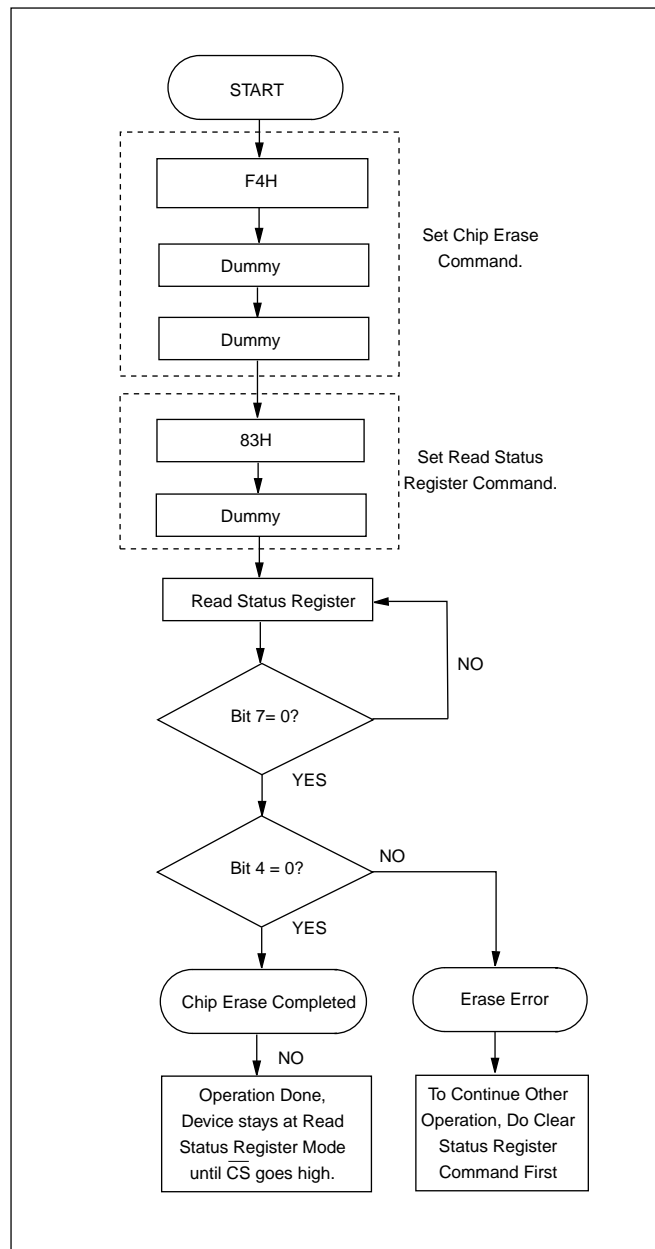
The address assignment is described as follows :

BA: Byte address Bit sequence:	X	A6	A5	A4	A3	A2	A1	A0
AD1:First Address Bit sequence:	X	X	A22	A21	A20	A19	A18	A17
AD2:Second Address Bit sequence:	A16	A15	A14	A13	A12	A11	A10	A9
AD3:Thrid Address Bit sequence:	X	X	X	X	X	X	A8	A7

## Auto Page Program Flow Chart

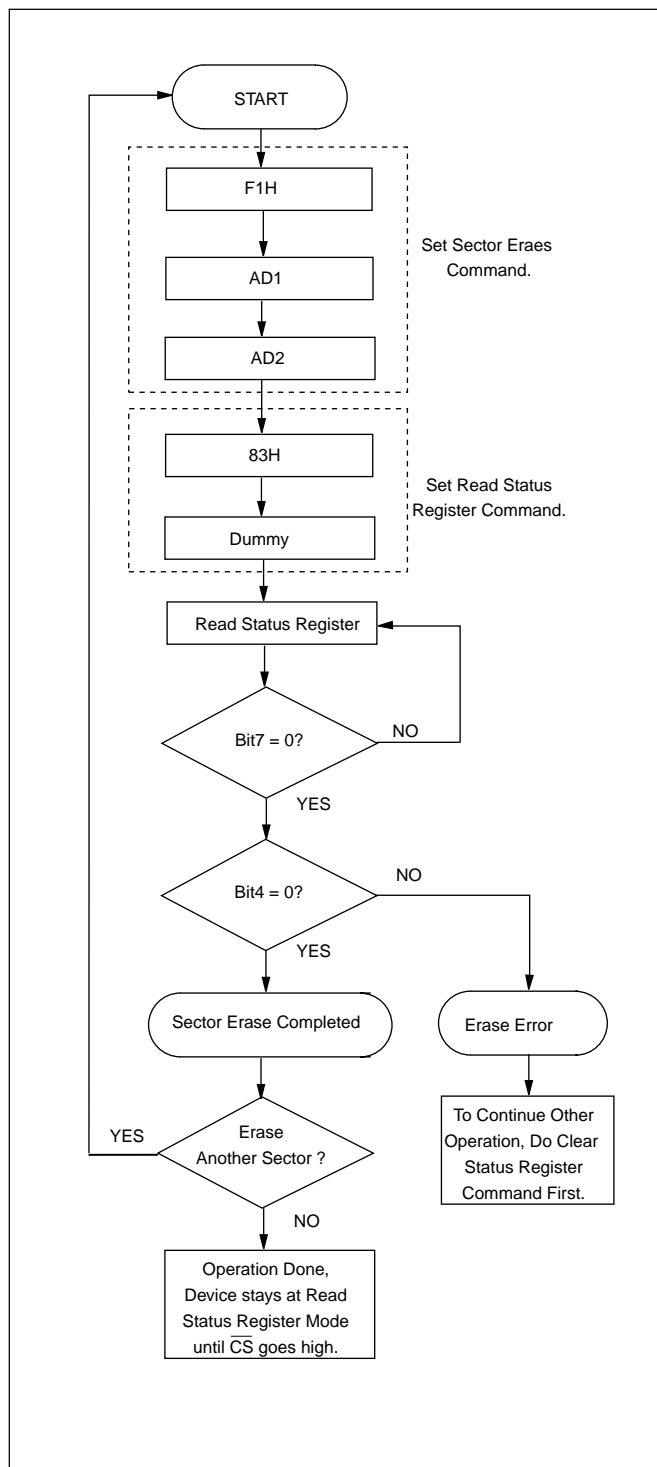


## Auto Chip Erase Flow Chart

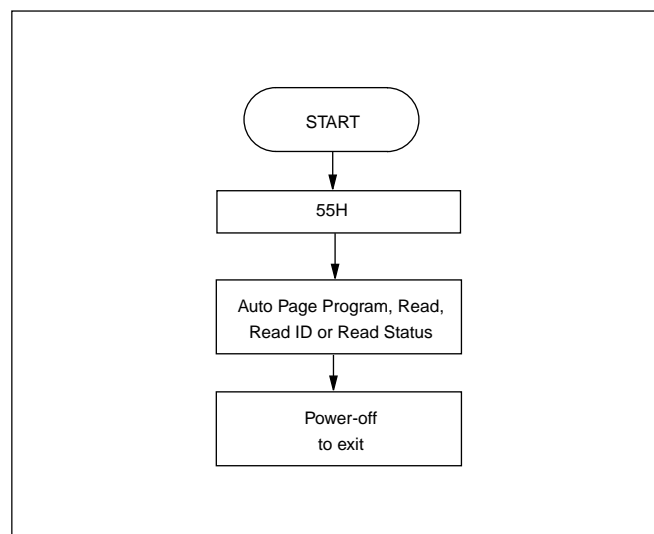




## Auto Sector Erase Flow Chart



## Parallel Mode for Read/Program Flow Chart



## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0° C to 70° C for Commercial grade -40° C to 85° C for Industrial grade
Storage Temperature	-55° C to 125° C
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

### NOTICE:

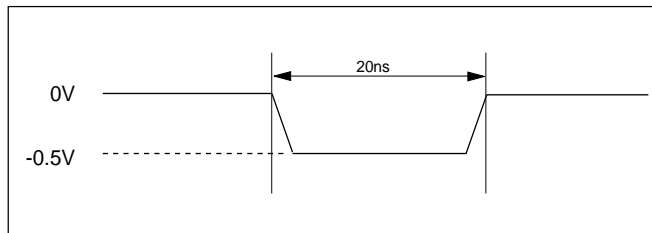
1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

2.Specifications contained within the following tables are subject to change.

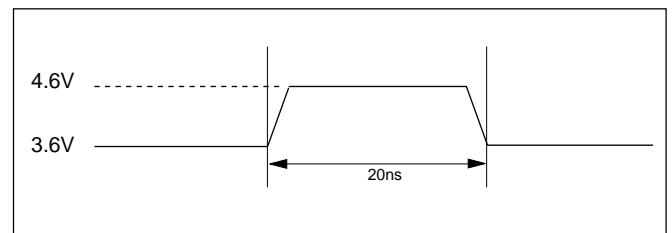
3.During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.

4.All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

### Maximum Negative Overshoot Waveform



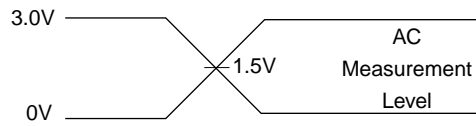
### Maximum Positive Overshoot Waveform



### CAPACITANCE TA = 25° C, f = 1.0 MHz

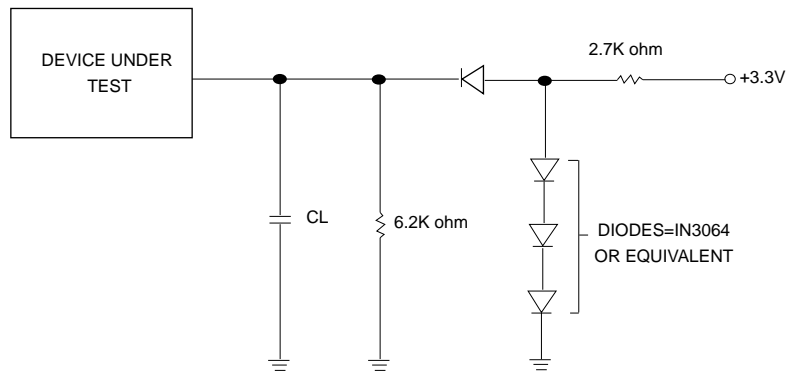
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			10	pF	VOUT = 0V

## INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are < 10ns

## OUTPUT LOADING



CL=50pF Including jig capacitance

**DC CHARACTERISTICS** (Temperature = -40° C to 85° C for Industrial grade, VCC = 2.7V ~ 3.6V)  
(Temperature = 0° C to 70° C for Commercial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1,3			± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			± 10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current(CMOS)	1		5	50	uA	VCC = VCC Max CS# = VCC ± 0.2V
ISB2	VCC Standby Current(TTL)			1	3	mA	VCC = VCC Max CS# = VIH
ICC1	VCC Read	1		24	29	mA	f=25MHz (serial) f=1.25MHz (parallel)
ICC2	VCC Program Current	1		35	60	mA	Program in Progress
ICC3	VCC Erase Current	1		35	70	mA	Erase in Progress
ICC4	VCC Reset Current	1		5	50	uA	RESET# = GND ± 0.3V
VHH	Voltage for ACC Program Acceleration	1	11.5		12.5	V	VCC=3.0V~3.6V
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.5	V	
VOL	Output Low Voltage				0.4	V	IOL = 500uA, VCC=2/3 x VCC
VOH	Output High Voltage		0.8VCC			V	IOH = -100uA, VCC=VCC min.

**NOTES:**

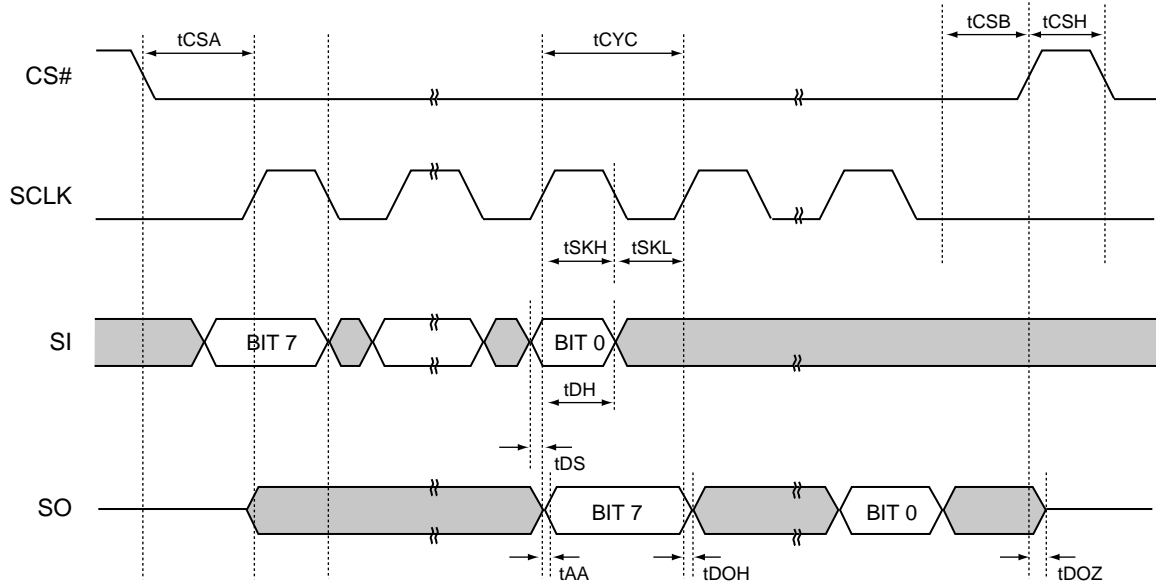
1. Typical values at VCC = 3.3V, T = 25° C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. For the DU pin only, the maximum input load current is ±5uA when DU pin=VIL (there is weak pull-up resistor from VCC to DU pin.)

**AC CHARACTERISTICS** (Temperature = -40° C to 85° C for Industrial grade, VCC = 2.7V ~ 3.6V)  
(Temperature = 0° C to 70° C for Commercial grade, VCC = 2.7V ~ 3.6V)

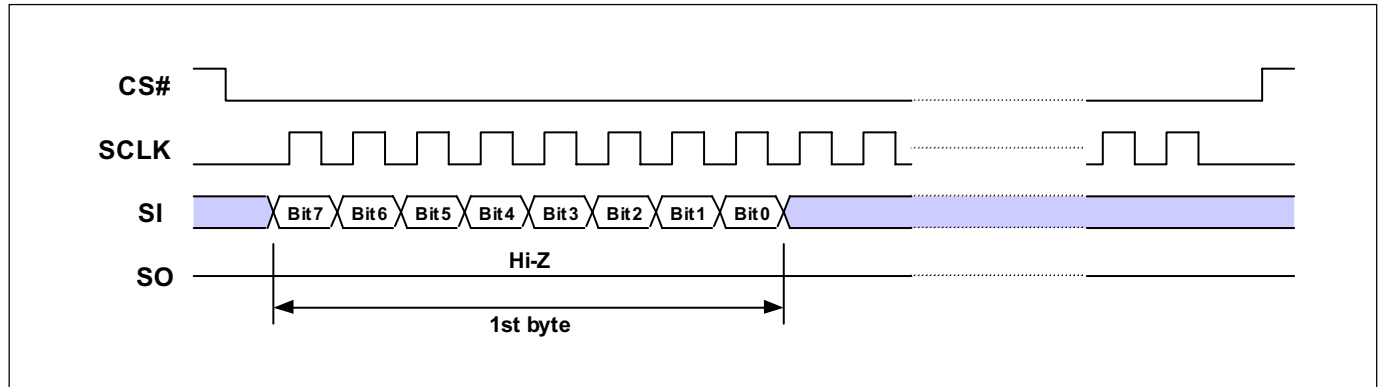
SYMBOL	PARAMETER		Min.	Typ.	Max.	Units	Condition
fSCLK	Clock Frequency	Serial			25	MHz	
		Parallel			1.25	MHz	
tCYC	Clock Cycle Time	Serial	40			ns	
		Parallel	800			ns	
tSKH	Clock High Time	Serial	20			ns	
		Parallel	400			ns	
tSKL	Clock Low Time	Serial	20			ns	
		Parallel	150			ns	
tR	Clock Rise Time	Serial			5	ns	f=25MHz
		Parallel			100	ns	f=1.25MHz
tF	Clock Fall Time	Serial			5	ns	f=25MHz
		Parallel			100	ns	f=1.25MHz
tCSA	CS# Lead Clock Time		40			ns	
tCSB	CS# Lag Clock Time		40			ns	
tCSH	CS# High Time		80			ns	
tCSR	CS# Rise Time				50	ns	
tCSF	CS# Fall Time				50	ns	
tCSHR	RESET# High Time to Write Command Valid		500			ns	
tRP	RESET# Pulse Width		500			ns	
tRST	RESET# Rise Time				100	us	
tRFT	RESET# Fall Time				100	us	
tDS	SI Setup Time		5			ns	
tDH	SI Hold Time		20			ns	
tAA	Access Time	Serial			30	ns	
		Parallel			50	ns	
tDOH	SO Hold Time		5			ns	
tDOZ	SO Floating Time		0		20	ns	

**NOTES:**

1. Typical value is calculated by simulation.

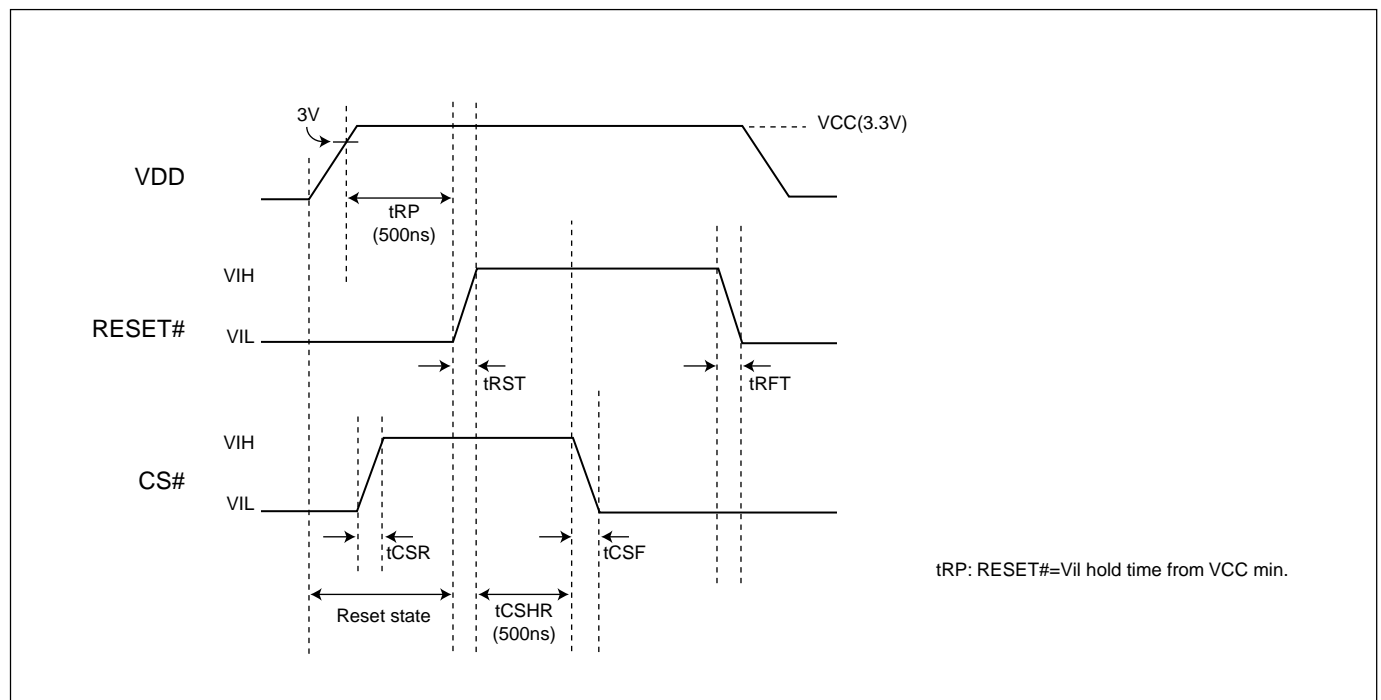
**SERIAL DATA INPUT/OUTPUT TIMING**


## STANDBY TIMING WAVEFORM

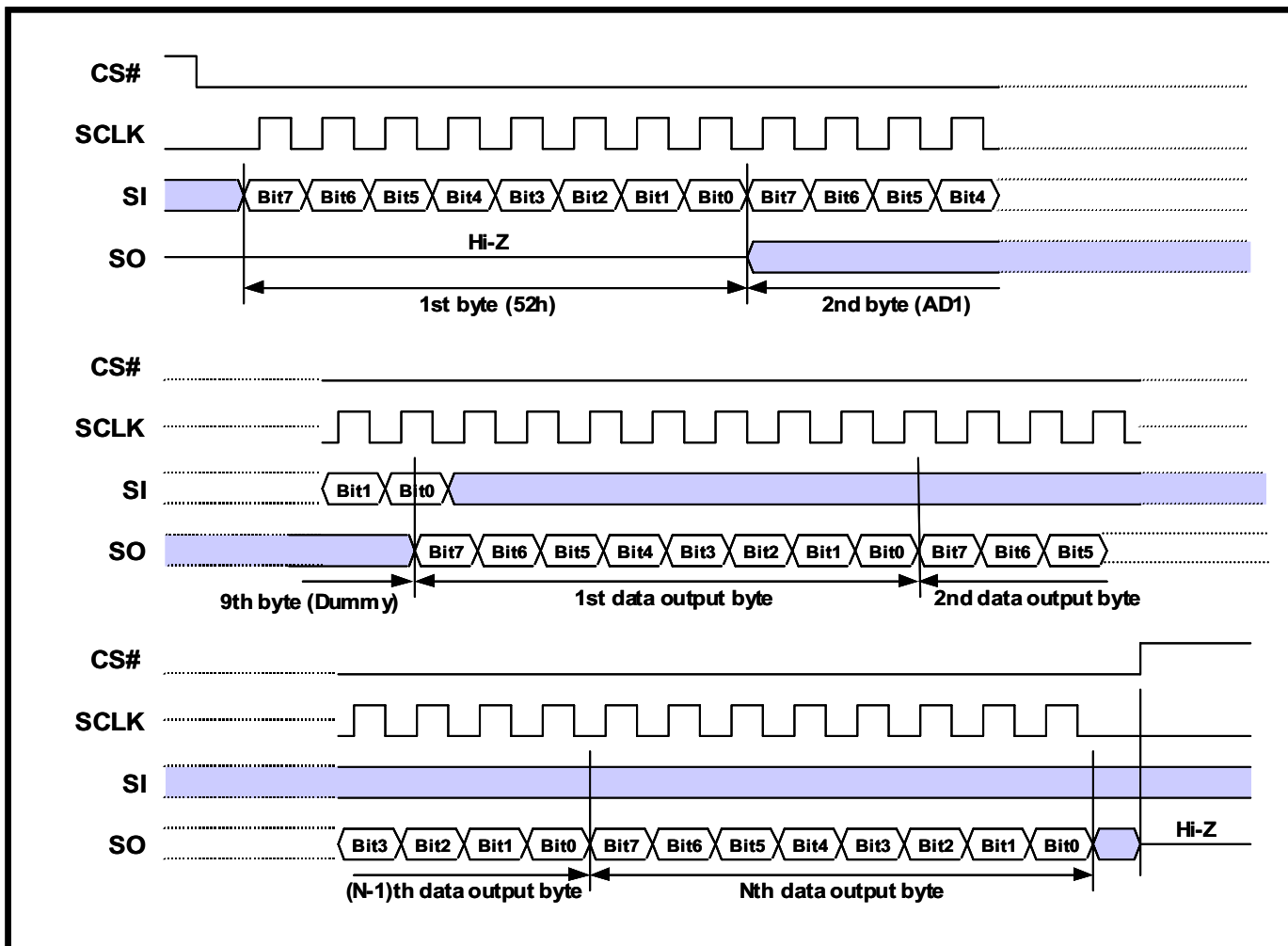


When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z. While CS#=VIH, current=standby current, while CS#=VIL and commands are issuing, or commands are invalid, current=24mA(typ.) to 29mA(max.).

## RESET# TIMING WAVEFORM



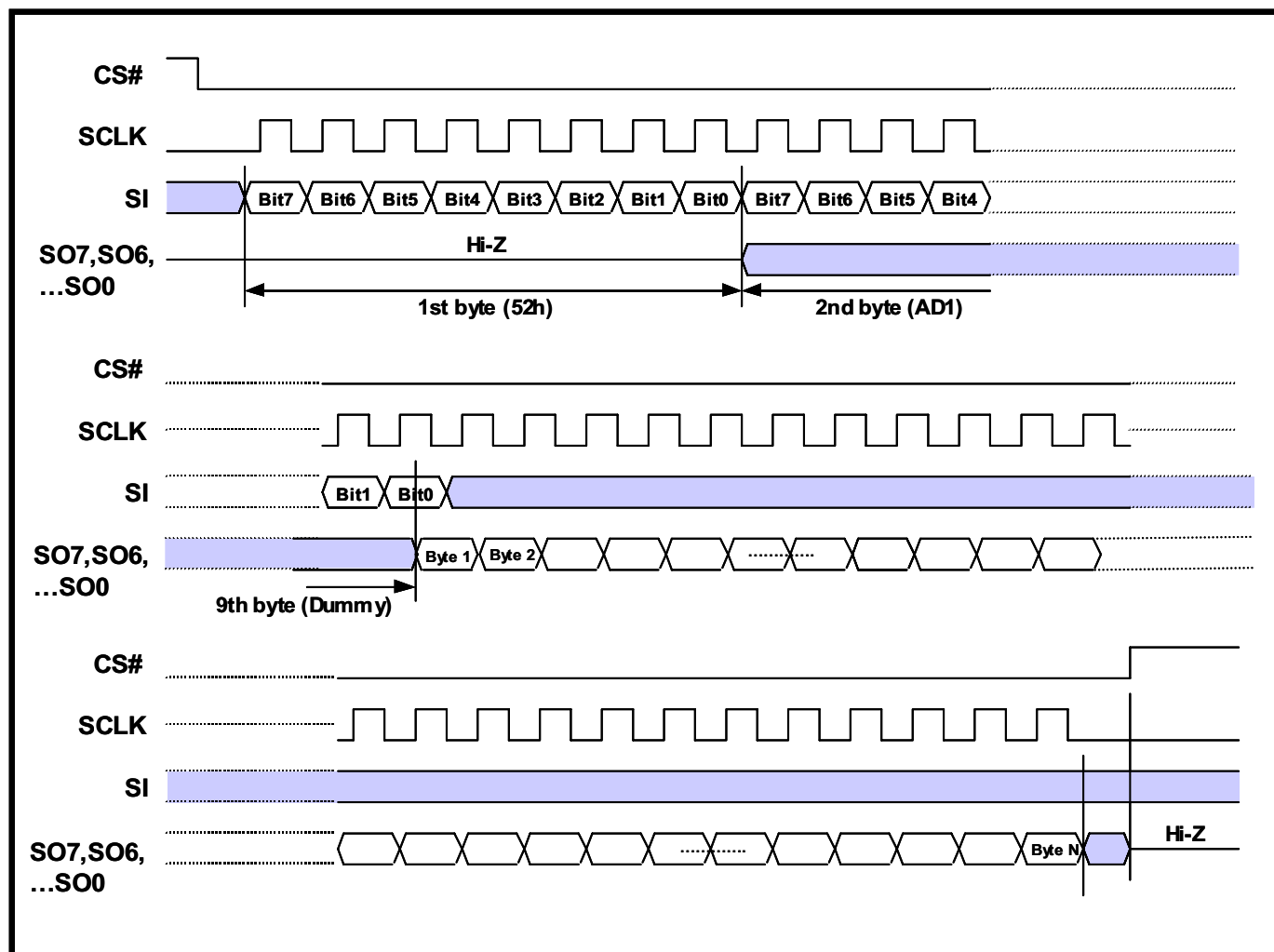
## READ ARRAY TIMING WAVEFORM (Serial)



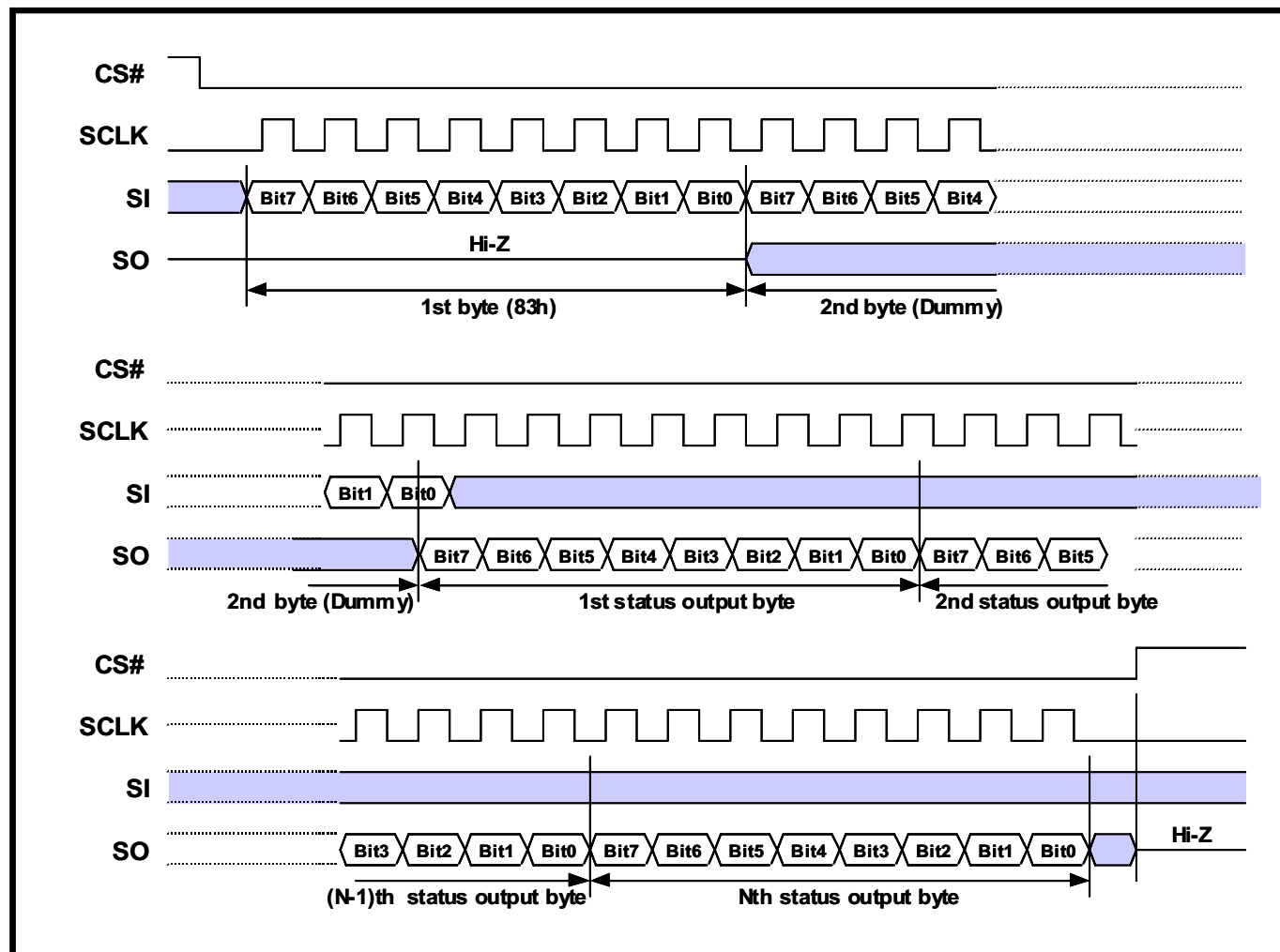
### NOTES:

1. 1st Byte='52h'
2. 2nd Byte=Address 1(AD1), A17=BIT 0, A18=BIT1, A19=BIT2, A20=BIT3, A21=BIT4, A22=BIT5.
3. 3rd Byte=Address 2(AD2), A9=BIT0, A10=BIT1,.....A16=BIT7
4. 4th Byte=Address 3(AD3), A7=BIT0, A8=BIT1
5. 5th Byte=Byte Address(BA), A0=BIT0, A1=BIT1,.....A6=BIT6
6. 6th-9th Bytes for SI ==> Dummy Bytes (Don't care)
7. From Byte 10, SO Would Output Array Data

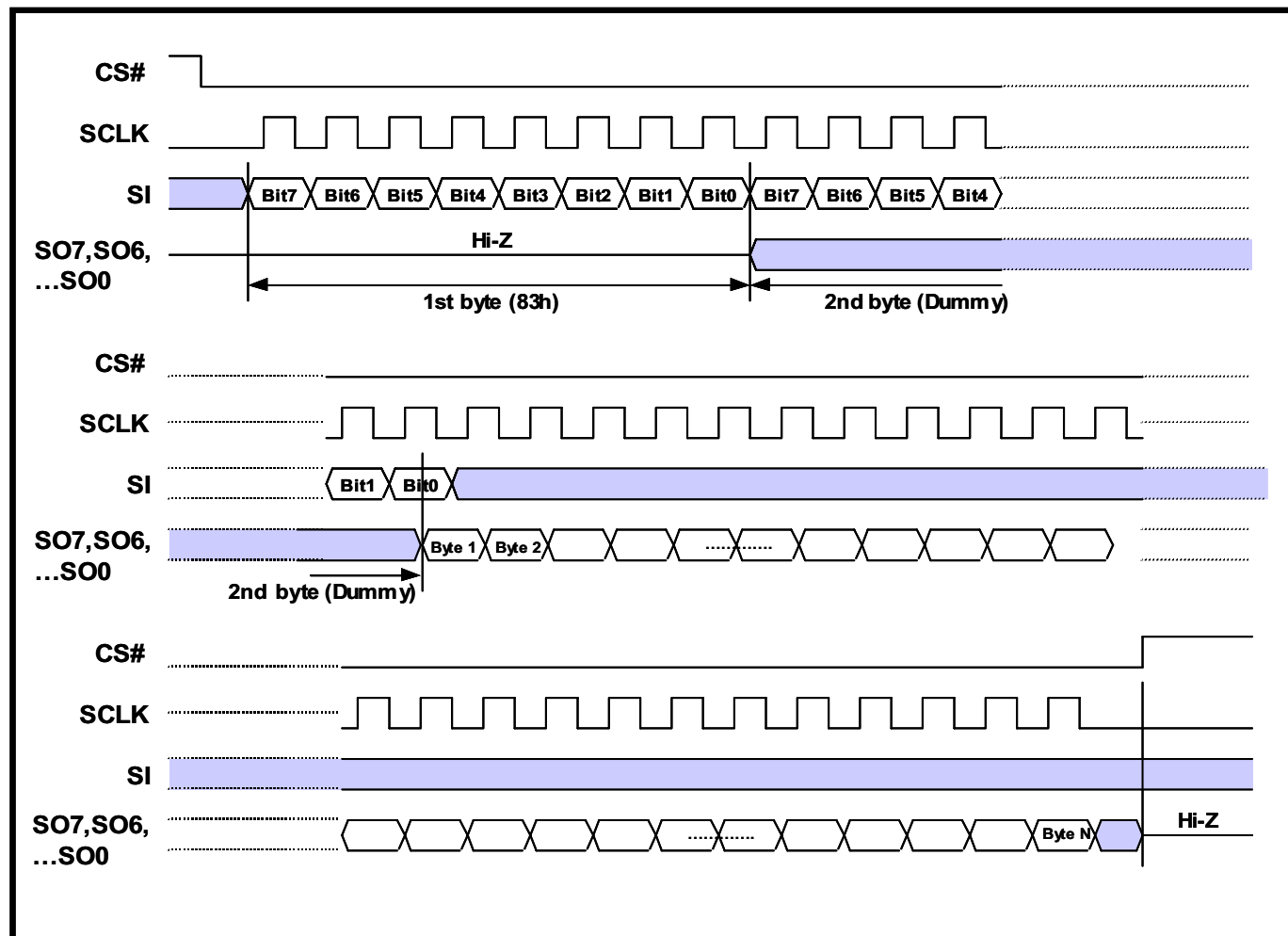


**READ ARRAY TIMING WAVEFORM (Parallel)**

**NOTES:**

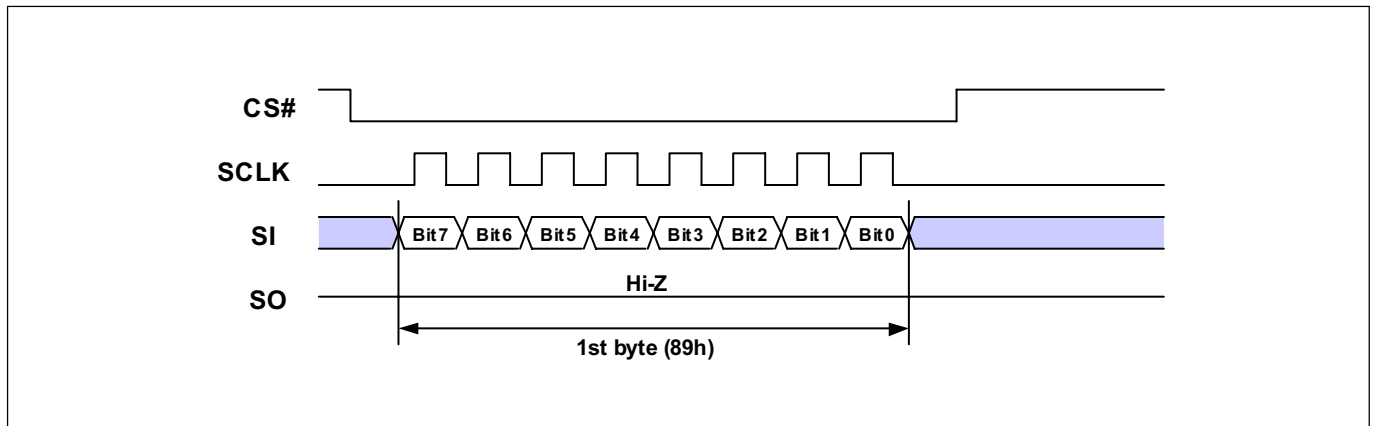
1. 1st Byte='52h'
2. 2nd Byte=Address 1(AD1), A17=BIT 0, A18=BIT1, A19=BIT2, A20=BIT3, A21=BIT4, A22=BIT5.
3. 3rd Byte=Address 2(AD2), A9=BIT0, A10=BIT1,.....A16=BIT7.
4. 4th Byte=Address 3(AD3), A7=BIT0, A8=BIT1.
5. 5th Byte=Byte Address(BA), A0=BIT0, A1=BIT1,.....A6=BIT6.
6. 6th-9th Bytes for SI ==> Dummy Bytes (Don't care).
7. From Byte 10, SO Would Output Array Data.
8. Under parallel mode, the fastest access clock freq. will be changed to 1.25MHz(SCLK pin clock freq.).
9. To read array in parallel mode requires a parallel mode command (55H) before the read command.  
Once in the parallel mode, eLite Flash™ Memory will not exit parallel mode until power-off.

**READ STATUS REGISTER TIMING WAVEFORM (Serial)**

**NOTES:**

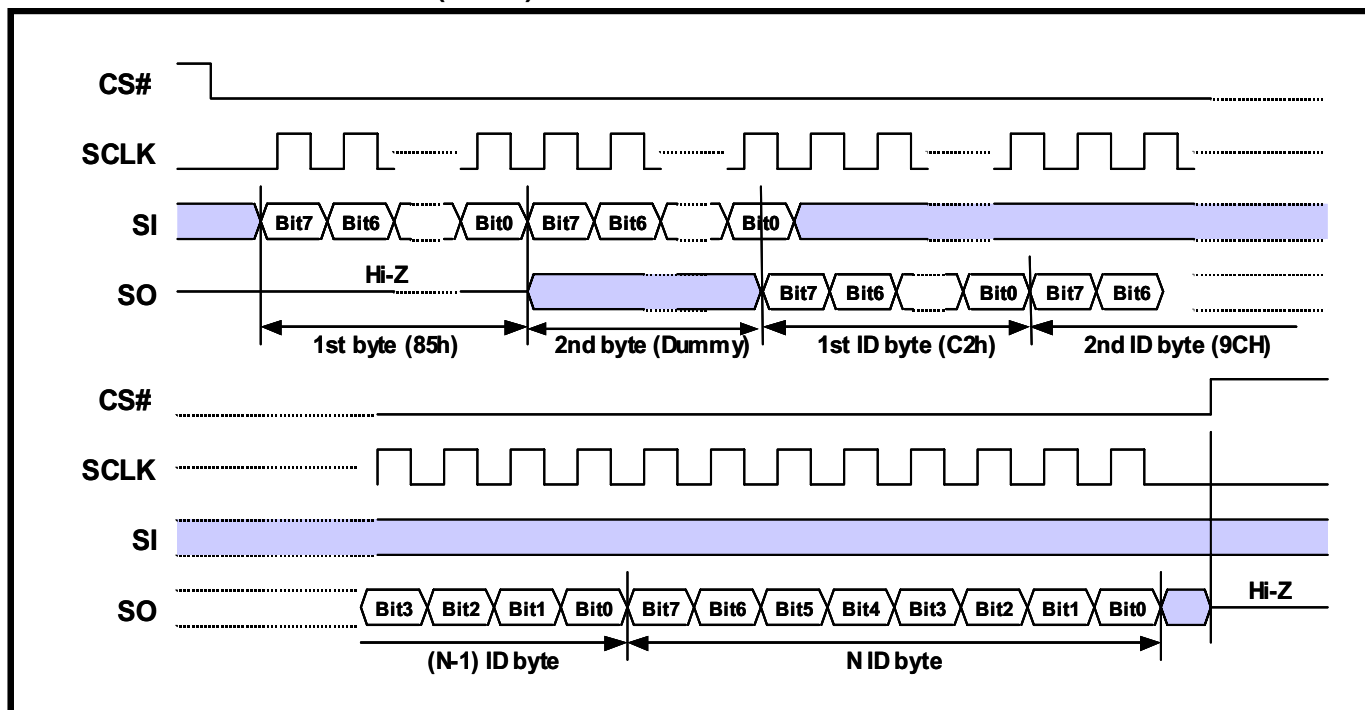
1. BIT 7=0 ==> Program/Erase completed
2. BIT 4=1 ==> Erase Error
3. BIT 3=1 ==> Program Error
4. BIT 1,2,5 ==> Reserve for future use
5. BIT 0=1 ==> Device is in ready state
6. BIT 6=0 ==> Device is not in parallel mode

**READ STATUS REGISTER TIMING WAVEFORM (Parallel)**

**NOTES:**

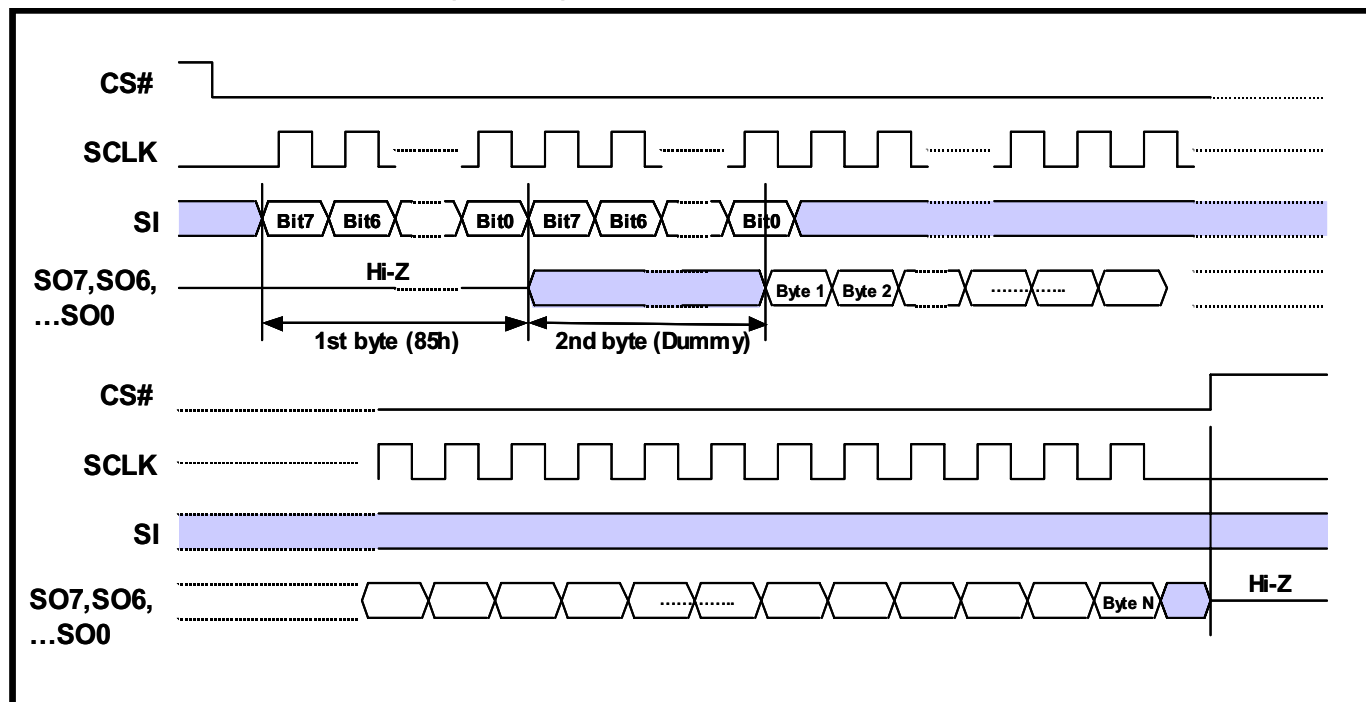
1. BIT 7=0 ==> Program/Erase completed
2. BIT 6=0 ==> Device is not in parallel mode
2. BIT 4=1 ==>Erase Error
3. BIT 3=1 ==>Program Error
4. BIT 1,2,5 ==> Reserve for future use
5. Bit 0=1 ==> Device is in ready state
6. Under parallel mode, the fastest access clock freq. will be changed to 1.25MHz(SCLK pin clock freq.).
7. To read status register in parallel mode, which requires a parallel mode command (55H) before the read status register command.  
Once in the parallel mode, eLite Flash™ Memory will not exit parallel mode until power-off.

**CLEAR STATUS REGISTER TIMING WAVEFORM****NOTES:**

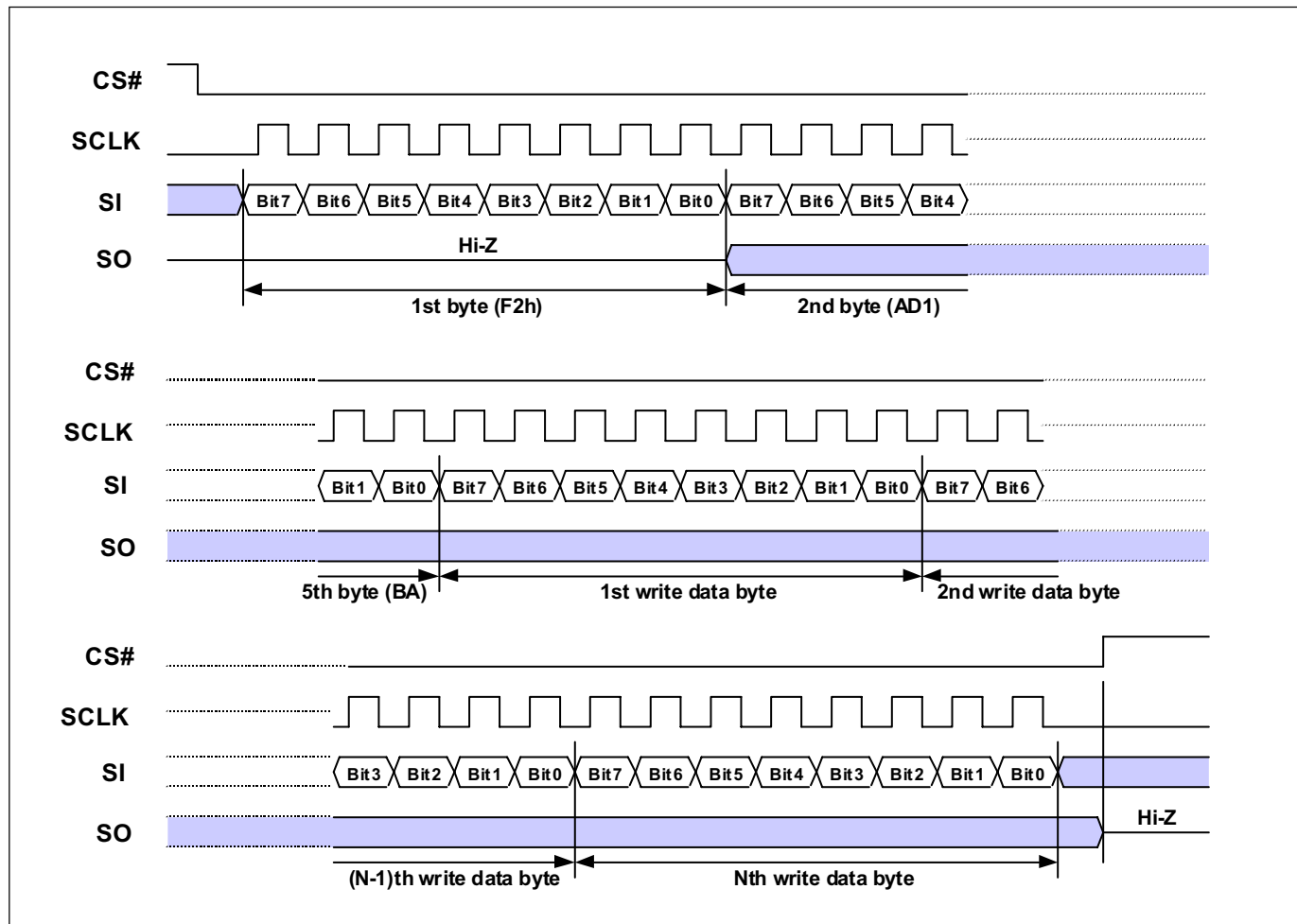
1. 1st Byte='89h' ==> CLEAR STATUS REGISTER
2. SO at Hi-Z state

**READ ID TIMING WAVEFORM (Serial)**

**NOTES:**

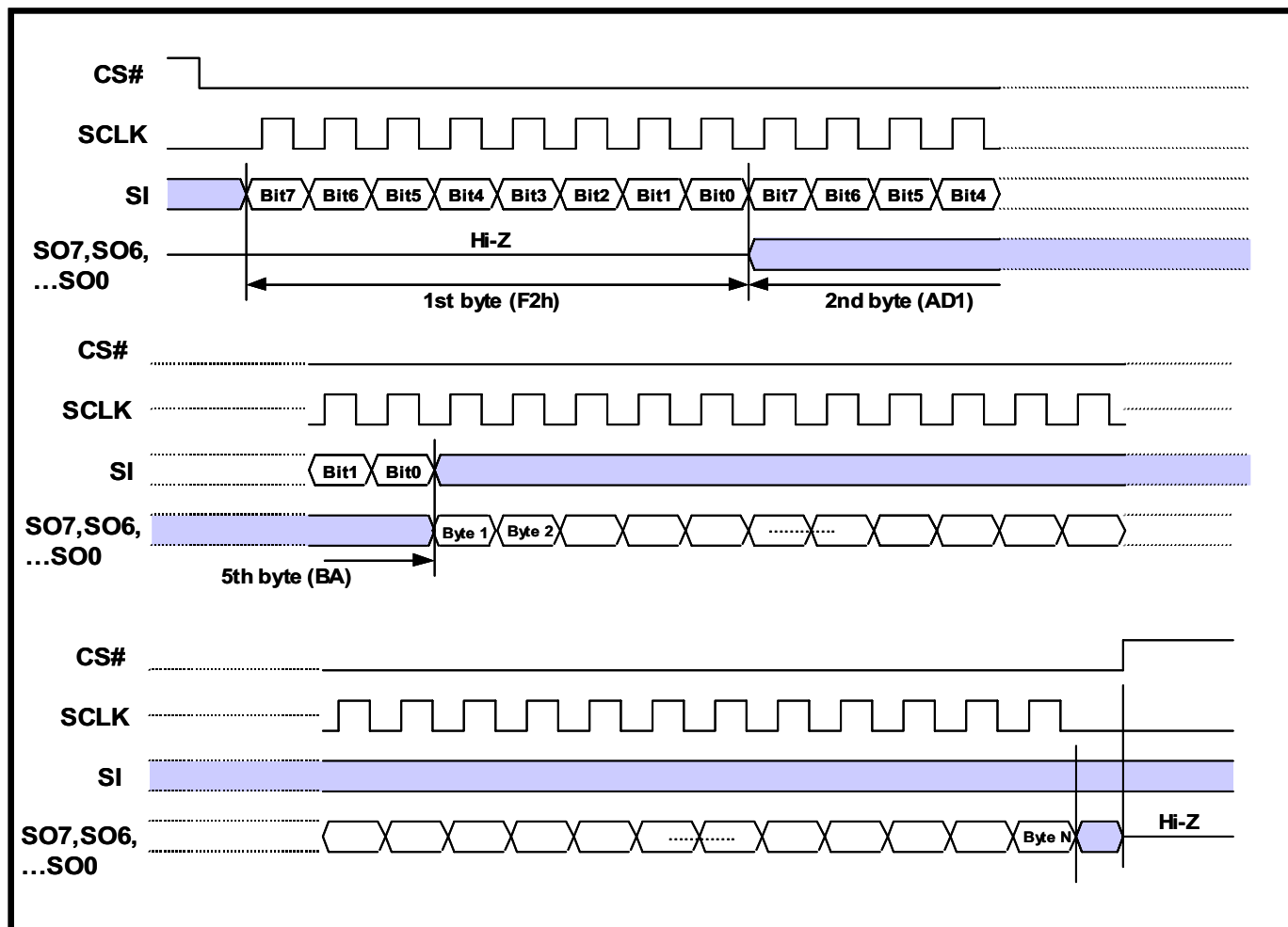
1. 1st Byte:85h.
2. 2nd Byte:Dummy Byte.
3. 3rd Byte:Output Manufacture Code(C2h).
4. 4th Byte:Output Device Code(9CH).
5. The 2 bytes ID output will be wrap around.

**READ ID TIMING WAVEFORM (Parallel)**

**NOTES:**

1. 1st Byte:85h.
2. 2nd Byte:Dummy Byte.
3. 3rd Byte:Output Manufacture Code(C2h).
4. 4th Byte:Output Device Code(9CH).
5. The 2 bytes ID output will be wrap around.
6. Under parallel mode, the fastest access clock freq. will be changed to 1.25MHz(SCLK pin clock freq.).
7. To read ID in parallel mode, which requires a parallel mode command (55H) before the read ID command. Once in the parallel mode, eLite Flash™ Memory will not exit parallel mode until power-off.

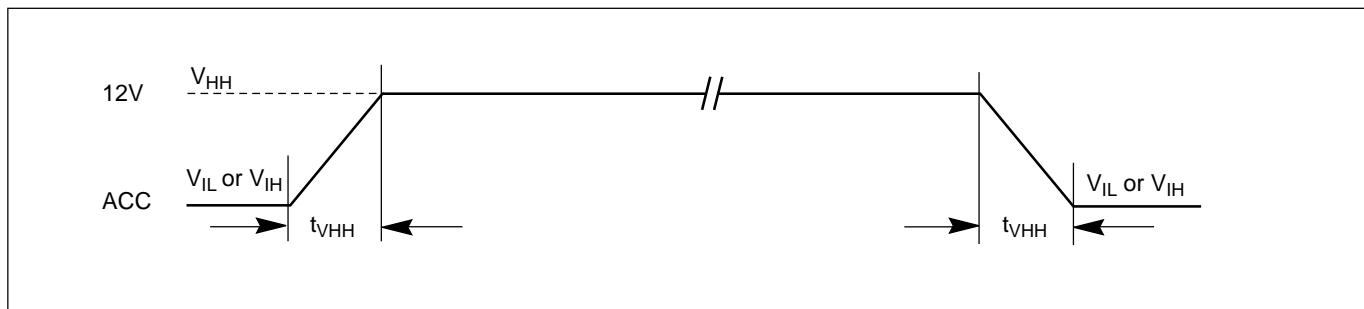
**AUTO PAGE PROGRAM TIMING WAVEFORM (Serial)**

**NOTES:**

1. 1st Byte:F2h.
2. 2nd Byte:Address AD1.
3. 3rd Byte:Address AD2
4. 4th Byte:Address AD3
5. 5th Byte:Address BA.
6. 6th byte:1st write data byte.
7. When the last byte of the page will be written, the Byte Address will be wrap around to the first byte of the Page.
8. The 128-byte page address (A6~A0) must start from 0.

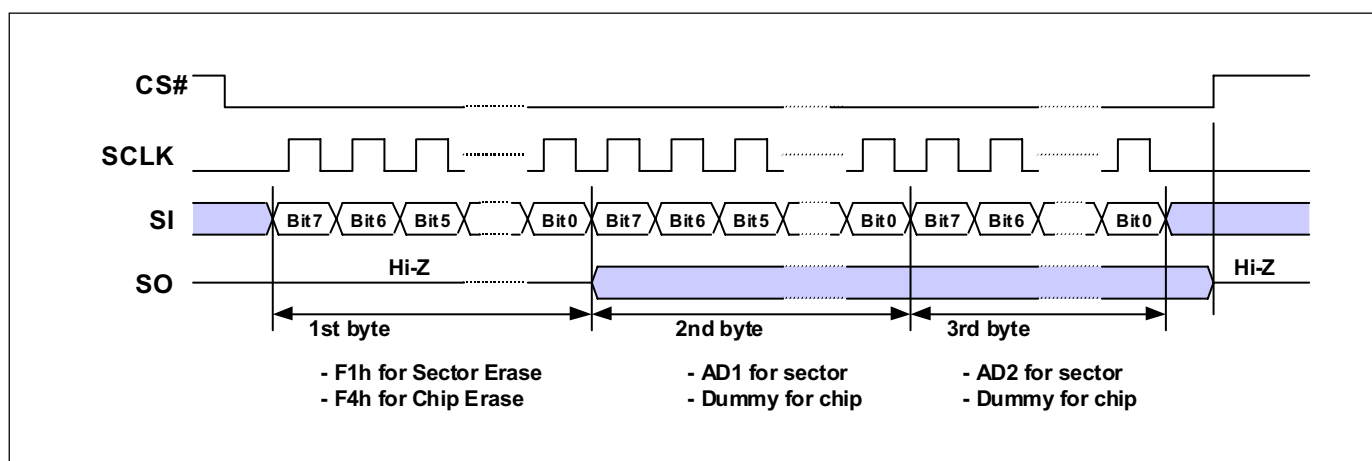
**AUTO PAGE PROGRAM TIMING WAVEFORM (Parallel)**

**NOTES:**

1. 1st Byte:F2h.
2. 2nd Byte:Address AD1.
3. 3rd Byte:Address AD2
4. 4th Byte:Address AD3
5. 5th Byte:Address BA.
6. 6th byte:1st write data byte.
7. When the last byte of the page will be written, the Byte Address will be wrap around to the first byte of the Page.
8. The 128-byte page address (A6~A0) must start from 0.
9. Under parallel mode, the fastest access clock freq. will be changed to 1.25MHz(SCLK pin clock freq.).
10. To program in parallel mode, which requires a parallel mode command (55H) before the page program command. Once in the parallel mode, eLite Flash™ Memory will not exit parallel mode until power-off.



**ACCELERATED PROGRAM TIMING DIAGRAM**


Note:  $t_{VHH}$  ( $V_{HH}$  Rise and Fall Time) min. 250ns

**AUTO SECTOR/CHIP ERASE TIMING WAVEFORM**

**NOTES:**

1. 1st byte:F1h for Sector Erase.
2. 2nd byte:Address AD1 for Sector Erase, Dummy byte for chip erase.
3. 3rd byte:Address AD2 for Sector Erase, Dummy byte for chip erase.

**ERASE AND PROGRAMMING PERFORMANCE**

PARAMETER	TYP. (1)	Max. (2)	UNIT	Comments
Chip Erase Time	160	512	s	Note (4)
Chip Erase Time (with ACC=12V)	128	410	s	Note (4)
Sector erase Time	2	16	s	Note (4)
Sector erase Time (with ACC=12V)	1.6	13	s	Note (4)
Page Programming Time	2	8	mS	Excludes system level overhead(3)
Page Programming Time (with ACC=12V)	1.6	6.4	mS	
Chip Programming Time	240	480	s	Excludes system level overhead(3)
Chip Programming Time (with ACC=12V)	180	360	s	

Note:

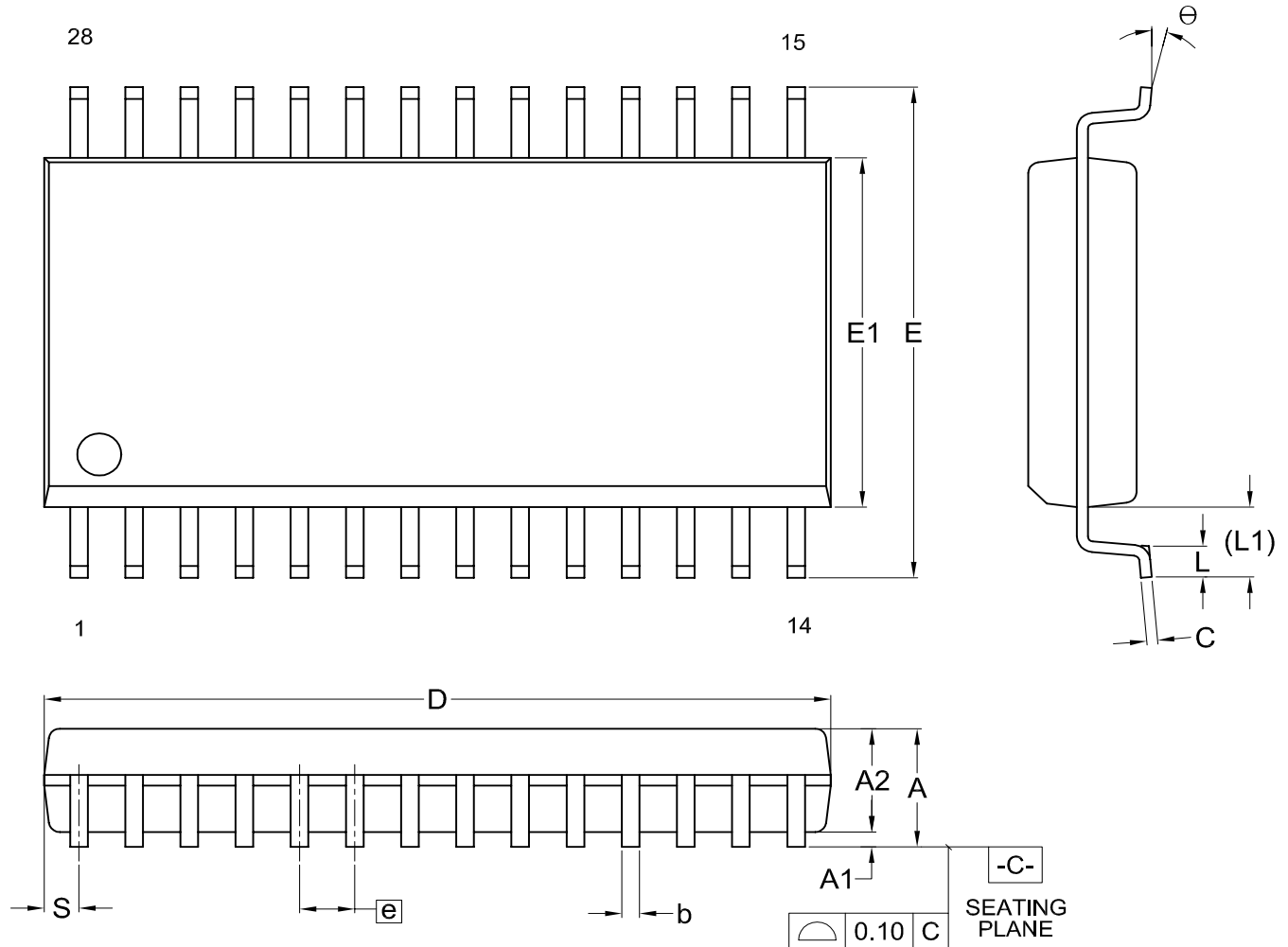
1. Typical program and erase time assumes the following conditions: 25° C, 3.0V, and all bits are programmed by checker-board pattern.
2. Under worst conditions of 70° C and 3.0V. Maximum values are up to including 100 program/erase cycles.
3. System-level overhead is the time required to execute the command sequences for the page program command.
4. Excludes 00H programming prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bits are programmed to 00H before erasure)

**LATCH-UP CHARACTERISTICS**

	MIN.	MAX.
Input Voltage with respect to GND on ACC	-1.0V	12.5V
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

**ORDERING INFORMATION**

<b>PART NO.</b>	<b>Access Time</b>	<b>Operating Current</b>	<b>Standby Current</b>	<b>Temperature Range</b>	<b>Package</b>	<b>Remark</b>
MX25L6402AMC-40	25MHz	24mA	50uA	0° C to 70° C	28 pin SOP (330 mil)	
MX25L6402AMC-40G	25MHz	24mA	50uA	0° C to 70° C	28 pin SOP (330 mil)	Pb-free
MX25L6402AMI-40	25MHz	24mA	50uA	-40° C to 85° C	28 pin SOP (330 mil)	
MX25L6402AMI-40G	25MHz	24mA	50uA	-40° C to 85° C	28 pin SOP (330 mil)	Pb-free

**PACKAGE INFORMATION**
**Title: Package Outline for SOP 28L (330MIL)**


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
UNIT														
mm	Min.	—	0.10	2.39	0.36	0.20	17.98	11.61	8.28		0.56	1.51	0.67	0
	Nom.	—	0.15	2.49	0.41	0.25	18.11	11.81	8.40	1.27	0.76	1.71	0.80	5
	Max.	2.84	0.25	2.59	0.51	0.30	18.24	12.02	8.53		0.96	1.91	0.92	8
Inch	Min.	—	0.004	0.094	0.014	0.008	0.708	0.457	0.326		0.022	0.059	0.026	0
	Nom.	—	0.006	0.098	0.016	0.010	0.713	0.465	0.331	0.050	0.030	0.067	0.031	5
	Max.	0.112	0.010	0.102	0.020	0.012	0.718	0.473	0.336		0.038	0.075	0.036	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1403	8	MO-059			11-26-'03



## REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed title "Preliminary" on page 1	P1	SEP/29/2004



**MX25L6402A**

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