



ispMACH 4000ZE Pico Development Kit

User's Guide

Introduction

Thank you for choosing the Lattice Semiconductor ispMACH® 4000ZE Pico Development Kit!

This user's guide describes how to start using the ispMACH 4000ZE Pico Development Kit, an easy-to-use platform for evaluating and designing with the LC4256ZE CPLD. Along with the evaluation board and accessories, this kit includes a pre-loaded Pico Power demonstration design. You may also reprogram the on-board LC4256ZE and ispPAC®-POWR6AT6 devices to review your own custom designs.

Note: Static electricity can severely shorten the lifespan of electronic components. See the [ispMACH 4000ZE Pico Development Kit QuickSTART Guide](#) for handling and storage tips.

Features

The ispMACH 4000ZE Pico Development Kit includes:

- **ispMACH 4000ZE Pico Evaluation Board** - The Pico board is a 2.5" x 2" form factor that features the following on-board components and circuits:
 - ispMACH 4256ZE CPLD (LC4256ZE-5MN144C)
 - Power Manager II ispPAC-POWR6AT6 mixed-signal PLD (ispPAC-POWR6AT6-01NN32I)
 - High-side current sensor circuits
 - Battery or USB power
 - LCD panel
 - USB B-mini connector for power and programming
 - 15x2 expansion header landing for general IO, I²C, and JTAG
 - Keyboard-style DIP switch bank
 - Push-button input
 - 3.3V and 1.8V supply rails
 - Optional battery recharge circuit
- **Pre-loaded Pico Power Demo** – The kit includes a pre-loaded demo design that highlights key CPLD applications and power-saving design methods that maximize battery life.
- **USB Connector Cable** – The Pico board is powered from the mini B USB socket when connected to a host PC. The USB channel also provides a programming interface to the LC4256ZE and POWR6AT6 JTAG ports.
- **QuickSTART Guide** – Provides information on connecting the Pico board, running the pre-loaded Pico Power demo.
- **ispMACH 4000ZE Pico Development Kit Web Page** – The ispMACH 4000ZE Pico Development Kit web page (www.latticesemi.com/4000ze-pico-kit) provides access to the latest documentation (including this guide), demo designs, and drivers for the kit.

The contents of this user's guide include demo operation, programming instructions, top-level functional descriptions of the evaluation board, descriptions of the on-board connectors, switches and a complete set of schematics of the Pico board.

Figure 1. Pico Evaluation Board, Top Side

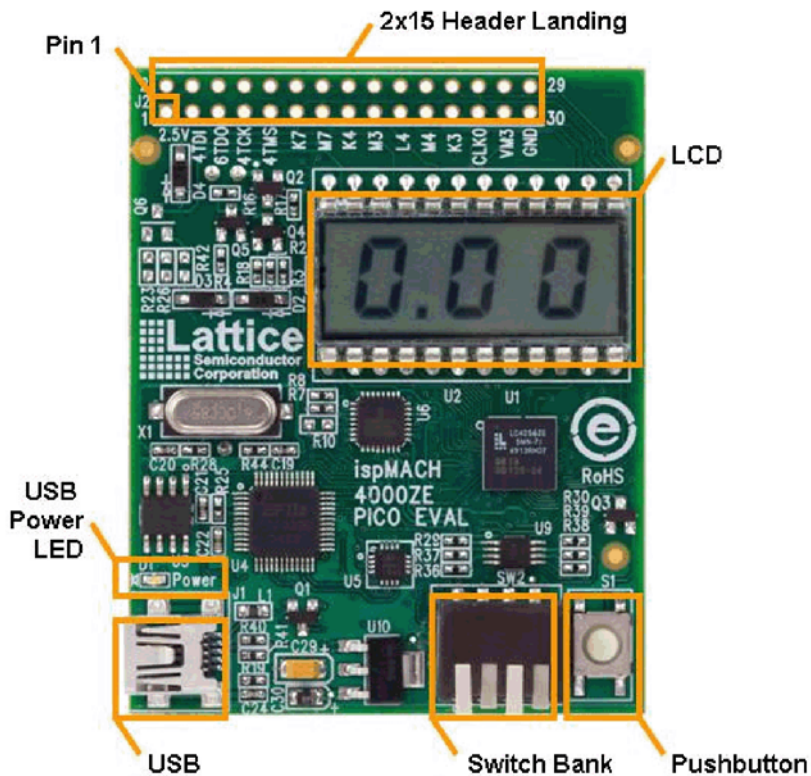
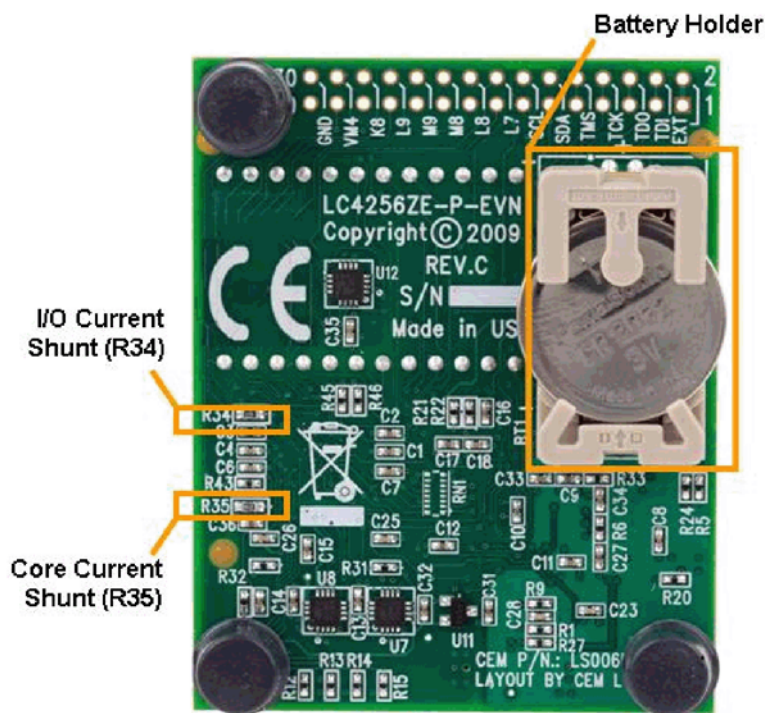


Figure 2. Pico Evaluation Board, Bottom Side



Software Requirements

Install the following software before you begin developing designs for the evaluation board:

- ispLEVER® Classic 1.3 (ispMACH 4000ZE CPLD support)
- PAC-Designer® 5.1 (ispPAC-POWR6AT6 mixed-signal PLD support)
- ispVM™ System 17.5 (Required for re-programming on-board PLDs)
- PicoView 1.04 (Required for the I²C GPIO Expansion Demo)

ispMACH 4000ZE Device

This board features the ispMACH 4000ZE CPLD which is ideal for ultra low-power, high-volume portable applications. The on-board LC4256ZE is the highest capacity of the family with 256 macrocells. The 144-pin csBGA package provides 108 user I/Os and four dedicated inputs in a 7mm x 7mm package. The LC4256ZE consumes standby current as low as 15µA. A complete description of this device can be found in the [ispMACH 4000ZE Family Data Sheet](#).

Demonstration Designs

Lattice provides two demos that illustrate key applications of the ispMACH 4000ZE CPLD device in the context of a consumer electronics application:

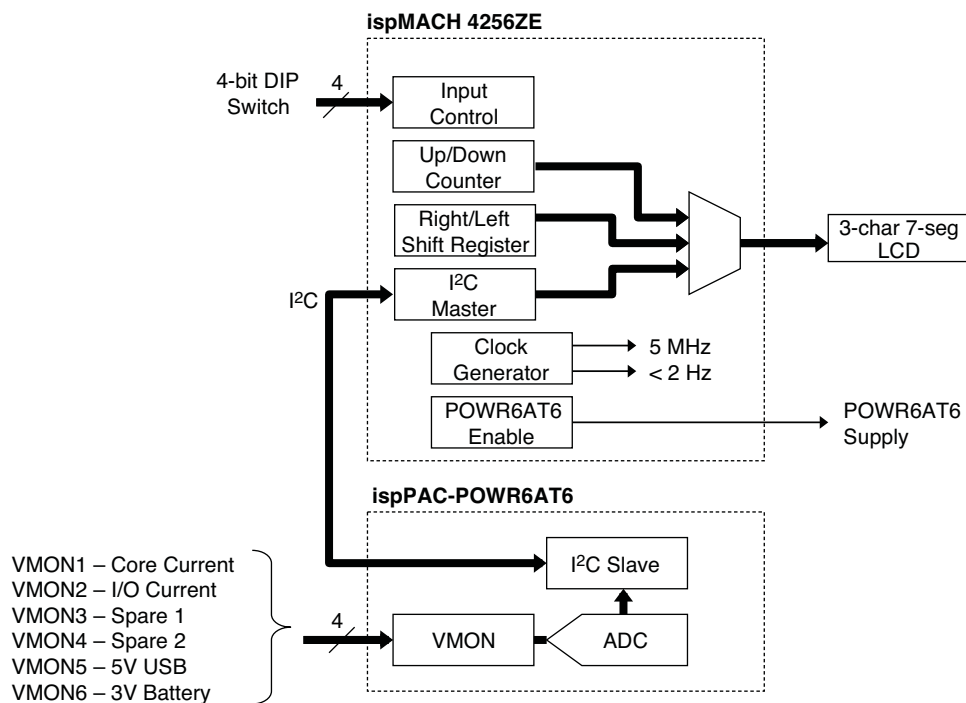
- **Pico Power** – Integrates an up/down counter, a right/left shift register, voltage/current meter display, and an I²C bus master controller that communicates with the on-board POWR6AT6 Power Manager II device. The POWR6AT6 provides analog power supply monitoring and a 2-wire I²C interface to measure various voltage supplies of the board. An LCD panel displays demo output using three characters. You can select demo features with the keyboard-style 4-bit DIP switch bank. The Pico Power demo is designed for battery operation but if one isn't available you can power the board by connecting the USB cable provided to a PC USB port.
- **GPIO I²C Expansion** – Shows an application of the LC4256ZE device as an I²C slave processing instructions issued by a CPU/MPU. CPLDs are ideal GPIO “expanders” for processors. Control registers of the CPLD's I²C module allow the processor to access counter and shift registers, I/O, and power measurements. An I²C software interface utility, PicoView, emulates the CPU/MPU component of the system. Visit www.latticesemi.com/4000ze-pico-kit to download PicoView.

Note: It is possible that you will obtain your Pico board after it has been reprogrammed. To restore the factory default demo and program it with other Lattice-supplied examples, see the Download Demo Designs section of this document.

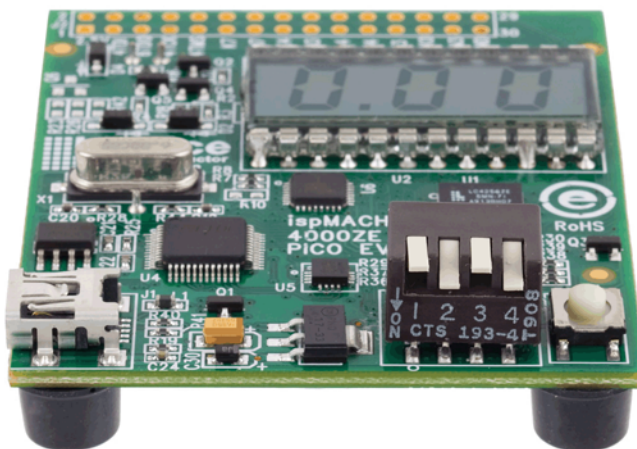
Pico Power Demo

The Pico Power design highlights low-power features of the LC4256ZE CPLD along with inexpensive PCB design techniques that help extend battery life, such as low-speed CPLD clocking, efficient use of the CPLD I/O cell's I/O bus maintenance feature, and gated supply rails. The demo design integrates an I²C master reference design (www.latticesemi.com/products/intellectualproperty) with LCD controller logic, an up/down counter and left/right shift register modules. You may switch the LCD display between a current/voltage meter and counter/shifter operation using the DIP switch bank. The demo shows a clock generator based on the LC4256ZE on-chip oscillator and timer (OSCTIMER) hardware feature. The counter and shift register modules can be clocked at either <2 Hz or 5 MHz to help illustrate the difference in dynamic power demands.

Current and voltage monitoring of the Pico board is provided by the POWR6AT6 mixed-signal PLD and on-board sensor circuits (see AN6049, [High-side Current Sensing Techniques for Power Manager Devices](#)). To minimize power consumption of the overall system, the POWR6AT6 supply rail is powered on momentarily by the LC4256ZE whenever a current or voltage display is requested or after the Pico board is reset.

Figure 3. Pico Power Demo Block Diagram

The following tables describe the 4-bit DIP switch and push-button inputs that control the pre-configured Pico Power demo. Use them as a reference for the procedure you must follow in the next step. A switch in the raised position of the 4-bit DIP switch indicates a logic level '1' input to the LC4256ZE. Depress a switch to indicate a low logic level '0'.

Figure 4. Pico Board with 4-Bit DIP Switch Example (1010)

Switch 1234 (Demo)	Pico Power Demo Features
0000 (Up) 0001 (Down)	Decimal Up/Down Counter Display – Displays an 8-bit decimal up/down counter (0.0-9.9) using the <2 Hz clock generated by the LC4256ZE On-Chip Oscillator and Timer (OSCTIMER). A 4-bit nibble is committed to the “ones” and “tenths” position of the LCD. The down counter will be initialized to 9.9 and up counter to 0.0 upon power-up, reset or if the count rolls over.
Slow clock <2 Hz: 1100 (VMON1 lcccore) 1001 (VMON2 lccio) Fast Clock 5 MHz: 1000 (VMON1 lcccore)	Current Meter Display – Displays current measurements of the LC4256ZE 1.8V core and 2.5V I/O supply rails. To help illustrate the relative dynamic power requirements of the board at <2 Hz or 5 MHz, lcccore can be measured at both clock frequencies. The current meter circuit includes a high-side current sensor amp and the POWR6AT6 mixed-signal PLD which provides the voltage monitor, analog-to-digital conversion (ADC), and an I ² C slave to register the measurement. The entire circuit is dynamically energized whenever the current meter function is selected or the Pico board push-button is pressed. Note that the additional draw of the meter circuit is factored into the display latched into the LCD panel by the CPLD. This will result in an additional 100-600 microamp over static measurements taken on the board at the lcccore and lccio shunts R35 and R34.
0010 (Shift Left) 0011 (Shift Right)	Left/Right Shift Register Display – Displays a shift register operating as serial-in, parallel-out using the <2 Hz clock source. Each bit of the register is associated with the corresponding segment of the 7-segment LCD such that reg(21) = Segment 7 of the left-most character and reg(0) = Segment 1 of the right-most character. When shifting left, the register will shift in '0' to the MSB upon each clock. When shifting right the register shifts in '0' to the LSB. The shift register will be initialized to 1FFFFEH upon power-up, reset, or if the shift result rolls over.
1010 (VMON5 5V USB) 1011 (VMON6 3V Battery)	Volt Meter – Displays voltage measurements of the 5V USB interface or the 3V button-cell battery. The volt meter function dynamically activates the POWR6AT6 supply rail in the same manner as the Current Meter Display function.
1111 (Standby)	Standby Mode (Default) – Demonstrates standby power of the LC4256ZE. No LCD output is available in this mode. In battery-powered, standby mode CPLD core current draw is ~10μA.
Other	Reserved switch settings. No LCD output.
Push Button Switch	Pico Power Demo Feature
SW1	Manual Reset is a push-button switch (SW1) used to assert a manual reset of the demo. All design modules including the CPLD OSCTIMER will be initialized when SW1 is pressed.

Run the Pico Power Demo

Follow the procedure below to explore the Pico Power demonstration on the evaluation board.

1. Select Switch Bank pattern 1111 (Standby)

The Pico board activates the LC4256ZE standby mode. To measure the current draw of the CPLD core (lcccore), touch voltmeter leads across R35, read the voltage drop, and then divide by 50 Ohms ($I=V/R$). The LC4256ZE draws approximately 10μA in Standby mode. Given a new button-cell battery the Pico board should be operational for approximately one year in standby mode. As a further measure to minimize CPLD current draw, I/O Bus Maintenance features are disabled and the DIP switch input is designed to pull input high rather than open, high-Z. This will avoid current leakage by the CPLD buffers by disabling the internal pull-down resistor circuits.

2. Select Switch Bank pattern 1100 (Low-speed CPLD core current meter)

The LCD displays CPLD core current (lcccore) in microamp (μA) units. The CPLD control logic performs the following operations to arrive at the result. First, the counter and the shift register modules of the CPLD are enabled by the internal slow clock (<2Hz) and the ispPAC-POWR6AT6 power supply rail is enabled. Next, the I²C master module issues three I²C bus cycles to initiate and read the analog-to-digital conversion result of the POWR6AT6 voltage monitor input (VMON1). Finally, the data is displayed on the LCD in microamp units. The POWR6AT6 VMON1 is driven by a high-side current sense circuit connected to the CPLD Vcccore supply rail. Power consumption of the CPLD in the slow speed operation is in the μA range. Note that a volt meter reading across R35 will reflect current draw after the POWR6AT6 has powered off and therefore be 100-600 microamps less than the value latched by the CPLD.

3. Select Switch bank pattern 0000 (decimal up counter).

The LCD displays a decimal up-counter. The counter uses a divided OSCTIMER clock source set for 5 kHz nominal (TIMER_DIV=1024). 5 kHz is further divided to produce a count frequency of < 2 Hz. Use the voltmeter technique in step 1 to measure core current.

4. Select Switch bank pattern 1000 (CPLD core current meter).

The LCD displays the VMON1 lccore in μA units as the CPLD OSCTIMER clocks the counter and shift register design modules at 5 MHz and the LCD at < 2 Hz. At this higher frequency the core current increases.

5. Select Switch bank pattern 0010 (left shift).

The LCD displays the 21-bit shift register module operating on each segment at < 2 Hz.

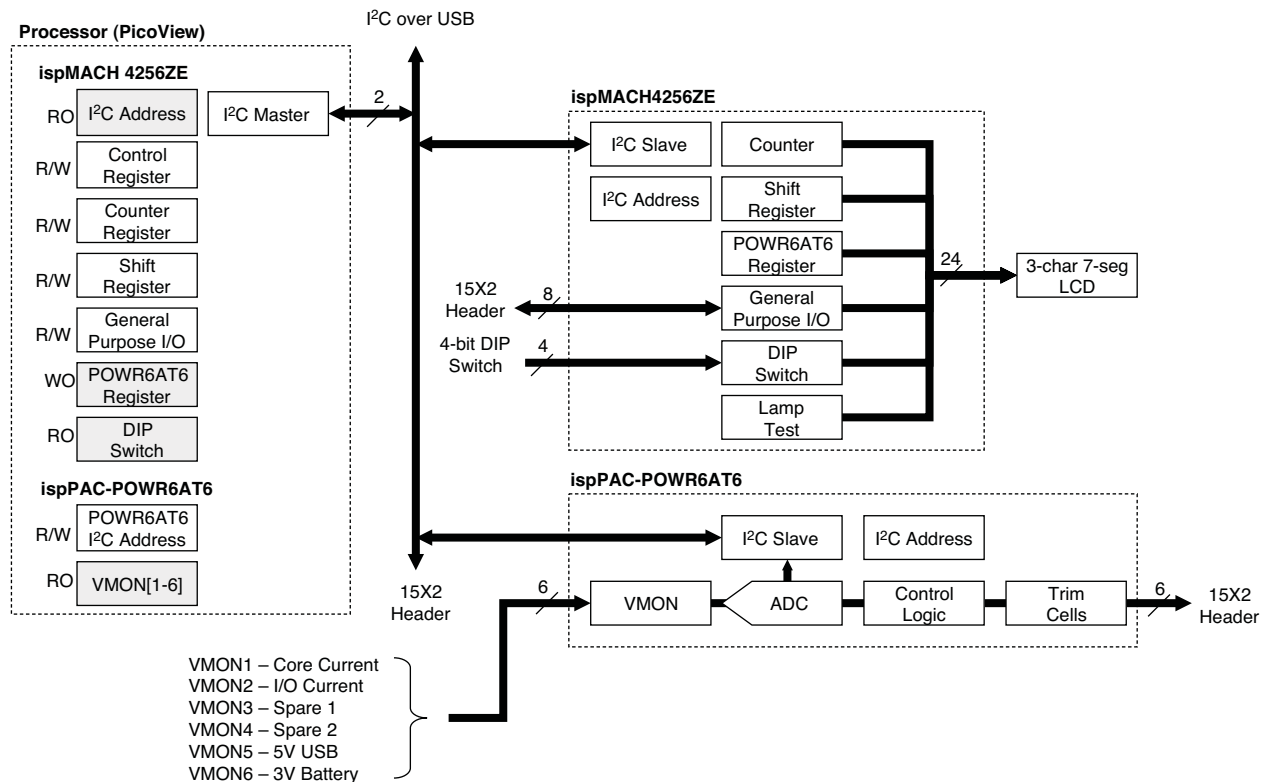
6. Experiment with other functions and measurements of the Pico Power Demo.

If the Pico board battery is missing you may connect the Pico board to a USB socket with the cable provided to enable the USB 5V supply rail.

I²C GPIO Expansion Demo

This demo illustrates I²C traffic between a PC host running the I²C Hardware Verification Utility program (PicoView) and the Pico board. Data is available at the expansion header landing or LCD display. Control and status registers of the I²C master and slave modules can be read or written via the PicoView user interface. These instructions highlight the LC4256ZE, providing general-purpose I/O for an I/O-constrained microprocessor.

Figure 5. GPIO I²C Expansion Demo



Download PicoView Software and I²C GPIO Expansion Demo

The following steps require a host PC with a USB port configured to communicate with the Pico board. Before you begin, you will need to obtain the I²C interface program, PicoView, and the I²C GPIO Expansion demo design, from the Lattice web site.

1. Browse to www.latticesemi.com/4000ze-pico-kit.
2. Select the PicoView for Windows Software download, review the software license agreement, save the ZIP file to your system, and unzip it to a location on your PC. For example: c:\4000ze-pico-kit. The ZIP archive contains picoview.exe.
3. Select the I²C GPIO Expansion Demo download, save the ZIP file to your system, and unzip it to a location on your PC. For example: c:\4000ze-pico-kit.

Connect to the Pico Evaluation Board

In this step, connect the evaluation board to your PC using the USB cable provided. Once connected you can use ispVM System software to reprogram the Pico board or use PicoView software to interact with the interface registers of the I²C GPIO Expansion demo.

Connect one USB cable from a USB port on your PC to the board's USB-to-I²C interface socket on the side of the board as shown in the PCB diagram. After connection is made, a blue Power LED will light up indicating the board power is now supplied from the USB cable.

Reprogram the Pico Evaluation Board

The Power demo design is pre-programmed into the Pico board by Lattice. To program the Pico board with the I²C GPIO Expansion Design, use ispVM System software. This step requires that ispVM System be installed. For more information see www.latticesemi.com/products/designsoftware/ispvmsystem.

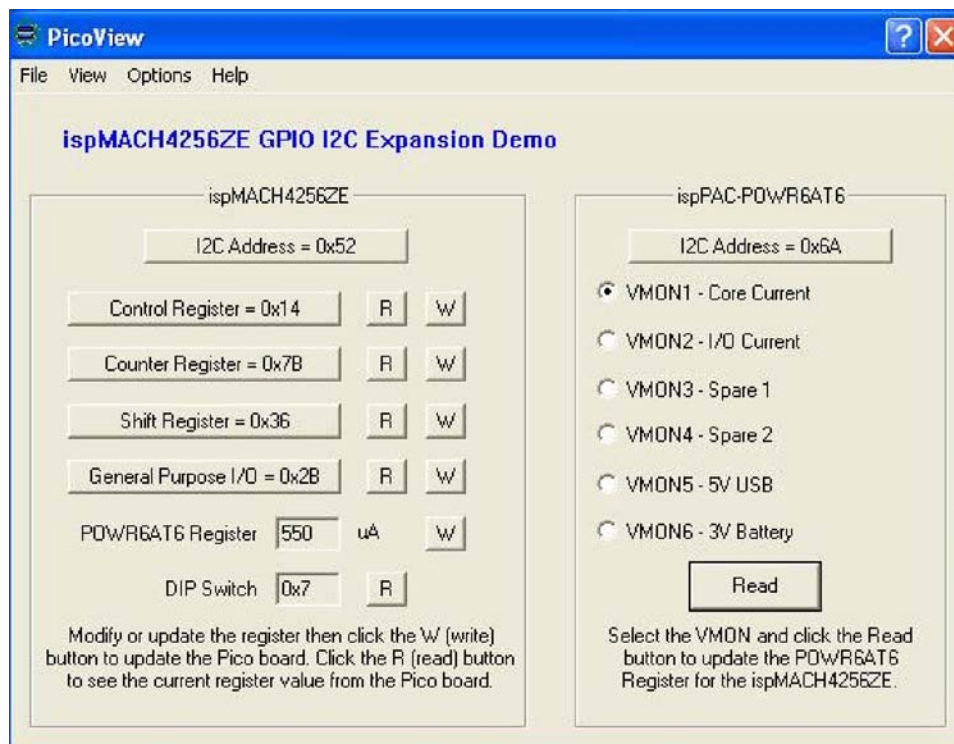
1. If not already connected, follow the procedure above to connect the Pico board and install hardware drivers. The USB cable must be attached and powered to enable the Pico board I²C channel and JTAG programming interface.
2. From the **Start** menu run **ispVM System**. ispVM appears.
3. Choose **Options > Cable and IO Port Setup...** The Cable and I/O Port Setup dialog appears.
4. Specify the following:
Cable Type: **USB2**
Port Setting: **FTUSB-0**
Click **OK**
5. The New Scan Configuration Setup window appears. The LC4256ZE appears in the device list.
6. Right-click the **LC4256ZE** entry and choose **Edit Device...** The Device Information dialog appears.
7. From the **Data File** section, click the **Browse** button. The **Open Data File** dialog appears.
8. Browse to the **c:\4000ze-pico-kit\gpio-demo** folder, select **gpio-demo.jed**, and click **Open**. From the **Operation** list choose **Erase, Program, Verify** and click **OK**.
9. Right-click the **ispPAC-POWR6AT6** row, from the **Set Device Operations** menu, choose **Bypass**.
10. Choose **Project > Download**. ispVM reprograms the Pico board. Programming requires about 20-40 seconds. A small timer window will appear to show elapsed programming time. At the end of programming, the configuration setup window should show a **PASS** in the **Status** column.

Run the I²C GPIO Expansion Demo

These instructions highlight the LC4256ZE providing general-purpose I/O for an I/O-constrained microprocessor or DSP. A host PC running the Lattice PicoView program emulates a processor reading and writing I²C traffic to I²C slaves embedded in the LC4256ZE and POWR6AT6 devices. The CPLD integrates Verilog-based I²C slave and LCD Controller reference designs to translate the traffic to parallel interfaces of the Pico board. The I²C interface to the POWR6AT6 allows you to monitor voltage or current of various Pico board power supplies.

1. If not already connected, follow the earlier procedures to connect the Pico board and reprogram it. The USB cable must be attached and powered to enable the Pico board I²C channel and JTAG programming interface.
2. Start a command prompt and run the PicoView program (c:\4000ze-pico-kit\picoview.exe). PicoView provides a push-button interface to provide read or read/write access to the registers of the LC4256ZE and POWR6AT6 devices. When PicoView initializes, all device registers are read and the dialog is refreshed. A column of "R" and "W" buttons provide read or read/write control over individual registers of the LC4256ZE. See Figure 5 for details.
3. Choose **Options > Control Register**. The Control Register dialog appears.
4. From the Counter/Shift Control section of the dialog select **Count Down/Shift Right**, from the LCD Display section, select **Shift Register**, and then click **OK**. The Control Register box is updated with value 0x14h.
5. Click the **Control Register W** button. PicoView writes the control settings to the Pico board to initiate the embedded shift register and display the results to the LCD panel.
6. From the ispPAC-POWR6AT6 section of the dialog, select **VMON1 – Core Current** and click the **Read** button. PicoView updates the POWR6AT6 Register with the core current in microamp units.

Figure 6. PicoView Screen Shot



Hardware Evaluation

How to evaluate hardware features of the on-board LC4256ZE.

Power Consumption

Tables 1 and 2 list a series of measurements for the CPLD I/O and core current running the Pico Power demonstration design when powered by battery or the USB cable interface.

CPLD power consumption can be measured by the on-board sensor circuits or by metering across resistors R34 (I/O, 100 ohm) and R35 (Core, 50 ohm) of the Pico board (see Figure 2). Use Ohm's Law to calculate current from the voltage drop across each resistor: $I = V / R$.

Note that voltmeter measurements reflect a lower static current level than what the on-board meter and PicoView results display which accounts for the additional current that occurs when the POWR6AT6, current sense amplifiers, and switch circuits are dynamically powered for a measurement.

The board will draw additional current when USB power is applied due to the LC4256ZE JTAG and I/O pins being biased from surrounding USB support circuits. When powered by the battery cell, the LC4256ZE pins are isolated by high-impedance circuits to minimize current leakage paths.

Table 1. Sample Current and Voltage Measurements – Battery Power

Feature		Static		Dynamic
		I/O Current	Core Current	Pico Board (LCD)
Counter	0000 - Decimal Up	0μA	390μA	N/A
	0001 - Decimal Down			
Current Meter	1000 - CPLD Core (5 MHz)	1μA	624μA	768μA
	1100 - CPLD Core		490μA	704μA
	1001 - CPLD I/O			688μA (I/O)
Shift	0010 - Left		390μA	N/A
	0011 - Right			
Voltage Meter	1010 - USB 5V		490μA	0V
	1011 - Battery 3V			2.88V
Standby	1111		10μA	N/A

Table 2. Sample Current and Voltage Measurements - USB Power

Feature		Static		Dynamic		
		I/O Current	Core Current	Pico Board (LCD)	PicoView	
					I/O Current	Core Current
Counter	0000 - Decimal Up	626μA	624μA	N/A	772μA	636μA
	0001 - Decimal Down			N/A	750μA	
Current Meter	1000 - CPLD Core (5 MHz)		690μA	768μA (Core)	740μA	784μA
	1100 - CPLD Core			688μA (Core)		682μA
	1001 - CPLD I/O			800μA (I/O)		693μA
Shift	0010 - Left		624μA	N/A	781μA	640μA
	0011 - Right			N/A		
Voltage Meter	1010 - USB 5V		690μA	4.96V	751μA	685μA
	1011 - Battery 3V			2.78V		
Standby	1111		450μA	N/A		450μA

Download Demo Designs

The Pico Power demo is preprogrammed into the Pico board, however over time it is likely your board will be modified. Lattice distributes source and programming files for demonstration designs compatible with the Pico board.

To download demo designs:

1. Browse to the ispMACH 4000ZE Pico Development Kit web page (www.latticesemi.com/4000ze-pico-kit) of the Lattice web site. Select the **Demo Applications download** and save the file.
2. Extract the contents of **Pico_DK_DemoSource.zip** to an accessible location on your hard drive. Three demo design directories (Demo_<device>_<demo>) are unpacked.

Demo	Directory
Pico Power	picopower-demo .\project .\source .\testbench
I2C GPIO Expansion	gpio-demo .\project .\source .\testbench
Both	supplymonitor-demo .\project

Where:

- **.\project** – ispLEVER Classic project (.syn) or PAC-Designer project (.pac) and programming file (.jed). This directory may contain intermediate results of the ispLEVER Classic or PAC-Designer compile process.
- **.\source** – HDL source files for the ispLEVER Classic project.
- **.\testbench** – HDL test fixture for the ispLEVER Classic project.

Recompile a LC4256ZE Demo Project with ispLEVER Classic

Use the procedure described below to recompile any of the LC4256ZE demo projects for the Pico Evaluation Board.

1. Install and license ispLEVER Classic software.
2. Download the demo source files from the ispMACH 4000ZE Pico Development Kit web page.
3. Run the ispLEVER Classic Project Navigator.
4. Open the <demo>.syn project file.
5. From the **Source** in project window, select the target device. The Fit Design process appears in the Processes for current source window.
6. Select **Fit Design**, right-click and choose, **Start**. After a few moments the JEDEC programming file is output.
7. See the Programming with ispVM section of this document for details on downloading a programming file to the board.

Recompile a POWR6AT6 Demo Project with PAC-Designer

Use the procedure described below to recompile any POWR6AT6 demo project for the Pico Evaluation Board. The POWR6AT6 has limited I/O access so trim output features are limited. The only programmable option that can be modified is the I²C address.

1. Install and license PAC-Designer software
2. Download the demo source files from the ispMACH 4000ZE Pico Development Kit web page.
3. Run PAC-Designer.
4. Open the **<demo>.pac** project file.
5. Choose **File > Export...** The Export dialog appears.
6. Select **Export What: Jedec File**.
7. Click the **Browse...** button. The Save As dialog appears.
8. Browse to the destination folder, specify a file name, and click **Save**.
9. Click **OK**. After a few moments the JEDEC programming file is output.
10. See the Programming with ispVM Section of this document for details on downloading a programming file to the board.

Programming with ispVM

The Pico Power demo design is pre-programmed into the Pico board by Lattice. To restore a Pico board to factory settings or load an alternative demo design, use the procedures in this section.

To install ispVM programming tools:

1. Install and license ispVM System software.
2. Connect the board to a host PC using the USB port header connection.
3. Follow the USB Cable Interface procedure below to program the evaluation board.

USB Cable Interface

The Pico board is equipped with a built-in USB-based programming circuit. This consists of a USB PHY and a USB connector. When the board is connected to a PC with a USB cable, it is recognized by the ispVM System software as a "USB Download Cable". The LC4256ZE and POWR6AT6 can then be scanned and programmed using the ispVM System software.

To program a demo programming file:

1. From the **Start** menu run ispVM System. ispVM appears.
2. Choose **Options > Cable and IO Port Setup...** The Cable and I/O Port Setup dialog appears.
3. Make the following selections:
Cable Type: **USB2**
Port Setting: **FTUSB**
Click **OK**
4. Choose **ispTools > Scan Chain**. The New Scan Configuration Setup window appears. The LC4256ZE and POWR6AT6 device(s) appear in the device list.
5. Right-click the **LC4256ZE** or **ispPAC-POWR6AT6** entry and choose **Edit Device...** The Device Information dialog appears.
6. From the Data File section, click the **Browse** button. The Open Data File dialog appears.

7. Browse to the <Demo Dir>\project folder, select <Demo>.jed, and click **Open**. From the Operation list choose **Erase, Program, Verify** and click **OK**.

*Optional: Choose the **Bypass** operation for devices in the scan chain that don't require re-programming.*

8. Choose **Project > Download**. ispVM reprograms the evaluation board.

Programming requires about 20-40 seconds. A small, timer window will appear to show elapsed programming time. At the end of programming, the configuration setup window should show a **PASS** in the **Status** column.

PicoView Software

This section describes the features of the PicoView for Windows software program.

Concepts

PicoView provides an easy-to-use interface to the I²C control and status registers within the GPIO I²C Expansion demo design. PicoView communicates between a Windows PC and the Pico board using an I²C-over-USB connection.

PicoView issues I²C commands just as would an I²C master controller. You can view, and in many cases preload, control registers prior to issuing a read or write command. To help understand the register set of the demo, see the I²C GPIO Expansion Demo section and Figure 5 for more information.

Procedures

This section describes how to navigate the PicoView user interface.

Running PicoView

To run PicoView:

1. See the connection and programming procedure for the GPIO I²C Expansion demo to prepare the Pico board.
2. Download PicoView from www.latticesemi.com/4000ze-pico-kit and unzip the archive file. Picoview.exe is unpacked.
3. From a Windows command prompt run: <install>\Picoview.exe.

Setup

By default, PicoView is set to communicate between a PC and the Pico board over a USB cable. PicoView can also be set up to operate in a demo mode without hardware. See the PicoView I²C Settings dialog for more information.

I²C Command Execution

To execute an I²C command:

1. From the PicoView Window, click a **Control Register Button**. A control register dialog box appears. A variety of dialog styles are available depending on the register. See the User Interface section below for details.
2. Set the register options and click **OK**. The PicoView user interface will refresh with the updated register command in hex format.
3. Click the **R** (read) and **W** (write) buttons to update the register of the related I²C slave/peripheral register. The PicoView user interface will refresh the status registers. In some cases the Pico board's LCD operation will change.

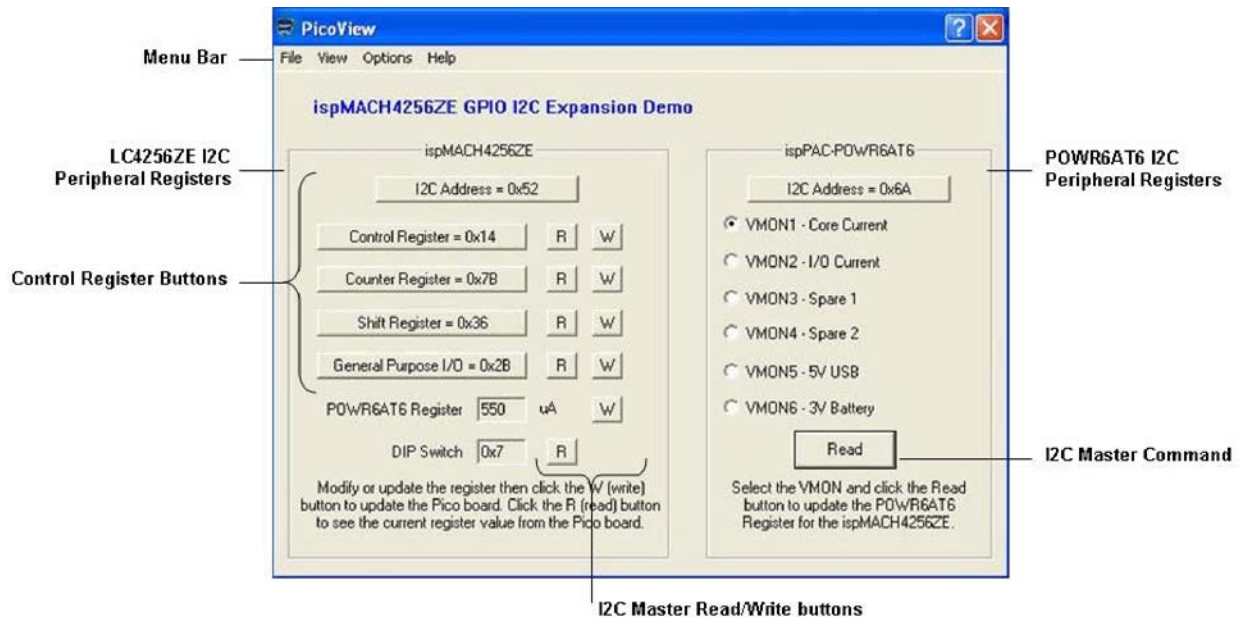
See the Run the I²C GPIO Expansion Demo section of this document for a PicoView operation example.

User Interface

This section describes elements contained within the PicoView graphical user interface. These elements include windows, menus, toolbars, and dialog boxes.

PicoView Window

The PicoView window provides access to control and status registers and a series of read or write actions that can be issued by the I²C bus master module emulated by PicoView.

Figure 7. PicoView Window**Table 3. PicoView Window Buttons and Command Descriptions**

Control Buttons	Button or I ² C Master Command Description
I ² C Address (ispMACH 4256ZE)	Open the PicoView Hex Entry dialog. Specify the hexadecimal value of the LC4256ZE CPLD I ² C bus address.
Control Register [R W]	Open the PicoView Control Register dialog. R – Read the current control register value and update the Control Register button display. W – Write the current control register commands to the I ² C slave peripherals.
Counter Register [R W]	Open the PicoView Hex Entry dialog. R – Read the counter value from the CPLD and update the Counter Register button display. W – Write the counter pre-load value to the CPLD. The counter will begin counting up or down from the preload value if it is not held in the Stop state. For more information about counter controls, see the Pico View Control Register dialog.
Shift Register [R W]	Open the PicoView Shift Register dialog. R – Read the 21-bit shift register value from the CPLD and update the Shift Register button display. W – Write the shift register pre-load value to the right-most 7-segment digit of the CPLD. The shift register will shift the pattern left or right from the pre-load value if it is not held in the Stop state. For more information about shift register controls, see the Pico View Control Register dialog.
General Purpose I/O	Open the PicoView General Purpose I/O Register R – Read the 8-bit register value from the CPLD prototype GPIOs connected to the 15x2 expansion header landing. W – Write the 8-bit register value specified to the CPLD prototype GPIOs.
POWR6AT6 Register	Display the current or voltage monitored by the POWR6AT6. W – Issue a write command to display the POWR6AT6 register value to the LCD panel of the Pico board.
DIP Switch	Display the value of the 4-bit DIP switch input as a hexadecimal value. R – Read the DIP switch input.

Table 3. PicoView Window Buttons and Command Descriptions (Continued)

I ² C Address (ispPAC-POWR6AT6)	Open the PicoView Hex Entry dialog. Specify the hexadecimal value of the POWR6AT6 I ² C bus address.
VMON1 – VMON6 radio buttons	Select the voltage monitor (VMON) to be read from the POWR6AT6 slave I ² C peripheral.
Read (ispPAC-POWR6AT6)	Read the VMON specified and update the POWR6AT6 Register display.

About PicoView Dialog

Function: Report the PicoView version.

From the LCD Display section, specify which CPLD register the LCD will display.

PicoView Control Register Dialog

Function: Specify Counter/Shift Control mode and LCD Display.

Counter / Shift Control Option	Description
Count Up/Shift Left	Specify the counter or shift register direction.
Count Down/Shift Right	
Stop	Pause the counter or shift register.

From the LCD Display section, specify which CPLD register the LCD will display.

PicoView General Purpose I/O Register dialog

Function: Specify the output value registered on the LC4256ZE Bank 1 GPIOs connected to the 15x2 expansion header landing. See Figure 10 for details.

PicoView Hex Entry Dialog

Function: User interface keypad to enter a hexadecimal value. Appears when the Counter Register button is pressed. Allows you to specify the pre-load value for the CPLD's counter module.

PicoView I²C Settings Dialog

Function: Controls the I²C interface between the PC and Pico board.

Option	Description
Bypass Hardware Checking	Ignore USB connections. Used for demonstrations when a Windows PC with a USB port and Pico board is not available.
Enable Address Change of LC4256ZE	Enable to update how PicoView addresses the LC4256ZE. Requires an updated LC4256ZE programming file.
I ² C Clock Frequency	Select between I ² C fast mode transfer rate at 400 kbit/s or 100 kbit/s.

PicoView Shift Register Dialog

Function: Specify the initial shift-register load pattern for the right-most 7-segment digit of the LCD panel.

ispMACH 4000ZE Pico Evaluation Board

This section describes the features of the ispMACH 4000ZE Pico evaluation board in detail.

Overview

The Pico board is a complete development platform for the LC4256ZE CPLD. The board includes a high-side current sensor circuit, a Power Manager II ispPAC-POWR6AT6 mixed-signal PLD, a USB program/power port, and an expansion header landing to support test connections. The board is powered by a 3V battery or a PC's USB port. You may create or modify PLD program files using ispLEVER and PAC-Designer and reprogram the board using ispVM software.

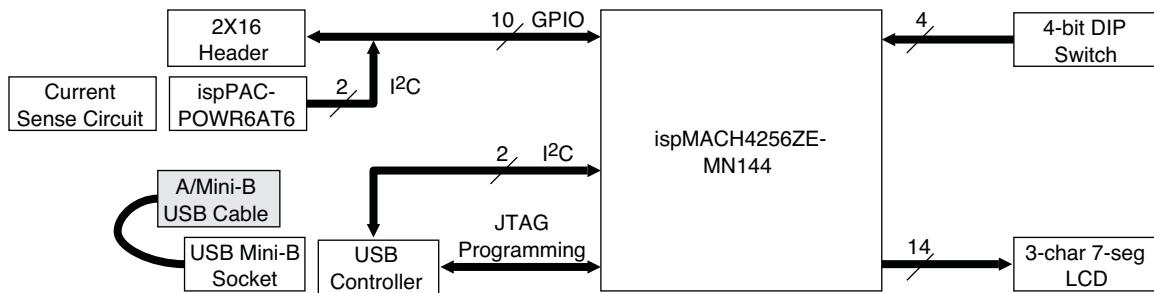
Figure 8. ispMACH 4000ZE Pico Evaluation Board Block Diagram

Table 4 describes the components on the board and the interfaces it supports.

Table 4. Pico Evaluation Board Components and Interfaces

Component/Interface	Type	Schematic Reference	Description
Circuits			
Power Circuit	Circuit	Figure 11	5V USB, 3V battery, and optional lithium-ion 20mA charge circuit.
High-Side Current Sense Circuit	Circuit	Figure 13	Resistive current sensor circuit to produce a voltage level proportional to the current level (see AN6049, High-side Current Sensing Techniques for Power Manager Devices).
USB Controller	Circuit	U4:FT2232D	USB-to-JTAG interface and dual USB UART/FIFO IC.
USB Mini B Socket	I/O	J1:USB_MINI_B	Programming and debug interface.
Components			
LC4256ZE	CPLD	U1: Lattice_4kZE	256-macrocell CPLD packaged in a 7 x 7mm, 144-ball chip-scale BGA.
POWR6AT6	Mixed Signal PLD	U6: ispPAC-POWR6AT6	Integrates analog DC-to-DC trim outputs, analog monitor, power supply margin/trim control, ADC, and I ² C interface in a 32-ball QFNS package.
Interfaces			
LCD Panel	Output	U2: LUMEX-LCD2	3-character, 7-segment LCD panel.
15x2 Header Landing	I/O	J2:HEADER 15X2	User-definable I/O.
4-Bit DIP Switch	Input	SW2: SWDIP-4	General purpose 4-bit DIP switch.
Push-button Switch	Input	SW1:GlobalReset	General purpose push-button.

Subsystems

This section describes the principle subsystems for the Pico board in alphabetical order.

Battery

A CR2032 watch cell battery provides a 3V supply rail for a portion of the Pico board and covers the LC4256ZE, current sensor circuit, and LCD power requirements. As a power saving measure a power MOSFET circuit enables the sensor circuit only upon measurement requests by the CPLD.

The Pico board can be populated by the user with a 20mA charger circuit for use with Li-Ion rechargeable batteries only. Do not try to recharge a standard CR2032 battery.

Clock Sources

All clocks for the Pico Power and GPIO I²C demonstration designs originate from the LC4256ZE CPLD on-chip oscillator and timer (OSCTIMER) block. You may use the expansion header landing to drive a CPLD input with an external clock source.

Current Sensor Circuits

The board is populated with current sensor circuits connected to the VCC core and VCC I/O supply rails of the LC4256ZE CPLD. For more information see AN6049, [High-side Current Sensing Techniques for Power Manager Devices](#).

DIP Switch

The evaluation board includes a 4-bit input piano button style switch located on the bottom-right corner of the board. All four are available as general purpose inputs for the LC4256ZE.

Table 5. DIP Switch Reference

Item	Description
Reference Designators	SW2
Part Number	193-4MS
Manufacturer	CTS
Web Site	www.ctscorp.com

Table 6. DIP Switch Pin Information

SW2	Description	LC4256ZE Pin
1	SW0 Input	K11
2	SW1 Input	J12
3	SW2 Input	J11
4	SW3 Input	H10

Expansion Header Landing

The expansion header provides user GPIOs connected to the LC4256ZE, VMON and TRIM analog I/Os connected to the POWR6AT6, and the on-board I²C/SMBus. The remaining pins serve as power supplies for external connections. The expansion connector is configured as one 2x15 100mil centered pin header.

Table 7. Expansion Connector Reference

Item	Description
Reference Designators	J2
Part Number	HEADER 15X2
Manufacturer	Molex/Waldom Electronics
Web Site	www.molex.com

Table 8. Expansion Header Pin Information

Pin Number	Function	LC4256ZE Pin
1	+3.1V	N/A
2	VCCIO_EXT	N/A
3	4K_TDI	TDI
4	USB_TDI	N/A
5	6AT6_TDO	N/A
6	USB_TDO	N/A

7	4K_TCK	TCK
8	USB_TCK	N/A
9	4K_TMS	TMS
10	USB_TMS	N/A
11	PROTO_K7	K7
12	USB_SDA	N/A
13	PROTO_M7	M7
14	USB_SCL	n/a
15	PROTO_K4	K4
16	PROTO_L7	L7
17	PROTO_M3	M3
18	PROTO_L8	L8
19	PROTO_L4	L4
20	PROTO_M8	M8
21	PROTO_M4	M4
22	PROTO_M9	M9
23	PROTO_K3	K3
24	PROTO_L9	L9
25	CLK0_MACH	CLK0
26	PROTO_K8	K8
27	VMON_3	N/A
28	VMON_4	N/A
29	GND	N/A
30	GND	N/A

ispMACH4256ZE-MN144 CPLD

The ispMACH4256ZE-MN144 is a 144-ball csBGA package CPLD device which provides 108 I/Os and 4 dedicated inputs in a 7 x 7mm package.

Table 9. LC4256ZE CPLD Interface Reference

Item	Description
Reference Designators	U1
Part Number	LC4256ZE
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

JTAG Interface Circuits

For power and programming an FTDI USB UART/FIFO IC converter provides a communication interface between a PC host and the JTAG programming chain of the Pico board. The USB 5V supply is also used as a source for the 3.3V and 1.8V supply rails. A USB B-type mini socket is provided for the USB connector cable.

Table 10. JTAG Interface Reference

Item	Description
Reference Designators	U4
Part Number	FT2232D
Manufacturer	FTDI (Future)
Web Site	www.ftdichip.com

Table 11. JTAG Programming Pin Information

Description	LC4256ZE Pin	POWR6AT6 Pin/Net
Test Data Output	B11:TDO / 4K_TDO	4:TDI / 6AT6_TDI
Test Data Output	-	1:TDO / 6AT6_TDO
Test Data Input	A1:TDI / 4K_TDI	-
Test Mode Select	M12:TMS / 4K_TMS	5:TMS / 6AT6_TMS
Test Clock	L2:TCK / 4K_TCK	3:TCK / 6AT6_TCK

LCD

A 3-character, 7-segment LCD panel is provided for CPLD outputs.

Table 12. LCD Reference

Item	Description
Reference Designators	U2
Part Number	LCD-S301C31TR
Manufacturer	Lumex
Web Site	www.lumex.com

LED

A blue LED (POWR - D1) is used to indicate USB 5V power.

Table 13. User LEDs Reference

Item	Description
Reference Designators	D1
Part Number	LTST-C190CKT
Manufacturer	Lite-On
Web Site	www.liteonit.com

Power Manager II ispPAC-POWR6AT6

The ispPAC-POWR6AT6-01-SN32 Power Manager II device is a 32-ball QFNS package programmable mixed-signal PLD which provides an interface between the on-board current sensor circuit and the I²C interface bus. The POWR6AT6 provides analog voltage monitors (VMON) and a 10-bit ADC to provide voltage measurements and an I²C interface to the LC4256ZE CPLD. The 15x2 External Header Landing provides access to VMON3 and VMON4 inputs for experiments with external circuit monitoring.

Table 14. ProcessorPM PLD Reference

Item	Description
Reference Designators	U6
Part Number	ispPAC-POWR6AT6-01-SN32I
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

Power Supply

Two optional power sources are provided depending on jumper settings. A 3.0V supply rail is provided from the battery and can power a subset of the board including the ispMACH 4000ZE, current sensor circuit, and LCD panel. Alternatively 3.3V and 1.8V supply rails are converted from the USB 5V interface when the board is connected to a host PC. The ispMACH4000ZE device will be isolated from other subsystems to accommodate accurate current/power measurements.

Pushbutton Switch

The board has one momentary push-button switch (S1). You may use the switch as a user-defined input for your own custom CPLD designs.

Table 15. Push-button Reference

Item	Description
Reference Designators	S1
Part Number	EVQ-Q2K03W
Manufacturer	Panasonic ECG
Web Site	www.panasonic.com/industrial/components/components.html

Table 16. Push-button Pin Information

Button	Description (Pre-Programmed Pico Power)	ProcessorPM Pin
S1	Pico board reset	H11

Test Points

In order to check the various voltage levels used, test points are provided:

- R35, VCC (CORE)
- R34, VCCIO of all banks

USB Programming and Debug Interface

The USB B-type Mini socket of the Pico board serves as the programming and debug interface.

JTAG Programming: For JTAG programming a preprogrammed USB PHY peripheral controller is provided on the Pico board to serve as the programming interface to the ispMACH 4000ZE CPLD.

Programming requires the ispVM System software (www.latticesemi.com/ispvm). The programming connection will appear to the ispVM System software as if a regular parallel-type ispDOWNLOAD™ cable is connected to the PC.

Modifying the Pico Board

The ispMACH 4000ZE Pico evaluation board provides landing areas for additional circuits to support the following functions:

- Rechargeable Lithium-Ion 20 mA rechargeable battery
- 15x2 Header

Note: Modifying your board requires good electronics handling and PCB fabrication techniques to avoid damage.

Add Support for a Rechargeable Battery

The Pico board can be upgraded to support a Lithium-Ion rechargeable battery. When connected to a PC's USB port the battery circuit will recharge the battery cell. Install R23, R26, R42 and Q6 (Figure 11) to provide a 20mA constant current charge.

15x2 Header

Install a 30-pin header at location J2 – HEADER 15x2 (Figure 10).

Mechanical Specifications

Dimensions: 2 ½ in. [L] x 2 in. [W] x 3/8 in. [H]

Environmental Requirements

The evaluation board must be stored between -40°C and 100°C. The recommended operating temperature is between 0°C and 90°C.

The evaluation board can be damaged without proper anti-static handling.

Glossary

CPLD: Complex Programmable Logic Device

DIP: Dual in-line package.

I²C: Inter-Integrated Circuit.

LED: Light Emitting Diode.

Mixed Signal PLD: A PLD integrated with analog and mixed signal support circuitry.

PCB: Printed Circuit Board.

RoHS: Restriction of Hazardous Substances Directive.

PLL: Phase Locked Loop.

SPI: Serial Peripheral Interface.

SRAM: Static Random Access Memory.

TransFR: Transparent Field Reconfiguration.

UART: Universal Asynchronous Receiver/Transmitter.

USB: Universal Serial Bus.

WDT: Watchdog timer

Troubleshooting

No Current/Voltage Meter Readings Available

A low battery can cause the current/voltage meter features of the Pico Power demo to read 0μA/0V. The demo's counter and shift register features may operate but the additional current required to energize the current sensor and POWR6AT6 may not be available once the battery begins to discharge. Install a new battery if this condition occurs.

Determine the Source of a Pre-Programmed Part

It is possible that you may receive your Pico board after it has been reprogrammed by someone else. To restore the board to the factory default, see the Download Demo Designs for details on downloading and reprogramming the device.

You can also determine which demo design is currently programmed onto the Pico board by comparing the JEDEC checksums against of the programming file with what is read from the programmed part.

To compare JEDEC file checksum:

1. Connect the Pico board to a host PC using the USB port.
 2. Start ispVM and choose **ispTools > Scan**. The POWR605 and POWR6AT6 devices appear in the Device List.
 3. Double-click the **device row**. The Device Information dialog appears.
-

4. Click the **Browse** button. The Save as Data File dialog appears.
5. Specify a new JEDEC Data File name and click the **Save** button.
6. From the Operation list choose **Read and Save JEDEC** and click **OK**.
7. Choose **Project > Download**. ispVM reads the contents from the device and writes the results to the JEDEC file specified.

Open the JEDEC file into a text editor and page to the bottom of the file.

Note the hexadecimal checksum at the line above the User Electronic Data note line. Compare this value against the checksum of the original JEDEC demo programming files.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
IspMACH 4000ZE Pico Development Kit	LC4256ZE-P-EVN	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
September 2009	01.0	Initial release.

© 2009 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal. All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Note: Add jumpers in copper (on bottom - layer # 4).
At pins 1, 3, 5, 7, 9 of J2
Cut to modify the JTAG chain.

PCB Footprint = SMT_SW
Part: NumbertEPO_22F338
Manufacturer: MMD

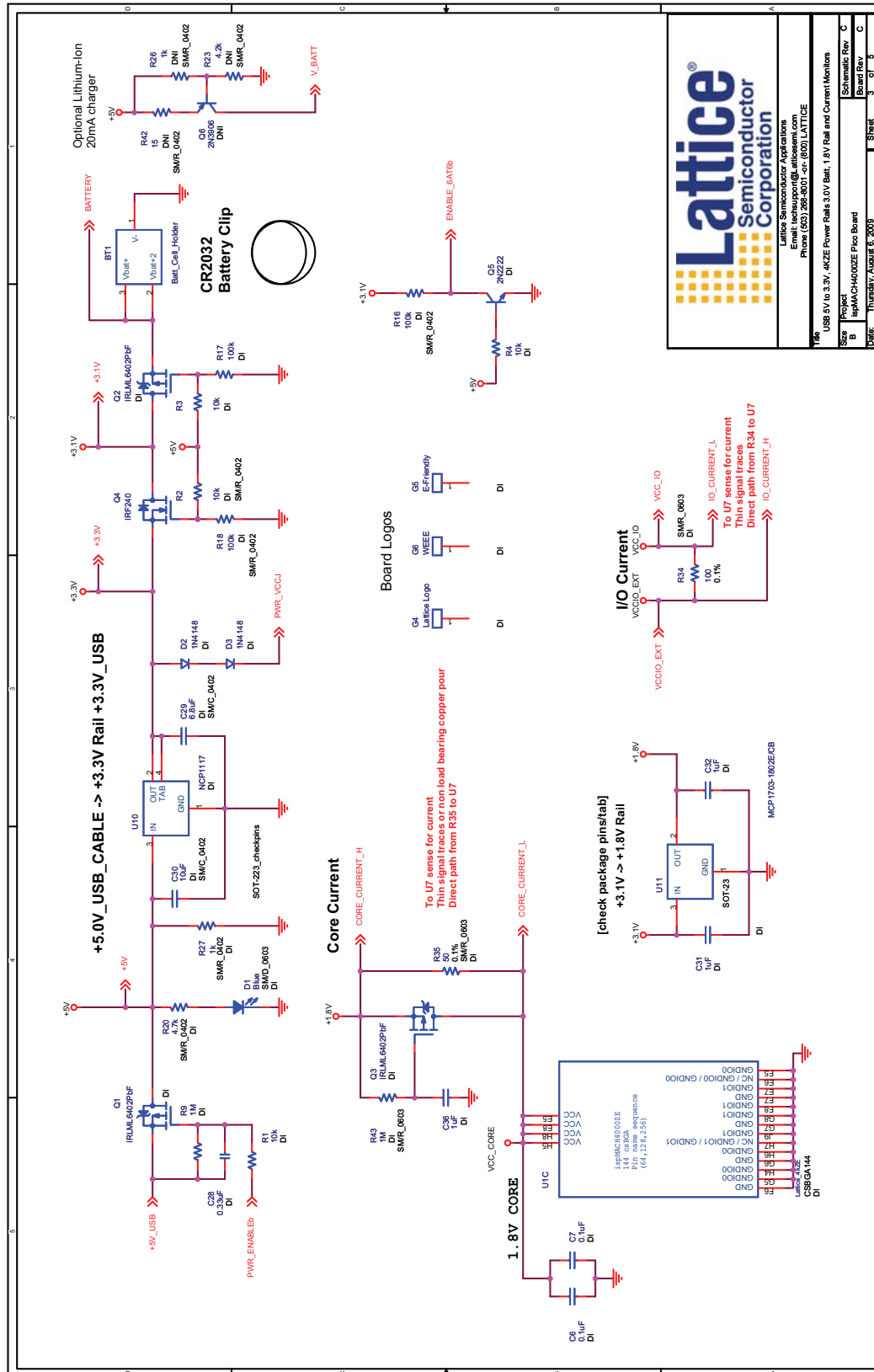
Bank 1

CSBG0414
Lattice iMP7400ZEE

Pinout:

Pin	Signal
1	VCC_IO
2	CLK2-1
3	IO00 / IOE10 / IOA10
4	IO01 / IOE11 / IOA11
5	IO02 / IOE12 / IOA12
6	IO03 / IOE13 / IOA13
7	IO04 / IOE14 / IOA14
8	IO05 / IOE15 / IOA15
9	IO06 / IOE16 / IOA16
10	IO07 / IOE17 / IOA17
11	IO08 / IOE18 / IOA18
12	IO09 / IOE19 / IOA19
13	IO10 / IOE20 / IOA20
14	IO11 / IOE21 / IOA21
15	IO12 / IOE22 / IOA22
16	IO13 / IOE23 / IOA23
17	IO14 / IOE24 / IOA24
18	IO15 / IOE25 / IOA25
19	IO16 / IOE26 / IOA26
20	IO17 / IOE27 / IOA27
21	IO18 / IOE28 / IOA28
22	IO19 / IOE29 / IOA29
23	IO20 / IOE30 / IOA30
24	IO21 / IOE31 / IOA31
25	IO22 / IOE32 / IOA32
26	IO23 / IOE33 / IOA33
27	IO24 / IOE34 / IOA34
28	IO25 / IOE35 / IOA35
29	IO26 / IOE36 / IOA36
30	IO27 / IOE37 / IOA37
31	IO28 / IOE38 / IOA38
32	IO29 / IOE39 / IOA39
33	IO30 / IOE40 / IOA40
34	IO31 / IOE41 / IOA41
35	IO32 / IOE42 / IOA42
36	IO33 / IOE43 / IOA43
37	IO34 / IOE44 / IOA44
38	IO35 / IOE45 / IOA45
39	IO36 / IOE46 / IOA46
40	IO37 / IOE47 / IOA47
41	IO38 / IOE48 / IOA48
42	IO39 / IOE49 / IOA49
43	IO40 / IOE50 / IOA50
44	IO41 / IOE51 / IOA51
45	IO42 / IOE52 / IOA52
46	IO43 / IOE53 / IOA53
47	IO44 / IOE54 / IOA54
48	IO45 / IOE55 / IOA55
49	IO46 / IOE56 / IOA56
50	IO47 / IOE57 / IOA57
51	IO48 / IOE58 / IOA58
52	IO49 / IOE59 / IOA59
53	IO50 / IOE60 / IOA60
54	IO51 / IOE61 / IOA61
55	IO52 / IOE62 / IOA62
56	IO53 / IOE63 / IOA63
57	IO54 / IOE64 / IOA64
58	IO55 / IOE65 / IOA65
59	IO56 / IOE66 / IOA66
60	IO57 / IOE67 / IOA67
61	IO58 / IOE68 / IOA68
62	IO59 / IOE69 / IOA69
63	IO60 / IOE70 / IOA70
64	IO61 / IOE71 / IOA71
65	IO62 / IOE72 / IOA72
66	IO63 / IOE73 / IOA73
67	IO64 / IOE74 / IOA74
68	IO65 / IOE75 / IOA75
69	IO66 / IOE76 / IOA76
70	IO67 / IOE77 / IOA77
71	IO68 / IOE78 / IOA78
72	IO69 / IOE79 / IOA79
73	IO70 / IOE80 / IOA80
74	IO71 / IOE81 / IOA81
75	IO72 / IOE82 / IOA82
76	IO73 / IOE83 / IOA83
77	IO74 / IOE84 / IOA84
78	IO75 / IOE85 / IOA85
79	IO76 / IOE86 / IOA86
80	IO77 / IOE87 / IOA87
81	IO78 / IOE88 / IOA88
82	IO79 / IOE89 / IOA89
83	IO80 / IOE90 / IOA90
84	IO81 / IOE91 / IOA91
85	IO82 / IOE92 / IOA92
86	IO83 / IOE93 / IOA93
87	IO84 / IOE94 / IOA94
88	IO85 / IOE95 / IOA95
89	IO86 / IOE96 / IOA96
90	IO87 / IOE97 / IOA97
91	IO88 / IOE98 / IOA98
92	IO89 / IOE99 / IOA99
93	IO90 / IOE100 / IOA100
94	IO91 / IOE101 / IOA101
95	IO92 / IOE102 / IOA102
96	IO93 / IOE103 / IOA103
97	IO94 / IOE104 / IOA104
98	IO95 / IOE105 / IOA105
99	IO96 / IOE106 / IOA106
100	IO97 / IOE107 / IOA107
101	IO98 / IOE108 / IOA108
102	IO99 / IOE109 / IOA109
103	IO100 / IOE110 / IOA110
104	IO101 / IOE111 / IOA111
105	IO102 / IOE112 / IOA112
106	IO103 / IOE113 / IOA113
107	IO104 / IOE114 / IOA114
108	IO105 / IOE115 / IOA115
109	IO106 / IOE116 / IOA116
110	IO107 / IOE117 / IOA117
111	IO108 / IOE118 / IOA118
112	IO109 / IOE119 / IOA119
113	IO110 / IOE120 / IOA120
114	IO111 / IOE121 / IOA121
115	IO112 / IOE122 / IOA122
116	IO113 / IOE123 / IOA123
117	IO114 / IOE124 / IOA124
118	IO115 / IOE125 / IOA125
119	IO116 / IOE126 / IOA126
120	IO117 / IOE127 / IOA127
121	IO118 / IOE128 / IOA128
122	IO119 /

Figure 11. USB 5V to 3.3V, ispMACH 4000ZE Power Rails 3.0V Batt, 1.8V Rail and Current Monitors



[illegible]

Appendix B. Bill of Materials**Table 17. Bill of Materials**

Item	Quantity	Reference	Part Number
1	2	C19, C20	ECJ-0EC1H120J
2	2	C21, C22	ECJ-0EC1H330J
3	4	C23, C24, C25, C26	ECJ-0EB1E103K
4	1	C27	ECJ-0EB1A333K
5	21	C1-C18, C33, C34, C35	ECJ-0EX1C104K
6	1	C28	GRM155R61A334KE15D
7	3	C31, C32, C36	ECJ-0EB1A105M
8	1	C29	TAJA685K020RNJ
9	1	C30	F920J106MPA
10	0		CRT0603-BY-10R0ELF
11	0	R42	ERJ-3EKF15R0V
12	2	R40, R41	ERJ-2GEJ270X
13	2	R36, R37	RG1005P-49R9-B-T5
14	1	R35	TNPW060349R9BEEA
15	4	R38, R39	ERA-2AEB101X
16	2	R34	ERA-3AEB101V
17	1	R33	ERJ-2GEJ331X
18	4	R29-R32	ERA-2AEB202X
19	2	R27, R28	ERJ-2GEJ102X
20	0	R26	ERJ-3EKF1001V
21	3	R21, R22, R25	ERJ-2GEJ152X
22	1	R24	ERJ-2GEJ222X
23	0	R23	ERJ-3EKF4221V
24	1	R20	ERJ-2RKF4701X
25	10	R1-R8, R45, R46	ERJ-2GEJ103X
26	0	R10	ERJ-3EKF1002V
27	9	R11-R19	ERJ-2GEJ104X
28	3	R9, R43, R44	ERJ-2GEJ105X
29	1	RN1	EXB-2HVR000V
30	1	L1	MI0603J600R-00
31	1	J1	UX60-MB-5ST
32	1	J2	90131-0800
33	1	U1	MACH4ZE LC4256ZE-05MN144C
34	1	U2	LCD-S301C31TR
35	1	U3	M93C46_WMN6TP
36	1	U4	FT2232D_R
37	4	U5, U7, U8, U12	STG3690QTR
38	1	U6	ISPPAC-POWR6AT6_QFN
39	1	U9	LMP7716MM/NOPB
40	1	U10	NCP1117ST33T3G
41	1	U11	MCP1703T-1802E/CB
42	1	S1	Push-Button SW SMD Tactile Raised White

Table 17. Bill of Materials (Continued)

43	1	SW2	193-4MS
44	3	Q1, Q2, Q3	IRLML6402PBF
45	1	Q5	MMBT2222LT1G
46	1	Q4	IRLML2502TRPBF
47	0	Q6	MMBT3906LT1G
48	1	X1	HCM49 6.000MABJ-UT
49	1	D1	LTST-C190TBKT
50	3	D2, D3, D4	1N4148W-TP
51	1	BT1	BATHLD001
52	1		CR2032
53	3		SJ61A3

Notes:

1. Quantity 0 (zero) indicates an optional component. See the Modifying the Pico Board section for more information.