LM124/LM324

Single-Supply Quad Operational Amplifier

Features

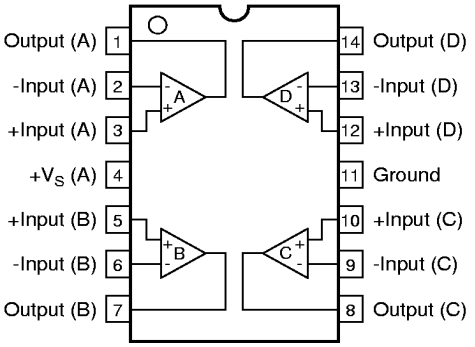
- Large DC voltage gain—100 dB
- Compatible with all forms of logic
- Temperature compensated
- Unity Gain Bandwidth—1 MHz
- Large output voltage swing—0V to (+V_S -1.5V)
- Input common mode voltage range includes ground

Description

Each of the devices in this series consists of four independent high-gain operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of crossover distortion may occur with loads to ground. An external current-sinking resistor to -V_S will reduce crossover distortion. There is no crossover distortion problem in single-supply operation if the load is direct-coupled to ground.

Pin Assignments



Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.	Units
Supply Voltage			+32 or ±16	V
Differential Input Voltage			32	V
Input Voltage		-0.3	+32	V
Output Short Circuit to Ground[1]	One Amplifier $+V_S \leq 15V$ and $T_A = +25°C$	Continuous		
Input Current[2]	$V_{IN} < -0.3V$		50	mA
Operating Temperature Range				
LM124		-55	+125	°C
LM324		0	+70	°C

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess d $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than 0.3V.

Thermal Characteristics

Parameter	SOIC	Plastic DIP	Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Max. P_D $T_A < 50°C$	300 mW	468 mW	1042 mW
Thermal Resistance, θ_{JC}	—	—	60°C/W
Thermal Resistance, θ_{JA}	200°C/W	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics

$+V_S$ = +5.0V (see Note 1) and T_A= +25°C, unless otherwise noted.

Parameters		Test Conditions	LM124			LM324			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage[1]				±2.0	±5.0		±2.0	±7.0	mV
Input Bias Current[2]				45	150		45	250	nA
Input Offset Current				±3.0	±30		±5.0	±50	nA
Input Voltage Range[3]		$+V_S$ = +30V	0		$+V_S$-1.5	0		$+V_S$-1.5	V
Supply Current (Over Temperature)		R_L = ∞, $+V_S$ = 30V		1.5	3.0		1.5	3.0	mA
		R_L = ∞ on all op amps		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain		$+V_S$ = 15V (for large V_{OUT} swing) $R_L \geq 2$ KΩ	50	100		25	100		V/mV
Output Voltage Swing	V_{OH}	$+V_S$ = +30V, R_L = 2KΩ	26			26			V
	V_{OH}	$R_L \geq 10$ KΩ	27	28		27	28		V
	V_{OL}	$+V_S$ = +5.0V, R_L = 10KΩ		5.0	20		5.0	20	mV
Common Mode Rejection Ratio			70	85		65	70		dB
Power Supply Rejection Ratio			65	100		65	100		dB
Channel Separation[4]		F = 1 KHz to 20 KHz (Input referred)		-120			-120		dB
Output Current	Source	V_{IN+} = 1V, V_{IN-} = 0V, $+V_S$ = 15V	20	40		20	40		mA
	Sink	V_{IN-} = 1V, V_{IN+} = 0V, $+V_S$ = 15V	10	20		10	20		mA
		V_{IN+} = 1V, V_{IN-} = 0V, $+V_{OUT}$ = 200 mV	12	50		12	50		µA

Notes:

1. V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full common mode range (0V to $+V_S$-1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$-1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these externall parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Electrical Characteristics

$+V_S$ = +5.0V, LM124 = -55° ≤ T_A ≤ 125°C, LM324 = 0°C ≤ T_A ≤ 70°C unless other wise noted.

Parameters		Test Conditions	LM124			LM324			Unit
			Min.	Typ .	Max .	Min.	Typ.	Max .	
Short Circuit Current[1]		T_A = +25°C		40	60		40	60	mA
Input Offset Voltage[2]					±7.0			±9.0	mV
Input Offset Voltage Drift		R_S = 0Ω		7.0			7.0		µV/°C
Input Offset Current					±100			±150	nA
Input Offset Current Drift				10			10		pA/°C
Input Bias Current[3]				40	300		40	500	nA
Input Voltage Range[4]		$+V_S$ = +30V	0		$+V_S$-2.0	0		$+V_S$-2.0	V
Large Signal Voltage Gain		+Vs - +15V (For Large V_{OUT} Swing) R_L ≥ 2.0 KΩ	25			15			V/mV
Output Voltage Swing	V_{OH}	$+V_S$ = +30V, R_L = 2 KΩ	26			26			V
	V_{OH}	R_L ≥ 10 KΩ	27	28		27	28		V
	V_{OL}	$+V_S$ = +5.0V, R_L = 10 KΩ		5.0	20		5.0	20	mV
Output Current	Source	V_{IN+} = +1.0V, V_{IN-} = 0V, $+V_S$ = +15V	10	20		10	20		mA
	Sink	V_{IN-} = +1.0V, V_{IN+} = 0V, $+V_S$ = +15V	5.0	8.0		5.0	8.0		mA
Differential Input Voltage[4]					$+V_S$			$+V_S$	V

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on an amplifiers.
2. V_{OUT} =1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V and over the full common mode range (0V to $+V_S$ -1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.

Typical Performance Characteristics

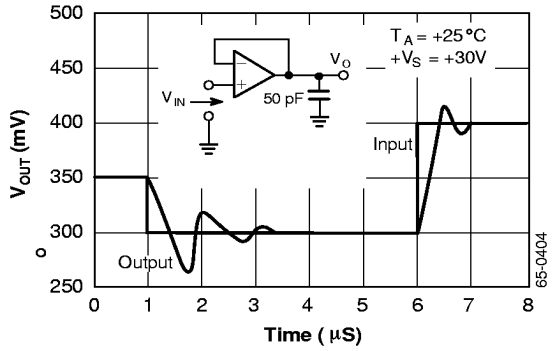


Figure 1. Follower Small Signal Pulse Response

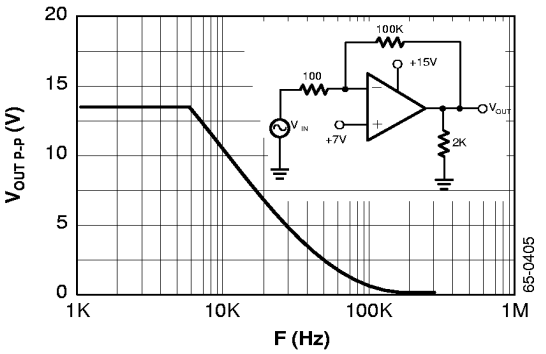


Figure 2. Output Voltage Swing vs. Frequency

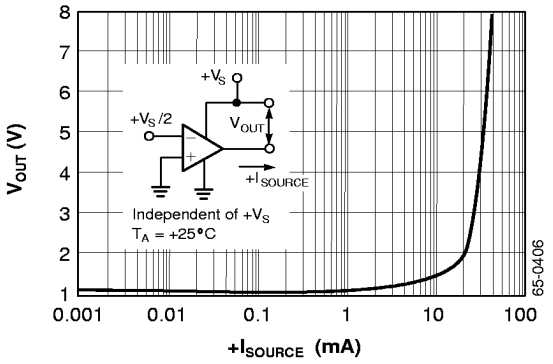


Figure 3. Output Voltage vs. Output Source Current

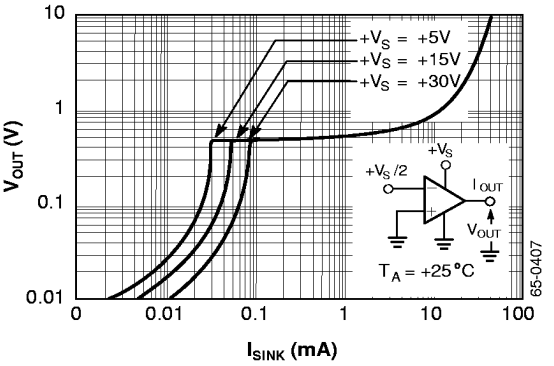


Figure 4. Output Voltage vs. Output Sink Current

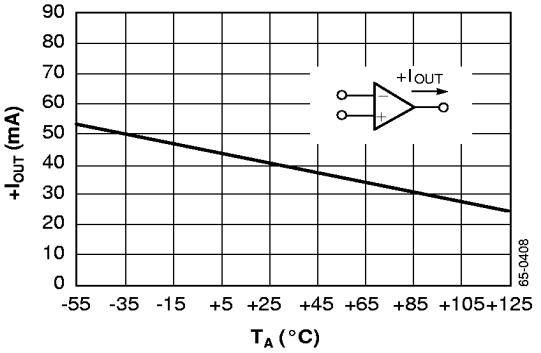


Figure 5. Current Limiting Output Current vs. Temperature

Typical Performance Characteristics (continued)

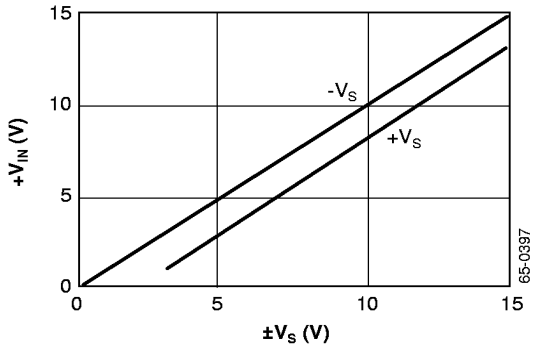


Figure 6. Input Voltage vs. Supply Voltage

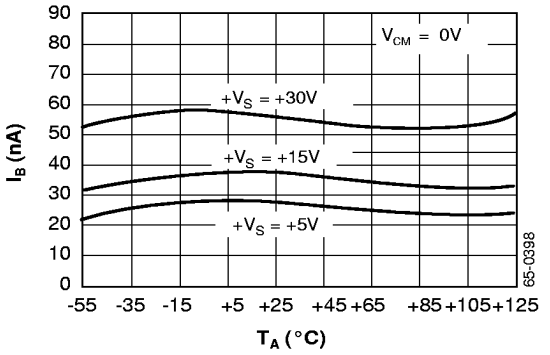


Figure 7. Input Bias Current vs. Temperature

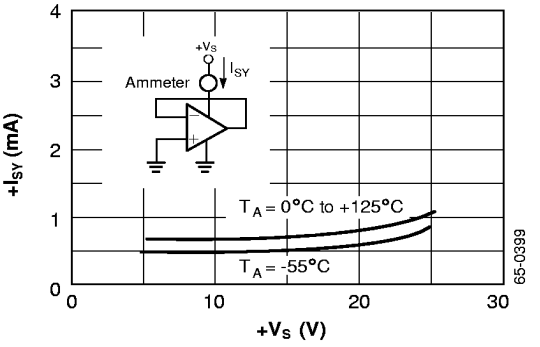


Figure 8. Supply Current vs. Supply Voltage

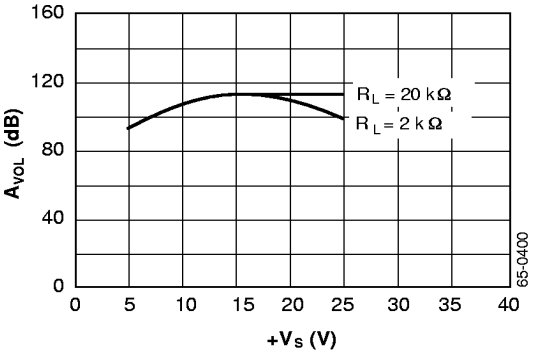


Figure 9. Open Loop Voltage Gain vs. Supply Voltage

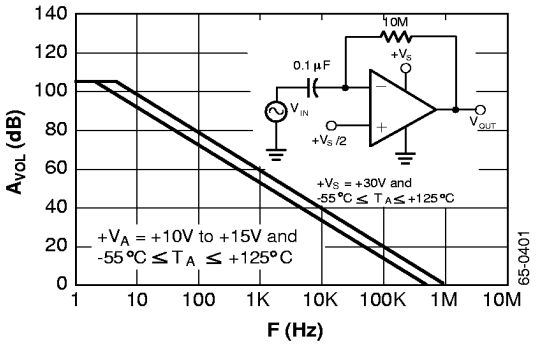


Figure 10. Open Loop Voltage Gain vs. Frequency

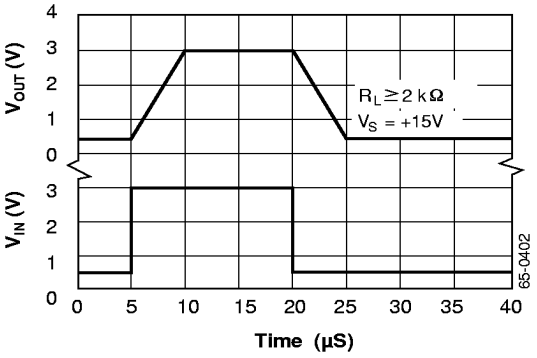


Figure 11. Follower Large Pulse Response Signal vs. Time

Notes:

Notes:

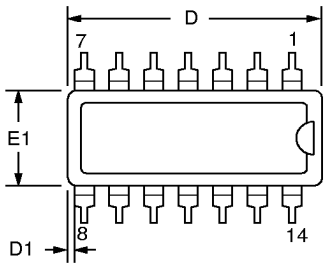
Mechanical Dimensions

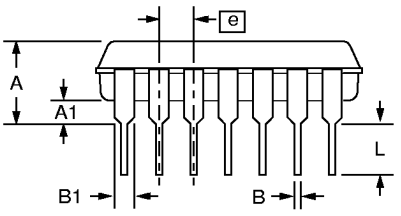
14-Lead Plastic DIP

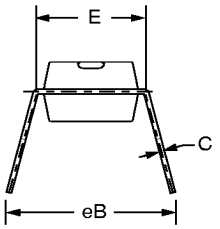
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







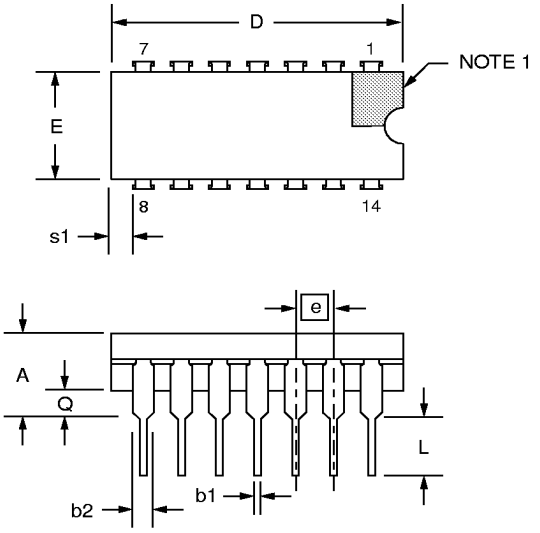
Mechanical Dimensions (continued)

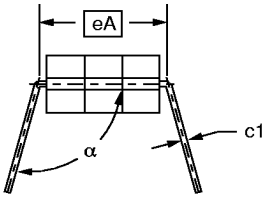
14-Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.





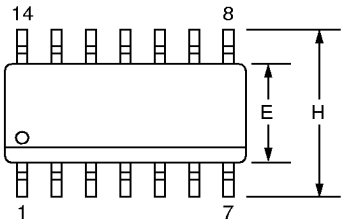
Mechanical Dimensions (continued)

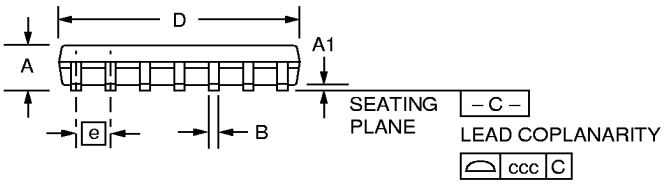
14-Lead SOIC

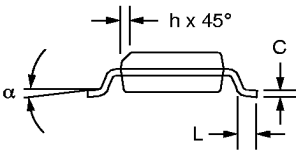
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
LM324M	14-Lead Plastic SOIC	0°C to +70°C
LM324N	14-Lead Plastic DIP	0°C to +70°C
LM124D	14-Lead Ceramic DIP	-55°C to +125°C
LM124D/883B	14-Lead Ceramic DIP	-55°C to +125°C

Note:

1. 883B suffix denotes Mil-Std-883, Level B processing.

5/20/98 0.0m 001
Stock#DS3000124