1 GByte/ 2 GByte / 4 GByte NANDrive
SST85LD1001K / SST85LD1002L / SST85LD1004M

Fact Sheet

FEATURES:

- **Industry Standard ATA/IDE Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6
  - Supports up to Multi-word DMA Mode-4
  - Supports up to Ultra DMA Mode-4
- **Low Power, 3.3V Power Supply**
- **5.0V or 3.3V Host Interface Through V_{DDQ} Pins**
- **Low Current Operation:**
  - Active mode: 85 mA Typical
  - Sleep mode: 160 µA Typical
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Expanded Data Protection**
  - WP#/PD# pin configurable by firmware for prevention of data overwrites
- **20-byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-byte Unique ID
  - User-Programmable 10-byte ID
- **Integrated Voltage Detector**
  - Prevents data loss due to unexpected power-down or brownout.
- **Endurance**
  - 10K cycles
- **Data Retention**
  - 10 years
- **Pre-programmed Embedded Firmware**
  - Executes industry standard ATA/IDE commands
  - Implements dynamic wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Robust Built-in ECC**
- **Multi-tasking Technology Enables Fast Sustained Write Performance (Host-to-Flash)**
  - Up to 8MByte/sec
- **Fast Sustained Read Performance (Flash-to-Host)**
  - Up to 30 MByte/sec
- **Commercial Temperature Range**
  - 0°C to 70°C for commercial operation
- **LBGA package**
  - 12mm x 24mm
- **All non-Pb (lead-free) Devices are RoHS Compliant**

PRODUCT DESCRIPTION

The SST85LD1001K, SST85LD1002L and SST85LD1004M NANDrive™ integrated circuits (IC) are high-performance, fully-integrated, embedded flash solid state drives. They combine an integrated ATA Controller and either 1GByte, 2GByte, or 4GByte of NAND Flash in a multi-chip package. These products are ideal for solid state mass storage applications offering new and expanded functionality while enabling cost effective designs.

ATA-based solid state mass storage technology is widely used in portable and desktop computers, digital cameras, music players, handheld data collection scanners, cellular phones, PCS phones, PDAs, handy terminals, personal communicators, robotics, audio recorders, monitoring devices, and set-top boxes.

SST NANDrive is a single device, solid state drive designed for embedded ATA/IDE protocol systems and supports standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4 and Ultra DMA Mode-4 interface. The built in microcontroller and file management firmware communicates with ATA standard interfaces; thereby eliminating the need for additional or proprietary software such as Flash File System (FFS) and Memory Technology Driver (MTD) software.

The SST85LD1001K / SST85LD1002L / SST85LD1004M NANDrives provide complete IDE Hard Disk Drive functionality and compatibility in a 12mm x 24mm BGA package for easy, space saving mounting to a system motherboard. It is a perfect solution for portable, consumer electronic products requiring smaller and more reliable data storage.

The NANDrive provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

The NANDrive is pre-programmed with a 10-byte unique serial ID. For even greater system security, the user has the option of programming an additional 10 Bytes of ID space to create a unique, 20-byte ID.

1.0 GENERAL DESCRIPTION

Each NANDrive contains an integrated ATA Controller and one or more NAND Flash dice in a LBGA package. Refer to Figure 2-1 for the NANDrive block diagram.

1.1 Performance-optimized NANDrive

The heart of the NANDrive is the ATA Flash Disk Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The NANDrive uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The power management unit controls the power consumption of the NANDrive. The PMU dramatically reduces the power consumption of the NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the NANDrive performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.
2. Provides dynamic flash media wear leveling to spread the flash writes across all unused memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.
4. Manages system security for the selected protection zones.

1.1.6 Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. Always provide SCI interface access to PCB design to aid in design validation.

1.1.8 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices.

1.2 NAND Flash

The NANDrive family utilize standard NAND Flash for data storage.

2.0 FUNCTIONAL BLOCKS

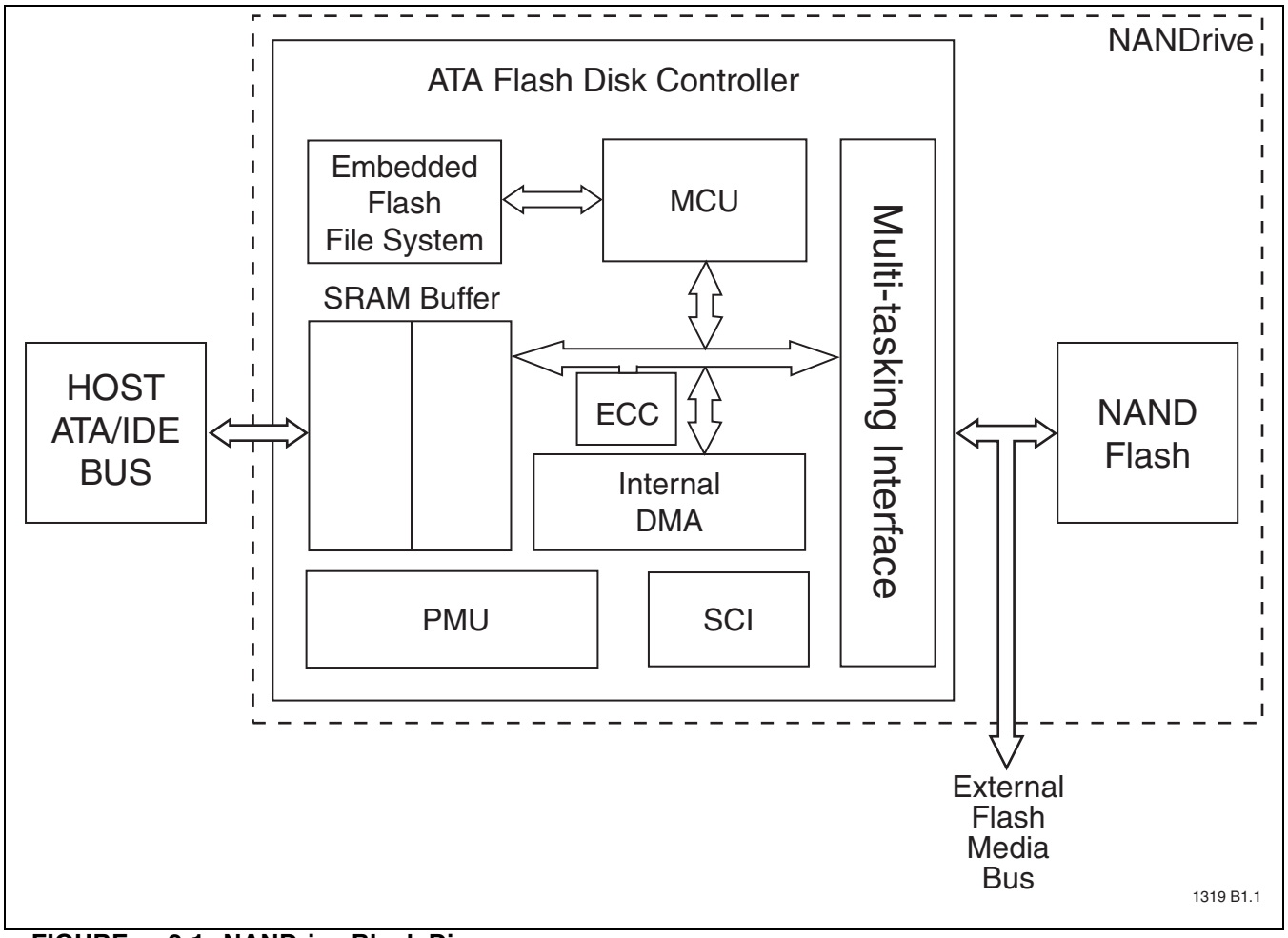

FIGURE 2-1: NANDrive Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a “#” suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NANDrive sources are outputs.

The NANDrive functions in ATA mode, which is compatible with IDE hard disk drives.

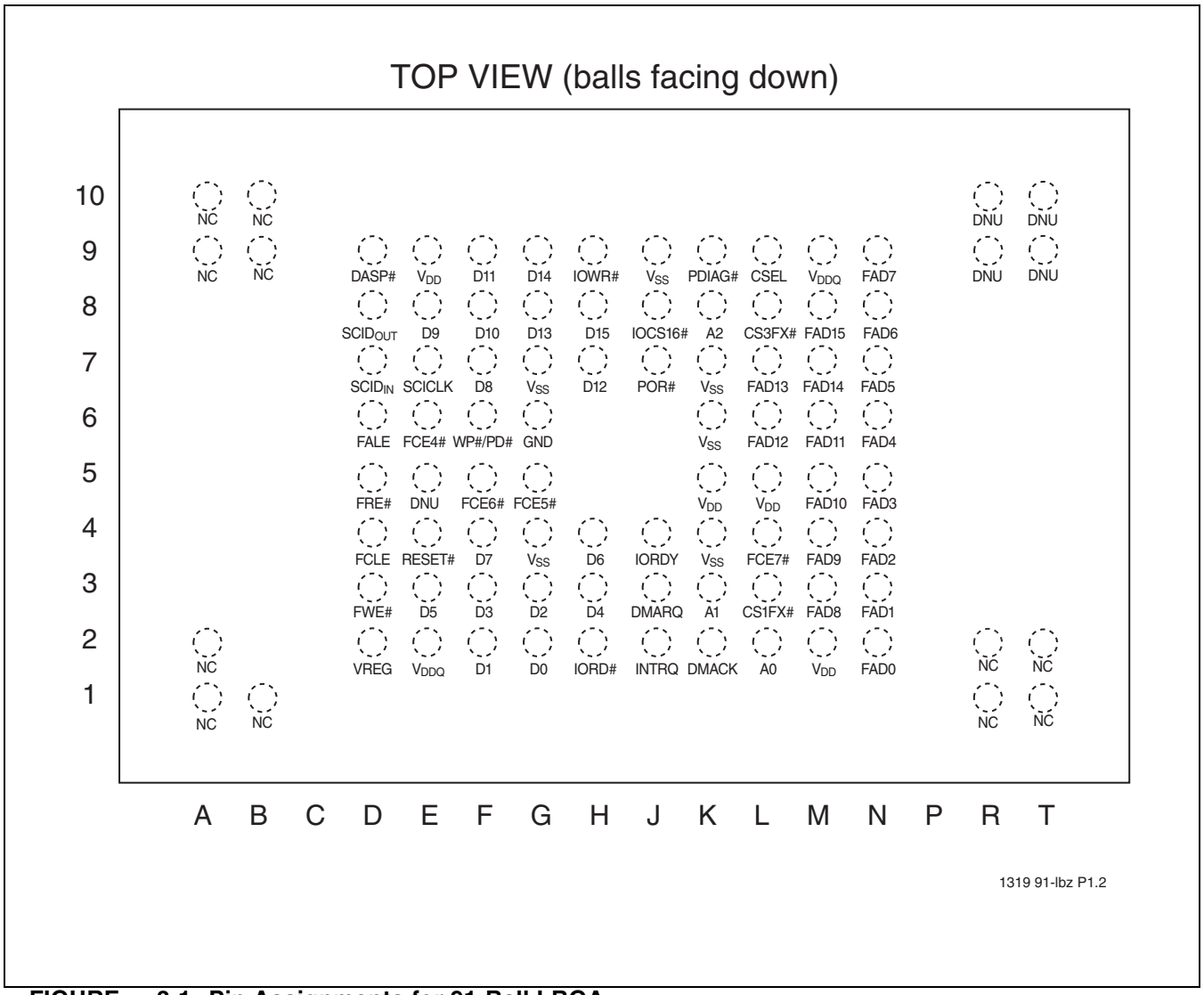

FIGURE 3-1: Pin Assignments for 91-Ball LBGA

TABLE 3-1: Pin Assignments (1 of 3)

Symbol	Pin No. 91-TFBGA	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	K3			
A0	L2			
D15	H8	I/O	I1Z/O2	D[15:0] Data bus
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7			
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK	K2	I	I2U	DMA Acknowledge - input from host
DMARQ	J3	O	O1	DMA Request to host
CS1FX#	L3	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	L8			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	IORD#: This is an I/O Read Strobe generated by the host. When Ultra DMA mode is not active, this signal gates I/O data from the device.
HDMARDY#				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
HSTROBE				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	H9	I	I2Z	This is an I/O Write Strobe generated by the host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device.
STOP				When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst

TABLE 3-1: Pin Assignments (Continued) (2 of 3)

Symbol	Pin No. 91-TFBGA	Pin Type	I/O Type	Name and Functions
IORDY	J4	O	I2Z	IORDY: When Ultra DMA mode DMA Write is not active and the device is not ready to respond to a data transfer request, this signal is negated to extend the Host transfer cycle. However, it is never negated by this controller.
DDMARDY#				DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is ready to receive Ultra DMA data-in bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
DSTROBE				DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-out strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
IOCS16#	J8	O	O2	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	J2	O	O1	This signal is the active high Interrupt Request to the host.
PDIAG#	K9	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the host.
WP#/PD#	F6	I	I3U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
External Flash Media Bus				
FRE#	D5	O	O5	Active Low Flash Media Chip Read
FWE#	D3			Active Low Flash Media Chip Write
FCLE	D4			Active High Flash Media Chip Command Latch Enable
FALE	D6			Active High Flash Media Chip Address Latch Enable
FAD15	M8	I/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	M7			
FAD13	L7			
FAD12	L6			
FAD11	M6			
FAD10	M5			
FAD9	M4			
FAD8	M3			
FAD7	N9	I/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	N8			
FAD5	N7			
FAD4	N6			
FAD3	N5			
FAD2	N4			
FAD1	N3			
FAD0	N2			
FCE7#	L4	I/O	O4	Active Low Flash Media Chip Enable pin.
FCE6#	F5	O	O4	Active Low Flash Media Chip Enable pin
FCE5#	G5			
FCE4#	E6			

TABLE 3-1: Pin Assignments (Continued) (3 of 3)

Symbol	Pin No. 91-TFBGA	Pin Type	I/O Type	Name and Functions
Serial Communication Interface (SCI)				
$SCID_{OUT}$	D8	O	O4	SCI interface data output
$SCID_{IN}$	D7	I	I3U	SCI interface data input
SCICLK	E7	I	I3U	SCI interface clock
Miscellaneous				
V_{SS}	G4, G6, G7, K4, K6, K7, J9	PWR		Ground
V_{DD}	E9, K5, L5, M2	PWR		V_{DD} (3.3V)
V_{DDQ}	E2, M9	PWR		V_{DDQ} (5V/3.3V) for Host interface
POR#	J7	I	Analog Input[1]	Power-on Reset (POR). Active Low
V_{REG}	D2	O		Capacitor pin, should connect 4.7µ cap to ground for future compatibility.
DNU[2]	E5, R9, R10, T9, T10			Do not use.
NC[3]	A1, A2, A9, A10, B1, B9, B10, R1, R2, T1, T2			No Connect

T3-1.3 1319(01)

1. Analog input for supply voltage detection
2. This pin is a no connect.
3. This pin is a no connect used for mechanical stability.

4.0 CAPACITY SPECIFICATION

Table 4-1 shows the default capacity and specific settings for heads, sectors, and cylinders. Users can change the default settings in the drive ID table using the Identity-Drive command. If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. It should also be noted that if the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance will be reduced.

TABLE 4-1: Default NANDrive Settings

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
128 MByte	128,057,344	977	8	32	250,112
256 MByte	256,901,120	980	16	32	501,760
512 MByte	512,483,328	993	16	63	1,000,944
1 GByte	1,024,966,656	1986	16	63	2,001,888
2 GByte	2,048,385,024	3969	16	63	4,000,752
4 GByte	4,096,253,952	7937	16	63	8,000,496

T4-1.6 1319(01)

TABLE 4-2: Sustained Performance

Product	Write Performance	Read Performance
SST85LD1001K-60-4C-LBTE	Up to 2 MByte/sec	Up to 13 MByte/sec
SST85LD1002L-60-4C-LBTE	Up to 4 MByte/sec	Up to 23 MByte/sec
SST85LD1004M-60-4C-LBTE	Up to 8 MByte/sec	Up to 30 MByte/sec

T4-2.1319(01)

TABLE 4-3: Supported ATA Modes

Products	PIO	MWDMA	UltraDMA
SST85LD1001K-60-4C-LBTE SST85LD1002L-60-4C-LBTE SST85LD1004M-60-4C-LBTE	Up to Mode-6	Up to Mode-4	Up to Mode-4

T4-3.1319(01)

5.0 CONFIGURABLE WRITE PROTECT/ POWER-DOWN MODES

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

5.1 Write Protect Mode

When the device is configured in the Write Protect mode, the WP#/PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP#/PD# pin should be asserted prior to issuing the destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Long-Sector, Write-Multiple, Write-Multiple-without-Erase, Write-Sector(s), Write-Sector-without-Erase, or Write-Verify. This will force the NANDrive to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

5.2 Power-down Mode

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, the NANDrive completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

6.0 POWER-ON INITIALIZATION AND CAPACITY EXPANSION

NANDrive is self-initialized during the first power-up. As soon as the power is applied to the NANDrive it reports busy for typically up to five seconds while performing bad blocks search and low level format. This initialization is a one time event.

During the first self-initialization, the NANDrive firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, the NANDrive performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format.

If the drive initialization fails, and a visual inspection is unable to determine the problem, SST provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

6.1 ATA/IDE Interface

The ATA interface can be used for NANDrive manufacturing support. SST provides an example of a DOS-based solution (an executable routine downloadable from www.sst.com) for manufacturing debug and rework.

6.2 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting. The SCI consists of 3 active signals: SCIDOUT, SCIDIN, and SCICLK. Always provide SCI interface access to PCB design to aid in design validation.

7.0 LIFETIME EXPECTANCY

NANDrive provides minimum endurance of 100,000 or 10,000 (as indicated by endurance sub-block of part number) program/erase cycles and 10 year data retention as stated by the selected NAND Flash components. The extensive ECC and wear leveling algorithms utilized in the NANDrive extend the life of the product.

8.0 PRODUCT ORDERING INFORMATION

SST 85 LD X XXXX - XXX - XC - XXX E
XX XX X XXXX - XXX - XX - XXX X

Environmental Attribute
E[1] = non-Pb

Package Modifier
T = 88 ball positions (nearest letter code to total ball count of 91)

Package Type
LB = LBGA

Operation Temperature
C = Commercial: 0°C to +70°C

Endurance
4 = 10,000 cycles minimum

Host Access Time
60 = 60ns - UDMA Mode - 4

Relative Performance Indicator
Higher letter indicates higher performance

Capacity
001 = 1 GByte
002 = 2 GByte
004 = 4 GByte

MByte or GByte Designator
1 = GByte

Voltage
L = 3.3V

Product Series
85 = NANDrive

1 Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

8.1 Valid Combinations

SST85LD1001K-60-4C-LBTE SST85LD1002L-60-4C-LBTE SST85LD1004M-60-4C-LBTE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

9.0 PACKAGING DIAGRAM

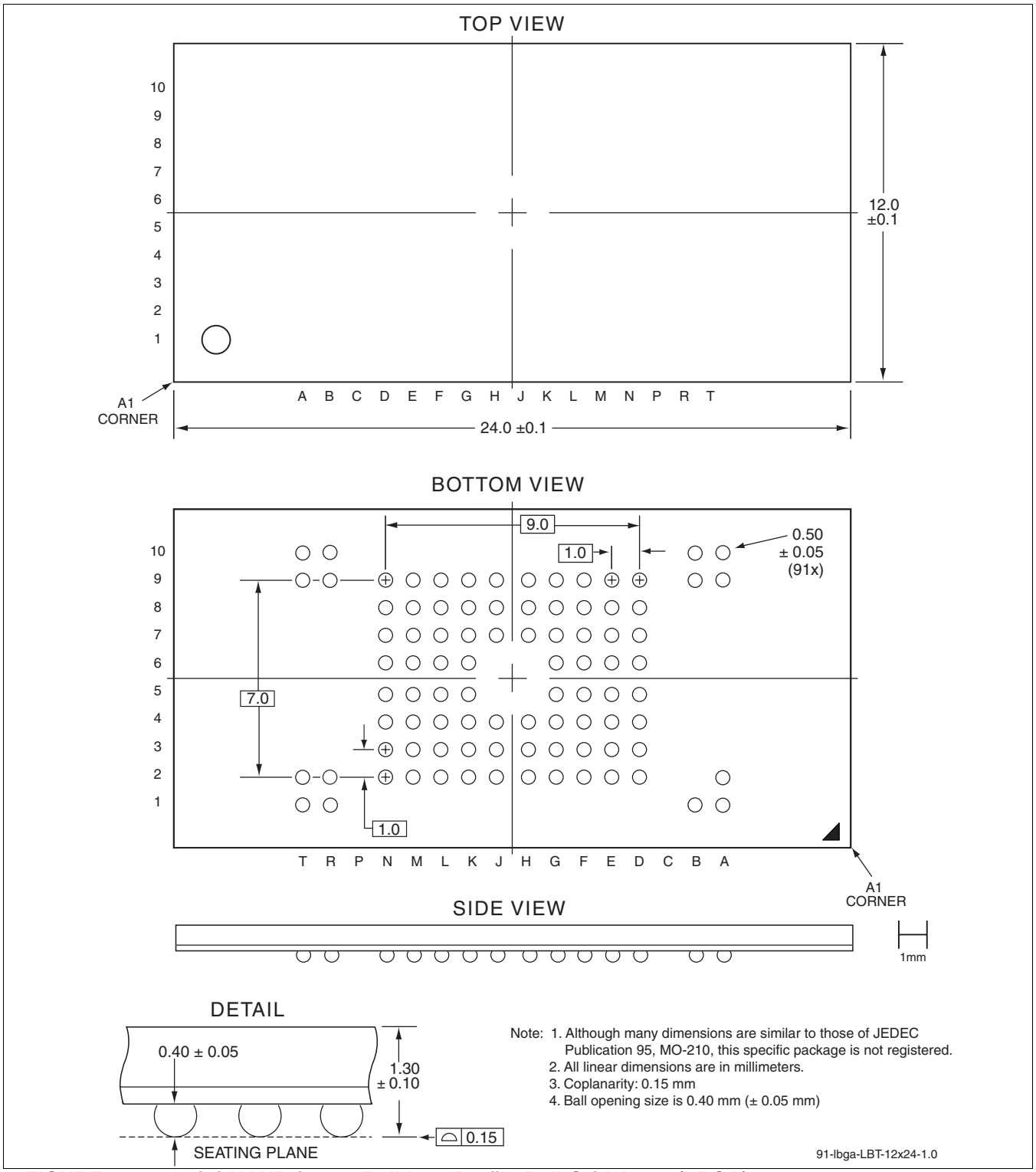

FIGURE 9-1: mini-NANDrive 91-Ball Low Profile Ball Grid Array (LBGA)
SST Package Code: LBT

TABLE 9-1: Revision History

Number	Description	Date
00	• Initial release of Fact Sheet for SST85LD1001K / SST85LD1002L / SST85LD1004M	Nov 2007

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

SST85LD1001K-60-4C-LBTE SST85LD1002L-60-4C-LBTE SST85LD1004M-60-4C-LBTE