

3 Gbps HD/SD SDI Cable Driver with Cable Detect

Check for Samples: [LMH0303](#)

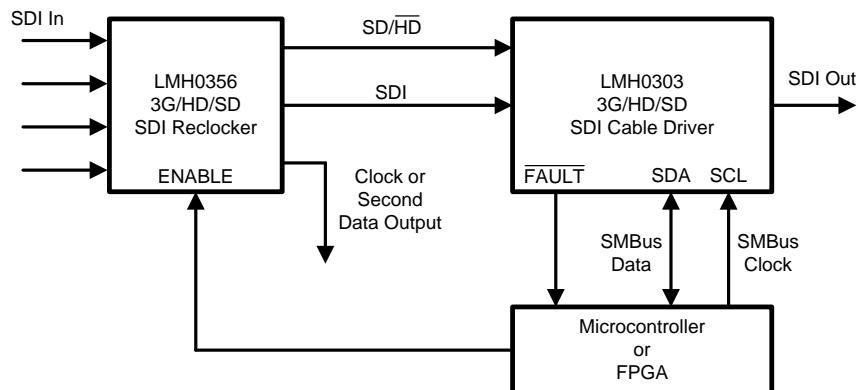
FEATURES

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M Compliant**
- **Data Rates to 2.97 Gbps**
- **Supports DVB-ASI at 270 Mbps**
- **Cable Detect on Output**
- **Loss of Signal Detect at Input**
- **Output Driver Power Down Control**
- **Typical Power Consumption: 130 mW in SD Mode and 155 mW in HD Mode**
- **Power Save Mode Typical Power Consumption: 4 mW**
- **Single 3.3V Supply Operation**
- **Differential Input**
- **75Ω Differential Output**
- **Selectable Slew Rate**
- **Industrial Temperature Range: -40°C to +85°C**
- **16-pin WQFN Package**
- **Footprint Compatible With the LMH0302**

APPLICATIONS

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M Serial Digital Interfaces**
- **Digital Video Routers and Switches**
- **Distribution Amplifiers**

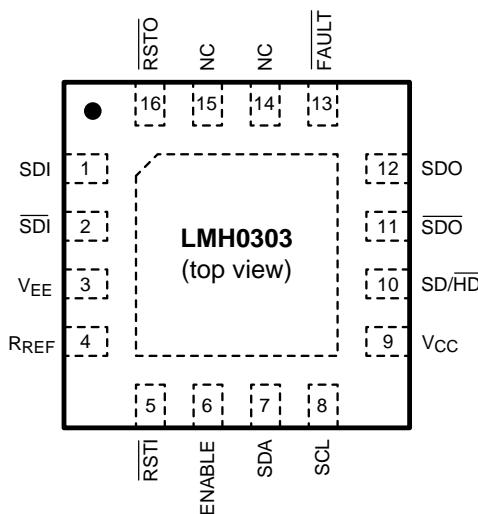
Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Connection Diagram



The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

Figure 1. 16-Pin WQFN Package Number RUM

PIN DESCRIPTIONS

Pin	Name	Description
1	SDI	Serial data true input.
2	$\overline{\text{SDI}}$	Serial data complement input.
3	V_{EE}	Negative power supply (ground).
4	R_{REF}	Bias resistor. Connect a 750Ω resistor to V_{cc} .
5	$\overline{\text{RSTI}}$	Reset input. $\overline{\text{RSTI}}$ has an internal pullup. H = Normal operation. L = Device reset. The device operates with default register settings. Forcing $\overline{\text{RSTI}}$ low also forces RSTO low.
6	ENABLE	Output driver enable. ENABLE has an internal pullup. H = Normal operation. L = Output driver powered off.
7	SDA	SMBus bidirectional data pin. When functioning as an output, it is open drain. This pin requires an external pullup.
8	SCL	SMBus clock input. SCL is input only. This pin requires an external pullup.
9	V_{cc}	Positive power supply (+3.3V).
10	$\text{SD}/\overline{\text{HD}}$	Output slew rate control. $\text{SD}/\overline{\text{HD}}$ has an internal pulldown. H = Output rise/fall time complies with SMPTE 259M. L = Output rise/fall time complies with SMPTE 424M / 292M.
11	$\overline{\text{SDO}}$	Serial data complement output.
12	SDO	Serial data true output.
13	$\overline{\text{FAULT}}$	Fault open drain output flag. Requires external pullup resistor and may be wire ORed with multiple cable drivers. H = Normal operation. L = Loss of signal or termination fault for any output.
14	NC	No connect. Not bonded internally.
15	NC	No connect. Not bonded internally.
16	$\overline{\text{RSTO}}$	Reset output. $\overline{\text{RSTO}}$ is automatically set to 1 when register 0 is written. It can be reset back to zero by forcing $\overline{\text{RSTI}}$ to zero to reset the device. Used to daisy chain multiple cable drivers on the same SMBus.
DAP	V_{EE}	Connect exposed DAP to negative power supply (ground).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage	−0.5V to 3.6V	
Input Voltage (all inputs)	−0.3V to $V_{CC}+0.3V$	
Output Current	28 mA	
Storage Temperature Range	−65°C to +150°C	
Junction Temperature	+125°C	
Lead Temperature (Soldering 4 Sec)	+260°C	
Package Thermal Resistance	θ_{JA} 16-pin WQFN	+43°C/W
	θ_{JC} 16-pin WQFN	+7°C/W
ESD Rating	HBM	8 kV
	MM	400V
	CDM	2 kV

(1) Absolute Maximum Ratings are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of [Electrical Characteristics](#) specifies acceptable device operating conditions.

Recommended Operating Conditions

Supply Voltage ($V_{CC} - V_{EE}$)	3.3V ±5%
Operating Free Air Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified⁽¹⁾⁽²⁾.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, \overline{SDI}	1.6 + $V_{SDI}/2$		$V_{CC} - V_{SDI}/2$	V
V_{SDI}	Input Voltage Swing			100		2200	mV_{P-P}
V_{CMOUT}	Output Common Mode Voltage		\overline{SDO} , \overline{SDO}		$V_{CC} - V_{SDO}$		V
V_{SDO}	Output Voltage Swing			720	800	880	mV_{P-P}
V_{IH}	Input Voltage High Level		SD/ \overline{HD} , ENABLE	2.0			V
V_{IL}	Input Voltage Low Level					0.8	V
I_{CC}	Supply Current	SD/ \overline{HD} = 0, \overline{SDO}/SDO enabled			47	57	mA
		SD/ \overline{HD} = 1, \overline{SDO}/SDO enabled			40	47	mA
		\overline{SDO}/SDO disabled			1.3	2.5	mA

SMBus DC Specifications

V_{SIL}	Data, Clock Input Low Voltage					0.8	V
V_{SIH}	Data, Clock Input High Voltage			2.1		V_{SDD}	V
$I_{SPULLUP}$	Current through pullup resistor or current source	$V_{OL} = 0.4$ V		4			mA
V_{SDD}	Nominal Bus Voltage			3.0		3.6	V
I_{SLEAKB}	Input Leakage per bus segment	(3)		-200		200	μA
I_{SLEAKP}	Input Leakage per pin			-10		10	μA
C_{SI}	Capacitance for SDA and SCL	(3) (4)				10	pF

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to $V_{EE} = 0$ Volts.

(2) Typical values are stated for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.

(3) Recommended value — Parameter not tested.

(4) Recommended maximum capacitive load per bus segment is 400 pF.

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified⁽¹⁾.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{SDI}	Input Data Rate		SDI, \overline{SDI}			2970	Mbps
t_{jit}	Additive Jitter	2.97 Gbps	SDO, \overline{SDO}		20		μs_{P-P}
		1.485 Gbps			18		μs_{P-P}
		270 Mbps			15		μs_{P-P}
t_r, t_f	Output Rise Time, Fall Time	$SD/\overline{HD} = 0, 20\% - 80\%$,		90	130		ps
		$SD/\overline{HD} = 1, 20\% - 80\%$		400		800	ps
	Mismatch in Rise/Fall Time	$SD/\overline{HD} = 0$				30	ps
		$SD/\overline{HD} = 1$				50	ps
	Duty Cycle Distortion	$SD/\overline{HD} = 0, 2.97 \text{ Gbps}^{(2)}$				27	ps
		$SD/\overline{HD} = 0, 1.485 \text{ Gbps}^{(2)}$				30	ps
		$SD/\overline{HD} = 1^{(2)}$				100	ps
t_{os}	Output Overshoot	$SD/\overline{HD} = 0^{(2)}$				10	%
		$SD/\overline{HD} = 1^{(2)}$				8	%
RL_{SDO}	Output Return Loss	5 MHz - 1.5 GHz ⁽³⁾		15			dB
		1.5 GHz - 3.0 GHz ⁽³⁾		10			dB

SMBus AC Specifications

f_{SMB}	Bus Operating Frequency			10		100	kHz
t_{BUF}	Bus free time between Stop and Start Condition			4.7			μs
$t_{HD:STA}$	Hold time after (repeated) Start Condition. After this period, the first clock is generated.	At $I_{SPULLUP} = MAX$		4.0			μs
$t_{SU:STA}$	Repeated Start Condition setup time			4.7			μs
$t_{SU:STO}$	Stop Condition setup time			4.0			μs
$t_{HD:DAT}$	Data hold time			300			ns
$t_{SU:DAT}$	Data setup time			250			ns
t_{LOW}	Clock low period			4.7			μs
t_{HIGH}	Clock high period			4.0		50	μs
t_F	Clock/Data Fall Time					300	ns
t_R	Clock/Data Rise Time					1000	ns
t_{POR}	Time in which device must be operational after power on					500	ms

(1) Typical values are stated for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.

(2) Specification is ensured by characterization.

(3) Output return loss is dependent on board design. The LMH0303 meets this specification on the SD303 evaluation board.

TIMING DIAGRAM

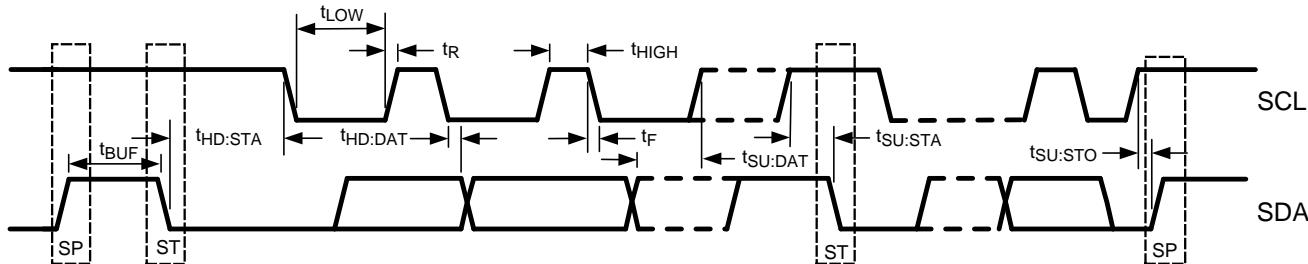


Figure 2. SMBus Timing Parameters

DEVICE OPERATION

INPUT INTERFACING

The LMH0303 accepts either differential or single-ended input. For single-ended operation, the unused input must be properly terminated.

OUTPUT INTERFACING

The LMH0303 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75Ω AC-coupled coaxial cable with an R_{REF} resistor of 750Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC} . The only resistor value that should be used for R_{REF} is 750Ω.

The R_{REF} resistor should be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network should be removed to minimize parasitic capacitance.

OUTPUT SLEW RATE CONTROL

The LMH0303 output rise and fall times are selectable for either SMPTE 259M or SMPTE 424M / 292M compliance via the SD/HD pin. For slower rise and fall times, or SMPTE 259M compliance, SD/HD is set high. For faster rise and fall times, or SMPTE 424M and SMPTE 292M compliance, SD/HD is set low. SD/HD may also be controlled using the SMBus, provided the SD/HD pin is held low. SD/HD has an internal pulldown.

OUTPUT ENABLE

The SDO/SDO output driver can be enabled or disabled with the ENABLE pin. When set low, the output driver is powered off and the LMH0303 enters a deep power save mode. ENABLE has an internal pullup.

INPUT LOS OF SIGNAL DETECTION (LOS)

The LMH0303 detects when the input signal does not have a video-like pattern. Self oscillation and low levels of noise are rejected. This loss of signal detect allows a very sensitive input stage that is robust against coupled noise without any degradation of jitter performance.

Via the SMBus, the loss of signal detect can either add an input offset or mute the outputs. An offset is added by default. Additionally, the loss of signal detect can be linked to the ENABLE functionality so that when the LOS goes low, ENABLE will also go low.

OUTPUT CABLE DETECTION

The LMH0303 detects when an output is locally terminated. When a video signal (or AC test signal) is present on SDI, the device senses the SDO and SDO amplitudes. If the output is not properly terminated (via a terminated cable or local termination), the amplitude will be higher than expected, and the Termination Fault signal is asserted. The Termination Fault signal is de-asserted when the proper termination is applied. This feature allows the system designer the flexibility to react to cable attachment and removal. Note that a long length of cable will look like a proper termination at the device output.

The cable driver must be enabled for the termination detection to operate. If the Termination Fault will be used to power down the LMH0303, then periodic polling (enabling) is recommended to monitor the output termination. For example, when a Fault condition is triggered, ENABLE can be driven low to power down the device. The LMH0303 should be re-enabled periodically to check the status of the output termination. The LMH0303 needs to be powered on for roughly 4 ms for Termination Fault detection to work.

SMBus Interface

The System Management Bus (SMBus) is a two-wire interface designed for the communication between various system component chips. By accessing the control functions of the circuit via the SMBus, pincount is kept to a minimum while allowing a maximum amount of versatility. The LMH0303 has several internal configuration registers which may be accessed via the SMBus.

The 7-bit default address for the LMH0303 is 17h. The LSB is set to 0b for a WRITE and 1b for a READ, so the 8-bit default address for a WRITE is 2Eh and the 8-bit default address for a READ is 2Fh. The SMBus address may be dynamically changed.

In applications where there might be several LMH0303s, the SDA, SCL, and FAULT pins can be shared. The SCL, SDA, and FAULT pins are open drain and require external pullup resistors. Multiple LMH0303s may have the FAULT pin wire ORed. This signal becomes active when either loss of signal is detected or any termination faults are detected. The registers may be read in order to determine the cause. Additionally, each signal can be masked from the FAULT pin.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See [Table 1](#) for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drives the 8-bit data byte.
6. The Device drives an ACK bit ("0").
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The Device (Slave) drives the ACK bit ("0").
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit ("0").
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
7. The Device drives an ACK bit "0".
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit "1" indicating end of the READ transfer.
10. The Host drives a STOP condition.

APPLICATION INFORMATION

Figure 3 shows the application circuit for the LMH0303.

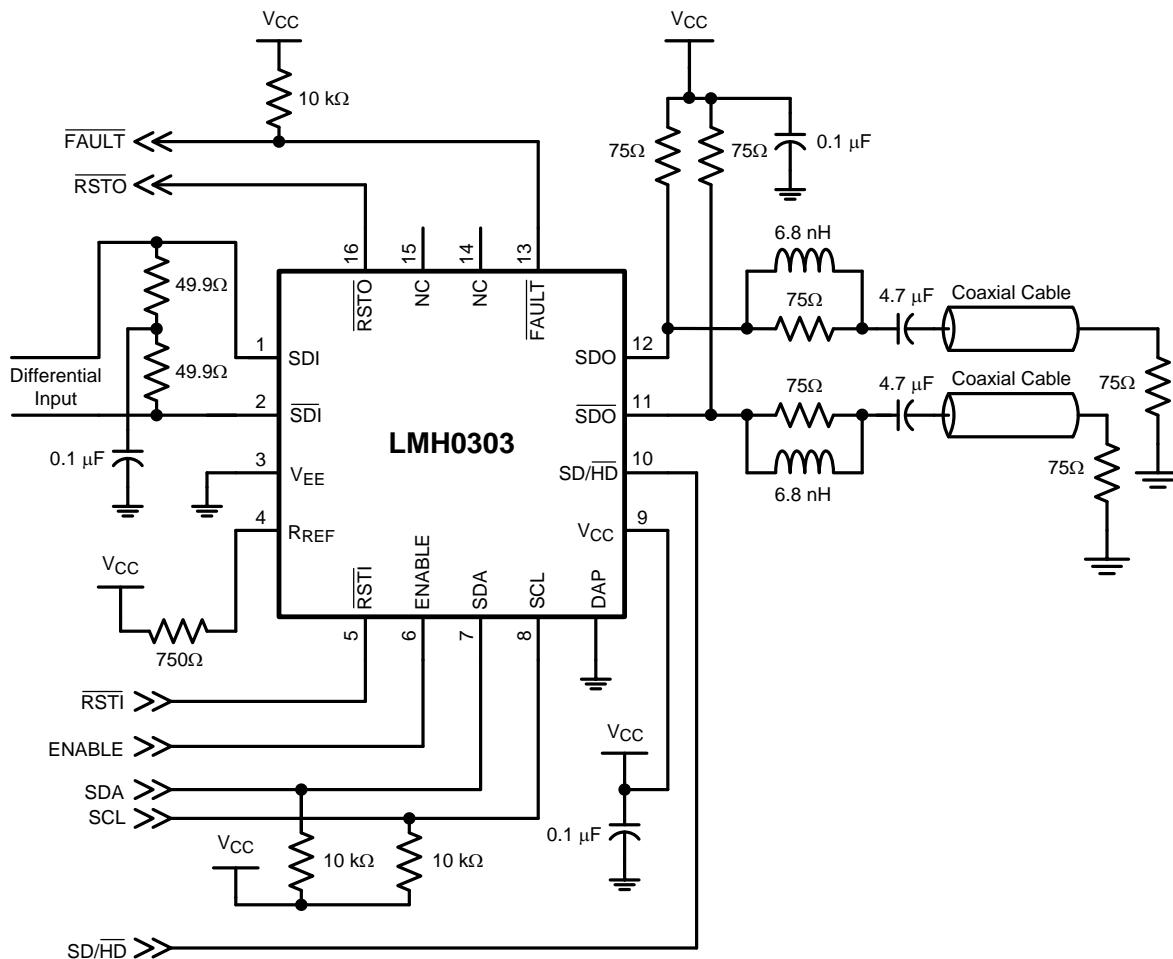


Figure 3. Application Circuit

COMMUNICATING WITH MULTIPLE LMH0303 CABLE DRIVERS VIA THE SMBus

A common application for the LMH0303 will utilize multiple cable driver devices. Even though the LMH0303 devices all have the same default SMBus device ID (address), it is still possible for them share the SMBus signals as shown in Figure 4. A third signal is required from the host to the first device. This signal acts as a “Enable / Reset” signal. Additional LMH0303s are controlled from the upstream device. In this control scheme, multiple LMH0303s may be controlled via the two-wire SMBus and the use of one GPO (General Purpose Output) signal. Other SMBus devices may also be connected to the two wires, assuming they have their own unique SMBus addresses.

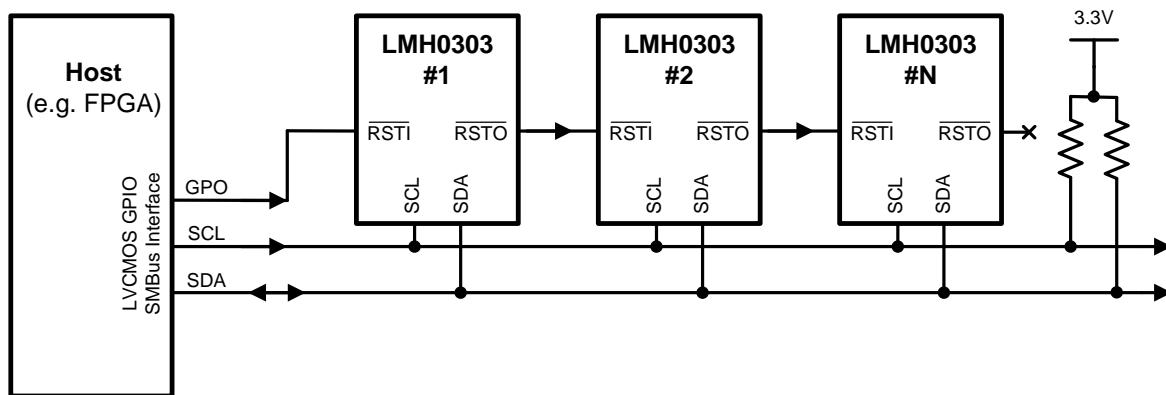


Figure 4. SMBus Configuration for Multiple LMH0303 Cable Drivers

The RSTI pin of the first device is controlled by the system with a GPO pin from the host. The first LMH0303 RSTO pin is then daisy chained to the next device's RSTI pin. That device's RSTO pin is connected to the next device and so on.

The procedure at initialization is to:

1. Hold the host GPO pin Low in RESET, to the first device. RSTO output default is also Low which holds the next device in RESET in the chain.
2. Raise the host GPO signal to LMH0303 #1 RSTI input pin.
3. Write to Address 8'h2E (7'h17) Register 0 with the new address value (e.g. 8'h2C (7'h16)).
4. Upon writing Register 0 in LMH0303 #1, its RSTO signal will switch High. Its new address is 8'h2C (7'h16), and the next LMH0303 in the chain will now respond to the default address of 8'h2E (7'h17).
5. The process is repeated until all LMH0303 devices have a unique address loaded.
6. Direct SMBus writes and reads may now take place between the host and any addressed device.

The 7-bit address field allows for 128 unique addresses. The above procedure allows for the reprogramming of the LMH0303 devices such that multiple devices may share the two-wire SMBus. Make sure all devices on the bus have unique device IDs.

If power is toggled to the system, the SMBus address routine needs to be repeated.

SMBUS REGISTERS

Table 1. SMBus Registers

Address	R/W	Name	Bits	Field	Default	Description
00h	R/W	ID	7:1	DEVID	0010111	Device ID. Writing this register will force the RSTO pin high. Further accesses to the device must use this 7-bit address.
			0	RSVD	0	Reserved as 0. Always write 0 to this bit.
01h	R	STATUS	7:3	RSVD	00000	Reserved.
			2	TFN	0	Termination Fault for SDI. 0: No Termination Fault Detected. 1: Termination Fault Detected.
			1	TFP	0	Termination Fault for SDI. 0: No Termination Fault Detected. 1: Termination Fault Detected.
			0	LOS	0	Loss Of Signal (<u>LOS</u>) detect at input. 0: No Signal Detected. 1: Signal Detected.
02h	R/W	MASK	7	SD	0	SD Rate select bit. If the SD/ <u>HD</u> pin is set to <u>V_{CC}</u> , it overrides this bit. With the SD/ <u>HD</u> pin set to ground, this bit selects the output edge rate as follows: 0: HD edge rate. 1: SD edge rate.
			6	RSVD	0	Reserved as 0. Always write 0 to this bit.
			5	PD	0	Power Down for SDO output stage. If the ENABLE pin is set to ground, it overrides this bit. With the ENABLE pin set to <u>V_{CC}</u> , PD functions as follows: 0: SDO active. 1: SDO powered down.
			4:3	RSVD	00	Reserved as 00. Always write 00 to these bits.
			2	MTFN	0	Mask TFN from affecting <u>FAULT</u> pin. 0: TFN=1 will cause <u>FAULT</u> to be 0. 1: TFN=1 will not affect <u>FAULT</u> ; the condition is masked off.
			1	MTFP	0	Mask TFP from affecting <u>FAULT</u> pin. 0: TFP=1 will cause <u>FAULT</u> to be 0. 1: TFP=1 will not affect <u>FAULT</u> ; the condition is masked off.
			0	MLOS	0	Mask <u>LOS</u> from affecting <u>FAULT</u> pin. 0: <u>LOS</u> =0 will cause <u>FAULT</u> to be 0. 1: <u>LOS</u> =0 will not affect <u>FAULT</u> ; the condition is masked off.

Table 1. SMBus Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
03h	R/W	DIRECTION	7	HDTFTThreshLSB	1	Least Significant Bit for HDTFTThresh detection threshold. Combines with HDTFTThresh bits in register 04h.
			6	SDTFTThreshLSB	1	Least Significant Bit for SDTFTThresh detection threshold. Combines with SDTFTThresh bits in register 05h.
			5:3	RSVD	000	Reserved as 000. Always write 000 to these bits.
			2	DTFN	0	Direction of TFN that affects <u>FAULT</u> pin (when not masked). 0: TFN=1 will cause <u>FAULT</u> to be 0 (when the condition is not masked off). 1: TFN=0 will cause <u>FAULT</u> to be 0 (when the condition is not masked off).
			1	DTFP	0	Direction of TFP that affects <u>FAULT</u> pin (when not masked). 0: TFP=1 will cause <u>FAULT</u> to be 0 (when the condition is not masked off). 1: TFP=0 will cause <u>FAULT</u> to be 0 (when the condition is not masked off).
			0	DLOS	0	Direction of LOS that affects <u>FAULT</u> pin (when not masked). 0: LOS=0 will cause <u>FAULT</u> to be 0 (when the condition is not masked off). 1: LOS=1 will cause <u>FAULT</u> to be 0 (when the condition is not masked off).
04h	R/W	OUTPUT	7:5	HDTFTThresh	100	Sets the Termination Fault threshold for SDO, when SD is set to HD rates (0). Combines with HDTFTThreshLSB in register 03h (default for combined value is 1001).
			4:0	AMP	10000	SDO output amplitude in roughly 5 mV steps.

Table 1. SMBus Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
05h	R/W	OUTPUTCTRL	7	RSVD	0	Reserved as 0. Always write 0 to this bit.
			6	FLOSOFF	0	Force <u>LOS</u> to always OFF in regard to its effect on the output signal. This forces the device into either the mute or "add offset" state. The <u>LOS</u> bit in register 01h still reflects the correct state of <u>LOS</u> . 0: <u>LOS</u> operates normally, muting or adding offset as specified by the MUTE bit. 1: Muting or adding offset is always in place as specified by the MUTE bit.
			5	FLOSON	0	Force <u>LOS</u> to always ON in regard to its effect on the output signal. This prevents the device from muting or adding offset. The <u>LOS</u> bit in register 01h still reflects the correct state of <u>LOS</u> . 0: <u>LOS</u> operates normally, muting or adding offset as specified in the MUTE bit. 1: Muting or adding offset never occurs.
			4	LOSEN	0	Configures <u>LOS</u> to be combined with the ENABLE functionality. 0: Only the PD bit and ENABLE pin affect the power down state of the output drivers. 1: If the ENABLE pin is set to ground, it powers down the output drivers regardless of the state of <u>LOS</u> or the PD bit. With the ENABLE pin set to V _{CC} , <u>LOS</u> =0 will power down the output drivers, and <u>LOS</u> =1 will leave the power down state dependent on the PD bit.
			3	MUTE	0	Selects whether the device will MUTE when loss of signal is detected or add an offset to prevent self oscillation. When an input signal is detected (<u>LOS</u> =1), the device will operate normally. 0: Loss of signal will force a small offset to prevent self oscillation. 1: Loss of signal will force the channel to MUTE.
			2:0	SDTFTThresh	010	Sets the Termination Fault threshold for SDO, when SD is set to SD rates (1). Combines with SDTFTThreshLSB in register 03h (default for combined value is 0101).
06h	R/W	RSVD	7:0	RSVD	00000000	Reserved as 00000000. Always write 00000000 to these bits.
07h	R/W	RSVD	7:0	RSVD	00000000	Reserved as 00000000. Always write 00000000 to these bits.
08h	R/W	TEST	7:5	CMPCMD	000	Compare command. Determines whether the peak value or the current value of the Termination Fault counters is read in registers 0Ah and 0Bh. 000: Resets compare value to 00; registers 0Ah and 0Bh show current counter values. Sets detection to look for MAX peak values. 001: Capture counter 0. Register 0Ah shows peak value. 010: Capture counter 1. Register 0Bh shows peak value. 011, 100: Reserved. 101: Resets compare value to 1Fh. Sets detection to look for MIN peak values. 110, 111: Reserved.
			4:0	RSVD	00000	Reserved as 00000. Always write 00000 to these bits.

Table 1. SMBus Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
09h	R	REV	7:5	RSVD	000	Reserved.
			4:3	DIREV	10	Die Revision.
			2:0	PARTID	011	Part Identifier. Note that single output devices (LMH0303) have the LSB=1. Dual output devices (LMH0307) have the LSB=0.
0Ah	R	TFPCOUNT	7:5	RSVD	000	Reserved.
			4:0	TFPCOUNT	00000	This is either the current value of TFP Counter, or the peak value of the counter, depending on CMPCMD in register 08h.
0Bh	R	TFNCOUNT	7:5	RSVD	000	Reserved.
			4:0	TFNCOUNT	00000	This is either the current value of TFN Counter, or the peak value of the counter, depending on CMPCMD in register 08h.

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH0303SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L0303	Samples
LMH0303SQE/NOPB	ACTIVE	WQFN	RUM	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L0303	Samples
LMH0303SQX/NOPB	ACTIVE	WQFN	RUM	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L0303	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

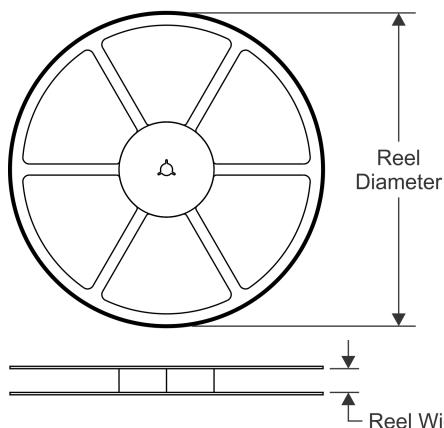
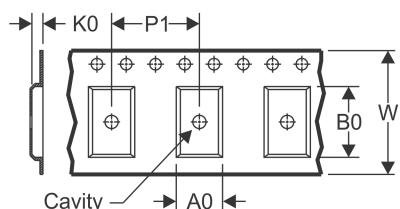
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

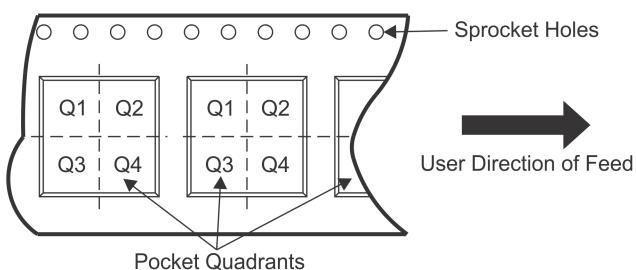
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

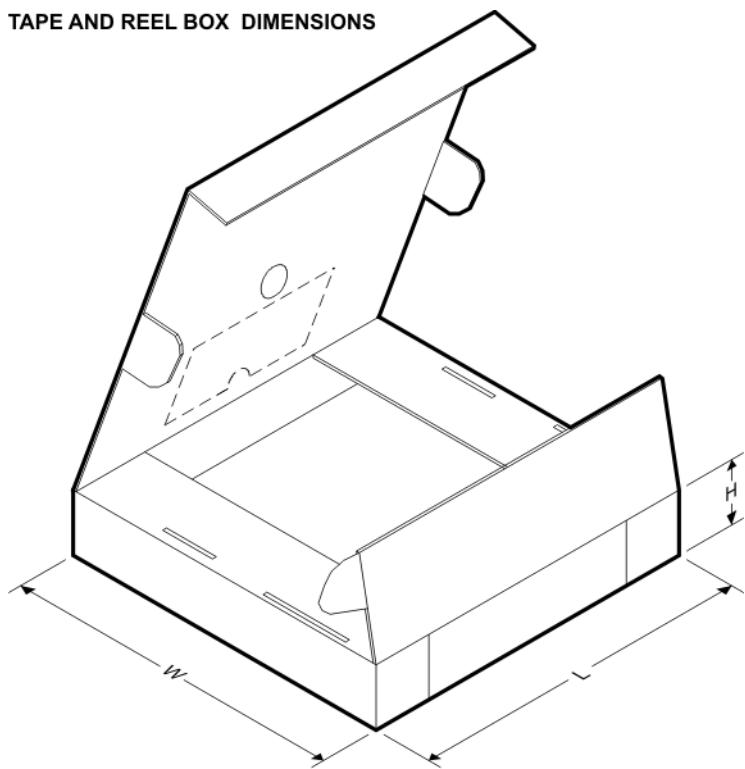
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0303SQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0303SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0303SQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

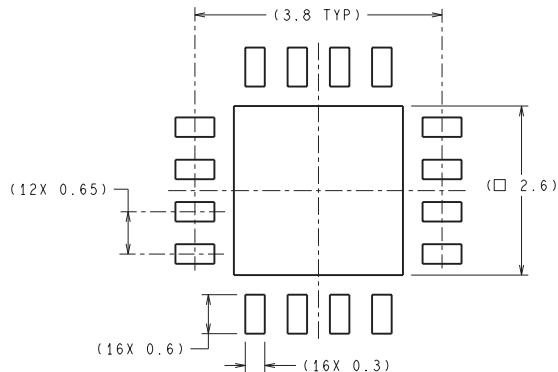
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0303SQ/NOPB	WQFN	RUM	16	1000	213.0	191.0	55.0
LMH0303SQE/NOPB	WQFN	RUM	16	250	213.0	191.0	55.0
LMH0303SQX/NOPB	WQFN	RUM	16	4500	367.0	367.0	35.0

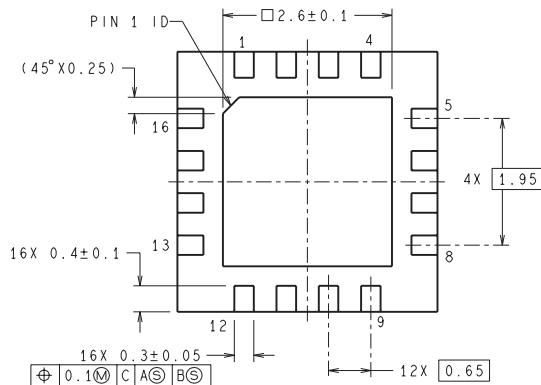
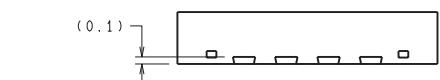
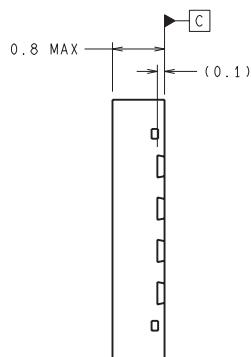
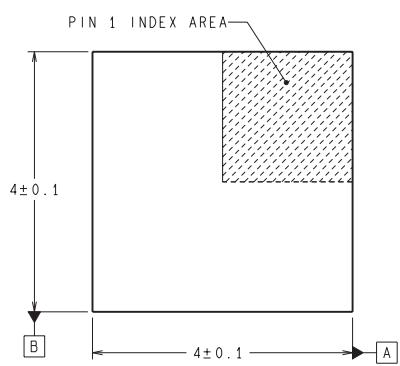
MECHANICAL DATA

RUM0016A



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN



SQB16A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity
	TI E2E Community
	e2e.ti.com