UM10391

90 Watt notebook adapter with TEA1751T and TEA1791T

Rev. 01 — 20 April 2010 **User manual**

Document information

Info	Content
Keywords	GreenChip III, TEA1751T, GreenChip SR, TEA1791T, PFC, flyback, synchronous rectification, high efficiency, adapter, notebook, PC power
Abstract	This manual provides the specification, performance, schematics, bill of materials and PCB layout of a 90 W notebook adapter with the TEA1751T and TEA1791T. For design details on the TEA1751T and TEA1791T please refer to the application notes.

Revision history

Rev	Date	Description
UM10391_1	20100420	First release

Contact information

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1. Introduction

This manual describes a universal input, 19.5 V, 4.62 A single output power supply using TEA1751T and TEA1791T devices from NXPsemiconductor's GreenChip III and GreenChip-SR family. It contains the power supply specifications, circuit diagram, component list to build the supply, PCB layout and component positions, PFC choke and transformer documentation, along with test data and oscilloscope pictures of the most important waveforms.

The GreenChip III combines the control and drive functions for both the PFC and the flyback stages into a single device. The TEA1751T provides complete SMPS control functionality to comply with the IEC61000-3-2 harmonic current emission requirements, obtain a significant reduction of components, save PCB space and give a cost benefit. It also offers extremely low power consumption in no-load mode, which makes it suitable for the low-power consumer markets. The special built-in green functions allow a high efficiency at all power levels which results in a design that can easily meet all existing and proposed energy efficiency standards such as Code of Conduct (Europe), Energy Star (US), California Energy Commission, Minimum Energy Performance Standards (Australian & New Zealand) and China Energy Conservation Program.

The GreenChip SR is the only synchronous rectification control IC available that needs no external components for tuning of the timing. Used in notebook adapter designs, the GreenChip SR offers a wide VCC operation range of 8.5 V to 38 V, minimizing the number of external components required and enabling simpler designs. In addition, the high driver output voltage (10 V) makes the GreenChip SR compatible with all brands of MOSfets.

Fig 1. 90 W TEA1751T and TEA1791T demo board

2. Specification

- Mains input voltage: 90 V to 264 V, 47 Hz to 63 Hz
- DC output: 19.5 V, 2 %
- Maximum continuous output current: 4.62 A
- Peak output current: 7.5 A
- Efficiency: > 87 % at maximum load
- CEC active mode efficiency: > 90 %
- No load power consumption: < 0.3 W
- Dynamic load response: < +1 V / −0.5 V
- Output ripple and noise: 100 $mV_{p-p(max.)}$
- CISPR22 class B conducted EMI
- EN61000-4-2 immunity against ESD
- EN61000-3-2 A14 (harmonics) compliance
- Short Circuit Protection (SCP) and output Over-Current Protection (OCP); input power < 3 W at both SCP and OCP test
- Latched output Over Voltage Protection (OVP): < 25 V
- Latched Over Temperature Protection (OTP)
- Fast Latch Reset (FLR): < 3 sec.

3. Performance data

3.1 Test setup

3.1.1 Test equipment

- Programmable AC Source: Chroma, Model 61503
- Power HiTester: Hioki, Model 3332
- DC Electronic Load: Chroma, Model 63030
- Digital Oscilloscope: Tektronix, Model TDS5104B
- Current Probe/Amplifier: Tektronix, Model TCP305/TCPA300
- 100 MHz, High Voltage Differential Probe: Tektronix, Model P5205
- 6-Digit Multimeter: Agilent, Model 34401A
- EMC receiver Rohde & Schwarz ESPI-3 + LISN ENV216

3.1.2 Test conditions

- Unit on the lab-table with the heat sinks downwards
- No casing was present on the unit
- Lab temperature between 20 °C and 25 °C
- Measurements were made after stabilization of temperature according “test method for calculating the efficiency of single-voltage external AC-DC and AC-AC power supplies” of Energy Star

3.2 Efficiency

3.2.1 Efficiency PFC plus flyback stage

Test conditions:

- Before any measurements were recorded, the unit was set to maximum load and well pre-heated so that stabilization of the input and output meter readings was achieved.

Remark: The output voltage was measured at the end of the output cable.

Criteria to pass:

- The efficiency must be > 87 % at the maximum continuous output load.

Table 1. Efficiency PFC plus flyback stage

Efficiency total converter (at full load) as a function of the mains input

Input Voltage V / Hz	I_{IN} RMS (A)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)	Power factor
90/60	1.134	88.43	99.98	88.45	0.991
100/50	1.016	88.45	99.41	88.96	0.990
115/60	0.883	88.45	98.59	89.72	0.984
230/50	0.468	88.42	97.84	90.37	0.924
264/50	0.414	89.27	97.58	90.46	0.907

3.2.2 Energy Star efficiency

To market adapters sold as stand-alone adapters, and adapters supplied with notebooks as Energy Star efficient, they have to pass the active mode and no-load criteria as stated in the Energy Star standard for External Power Supplies; EPS2.0. The minimum active-mode efficiency is defined as the arithmetic average efficiency at 25 %, 50 %, 75 % and 100 % of the rated output power as printed on the name plate of the adapter.

3.2.2.1 Active mode efficiency

Test Conditions:

- The unit was set to maximum load and well pre-heated until temperature stabilization was achieved.
- Temperature stabilization was established for every load step before recording any measurements.

Remark: The output voltage was measured at the end of the output cable.

Criteria to pass:

- To comply with Energy Star EPS2.0, the arithmetic average of the four efficiency measurements must be greater than, or equal to, 87 %.
- Universal mains adapters have to pass the criteria at both 115 V / 60 Hz and 230 V / 50 Hz.

Table 2. Active mode efficiency at 115 V / 60 Hz

Load percentage	I_{OUT} (A)	V_{OUT} (V)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)	Power factor
100	4.624	19.130	88.45	98.59	89.72	0.984
75	3.468	19.198	66.58	73.47	90.63	0.973
50	2.312	19.266	44.53	49.05	90.80	0.950
25	1.156	19.329	22.35	24.61	90.83	0.452
Average	-	-	-	-	90.49	-

Table 3. Active mode efficiency at 230 V / 50 Hz

Load percentage	I_{OUT} (A)	V_{OUT} (V)	P_{OUT} (W)	P_{IN} (W)	Efficiency (%)	Power factor
100	4.624	19.124	88.42	97.84	90.37	0.924
75	3.468	19.195	66.57	73.76	90.25	0.901
50	2.312	19.262	44.53	50.18	88.74	0.880
25	1.157	19.330	22.36	24.59	90.94	0.379
Average	-	-	-	-	90.08	-

3.2.2.2 No-load input power

Test Conditions:

- The unit was set to maximum load and preheated.
- After 5 minutes the load was removed.
- The no-load input power measurements were recorded after stabilization of the input power reading.

Criteria to pass:

- To comply with Energy Star EPS2.0, the input power shall be less than 0.5 W.
- Universal mains adapters have to pass the criteria at both maximum input voltages (115 V / 60 Hz and 230 V / 50 Hz).

Table 4. No-load input power

No-load input power as a function of the mains input voltage

V / Hz	90 / 60	115 / 60	132 / 60	180 / 50	230 / 50	264 / 50
Input power P_{IN} (W)	0.124	0.130	0.137	0.158	0.186	0.200

3.3 Timing and protection

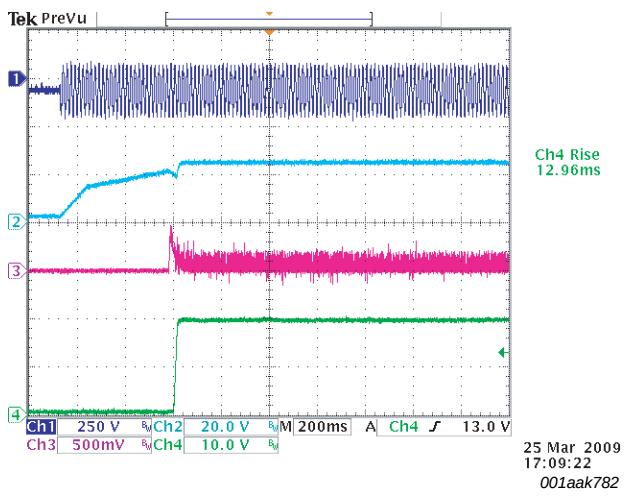
3.3.1 Switch-on delay and output rise time

Test conditions:

- The electronic load was set to Constant Current (CC) mode and V_{on} = 0 V.
- The electronic load was set to the maximum output current.

Criteria to pass:

- Switch-on delay: two seconds maximum after the AC mains voltage is applied to the time when the output is within regulation.
- Output rise time: The output voltage shall rise from 10 % of the maximum to the regulation limit within 30 mS. There must be a smooth and continuous ramp-up of the output voltage. No voltage with a negative polarity shall be present at the output during start-up.



Mains input 90 V / 60 Hz, delay time 488 ms

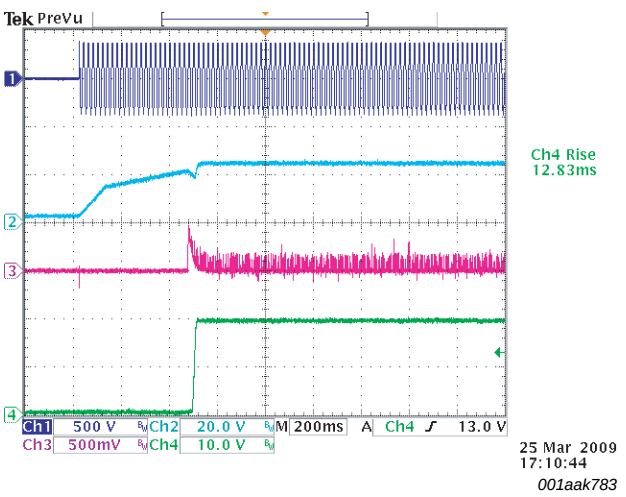
Load = 4.63 A

CH1: mains input

CH2: VCC pin TEA1751T

CH3: FBSENSE pin TEA1751T (soft start)

CH4: Vout



Mains input 264 V / 50 Hz, delay time 488 ms

Load = 4.63 A

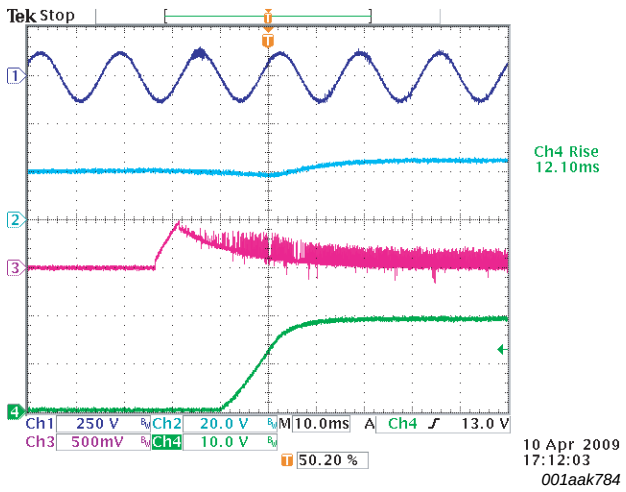
CH1: mains input

CH2: VCC pin TEA1751T

CH3: FBSENSE pin TEA1751T (soft start)

CH4: Vout

Fig 2. Delay between switch-on and output in regulation



Mains input 90 V / 60 Hz, output rise time 12.64 ms

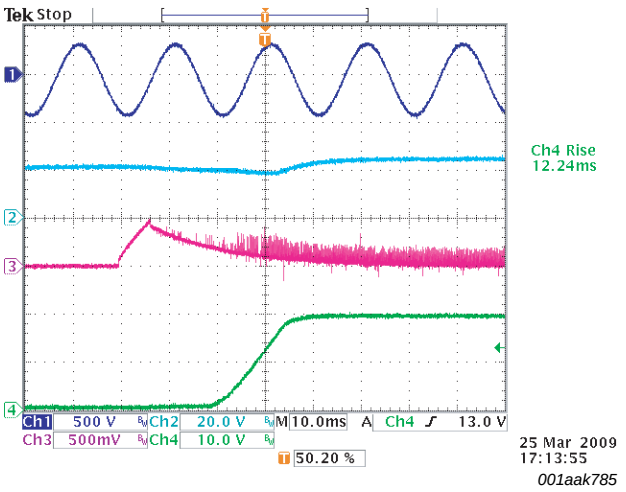
Load = 4.63 A

CH1: mains input

CH2: VCC pin TEA1751T

CH3: FBSENSE pin TEA1751T (soft start)

CH4: Vout



Mains input 264 V / 50 Hz, output rise time 12.24 ms

Load = 4.63 A

CH1: mains input

CH2: VCC pin TEA1751T

CH3: FBSENSE pin TEA1751T (soft start)

CH4: Vout

Fig 3. Output rise time at full load start-up

3.3.2 Brownout and brownout recovery

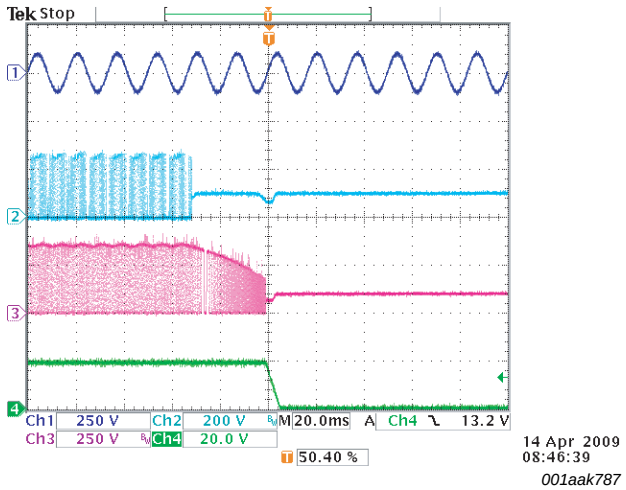
The voltage on the VINSENSE pin is sensed continuously to prevent the PFC from operating at very low mains input voltages.

Test Conditions:

- The mains input voltage decreased from 90 V AC down to zero and then increased from zero to 90 V AC.
- The electronic load was set to Constant Current (CC) mode and Von = 0 V.
- The electronic load was set to the maximum output current.

Criteria to pass:

- The unit shall survive the test without damage and not exceeding specified operating temperature test limits.
- The output voltage remains within the specified regulation limits or switch-off.
- No output bounce or hiccup is allowed during switch-on or switch-off.
- The unit shall power-up by the time the input AC line voltage reaches 85 V (max.).



Mains input from 90 V AC to 0 V AC, brownout voltage 70 V AC

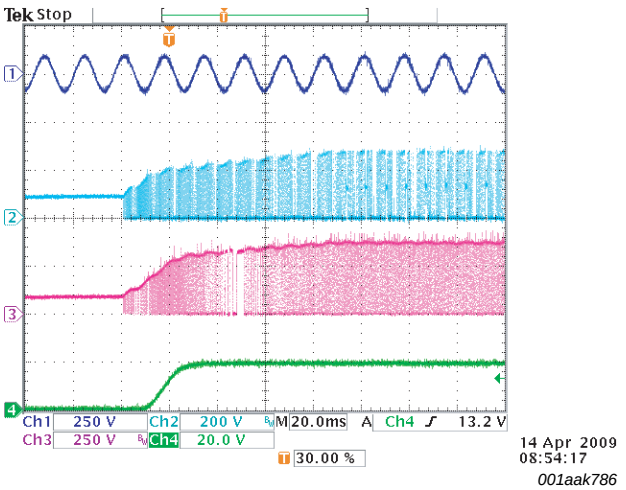
Load = 4.63 A

CH1: mains input

CH2: Vdrn PFC Mosfet

CH3: Vdrn flyback Mosfet

CH4: Vout



Mains input from 0 V AC to 90 V AC, brownout recovery 75 V AC

Load = 4.63 A

CH1: mains input

CH2: Vdrn PFC Mosfet

CH3: Vdrn flyback Mosfet

CH4: Vout

Fig 4. Brownout and brownout recovery

3.3.3 Output short circuit and open loop protection

To protect the adapter and application against an output short circuit or a single fault open (flyback) feedback loop situation, a time-out protection is implemented. When the voltage on FBCTRL pin rises above 4.5 V (typ.), a fault is assumed and switching is blocked.

The time-out protection should not trigger during a normal start-up with maximum load.

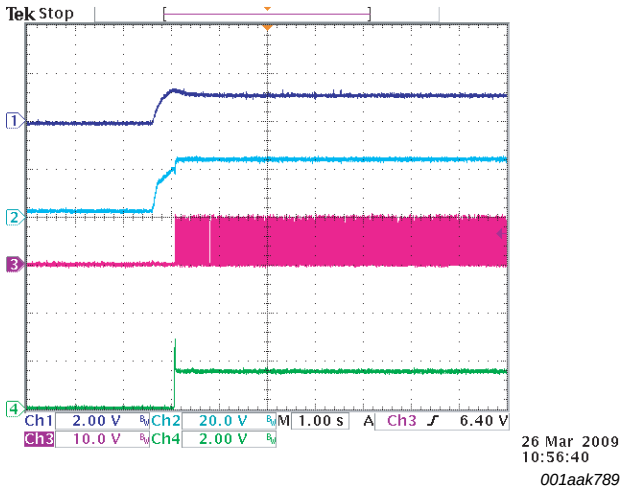
3.3.3.1 Open loop protection

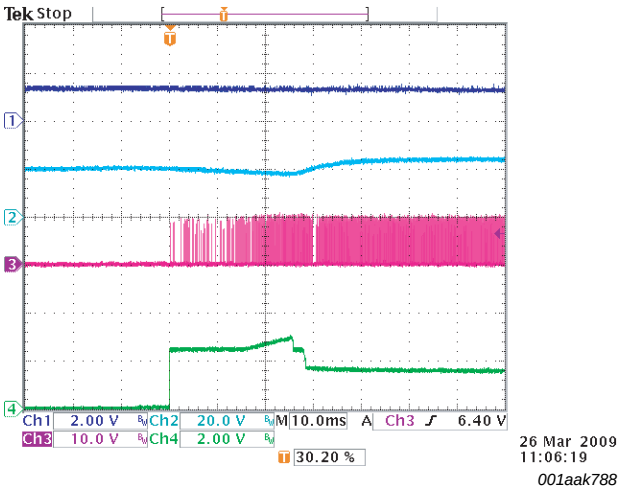
Test Conditions:

- The electronic load was set to Constant Current (CC) mode and Von = 0 V.
- The electronic load is set to the maximum output current.

Criteria to pass:

- A normal start-up with a smooth and continuous ramp-up of the output voltage.
- No output bounce or hiccup is allowed during switch-on or switch-off.
- There be must be sufficient margin between the FBCTRL level and the 4.5 V time-out trigger level to avoid false triggering of the time-out protection due to component tolerances.





Overview picture

Load = 4.63 A

CH1: VINSENSE pin TEA1751T

CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Detail of left side picture

Load = 4.63 A

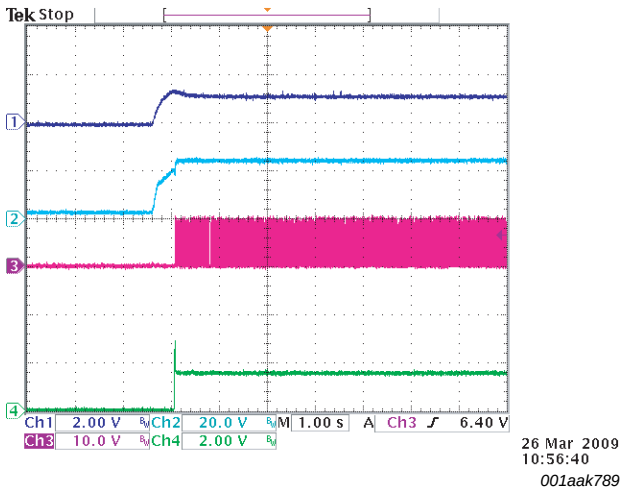
CH1: VINSENSE pin TEA1751T

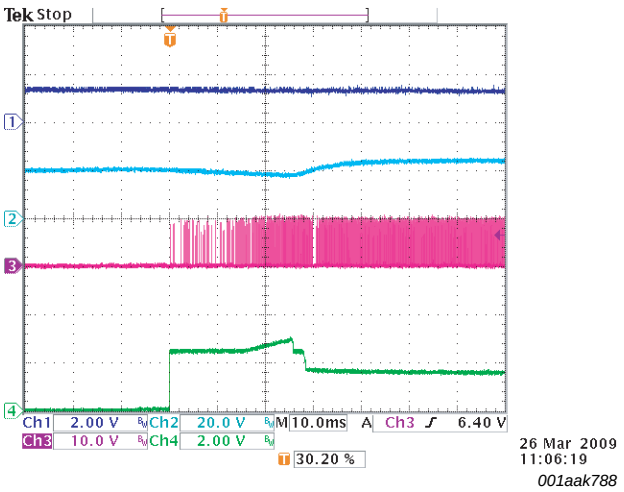
CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Fig 5. Normal start-up at 90 V / 60 Hz





Overview picture

Load = 4.63 A

CH1: VINSENSE pin TEA1751T

CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Detail of left side picture

Load = 4.63 A

CH1: VINSENSE pin TEA1751T

CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Fig 6. Normal start-up at 264 V / 50 Hz

3.3.3.2 Short-circuit protection

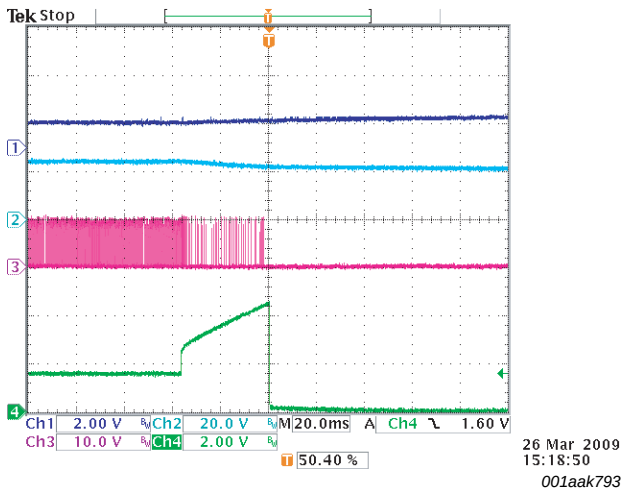
Test Conditions:

- The adapter is switched on with no load on the output. A short circuit is applied manually to the output at the end of the cable. The mains voltage is adopted to obtain the worst-case condition.
- A short circuit is applied to the output at the end of the cable before startup of the adapter. The adapter is switched on with a short circuit at the output. The mains voltage is adopted to obtain the worst-case condition.

Remark: An output short-circuit is defined as an output impedance of less than 0.1 ohm.

Criteria to pass:

- The unit shall be capable of withstanding a continuous short-circuit at the output without damage or overstress of the unit under any input conditions.
- The average input power must be less than 3 W during the short-circuit test.
- After removal of the short circuit, the unit shall recover automatically.



Output short-circuit during normal operation

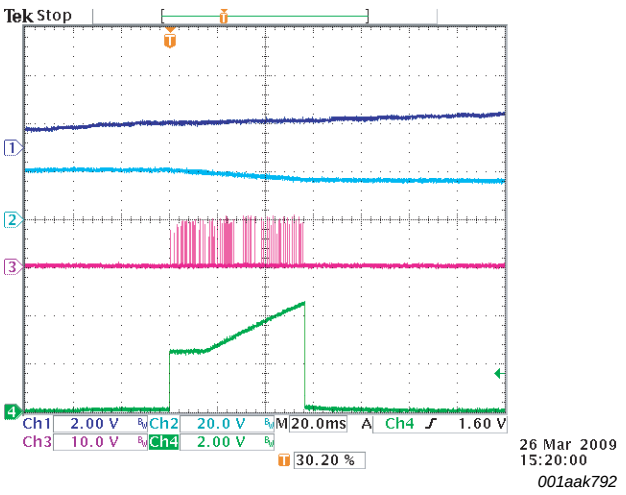
Load = 4.63 A

CH1: VINSENSE pin TEA1751T

CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T



Output short-circuit applied before start-up

Load = 4.63 A

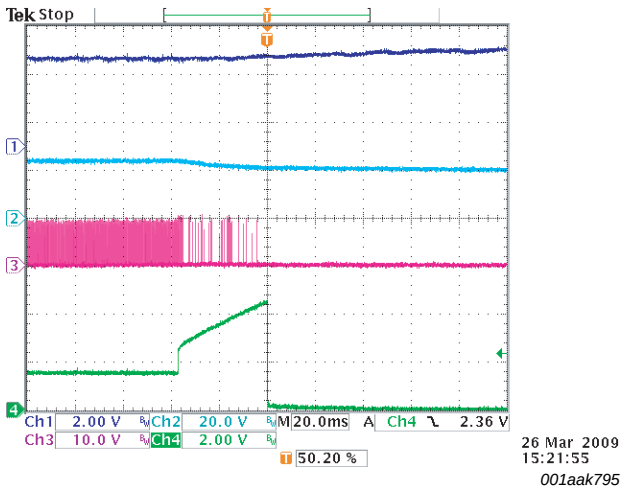
CH1: VINSENSE pin TEA1751T

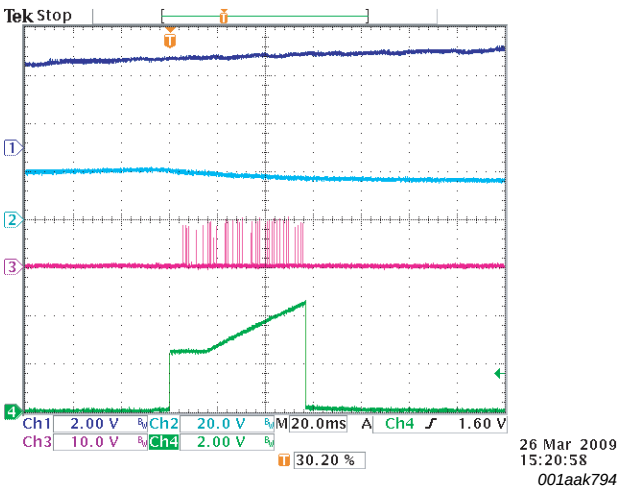
CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Fig 7. Output short-circuit at 90 V / 60 Hz





Output short-circuit during normal operation

Load = 4.63 A

CH1: VINSENSE pin TEA1751T

CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Output short-circuit applied before start-up

Load = 4.63 A

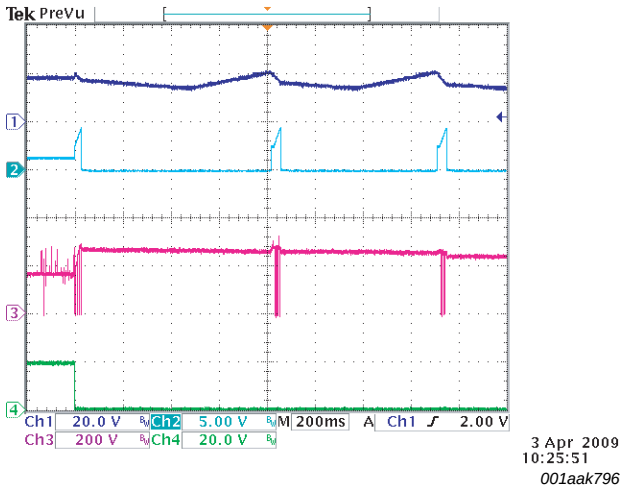
CH1: VINSENSE pin TEA1751T

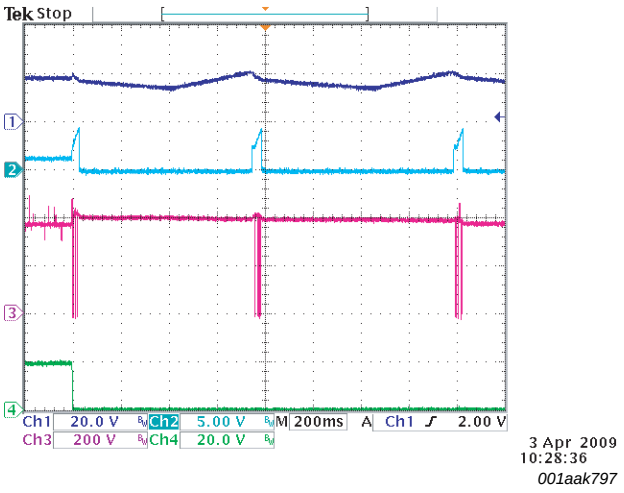
CH2: VCC pin TEA1751T

CH3: FBDRIVER pin TEA1751T

CH4: FBCTRL pin TEA1751T

Fig 8. Output short-circuit at 264 V / 50 Hz





Mains input 90 V / 60 Hz; input power 0.96 W

Load = 0 A

CH1: VCC pin TEA1751T

CH2: FBCTRL pin TEA1751T

CH3: Vdrn flyback Mosfet

CH4: Vout

Mains input 264 V / 50 Hz; input power 0.84 W

Load = 0 A

CH1: VCC pin TEA1751T

CH2: FBCTRL pin TEA1751T

CH3: Vdrn flyback Mosfet

CH4: Vout

Fig 9. Output short-circuit protection

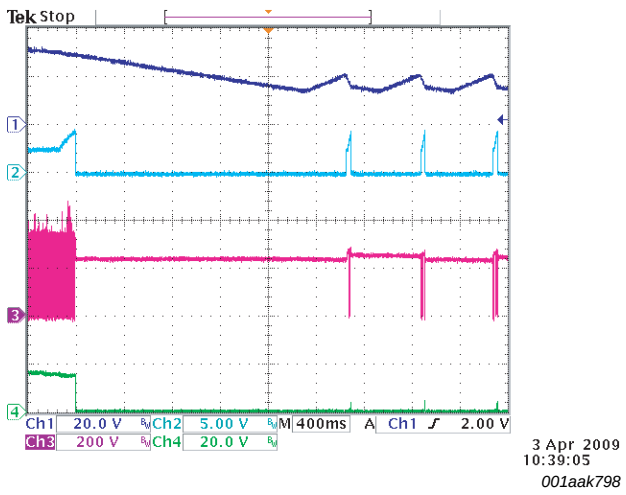
3.3.4 Over-current protection

Test Conditions:

- The load was increased from the maximum value to an estimated over-current value in several steps.
- The test was repeated for different input voltages.

Criteria to pass:

- The output power should be limited and may not exceed 240 W, just before the triggering of the over current protection.
- The average input power shall be less than 3 W once the over current protection has been triggered.



Mains input 90 V / 60 Hz; Io_OCP 8.72 A; input power 1.26 W

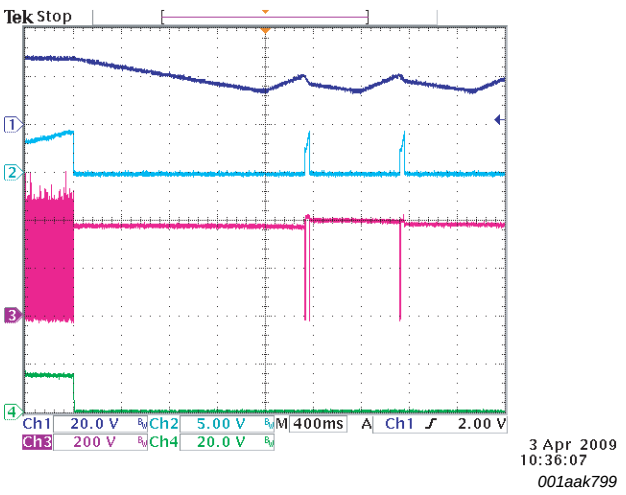
Load before short-circuit = 0 A

CH1: VCC pin TEA1751T

CH2: FBCTRL pin TEA1751T

CH3: Vdrn flyback Mosfet

CH4: Vout



Mains input 264 V / 50 Hz; Io_OCP 9.02 A; input power 1.14 W

Load before short-circuit = 0 A

CH1: VCC pin TEA1751T

CH2: FBCTRL pin TEA1751T

CH3: Vdrn flyback Mosfet

CH4: Vout

Fig 10. Output over current protection

3.3.5 Output Over-Voltage Protection (OVP)

Test Conditions:

- An output overvoltage was created by applying a short circuit across the opto LED of U2.
- An AC input voltage was selected so that the worst-case condition occurred.
- There was no load on the output.

Criteria to pass:

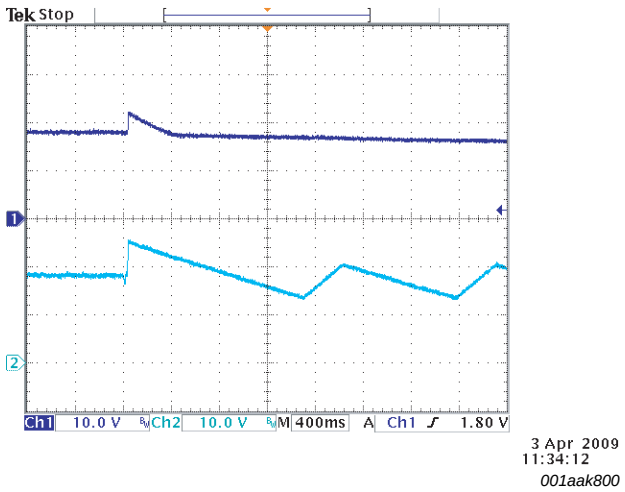
- The output voltage may not exceed 25 V or stabilize between 25 V and the rated voltage.

- At the moment OVP occurs, the primary side controller should shut down and stay in a latched mode.
- A single point fault should not cause a sustained over-voltage condition at the output.

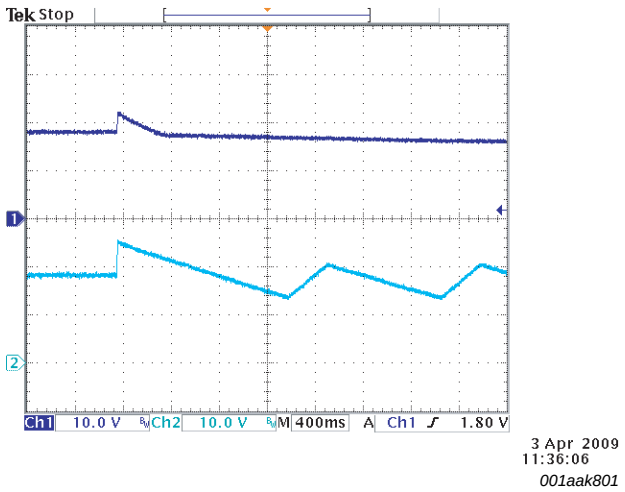
Table 5. Output over-voltage protection

Output over-voltage at no-load as a function of the mains input voltage with protection mode latched

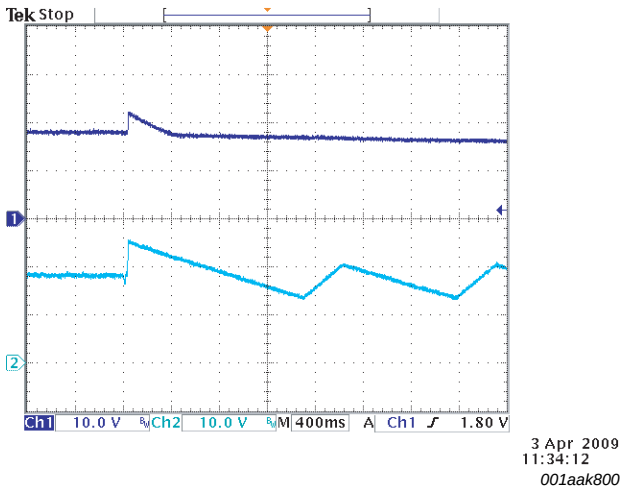
Input voltage (V / Hz)	90 / 60	132 / 60	180 / 50	264 / 50
OVP trip point (V)	22.0	22.4	22.6	22.5



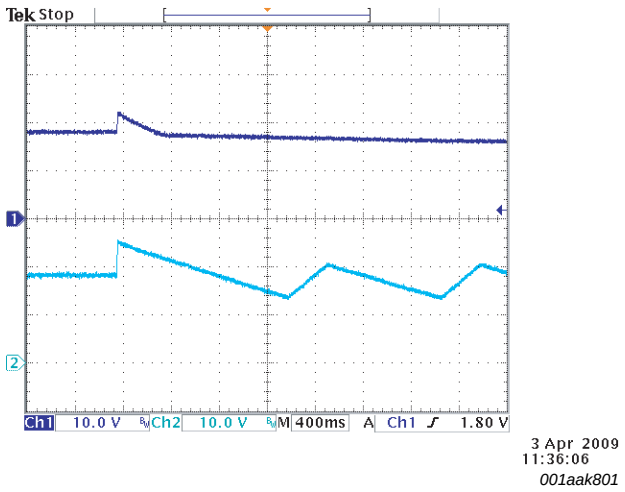
a. **Mains input 90 V / 60 Hz**



b. **Mains input 132 V / 60 Hz**



c. **Mains input 180 V / 50 Hz**



d. **Mains input 264 V / 50 Hz**

CH1: Vout

CH2: VCC pin TEA1751T

Fig 11. Output over-voltage protection

3.3.6 Over-temperature protection

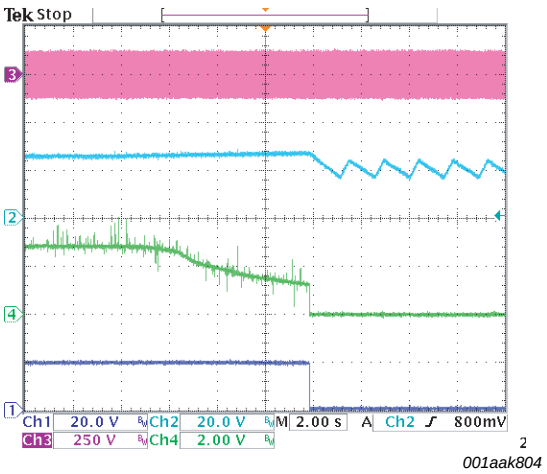
An accurate external over temperature protection (TEA1751T LATCH pin, RT2, R26 and C19) is provided in the demo board to protect the flyback transformer against overheating. Normally, the flyback transformer is the most heat sensitive component.

Test Conditions:

- The NTC temperature sensor, glued to the transformer, was heated using a heat gun.

Criteria to pass:

- The IC should latch off the output at a VLATCH trip level of 1.25V. No output bounce or hiccup is allowed.



OTP trigger temperature 108 ×C

Load before short-circuit = 0 A

CH1: Vout

CH2: TEA1751T VCC pin

CH3: Mains input voltage

CH4: TEA1751T LATCH pin

Fig 12. External Over Temperature Protection (OTP)

3.3.7 Fast latch reset

A fast latch reset function (FLR) is implemented to enable latched protection to be reset without discharging the bulk electrolytic capacitor. The latch protection will be reset as soon as the voltage on VINSENSE pin drops below 0.75 V and then raised to 0.87 V.

Test conditions:

- No load at the output.

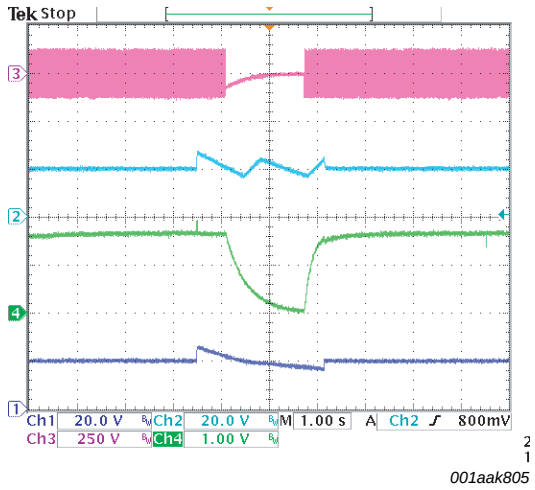
The test sequence was as follows:

1. The latch protection was triggered by an OVP caused by a short-circuit across the opto LED.
2. The mains input was switched off and the voltage at VINSENSE dropped below 0.75 V.
3. The mains input was reinstated and, as soon as the voltage at VINSENSE rose above 0.87 V, the latch reset

Remark: Both live and neutral must be switched.

Criteria to pass:

- The latch should be reset within 3 seconds after switching off, and subsequently switching on, the mains input voltage.



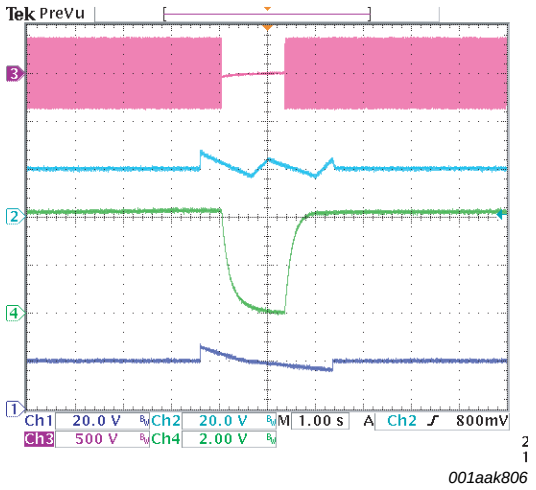
Mains input 90 V / 60 Hz; FLR = 1.6 s

CH1: Vout

CH2: VCC pin TEA1751T

CH3: AC mains input

CH4: VINSENSE pin TEA1751T



Mains input 264 V / 50 Hz; IFLR = 1.3 s

CH1: Vout

CH2: VCC pin TEA1751T

CH3: AC mains input

CH4: VINSENSE pin TEA1751T

Fig 13. Fast Latch Reset (FLR)

3.4 Output regulation and characterization

3.4.1 Load regulation

Test conditions:

- The output voltage deviation was measured while the load current on the output was increased from 0 A to 4.62 A.
- The measurement was repeated for different mains input voltages.

Remark: The output voltage was measured at the end of the output cable.

Criteria to pass:

- The output load regulation must remain within 2 %.

The load regulation was calculated using the following equation:

$$\frac{V_{OUTmax} - V_{OUTmin}}{V_{OUTnom}} \times 100\ \% \quad (1)$$

where V_{OUTnom} = 19.5 V.

Table 6. Load regulation

Output voltage as a function of the output load and the mains input voltage

Input voltage V / Hz	90 / 60	90 / 60	264 / 50	264 / 50
V_{OUT} / I_{OUT} (V/A)	19.404 / 0	19.147 / 4.62	19.403 / 0	19.143 / 4.62

Load regulation at 90 V / 60 Hz is calculated as follows:

$$\frac{19.404\ V - 19.147\ V}{19.5\ V} \times 100\ \% = 1.32\ \% \quad (2)$$

Load regulation at 264 V / 50 Hz is calculated as follows:

$$\frac{19.403\ V - 19.143\ V}{19.5\ V} \times 100\ \% = 1.33\ \% \quad (3)$$

3.4.2 Line regulation

Test conditions:

- The output voltage deviation was measured while the mains voltage on the input was increased from 90 V AC to 264 V AC.
- The measurement was repeated for different mains input voltages.

Remark: The output voltage was measured at the end of the output cable. The load current was 4.62 A.

The line regulation was calculated using the following equation:

$$\frac{V_{OUTmax} - V_{OUTmin}}{V_{OUTnom}} \times 100\ \% \quad (4)$$

where V_{OUTnom} = 19.5 V.

Criteria to pass:

- The output voltage deviation must remain within 0.05 %.

Table 7. Line regulation

Output voltage (at full load) as a function of the mains input voltage

Input voltage V / Hz	90 / 60	115 / 60	132 / 60	180 / 50	230 / 50	264 / 50
V_{OUT} (V)	19.147	19.147	19.147	19.143	19.143	19.143

Load regulation at 90 V / 60 Hz was calculated using the following equation:

$$\frac{19.147\ V - 19.143\ V}{19.5\ V} \times 100\ \% = 0.02\ \% \quad (5)$$

3.4.3 Ripple and noise PARD. (Periodic And Random Deviation)

Ripple and noise are defined as the periodic or random signals over a frequency band of 10 Hz to 20 MHz.

Test Conditions:

- The measurement was made with an oscilloscope having a 20 MHz bandwidth.
- The output was shunted at the end of the output cable, by a 0.1 μF ceramic disk capacitor and a 22 μF electrolytic capacitor, to simulate loading.

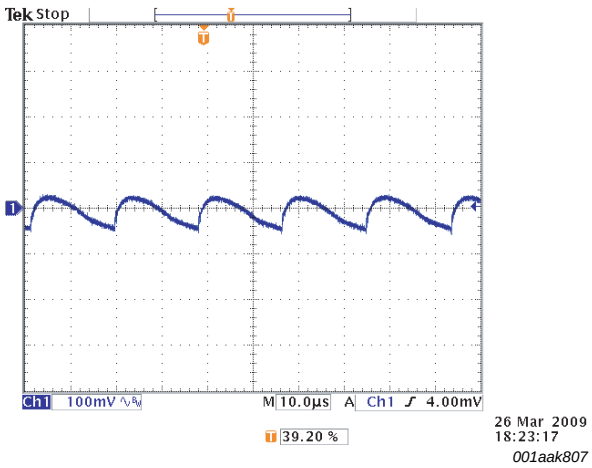
Criteria to pass:

- The P.A.R.D. of the output must remain within the specified limits (100 mV_{p-p}) at a maximum load current of 4.62 A.

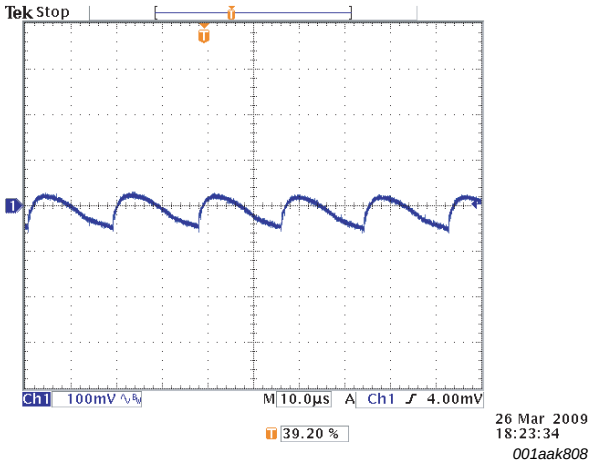
Table 8. Ripple and noise P.A.R.D.

Ripple and noise (at maximum load) as a function of the mains input voltage

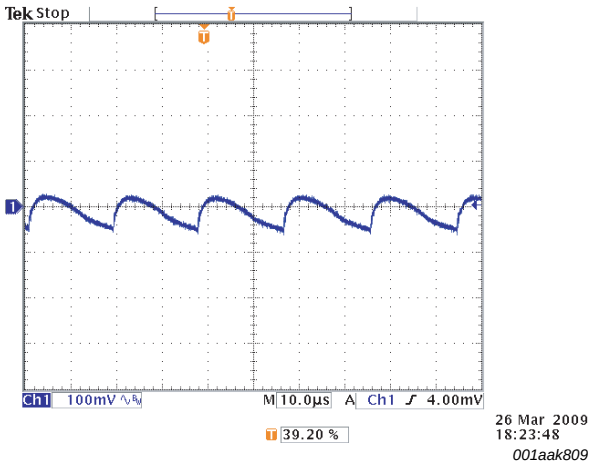
Input voltage V / Hz	90 / 60	115 / 60	132 / 60	180 / 50	230 / 50	264 / 50
PARD (mV)	84	88	83	62	60	60



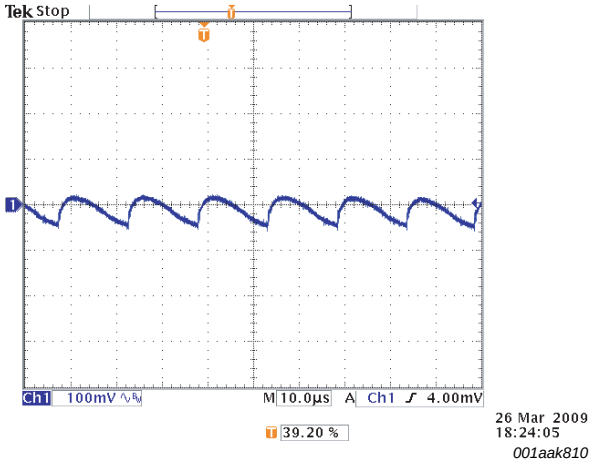
a. **Mains input 90 V / 60 Hz (Ch1 = V_{OUT})**



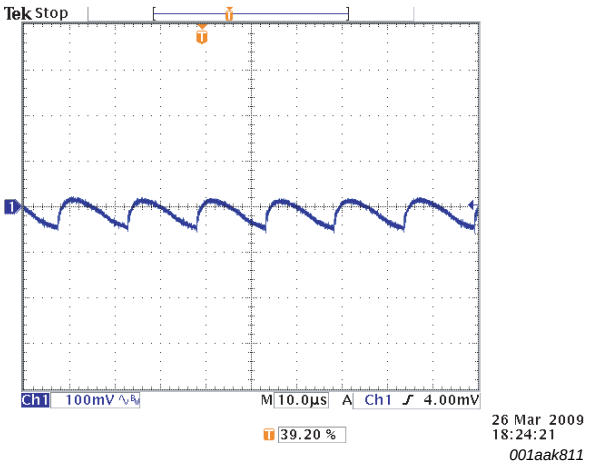
b. **Mains input 115 V / 60 Hz (Ch1 = V_{OUT})**



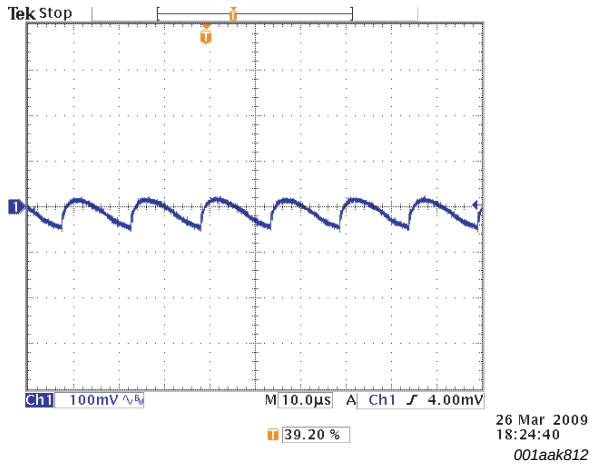
c. **Mains input 132 V / 60 Hz (Ch1 = V_{OUT})**



d. **Mains input 180 V / 50 Hz (Ch1 = V_{OUT})**



e. **Mains input 230 V / 50 Hz (Ch1 = V_{OUT})**



f. **Mains input 264 V / 50 Hz (Ch1 = V_{OUT})**

Fig 14. Ripple and noise

3.4.4 Dynamic load response

Test Conditions:

- The unit was subjected to a load change from 0 % to 100 % at a slew rate of 1 A / msec.
- The frequency of change was set to give the best readability of the deviation and setting time.

Remark: The voltage was measured at the end of the output cable.

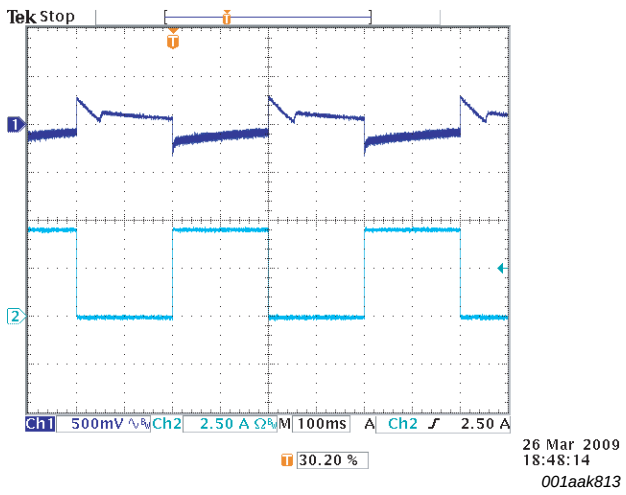
Criteria to pass:

- The output is not allowed to have an overshoot or undershoot beyond the specified limits (+1 V to −0.5 V) after a load change.

Table 9. Dynamic load response

Deviation of the output voltage at a load step from 4.62 A to 0 A and from 0 A to 4.62 A

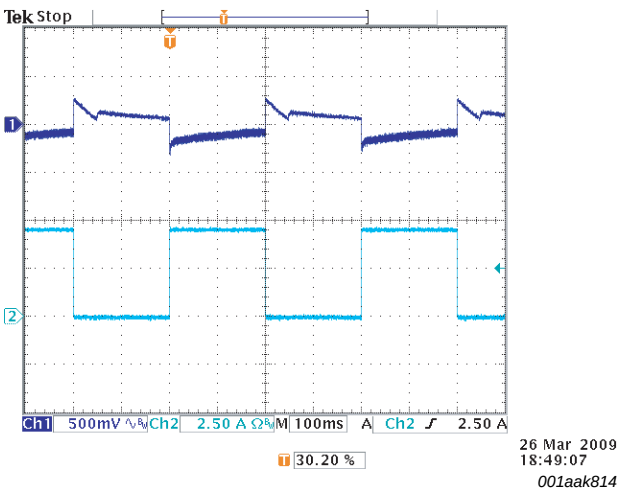
Input voltage V / Hz	90 / 60	264 / 50
Deviation (mV)	600	580



Mains input 90 V / 60 Hz

CH1: Vout

CH2: Iout



Mains input 264 V / 50 Hz

CH1: Vout

CH2: Iout

Fig 15. Dynamic load response

4. ElectroMagnetic Compatibility (EMC)

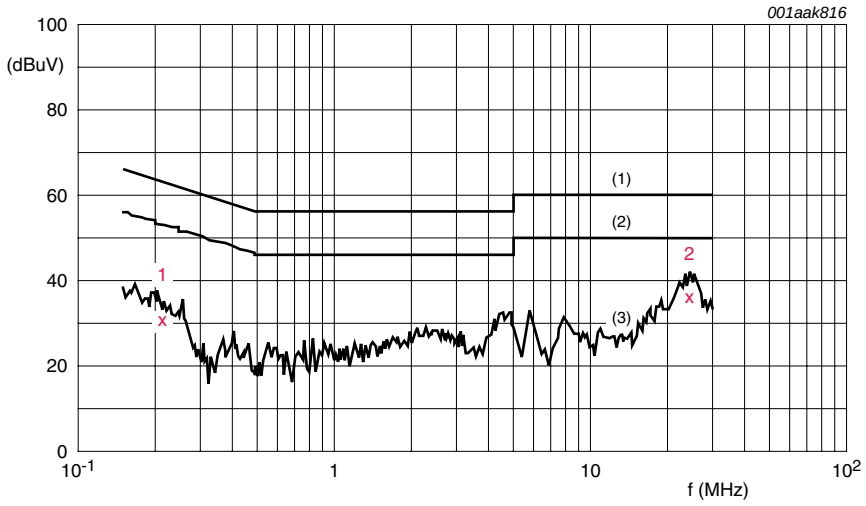
4.1 Conducted emission

Test Conditions:

- The unit was subjected to maximum load.
- The ground connection of the output cable was connected to EMC ground.

Criteria to pass:

- CISPR22 Class B with –10 dB production margin.



(1) QP limit
(2) AV limit
(3) Peak reading

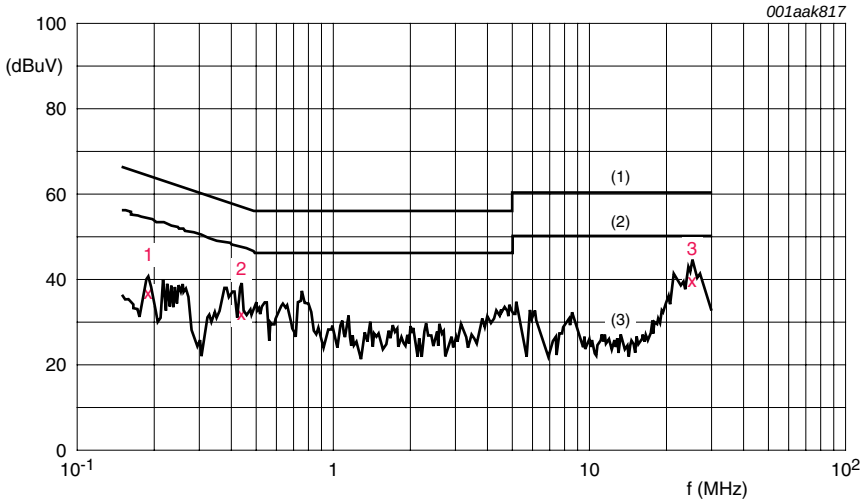
The conducted EMI measurement of 110 V neutral is close to 110 V line

Fig 16. Conducted EMI 110 V line

Table 10. Conducted EMI measurements 110 V line

Refer to Figure 16 points 1 and 2 on the peak reading graph.

	Frequency	Correction factor	Reading dBuV		Emission dBuV		Limit dBuV		Margins dB	
No.	MHz	dB	QP	AV	QP	AV	QP	AV	QP	AV
1	0.20112	0.12	32.67	27.68	32.79	27.80	63.56	53.56	–30.77	–25.76
2	24.36328	1.50	35.94	30.50	37.44	32.00	60.00	50.00	–22.56	–18.00



(1) QP limit
(2) AV limit
(3) Peak reading

The conducted EMI measurement of 230 V neutral is close to 230 V line

Fig 17. Conducted EMI 230 V line

Table 11. Conducted EMI measurements 230 V line

Refer to Figure 17 points 1, 2 and 3 on the peak reading graph.

	Frequency	Correction factor	Reading dBuV		Emission dBuV		Limit dBuV		Margins dB	
No.	MHz	dB	QP	AV	QP	AV	QP	AV	QP	AV
1	0.18906	0.09	38.38	37.05	38.47	37.14	64.508	54.08	−25.01	−16.94
2	0.43516	0.20	32.37	24.52	32.57	24.72	5715	47.15	−24.58	−22.43
3	25.11328	1.14	38.45	32.14	39.59	33.28	60.00	50.00	−20.41	−16.72

4.2 Immunity against lighting surges

Test conditions:

- Combination wave: 1.2/50 μs open circuit voltage and 8/20 μs short circuit current.
- Test voltage: 2 kV.
- L1-L2: 2 ohm; L1-PE, L2-PE & L1+L2-PE: 12 ohm.
- Phase angle: 0, 90, 180 and 270 degrees.
- Number of tests: 5 positive and 5 negative.
- Pulse repetition rate: 20 s.

Test result:

There was no disruption of functionality.

4.3 Immunity against ESD

Test conditions:

- ESD air discharge at the ground terminal of the output cable connector.

Criteria to pass:

- IEC61000-4-2 air discharge level 3 (8 kV) and level 4 (15 kV).

Table 12. Immunity against ESD

Performance of the adapter at an ESD air discharge

ESD performance	No disruption of function	Auto recovery
Demo board according to schematic	± 12 kV	± 15 kV
Demo board with 6 x 10 M across Y-cap	± 16.5 kV	-

4.4 Mains harmonic reduction

Test conditions:

- The unit was set to maximum load.
- The input voltage was 230 V / 50 Hz.

Criteria to pass:

- Compliance with EN61000-3-2 A14 class D.

Test result:

Passed, see Figure 18 and Figure 19.

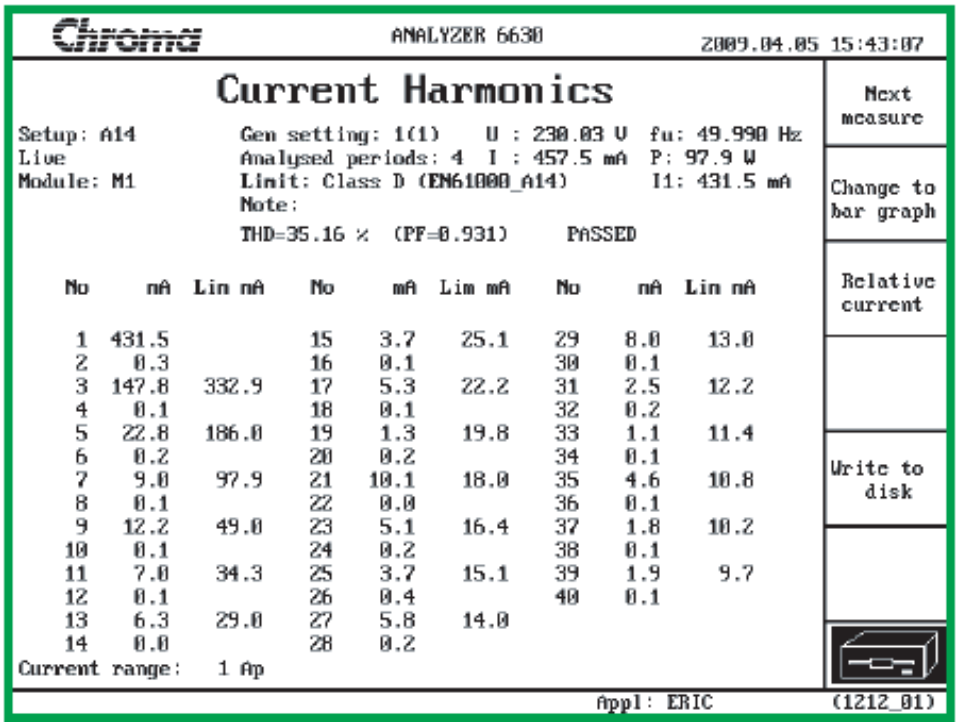


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Fig 18. Mains harmonic currents; absolute values

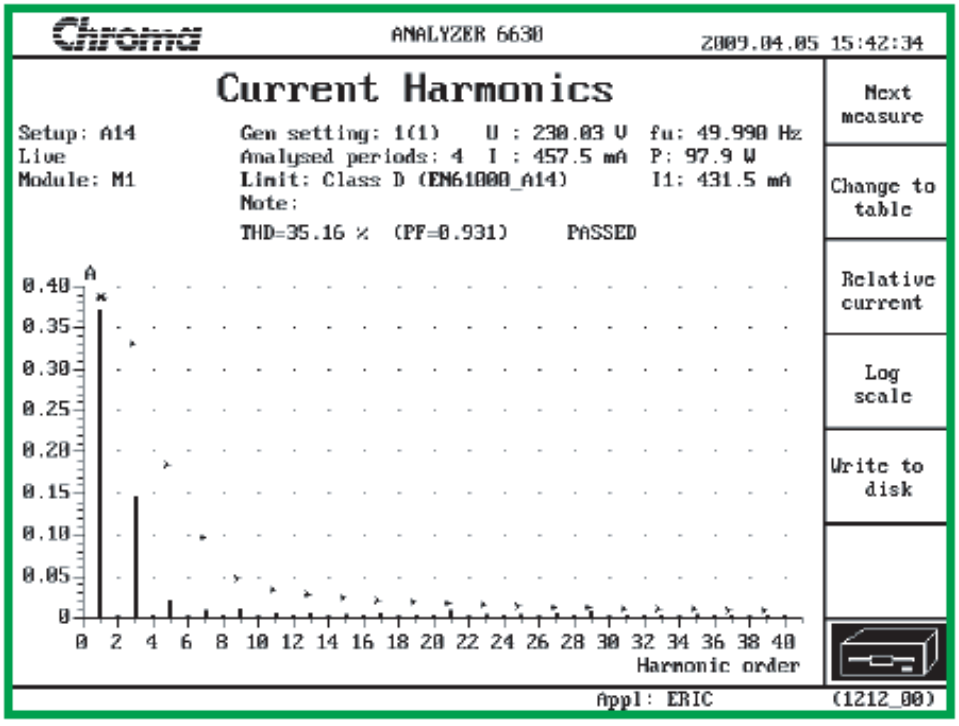

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Fig 19. Mains harmonic currents; graphic representation

5. Schematic diagram

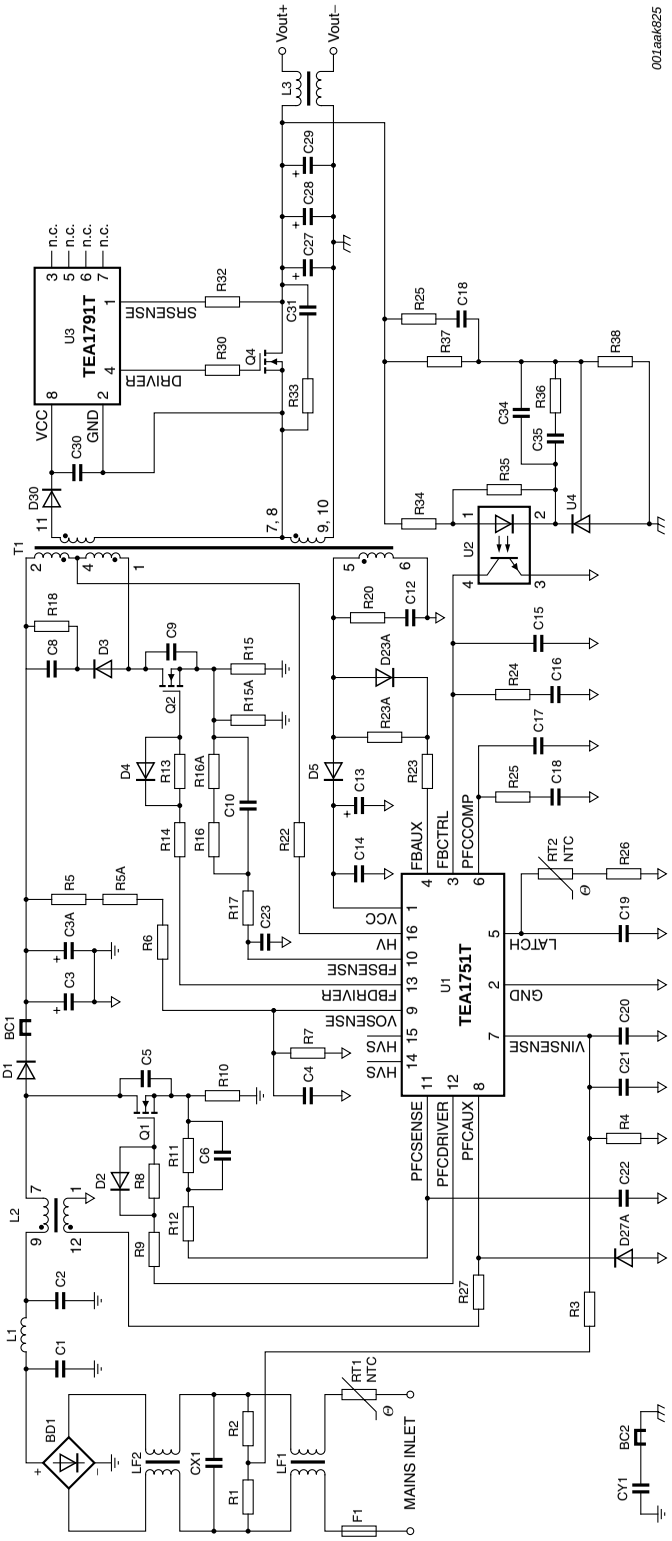

Fig 20. Schematic of 90 W TEA1751T and TEA1791T adapter solution

6. Bill of materials

Table 13. Default bill of materials for a 90 W TEA1751T and TEA1791T adapter solution

Reference	Component	Package	Remark
R1	2 MΩ, 1 %	1206	
R2	2 MΩ, 1 %	1206	
R3	560 kΩ, 1 %	1206	
R4	47 kΩ, 1 %	0603	
R5	3.3 MΩ, 1 %	1206	
R5A	3.3 MΩ, 1 %	1206	
R6	2.7 MΩ, 1 %	1206	
R7	60.4 kΩ, 1 %	0603	
R8	10 Ω, 5 %	0805	
R9	10 Ω, 5 %	0805	
R10	0.1 Ω, 5 %, 1 W	Axial	metal oxide film
R11	15 kΩ, 5 %	0603	
R12	1 kΩ, 5 %	0805	
R13	10 Ω, 5 %	0805	
R14	10 Ω, 5 %	0805	
R15	0.1 Ω, 5 %, 1 W	Axial	metal oxide film
R15A	0.3 Ω, 1 %	RL1632	
R16	27 kΩ, 5 %	0603	
R16A	750 Ω, 5 %	0603	
R17	1 kΩ, 5 %	0603	
R18	43 kΩ, 5 %	1206	
R19	43 kΩ, 5 %	1206	
R20	47 Ω, 5 %	0805	
R21	0 Ω	0805	
R22	10 kΩ, 5 %	0805	
R23	82 kΩ, 1 %	0603	
R23A	47 kΩ, 1 %	0603	
R24	39 kΩ, 5 %	0603	
R25	39 kΩ, 5 %	0603	
R26	10 kΩ, 5 %	0603	
R27	5.1 kΩ, 5 %	1206	
R30	10 Ω, 5 %	0805	
R32	1 kΩ, 5 %	0805	
R33	Not Mounted		
R34	1 kΩ, 5 %	0603	
R35	2.7 kΩ, 5 %	0603	
R36	10 kΩ, 5 %	0603	
R37	35.7 kΩ, 1 %	0603	
R38	5.23 kΩ, 1 %	0603	

Table 13. Default bill of materials for a 90 W TEA1751T and TEA1791T adapter solution *…continued*

Reference	Component	Package	Remark
R39	not mounted		
RT1	Jumper		
RT2	NTC 100 kΩ, D = 5 mm	Radial lead	TTC050104
C1	Film capacitor 0.47 μF / 450 V, 10 %		
C2	Film capacitor 0.47 μF / 450V, 10 %		
C3	Electrolytic capacitor 100 μF / 400V, 105 °C	Radial 16x30 mm	
C3A	10 nF / 1 kV, Z5U	Disk 11.5 mm	
C4	10 nF / 25 V, X7R	0603	
C5	220 pF / 630 V, NP0	1206	
C6	0.1 μF / 25 V, X7R	0603	
C8	3300 pF / 630 V	1206	
C9	100 pF / 630 V, NP0	1206	
C10	0.1 μF / 25 V, X7R	0805	
C12	220 pF / 100 V, NP0	0805	
C13	Electrolytic capacitor 47 μF / 35V, 105 °C	Radial 5 x 11 mm	low impedance type
C14	1 μF / 50 V, Y5V	0805	
C15	10 nF / 25 V, X7R	0603	
C16	0.33 μF / 10 V, X7R	0603	timing capacitor; review tolerance
C17	0.33 μF / 10 V, X7R	0603	
C18	0.47 μF / 10 V, X7R	0603	
C19	10 nF / 25 V, X7R	0603	
C20	2.2 μF / 10 V, Y5V	0603	
C21	2.2 μF / 10 V, Y5V	0603	
C22	220 pF / 50 V, NP0	0603	10 V is permitted
C23	220 pF / 50 V, NP0	0603	10 V is permitted
C27	Electrolytic capacitor 470 μF / 25V, 105 °C	Radial 10 x 12.5 mm	low impedance type
C28	Electrolytic capacitor 470 μF / 25V, 105 °C	Radial 10 x 12.5 mm	low impedance type
C29	Electrolytic capacitor 470 μF / 25V, 105 °C	Radial 10 x 12.5 mm	low impedance type
C30	1 μF / 50 V, Y5V	0805	
C31	Not mounted		
C34	0.1 μF / 25 V, X7R	0603	
C35	10 nF / 25 V, X7R	0603	
C36	Not mounted		
CX1	0.33 μF / 275 V AC, X2	MKP	
CY1	1000 pF / 400 V AC, Y1	Pitch 10 mm	

Table 13. Default bill of materials for a 90 W TEA1751T and TEA1791T adapter solution *…continued*

Reference	Component	Package	Remark
BD1	GBU806, 8 A / 600 V	Flat / mini	
D1	MUR460, 4 A / 600 V	DO-201AD	Vishay
D2	1N4148W	SOD-123	
D3	S2M	SMB	
D4	1N4148W	SOD-123	
D5	BAS21	SOT23	NXP, BAS20 is permitted
D23A	BAS21	SOT23	NXP, BAS20 is permitted
D27A	1N4148W	SOD-123	
D30	BAS21	SOT23	NXP
Q1	2SK3568	TO220F	
Q2	2SK3569	TO220F	
Q4	PSMN015-100P	TO220	NXP
U1	TEA1751T	SO16	NXP, GreenChip III PFC + flyback controller
U2	LTV817B	DIP4-W	CTR 130-260, spacing 10.16 mm
U3	TEA1791T	SO8	NXP, GreenChip-SR controller
U4	AP431SR	SOT-23R	diodes
T1	Flyback transformer 450 μH	PQ3220	see specification
L1	Inductor 210 μH	T50-52	
L2	PFC inductor 250 μH	RM10	see specification
L3	Inductor CM 200 μH	T12*6*4	
LF1	Inductor CM 500 μH	T12*6*4	
LF2	Inductor CM 12.8 MH	T16*12*18	
BC1	Bead core R5B/XP N4/AMAX	RH 4*6*2	placed at cathode of D1
BC2	Bead core S6H/JK N6/AMAX	RH 3.5*4.2*1.3	placed at lead of CY1
F1	Fuse T3, 15 A / 250 V	LT5	

7. Transformer and inductor specifications

7.1 Flyback transformer T1 specifications

- Primary inductance: 450 μH (±±5 %).
- Leakage inductance: 6 μH (max).
- Core / Bobbin: PQ3220.
- Core material: PC44.
- HI-POT prim - sec: 3 kV / 5 mA, 3 sec.

Manufacturer: Send Power Electronics. Co., LTD, Taiwan ROC.

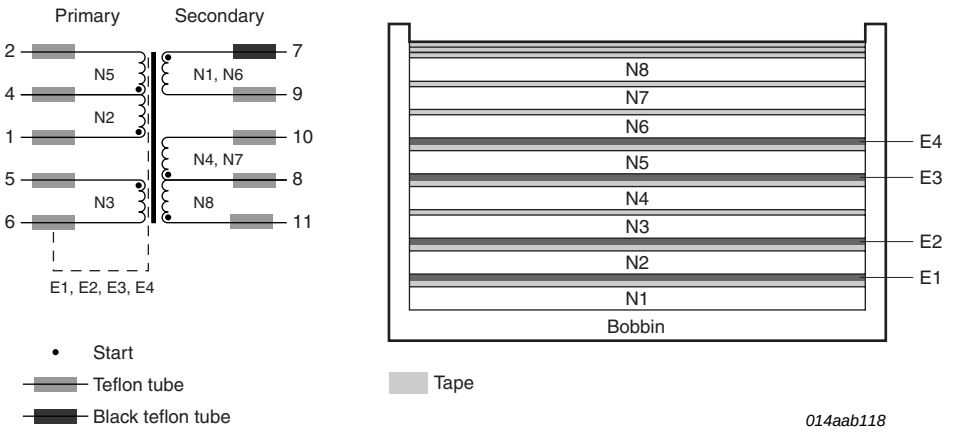

Fig 21. Flyback transformer schematic

Table 14. Flyback transformer winding details

Winding order		Pin number		Wire type	Number of wires	Number of turns		Remarks
		Start	Finish			Winding	MYLAR tape	
1:	N1	7	9	TEX-E (3L) 0.3 mm ∅	2	6	1	
2:	E1		6	Copper foil 0.025 mm x 7 mm		1	1	finished with wire 0.3 ∅
3:	N2	1	4	2-UEW 0.5 mm ∅	1	16	1	
4:	E2		6	Copper foil 0.025 mm x 7 mm		1	1	finished with wire 0.3 ∅
5:	N3	5	6	2-UEW 0.25 mm ∅	2	7	1	
6:	N4	8	10	TEX-E (3L) 0.3 mm ∅	2	6	1	
7:	E3		6	Copper foil 0.025 mm x 7 mm		1	1	finished with wire 0.3 ∅
8:	N5	4	2	2-UEW 0.5 mm ∅	1	16	1	
9:	E4		6	Copper foil 0.025 mm x 7 mm		1	1	finished with wire 0.3 ∅
10:	N6	7	9	TEX-E (3L) 0.3 mm ∅	2	6	1	
11:	N7	8	10	TEX-E (3L) 0.3 mm ∅	2	6	1	
12:	N8	11	8	TEX-E (3L) 0.3 mm ∅	1	5	3	close winding method

7.2 PFC inductor L2 specifications

7.2.1 Inductor L2 specifications

- Primary inductance: 250 μH (±10 %).
- Core / Bobbin: RM10.
- Core material: NC-2H.

Manufacturer: Send Power Electronics. Co., LTD, Taiwan ROC.

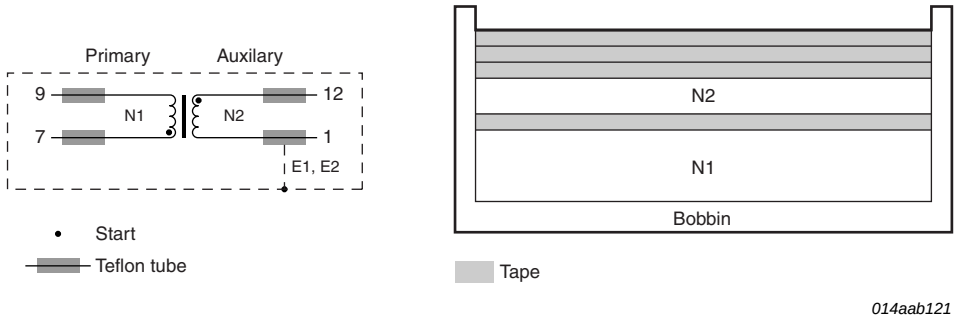

Fig 22. PFC inductor L2 schematic

Table 15. PFC inductor L2 winding details

Layer order		Pin number		Wire type	Number of wires	Number of turns		Remarks
		Start	Finish			Winding	MYLAR tape	
1:	N1	9	7	USTC 30 x 0.1 mm ∅	1	40	1	
2:	N2	12	1	2-UEW 0.22 mm ∅	2	2.5	3	

8. PCB layout

The SMPS printed circuit board is a single sided board. Dimensions are 125 mm x 59 mm.

The PCBs are produced on 1.6 mm FR2 with single sided 2 Oz. copper (70 μm).

The Gerber File set for production of the PCB is available through the local NXP sales office.

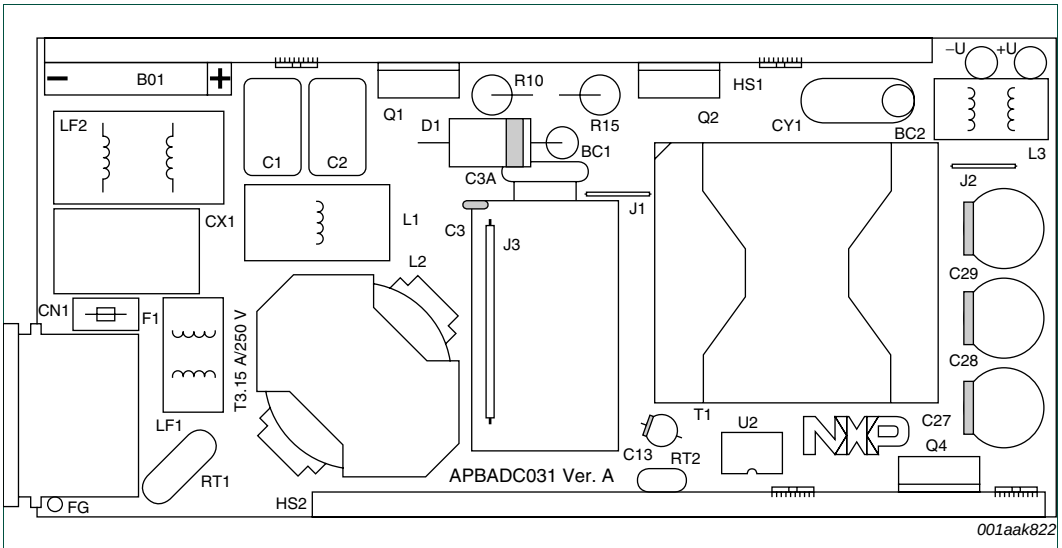

Fig 23. Demo board top silk (top view)

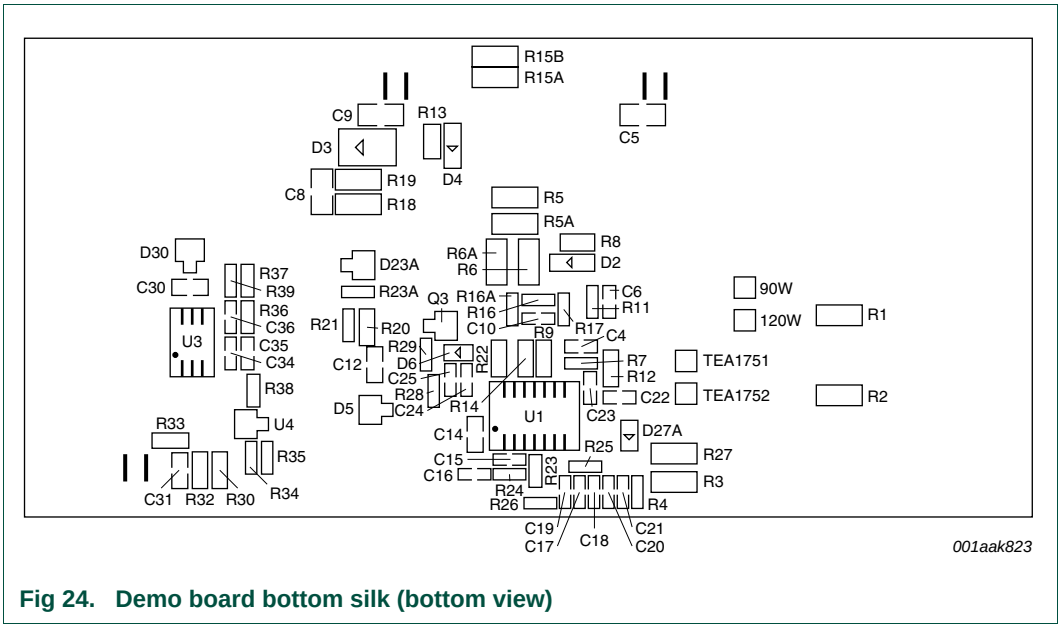

Fig 24. Demo board bottom silk (bottom view)

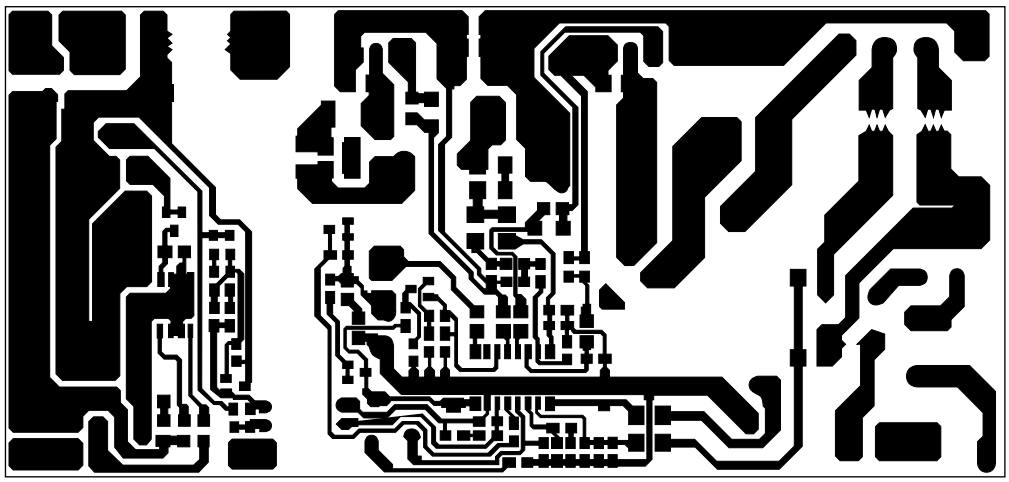

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Fig 25. Demo board bottom copper (bottom view)

9. Abbreviations

Table 16. Abbreviations table

Acronym	Description
CC	Constant Current
CR	Constant Resistance
CV	Constant Voltage
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	ElectroMagnetic Susceptibility
ESD	ElectroStatic discharge
FLR	Fast Latch Reset
LISN	Line Impedance Standardization Network
MHR	Mains Harmonic Reduction
OTP	Over Temperature Protection
OCP	Over Current Protection
OVP	Over Voltage Protection
PCB	Printed Circuit Board
PE	Protective Earth
PFC	Power Factor Correction
SCP	Short Circuit Protection
SMPS	Switched Mode Power Supply
SR	Synchronous Rectification
TIW	Triple Insulated Wire
UEW	PolyUrethane Enameled Wire
USTC	PolyUrethane Silk Tetrone Covered

10. Legal information

10.1 Definitions

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11. Tables

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