NTLUS3A18PZC

Power MOSFET

−20 V, −8.2 A, Single P−Channel, 2.0x2.0x0.55 mm μCool™ UDFN Package

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- Ultra Low $R_{DS(on)}$
- ESD Diode−Protected Gate
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Optimized for Power Management Applications for Portable Products, such as Cell Phones, Media Tablets, PMP, DSC, GPS, and Others
- Battery Switch
- High Side Load Switch

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−8.2	A
		T_A = 85°C		−5.9	
Continuous Drain Current (Note 1)	t ≤ 5 s	T_A = 25°C		−12.2	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.7	W
	t ≤ 5 s	T_A = 25°C		3.8	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	−5.1	A
		T_A = 85°C		−3.7	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.7	W
Pulsed Drain Current		tp = 10 μs	I_{DM}	−25	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	°C
ESD (HBM, JESD22−A114)			V_{ESD}	2000	V
Source Current (Body Diode) (Note 2)			I_S	−1.7	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

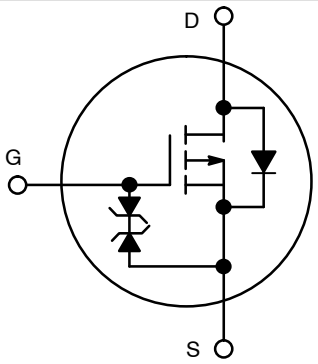
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm^2, 2 oz. Cu.

ON Semiconductor®

http://onsemi.com

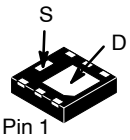
MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−20 V	18 mΩ @ −4.5 V	−8.2 A
	25 mΩ @ −2.5 V	
	50 mΩ @ −1.8 V	
	90 mΩ @ −1.5 V	



P−Channel MOSFET

MARKING DIAGRAM

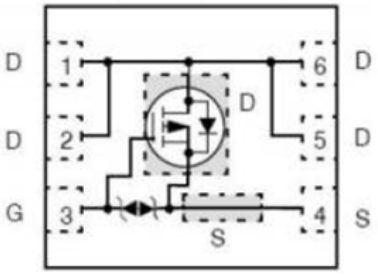


UDFN6
(μCOOL™)
CASE 517BG

AE = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	72	°C/W
Junction-to-Ambient – t ≤ 5 s (Note 3)	$R_{\theta JA}$	33	
Junction-to-Ambient – Steady State min Pad (Note 4)	$R_{\theta JA}$	189	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm^2, 2 oz. Cu.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			+10		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −20 V	T_J = 25°C			−1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5.0 V				±5	μA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−0.4		−1.0	V
Negative Threshold Temp. Coefficient	$V_{GS(TH)}/T_J$				3.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −7.0 A			14.6	18	mΩ
		V_{GS} = −2.5 V, I_D = −5.0 A			19	25	
		V_{GS} = −1.8 V, I_D = −3.0 A			25	50	
		V_{GS} = −1.5 V, I_D = −1.0 A			40	90	
Forward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −3.0 A			40		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = −15 V			2240		pF
Output Capacitance	C_{OSS}				240		
Reverse Transfer Capacitance	C_{RSS}				210		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V; I_D = −4.0 A			28		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.0		
Gate-to-Source Charge	Q_{GS}				2.9		
Gate-to-Drain Charge	Q_{GD}				8.8		
SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 6)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −4.0 A, R_G = 1 Ω			8.6		ns
Rise Time	t_r				15		
Turn-Off Delay Time	$t_{d(OFF)}$				150		
Fall Time	t_f				88		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −1.0 A	T_J = 25°C		0.63	1.0	V
			T_J = 125°C		0.50		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = −1.0 A			26.1		ns
Charge Time	t_a				10.2		
Discharge Time	t_b				15.9		
Reverse Recovery Charge	Q_{RR}				12		nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

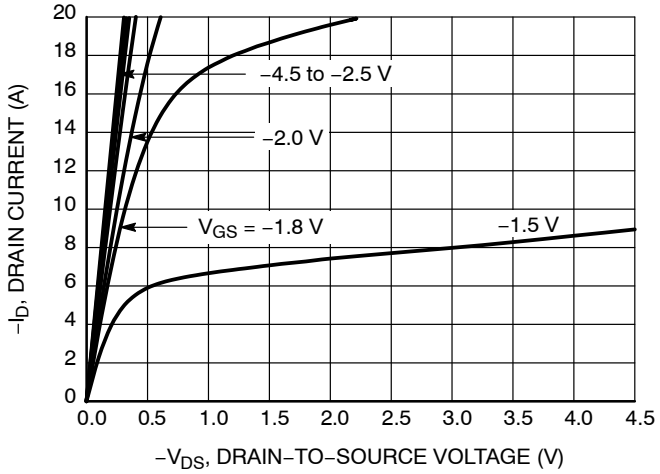


Figure 1. On−Region Characteristics

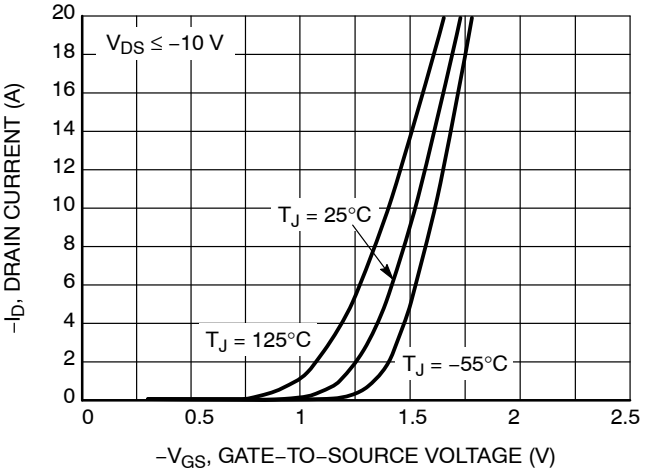


Figure 2. Transfer Characteristics

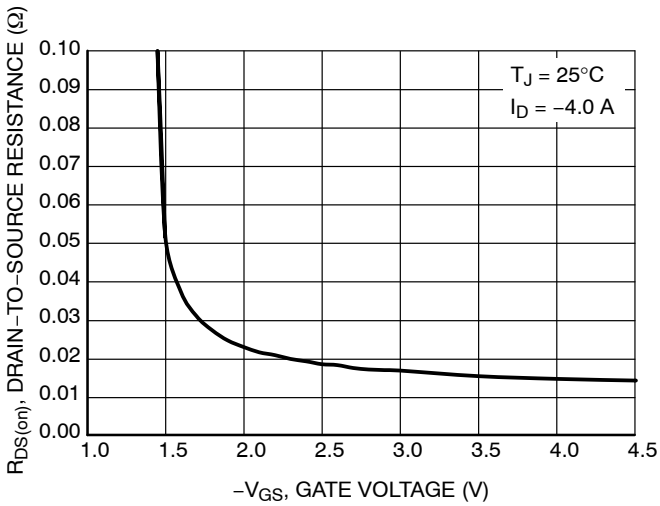


Figure 3. On−Resistance vs. Gate−to−Source Voltage

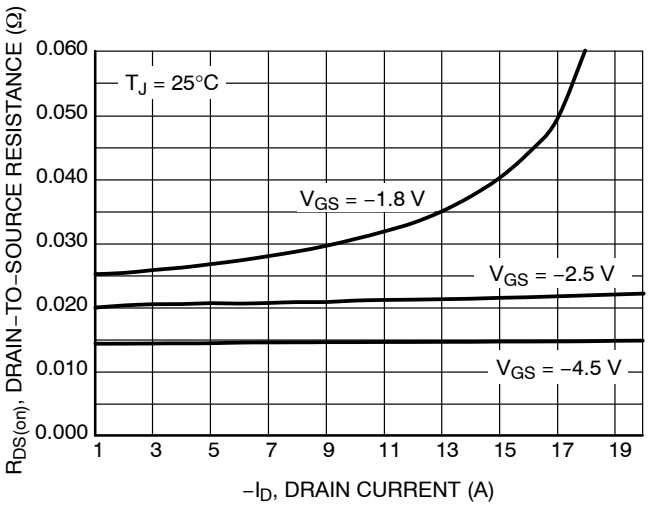


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

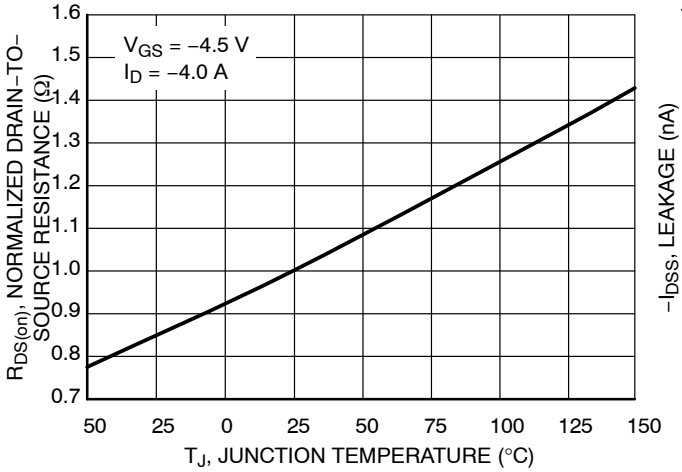


Figure 5. On−Resistance Variation with Temperature

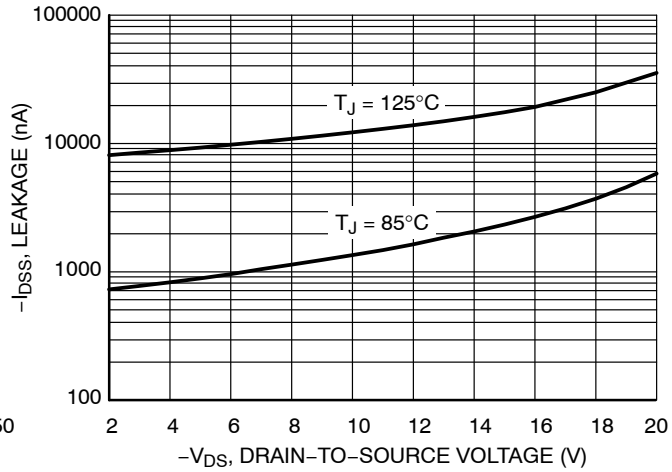


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

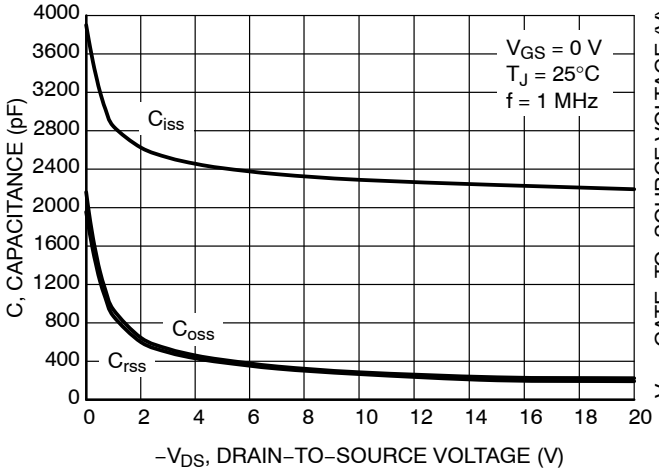


Figure 7. Capacitance Variation

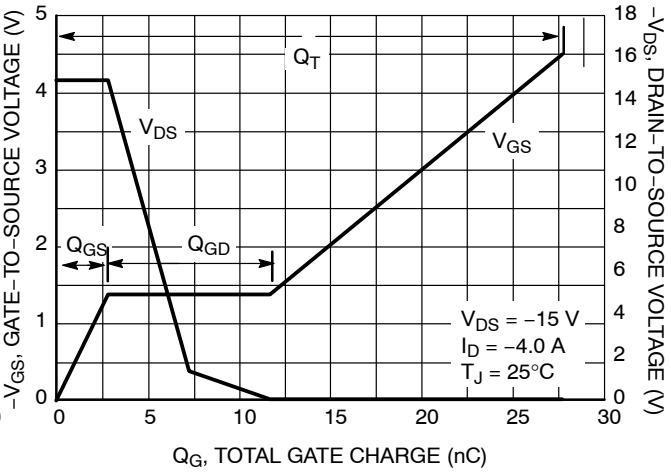


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

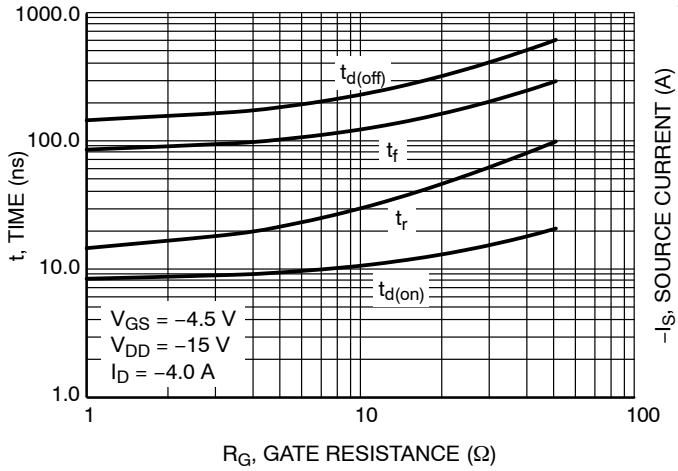


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

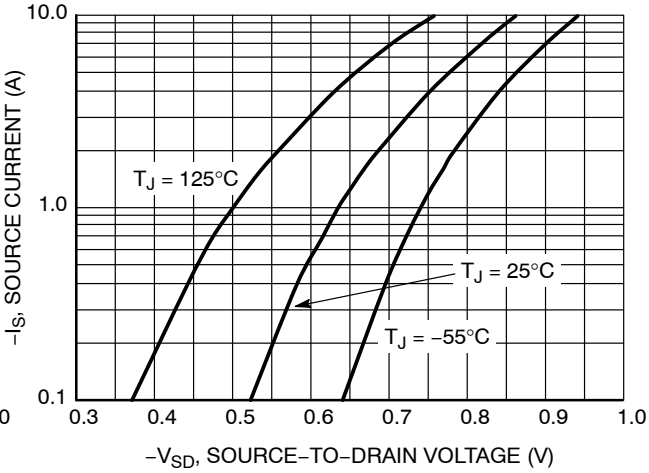


Figure 10. Diode Forward Voltage vs. Current

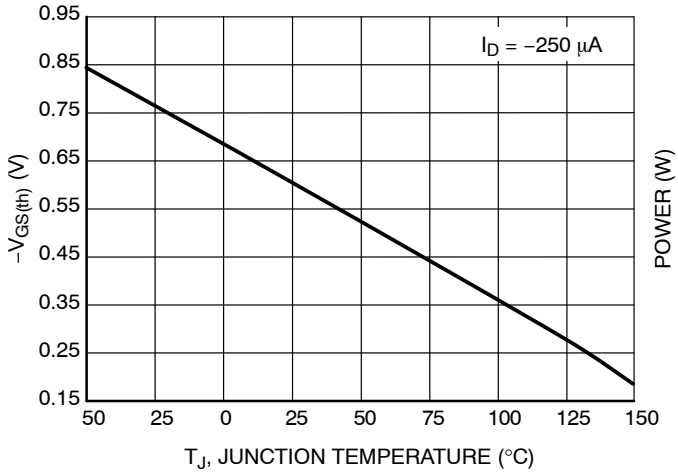


Figure 11. Threshold Voltage

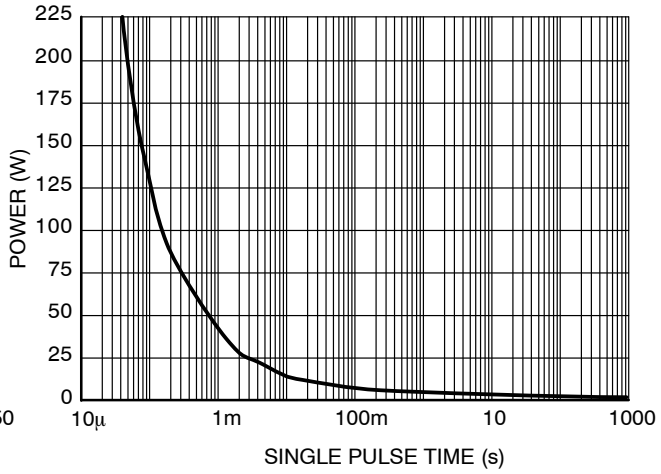


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

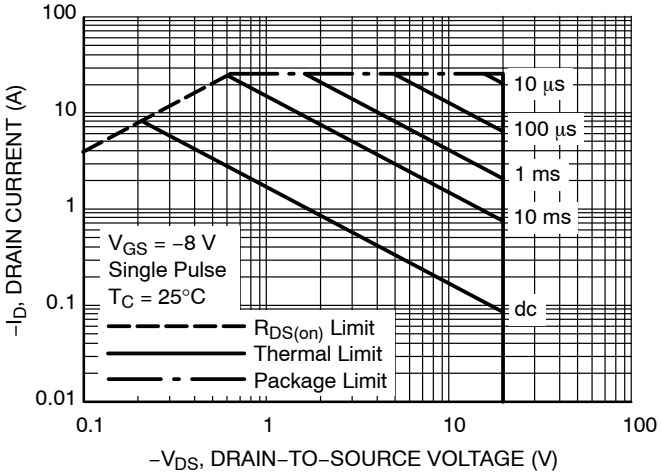


Figure 13. Maximum Rated Forward Biased Safe Operating Area

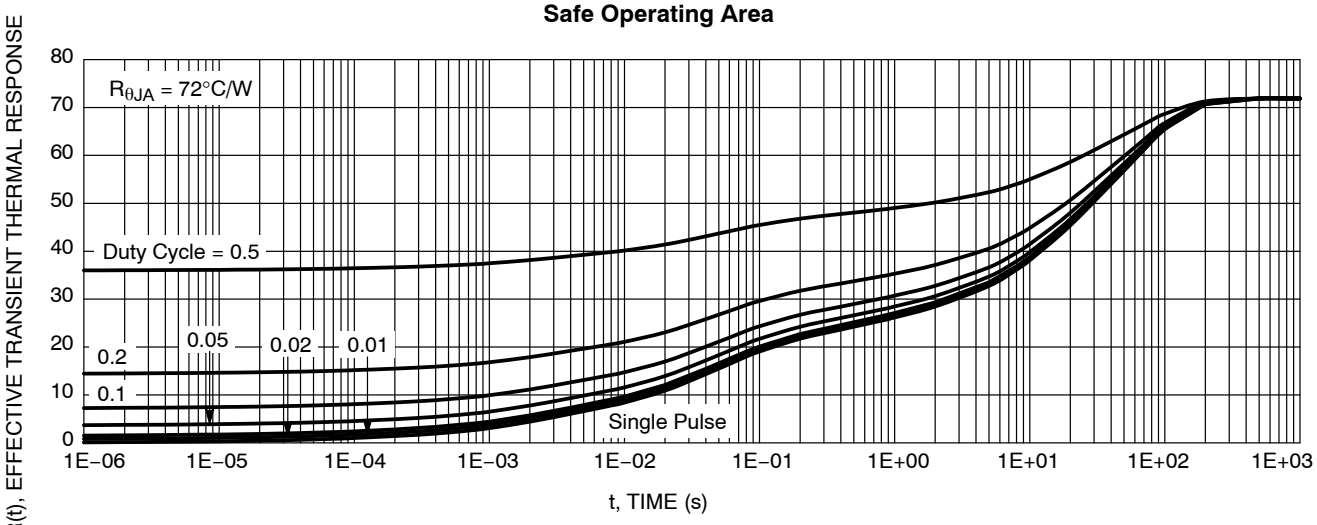


Figure 14. FET Thermal Response

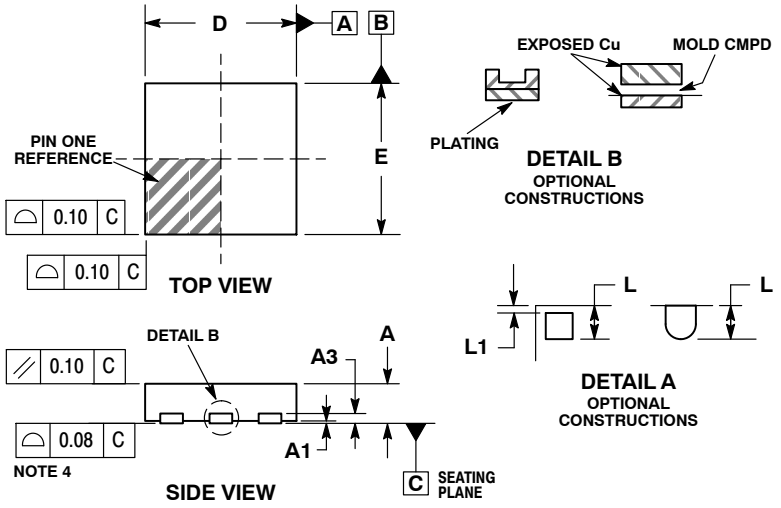
DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLUS3A18PZCTAG	UDFN6 (Pb−Free)	3000 / Tape & Reel
NTLUS3A18PZCTBG	UDFN6 (Pb−Free)	3000 / Tape & Reel
NTLUS3A18PZCTCG	UDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

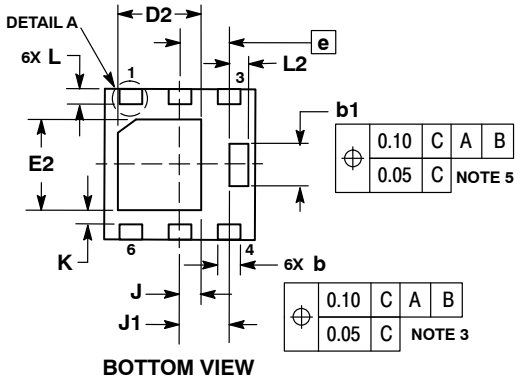
PACKAGE DIMENSIONS

UDFN6 2x2, 0.65P
CASE 517BG
ISSUE A

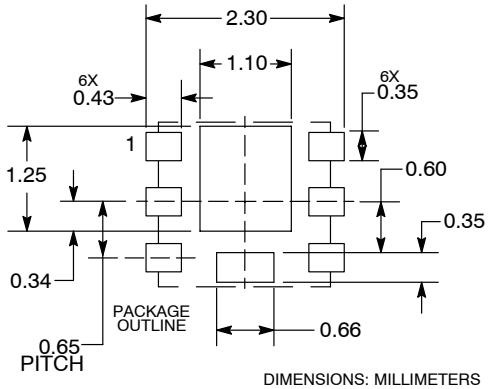


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. CENTER TERMINAL IS CONNECTED TO TERMINAL LEAD # 4.
6. LEADS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
J	0.27 BSC	
J1	0.65 BSC	
L	0.20	0.30
L1	---	0.10
L2	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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