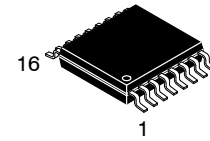


# 3.3 V, Crystal to 25 MHz, 100 MHz, 125 MHz and 200 MHz HCSL Clock Generator

## NB3N3002



TSSOP-16  
DT SUFFIX  
CASE 948F

### Description

The NB3N3002 is a precision, low phase noise clock generator that supports PCI-Express and Ethernet requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal and generates a differential HCSL output at 25 MHz, 100 MHz, 125 MHz or 200 MHz clock frequencies. Outputs can interface with LVDS with proper termination (See Figure 5).

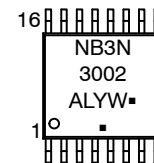
This device is housed in 5.0 mm x 4.4 mm narrow body TSSOP 16 pin package.

### Features

- Uses 25 MHz Fundamental Mode Parallel Resonant Crystal
- External Loop Filter is Not Required
- HCSL Differential Output or LVDS with Proper Termination
- For Selectable Multipliers of the Input Frequency
- Output Enable with Tri-State Outputs
- PCIe Gen1, Gen2, Gen3, Gen4, QPI, UPI Jitter Compliant
- Typical TIE RMS jitter of 2.5 ps
- Phase Noise: @ 100 MHz
 

| Offset  | Noise Power |
|---------|-------------|
| 100 Hz  | -109.4 dBc  |
| 1 kHz   | -127.8 dBc  |
| 10 kHz  | -136.2 dBc  |
| 100 kHz | -138.8 dBc  |
| 1 MHz   | -138.2 dBc  |
| 10 MHz  | -161.4 dBc  |
| 20 MHz  | -163.00 dBc |
- Operating Range 3.3 V  $\pm 5\%$
- Industrial Temperature Range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- These are Pb-Free Devices

### MARKING DIAGRAM



|   |                     |
|---|---------------------|
| A | = Assembly Location |
| L | = Wafer Lot         |
| Y | = Year              |
| W | = Work Week         |
| ▪ | = Pb-Free Package   |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

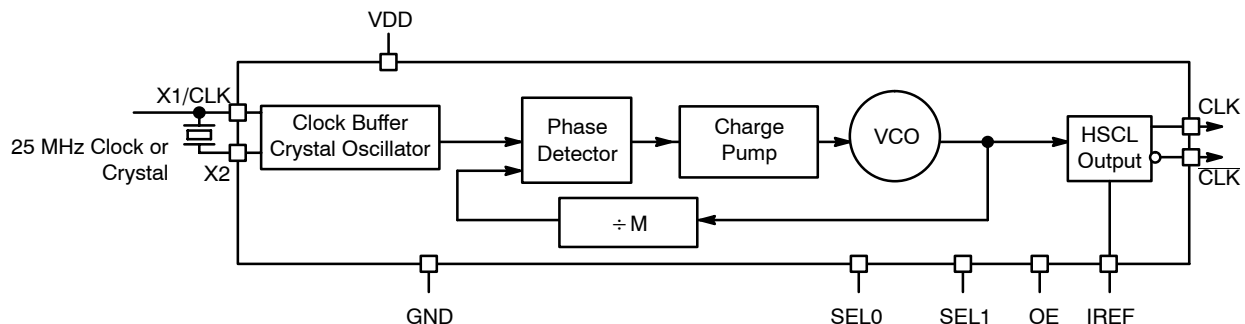
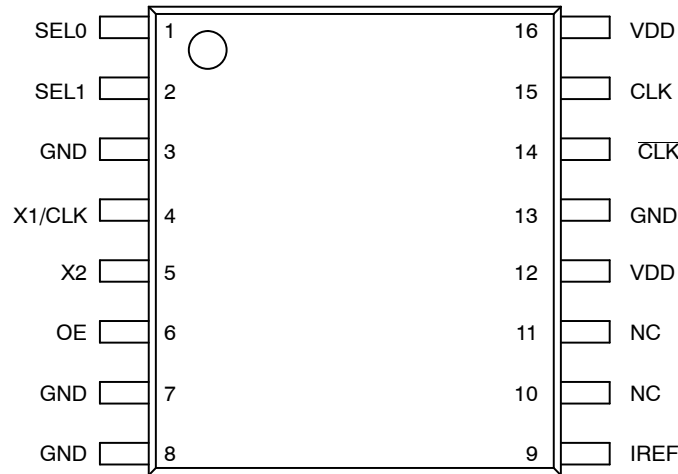


Figure 1. NB3N3002 Simplified Logic Diagram

# NB3N3002



**Figure 2. Pin Configuration (Top View)**

**Table 1. PIN DESCRIPTION**

| Pin         | Symbol                  | I/O                 | Description                                                                                                                     |
|-------------|-------------------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------|
| 1           | Sel0                    | Input               | LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to $V_{DD}$ . See output select table 2 for details.            |
| 2           | Sel1                    | Input               | LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to $V_{DD}$ . See output select Table 2 for details.            |
| 12, 16      | $V_{DD}$                | Power Supply        | Positive supply voltage pins are connected to +3.3 V supply voltage.                                                            |
| 4           | X1/CLK                  | Input               | Crystal or Clock input. Connect to 25 MHz crystal source or single-ended clock.                                                 |
| 5           | X2                      | Input               | Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input.                                                |
| 6           | OE                      | Input               | Output enable tri-states output when connected to GND. Internal pullup resistor to $V_{DD}$ .                                   |
| 3, 7, 8, 13 | GND                     | Power Supply        | Ground 0 V. These pins provide GND return path for the devices.                                                                 |
| 9           | IREF                    | Output              | Output current reference pin. Precision resistor (typ. 475 $\Omega$ ) is connected from pin 9 to GND to set the output current. |
| 15          | CLK                     | HCSL or LVDS Output | Noninverted clock output. (For LVDS levels see Figure 5)                                                                        |
| 14          | $\overline{\text{CLK}}$ | HCSL or LVDS Output | Inverted clock output. (For LVDS levels see Figure 5)                                                                           |
| 10,11       | NC                      |                     | Do not connect                                                                                                                  |

**Table 2. OUTPUT FREQUENCY SELECT TABLE WITH 25MHz CRYSTALS**

| SEL1* | SEL0* | CLK Multiplier | $f_{CLK}$ (MHz) |
|-------|-------|----------------|-----------------|
| L     | L     | 1x             | 25              |
| L     | H     | 4x             | 100             |
| H     | L     | 5x             | 125             |
| H     | H     | 8x             | 200             |

\*Pins SEL1 and SEL0 default high when left open.

## Recommended Crystal Parameters

|                              |                    |
|------------------------------|--------------------|
| Crystal                      | Fundamental AT-Cut |
| Frequency                    | 25 MHz             |
| Load Capacitance             | 16–20 pF           |
| Shunt Capacitance, C0        | 7 pF Max           |
| Equivalent Series Resistance | 50 $\Omega$ Max    |
| Initial Accuracy at 25 °C    | $\pm 20$ ppm       |
| Temperature Stability        | $\pm 30$ ppm       |
| Aging                        | $\pm 20$ ppm       |

Table 3. ATTRIBUTES

| Characteristic                                                 | Value                |
|----------------------------------------------------------------|----------------------|
| ESD Protection Human Body Model                                | > 2 kV               |
| RPU – OE, SEL0 and SEL1 Pull-up Resistor                       | 100 k $\Omega$       |
| Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1) | Level 1              |
| Flammability Rating Oxygen Index: 28 to 34                     | UL 94 V-0 @ 0.125 in |
| Transistor Count                                               | 7623                 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test         |                      |

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

| Symbol           | Parameter                                | Condition 1        | Condition 2                                      | Rating                           | Units        |
|------------------|------------------------------------------|--------------------|--------------------------------------------------|----------------------------------|--------------|
| V <sub>DD</sub>  | Positive Power Supply                    | GND = 0 V          |                                                  | 4.6                              | V            |
| V <sub>I</sub>   | Input Voltage (V <sub>IN</sub> )         | GND = 0 V          | GND $\leq$ V <sub>I</sub> $\leq$ V <sub>DD</sub> | –0.5 V to V <sub>DD</sub> +0.5 V | V            |
| T <sub>A</sub>   | Operating Temperature Range              |                    |                                                  | –40 to +85                       | °C           |
| T <sub>stg</sub> | Storage Temperature Range                |                    |                                                  | –65 to +150                      | °C           |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | TSSOP–16<br>TSSOP–16                             | 138<br>108                       | °C/W<br>°C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)    | (Note 3)           | TSSOP–16                                         | 33 to 36                         | °C/W         |
| T <sub>sol</sub> | Wave Solder                              |                    |                                                  | 265                              | °C           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS (V<sub>DD</sub> = 3.3 V  $\pm$ 5%, GND = 0 V, T<sub>A</sub> = –40°C to +85°C)

| Symbol             | Characteristic                                  | Min                   | Typ | Max                   | Unit |
|--------------------|-------------------------------------------------|-----------------------|-----|-----------------------|------|
| I <sub>DD</sub>    | Power Supply Current (Note 4)                   | 65                    |     | 95                    | mA   |
| I <sub>DDOE</sub>  | Power Supply Current when OE is Set Low         | 35                    |     | 65                    | mA   |
| V <sub>IH</sub>    | Input HIGH Voltage (X1/CLK, Sel0, Sel1, and OE) | 0.7 * V <sub>DD</sub> |     | V <sub>DD</sub> + 300 | mV   |
| V <sub>IL</sub>    | Input LOW Voltage (X1/CLK, Sel0, Sel1, and OE)  | GND – 300             |     | 0.3* V <sub>DD</sub>  | mV   |
| V <sub>OH</sub>    | Output HIGH Voltage (See Figure 4)              | 660                   | 700 | 850                   | mV   |
| V <sub>OL</sub>    | Output LOW Voltage (See Figure 4)               | –150                  | 0   | 150                   | mV   |
| V <sub>cross</sub> | Crossing Voltage Magnitude (Absolute)           | 250                   |     | 400                   | mV   |
| $\Delta V_{cross}$ | Change in Magnitude of V <sub>cross</sub>       |                       |     | 150                   | mV   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. NB3N circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
5. Measurement taken with outputs terminated with R<sub>S</sub> = 33.2  $\Omega$ , R<sub>L</sub> = 49.9  $\Omega$ , with load capacitance of 2 pF and current biasing resistor, R<sub>REF</sub> from I<sub>REF</sub> (Pin 9) to GND of 475  $\Omega$ . See Figure 3.

## NB3N3002

**Table 6. AC CHARACTERISTICS** ( $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $GND = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; Note 7)

| Symbol                     | Characteristic                                                          | Min | Typ         | Max  | Unit          |
|----------------------------|-------------------------------------------------------------------------|-----|-------------|------|---------------|
| $f_{CLKIN}$                | Clock/Crystal Input Frequency                                           |     | 25          |      | MHz           |
| $f_{CLKOUT}$               | Output Clock Frequency                                                  | 25  |             | 200  | MHz           |
| $\theta_{NOISE}$           | Phase-Noise Performance $f_{CLK} = 200 \text{ MHz}/100 \text{ MHz}$     |     |             |      | dBc/Hz        |
|                            | @ 100 Hz offset from carrier                                            |     | -103/-109   |      |               |
|                            | @ 1 kHz offset from carrier                                             |     | -118/-127.8 |      |               |
|                            | @ 10 kHz offset from carrier                                            |     | -122/-136.2 |      |               |
|                            | @ 100 kHz offset from carrier                                           |     | -130/-138.8 |      |               |
|                            | @ 1 MHz offset from carrier                                             |     | -138/-138.2 |      |               |
|                            | @ 10 MHz offset from carrier                                            |     | -149/-164   |      |               |
| $t_{jit(\phi)}$            | RMS Phase Jitter (at 125 MHz @ 1 MHz – 40 MHz)                          |     | 0.25        | 0.50 | ps            |
| $t_{jitter} \text{ (TIE)}$ | TIE RMS Jitter (Note 8) $f_{CLK} = 200 \text{ MHz}$                     |     | 2.5         |      | ps            |
|                            | Cycle-to-Cycle RMS Jitter (Note 9) $f_{CLK} = 200 \text{ MHz}$          |     | 2           | 5    |               |
|                            | Cycle-to-Cycle Peak to Peak Jitter (Note 9) $f_{CLK} = 200 \text{ MHz}$ |     | 20          | 35   |               |
|                            | Period RMS Jitter (Note 9) $f_{CLK} = 200 \text{ MHz}$                  |     | 1.5         | 3    |               |
|                            | Period Peak-to-Peak Jitter (Note 9) $f_{CLK} = 200 \text{ MHz}$         |     | 10          | 20   |               |
| OE                         | Output Enable/Disable Time                                              |     |             | 1.0  | $\mu\text{s}$ |
| $t_{DUTY\_CYCLE}$          | Output Clock Duty Cycle (Measured at cross point)                       | 45  | 50          | 55   | %             |
| $t_R$                      | Output Risetime (Measured from 175 mV to 525 mV, Figure 4)              | 175 | 340         | 700  | ps            |
| $t_F$                      | Output Falltime (Measured from 525 mV to 175 mV, Figure 4)              | 175 | 340         | 700  | ps            |
| $\Delta t_R$               | Output Risetime Variation (Single-Ended)                                |     |             | 125  | ps            |
| $\Delta t_F$               | Output Falltime Variation (Single-Ended)                                |     |             | 125  | ps            |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

6. NB3N circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
7. Measurement taken from differential output on single-ended channel terminated with  $R_S = 33.2 \Omega$ ,  $R_L = 49.9 \Omega$ , with load capacitance of 2 pF and current biasing resistor,  $R_{REF}$  from  $I_{REF}$  (Pin 9) to GND of 475  $\Omega$ . See Figures 3 and 4.
8. Sampled with 20000 cycles to capture jitter component down to 100 kHz.
9. Sampled with 20000 cycles.

**Table 7. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS,** $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

| Symbol                  | Parameter                                           | Conditions (Notes 10 and 11)                                               | Min  | Typ  | Max  | Industry Limit | Unit     |
|-------------------------|-----------------------------------------------------|----------------------------------------------------------------------------|------|------|------|----------------|----------|
| t <sub>jphPCleG1</sub>  | RMS Phase Jitter                                    | PCIe Gen 1 (Notes 12 and 13)                                               |      | 10   | 16   | 86             | ps (p–p) |
| t <sub>jphPCleG2</sub>  |                                                     | PCIe Gen 2 Lo Band<br>10 kHz < f < 1.5 MHz (Note 12)                       |      | 0.2  | 0.25 | 3              | ps (rms) |
|                         |                                                     | PCIe Gen 2 High Band<br>1.5 MHz < f < Nyquist (50 MHz) (Note 12)           |      | 0.9  | 1.2  | 3.1            | ps (rms) |
| t <sub>jphPCleG3</sub>  |                                                     | PCIe Gen 3<br>(PLL BW of 2–4 MHz, CDR = 10 MHz) (Note 12)                  |      | 0.2  | 0.3  | 1              | ps (rms) |
| t <sub>jphPCleG4</sub>  |                                                     | PCIe Gen 4<br>(PLL BW of 2–4 MHz, CDR = 10 MHz) (Note 12)                  |      | 0.21 | 0.3  | 0.5            | ps (rms) |
| t <sub>jphUPI</sub>     |                                                     | UPI<br>(9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI)                  |      | 0.62 | 0.7  | 1.0            | ps (rms) |
| t <sub>jphQPI_SMI</sub> |                                                     | QPI & SMI<br>(100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Note 14) |      | 0.1  | 0.3  | 0.5            | ps (rms) |
|                         |                                                     | QPI & SMI<br>(100.00 MHz, 8.0 Gb/s, 12UI) (Note 14)                        |      | 0.1  | 0.15 | 0.3            | ps (rms) |
|                         | QPI & SMI<br>(100.00 MHz, 9.6 Gb/s, 12UI) (Note 14) |                                                                            | 0.07 | 0.1  | 0.2  | ps (rms)       |          |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

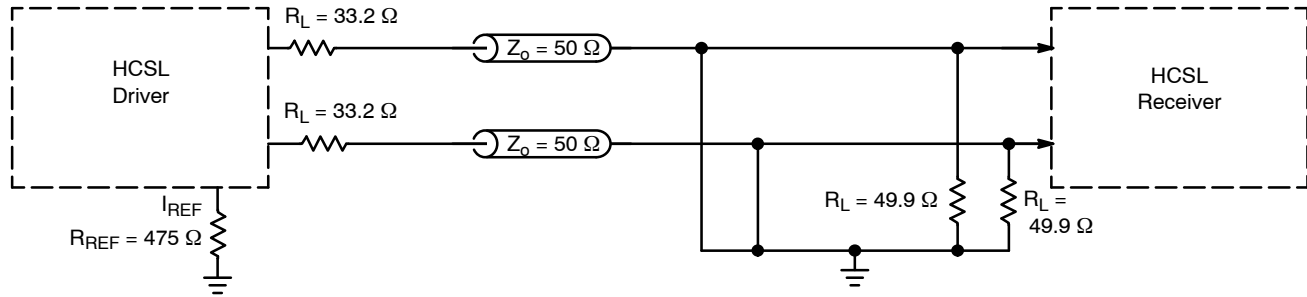
10. Applies to all outputs.

11. Guaranteed by design and characterization, not tested in production

12. See <http://www.pcisig.com> for complete specs

13. Sample size of at least 100K cycles. This figures extrapolates to 108 ps pk-pk @ 1M cycles for a BER of 1–12.

14. Calculated from Intel-supplied Clock Jitter Tool v 1.6.3.

**Figure 3. Typical Termination for Output Driver and Device Evaluation**

## NB3N3002

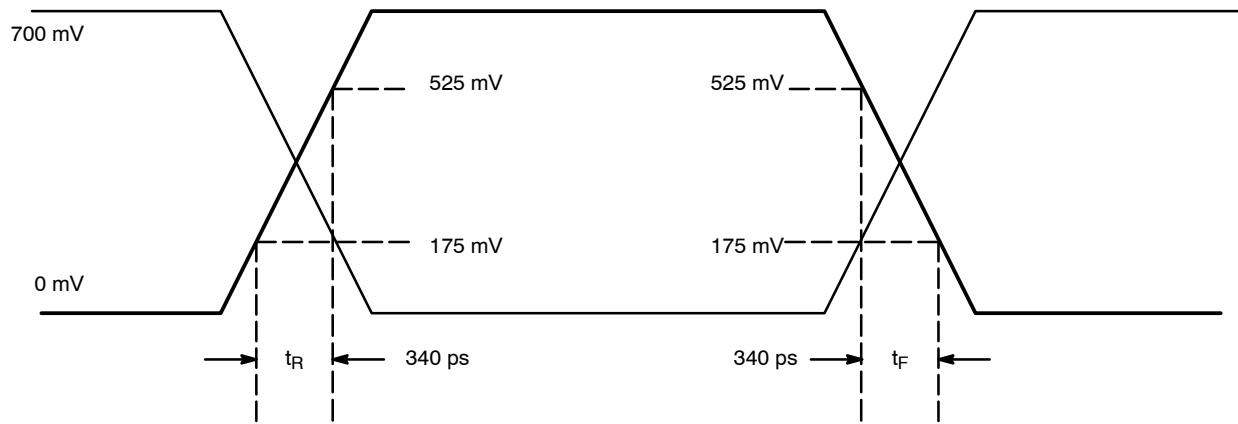


Figure 4. HCSL Output Parameter Characteristics

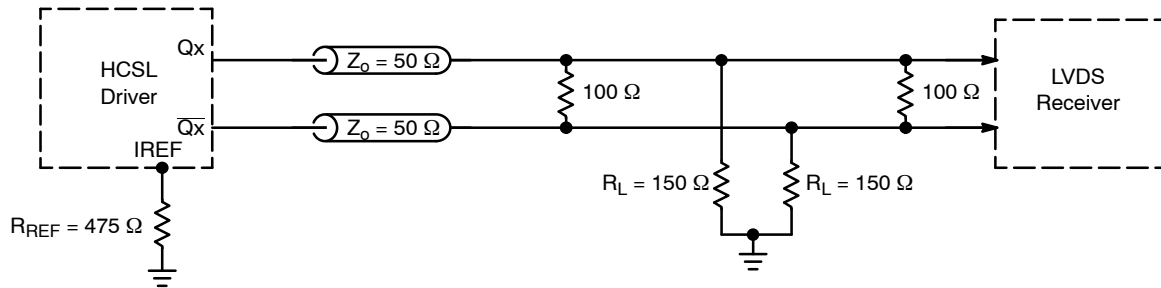
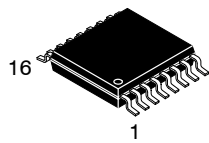


Figure 5. HCSL Interface Termination to LVDS

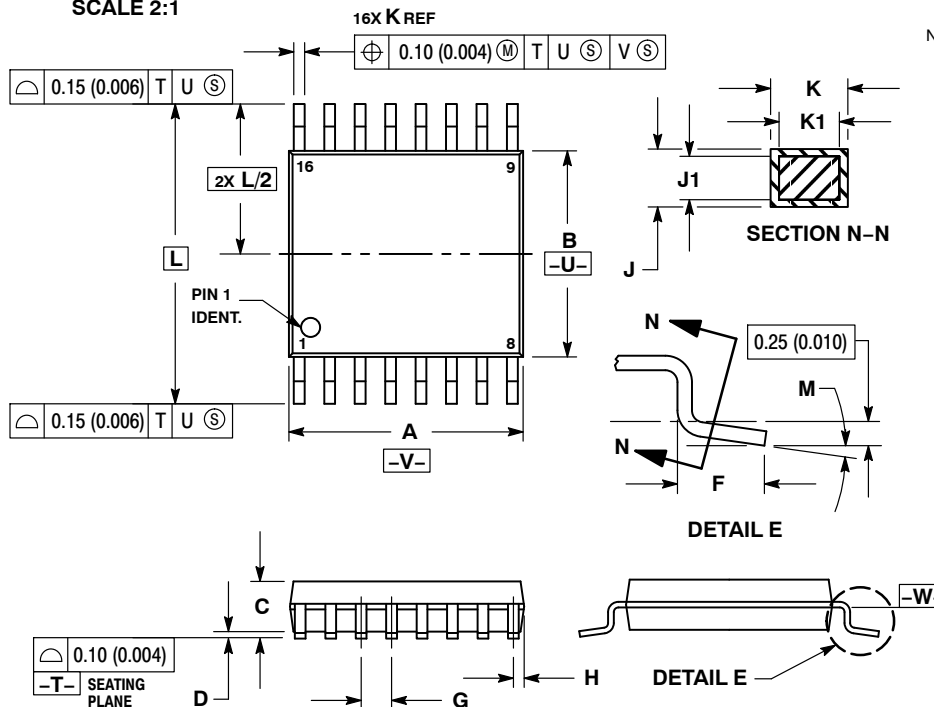
### ORDERING INFORMATION

| Device        | Package               | Shipping <sup>†</sup> |
|---------------|-----------------------|-----------------------|
| NB3N3002DTG   | TSSOP-16<br>(Pb-Free) | 96 Units / Rail       |
| NB3N3002DTR2G | TSSOP-16<br>(Pb-Free) | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

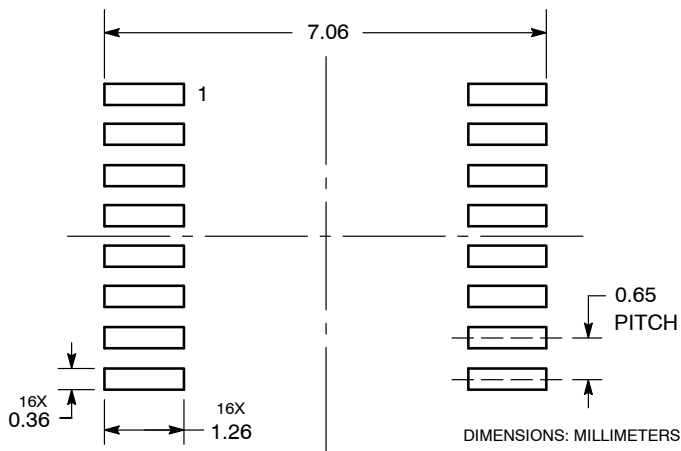

**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006

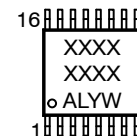

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                         |                    |                                                                                                                                                                                  |
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