

# Dual D-Type Flip-Flop with Set and Reset

The MC74VHC74 is an advanced high speed CMOS D-type flip-flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

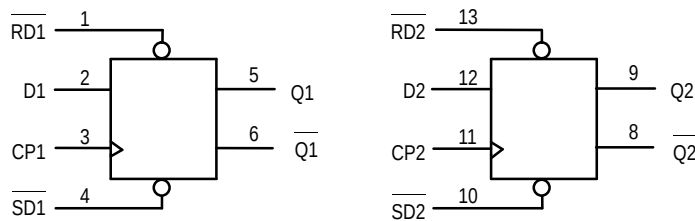
The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset (RD) and Set (SD) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed:  $f_{max} = 170\text{MHz}$  (Typ) at  $V_{CC} = 5\text{V}$
- Low Power Dissipation:  $I_{CC} = 2\mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise:  $V_{OLP} = 0.8\text{V}$  (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 128 FETs or 32 Equivalent Gates

### LOGIC DIAGRAM



### FUNCTION TABLE

| Inputs |    |    |   | Outputs   |    |
|--------|----|----|---|-----------|----|
| SD     | RD | CP | D | Q         | Q  |
| L      | H  | X  | X | H         | L  |
| H      | L  | X  | X | L         | H  |
| L      | L  | X  | X | H*        | H* |
| H      | H  | ↗  | H | H         | L  |
| H      | H  | ↘  | L | L         | H  |
| H      | H  | L  | X | No Change |    |
| H      | H  | H  | X | No Change |    |
| H      | H  | ↺  | X | No Change |    |

\* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

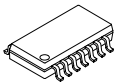
# MC74VHC74



**D SUFFIX**  
14-LEAD SOIC PACKAGE  
CASE 751A-03



**DT SUFFIX**  
14-LEAD TSSOP PACKAGE  
CASE 948G-01



**M SUFFIX**  
14-LEAD SOIC EIAJ PACKAGE  
CASE 965-01

### ORDERING INFORMATION

|             |           |
|-------------|-----------|
| MC74VHCXXD  | SOIC      |
| MC74VHCXXDT | TSSOP     |
| MC74VHCXXM  | SOIC EIAJ |

### PIN ASSIGNMENT

|     |   |    |                 |
|-----|---|----|-----------------|
| RD1 | 1 | 14 | V <sub>CC</sub> |
| D1  | 2 | 13 | RD2             |
| CP1 | 3 | 12 | D2              |
| SD1 | 4 | 11 | CP2             |
| Q1  | 5 | 10 | SD2             |
| Q1  | 6 | 9  | Q2              |
| GND | 7 | 8  | Q2              |



## MAXIMUM RATINGS\*

| Symbol    | Parameter                                                        | Value                   | Unit |
|-----------|------------------------------------------------------------------|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage                                                | – 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage                                                 | – 0.5 to + 7.0          | V    |
| $V_{out}$ | DC Output Voltage                                                | – 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input Diode Current                                              | – 20                    | mA   |
| $I_{OK}$  | Output Diode Current                                             | ± 20                    | mA   |
| $I_{out}$ | DC Output Current, per Pin                                       | ± 25                    | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                         | ± 50                    | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Packages†<br>TSSOP Package† | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature                                              | – 65 to + 150           | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C  
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter                                                                        | Min    | Max       | Unit |
|------------|----------------------------------------------------------------------------------|--------|-----------|------|
| $V_{CC}$   | DC Supply Voltage                                                                | 2.0    | 5.5       | V    |
| $V_{in}$   | DC Input Voltage                                                                 | 0      | 5.5       | V    |
| $V_{out}$  | DC Output Voltage                                                                | 0      | $V_{CC}$  | V    |
| $T_A$      | Operating Temperature, All Package Types                                         | – 40   | + 85      | °C   |
| $t_r, t_f$ | Input Rise and Fall Time<br>$V_{CC} = 3.3V \pm 0.3V$<br>$V_{CC} = 5.0V \pm 0.5V$ | 0<br>0 | 100<br>20 | ns/V |

## DC ELECTRICAL CHARACTERISTICS

| Symbol   | Parameter                         | Test Conditions                                                                          | $V_{CC}$<br>V     | $T_A = 25^\circ\text{C}$    |                   |                             | $T_A = -40 \text{ to } 85^\circ\text{C}$ |                             | Unit |
|----------|-----------------------------------|------------------------------------------------------------------------------------------|-------------------|-----------------------------|-------------------|-----------------------------|------------------------------------------|-----------------------------|------|
|          |                                   |                                                                                          |                   | Min                         | Typ               | Max                         | Min                                      | Max                         |      |
| $V_{IH}$ | Minimum High-Level Input Voltage  |                                                                                          | 2.0<br>3.0 to 5.5 | 1.50<br>$V_{CC} \times 0.7$ |                   |                             | 1.50<br>$V_{CC} \times 0.7$              |                             | V    |
| $V_{IL}$ | Maximum Low-Level Input Voltage   |                                                                                          | 2.0<br>3.0 to 5.5 |                             |                   | 0.50<br>$V_{CC} \times 0.3$ |                                          | 0.50<br>$V_{CC} \times 0.3$ | V    |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$I_{OH} = -50\mu\text{A}$                        | 2.0<br>3.0<br>4.5 | 1.9<br>2.9<br>4.4           | 2.0<br>3.0<br>4.5 |                             | 1.9<br>2.9<br>4.4                        |                             | V    |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$I_{OH} = -4\text{mA}$<br>$I_{OH} = -8\text{mA}$ | 3.0<br>4.5        | 2.58<br>3.94                |                   |                             | 2.48<br>3.80                             |                             |      |
| $V_{OL}$ | Maximum Low-Level Output Voltage  | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$I_{OL} = 50\mu\text{A}$                         | 2.0<br>3.0<br>4.5 |                             | 0.0<br>0.0<br>0.0 | 0.1<br>0.1<br>0.1           |                                          | 0.1<br>0.1<br>0.1           | V    |
|          |                                   | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$I_{OL} = 4\text{mA}$<br>$I_{OL} = 8\text{mA}$   | 3.0<br>4.5        |                             |                   | 0.36<br>0.36                |                                          | 0.44<br>0.44                |      |

## DC ELECTRICAL CHARACTERISTICS

| Symbol          | Parameter                        | Test Conditions                          | V <sub>CC</sub><br>V | T <sub>A</sub> = 25°C |     |       | T <sub>A</sub> = – 40 to 85°C |       | Unit |
|-----------------|----------------------------------|------------------------------------------|----------------------|-----------------------|-----|-------|-------------------------------|-------|------|
|                 |                                  |                                          |                      | Min                   | Typ | Max   | Min                           | Max   |      |
| I <sub>in</sub> | Maximum Input Leakage Current    | V <sub>in</sub> = 5.5V or GND            | 0 to 5.5             |                       |     | ± 0.1 |                               | ± 1.0 | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current | V <sub>in</sub> = V <sub>CC</sub> or GND | 5.5                  |                       |     | 2.0   |                               | 20.0  | μA   |

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

| Symbol                                 | Parameter                                        | Test Conditions                                                               | T <sub>A</sub> = 25°C |             |              | T <sub>A</sub> = – 40 to 85°C |              | Unit |
|----------------------------------------|--------------------------------------------------|-------------------------------------------------------------------------------|-----------------------|-------------|--------------|-------------------------------|--------------|------|
|                                        |                                                  |                                                                               | Min                   | Typ         | Max          | Min                           | Max          |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay,<br>CP to Q or Q       | V <sub>CC</sub> = 3.3 ± 0.3V   C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 6.7<br>9.2  | 11.9<br>15.4 | 1.0<br>1.0                    | 14.0<br>17.5 | ns   |
|                                        |                                                  | V <sub>CC</sub> = 5.0 ± 0.5V   C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 4.6<br>6.1  | 7.3<br>9.3   | 1.0<br>1.0                    | 8.5<br>10.5  |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay,<br>SD or RD to Q or Q | V <sub>CC</sub> = 3.3 ± 0.3V   C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 7.6<br>10.1 | 12.3<br>15.8 | 1.0<br>1.0                    | 14.5<br>18.0 | ns   |
|                                        |                                                  | V <sub>CC</sub> = 5.0 ± 0.5V   C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 4.8<br>6.3  | 7.7<br>9.7   | 1.0<br>1.0                    | 9.0<br>11.0  |      |
| f <sub>max</sub>                       | Maximum Clock Frequency<br>(50% Duty Cycle)      | V <sub>CC</sub> = 3.3 ± 0.3V   C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF | 80<br>50              | 125<br>75   |              | 70<br>45                      |              | MHz  |
|                                        |                                                  | V <sub>CC</sub> = 5.0 ± 0.5V   C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF | 130<br>90             | 170<br>115  |              | 110<br>75                     |              |      |
| C <sub>in</sub>                        | Maximum Input Capacitance                        |                                                                               |                       | 4           | 10           |                               | 10           | pF   |

|                 |                                         |                                        |    |
|-----------------|-----------------------------------------|----------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Note 1.) | Typical @ 25°C, V <sub>CC</sub> = 5.0V | pF |
|                 |                                         | 25                                     |    |

1. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub> / 2 (per flip-flop). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

| Symbol           | Parameter                             | V <sub>CC</sub><br>V   | Guaranteed Limit      |                               | Unit |
|------------------|---------------------------------------|------------------------|-----------------------|-------------------------------|------|
|                  |                                       |                        | T <sub>A</sub> = 25°C | T <sub>A</sub> = – 40 to 85°C |      |
| t <sub>w</sub>   | Minimum Pulse Width, CP               | 3.3 ± 0.3<br>5.0 ± 0.5 | 6.0<br>5.0            | 7.0<br>5.0                    | ns   |
| t <sub>w</sub>   | Minimum Pulse Width, RD or SD         | 3.3 ± 0.3<br>5.0 ± 0.5 | 6.0<br>5.0            | 7.0<br>5.0                    | ns   |
| t <sub>su</sub>  | Minimum Setup Time, D to CP           | 3.3 ± 0.3<br>5.0 ± 0.5 | 6.0<br>5.0            | 7.0<br>5.0                    | ns   |
| t <sub>h</sub>   | Minimum Hold Time, D to CP            | 3.3 ± 0.3<br>5.0 ± 0.5 | 0.5<br>0.5            | 0.5<br>0.5                    | ns   |
| t <sub>rec</sub> | Minimum Recovery Time, SD or RD to CP | 3.3 ± 0.3<br>5.0 ± 0.5 | 5.0<br>3.0            | 5.0<br>3.0                    | ns   |

SWITCHING WAVEFORMS

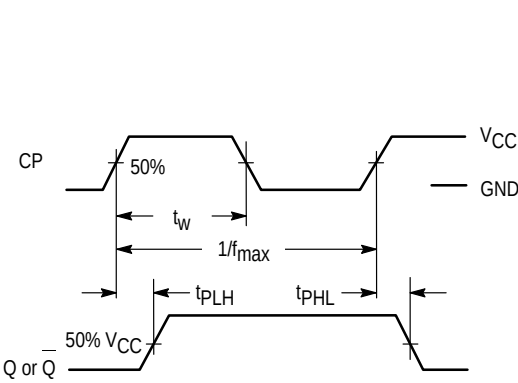


Figure 1.

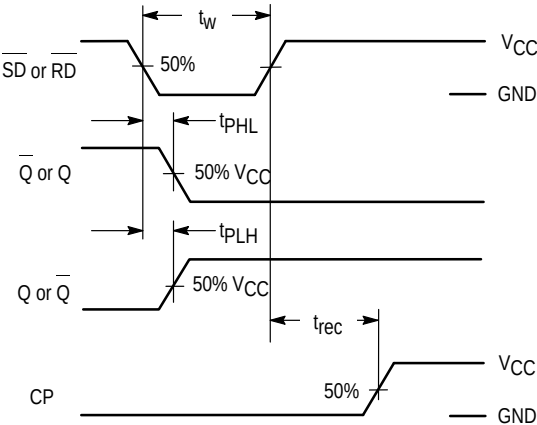


Figure 2.

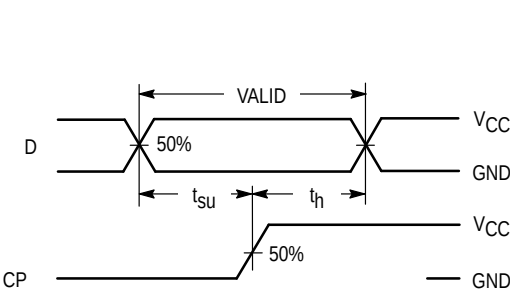
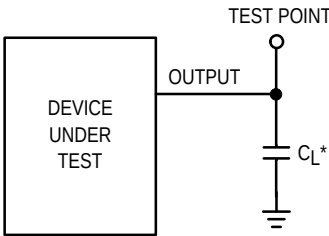


Figure 3.



\* Includes all probe and jig capacitance

Figure 4.

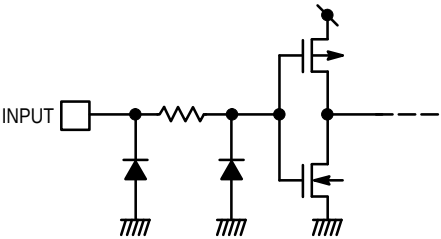
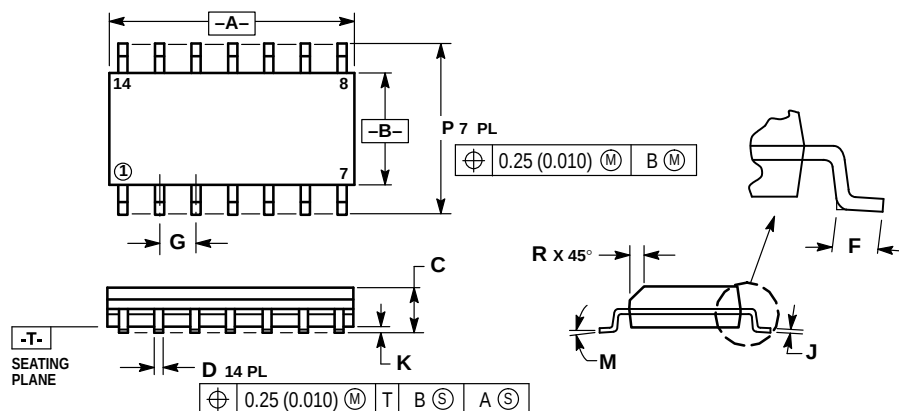


Figure 5. Input Equivalent Circuit

## OUTLINE DIMENSIONS

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751A-03**  
**ISSUE F**

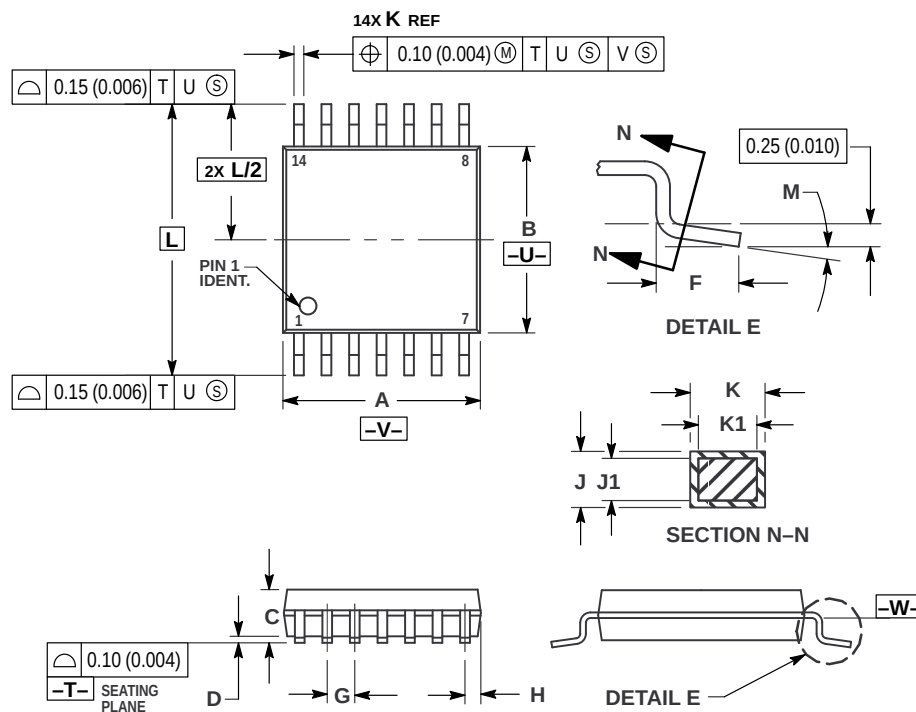


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| E   | 0.40        | 1.25 | 0.016     | 0.049 |
| F   | 1.27 BSC    |      | 0.050 BSC |       |
| G   | 0.19        | 0.25 | 0.008     | 0.009 |
| H   | 0.10        | 0.25 | 0.004     | 0.009 |
| I   | 0°          | 7°   | 0°        | 7°    |
| J   | 5.80        | 6.20 | 0.228     | 0.244 |
| K   | 0.25        | 0.50 | 0.010     | 0.019 |

**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
**CASE 948G-01**  
**ISSUE O**



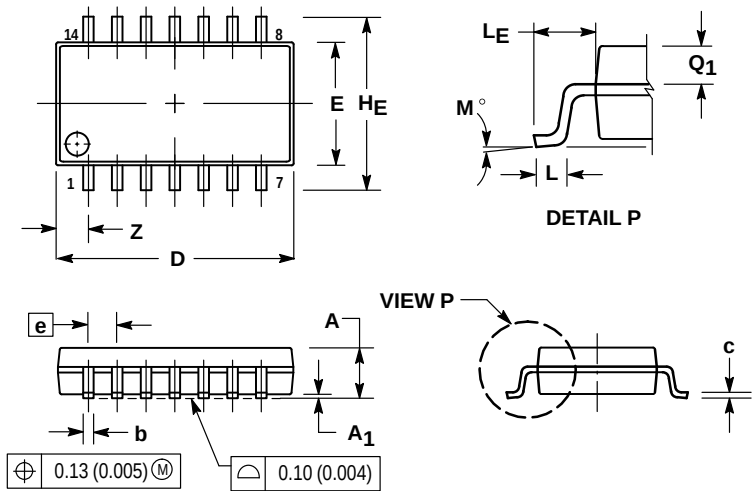
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | —           | 1.20 | —         | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| E   | 0.50        | 0.75 | 0.020     | 0.030 |
| F   | 0.65 BSC    |      | 0.026 BSC |       |
| G   | 0.50        | 0.60 | 0.020     | 0.024 |
| H   | 0.09        | 0.20 | 0.004     | 0.008 |
| I   | 0.09        | 0.16 | 0.004     | 0.006 |
| J   | 0.19        | 0.30 | 0.007     | 0.012 |
| K   | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

OUTLINE DIMENSIONS

M SUFFIX  
PLASTIC SOIC EIAJ PACKAGE  
CASE 965-01  
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | —           | 2.05  | —         | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| HE             | 7.40        | 8.20  | 0.291     | 0.323 |
| 0.50           | 0.50        | 0.85  | 0.020     | 0.033 |
| LE             | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0 °         | 10 °  | 0 °       | 10 °  |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | —           | 1.42  | —         | 0.056 |

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

**How to reach us:**  
**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,  
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

**Mfax™:** RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609  
– US & Canada ONLY 1-800-774-1848

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

**INTERNET:** <http://motorola.com/sps>

