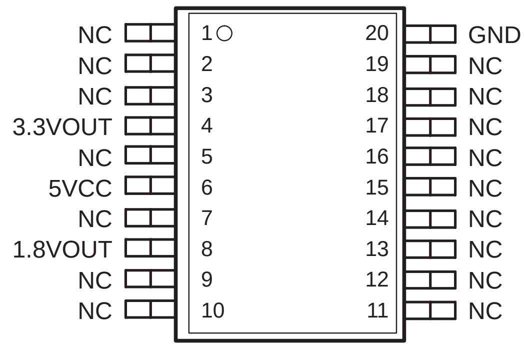
- **Dual Voltage Output, 3.3 V ±3% and 1.8 V ±2%**
- **3.3-V Output Within 2 V of 1.8-V Output Under All Conditions**
- **1.5-A Load Current Capability on 3.3-V Output**
- **300-mA Load Current Capability on 1.8-V Output**
- **Overcurrent Protection for Both Outputs**
- **Thermally-Enhanced Packaging Concept for Efficient Heat Management**
- **Thermal Shutdown to Protect Device During Excessive Power Dissipation**

**DWP HSOP PACKAGE
(TOP VIEW)**

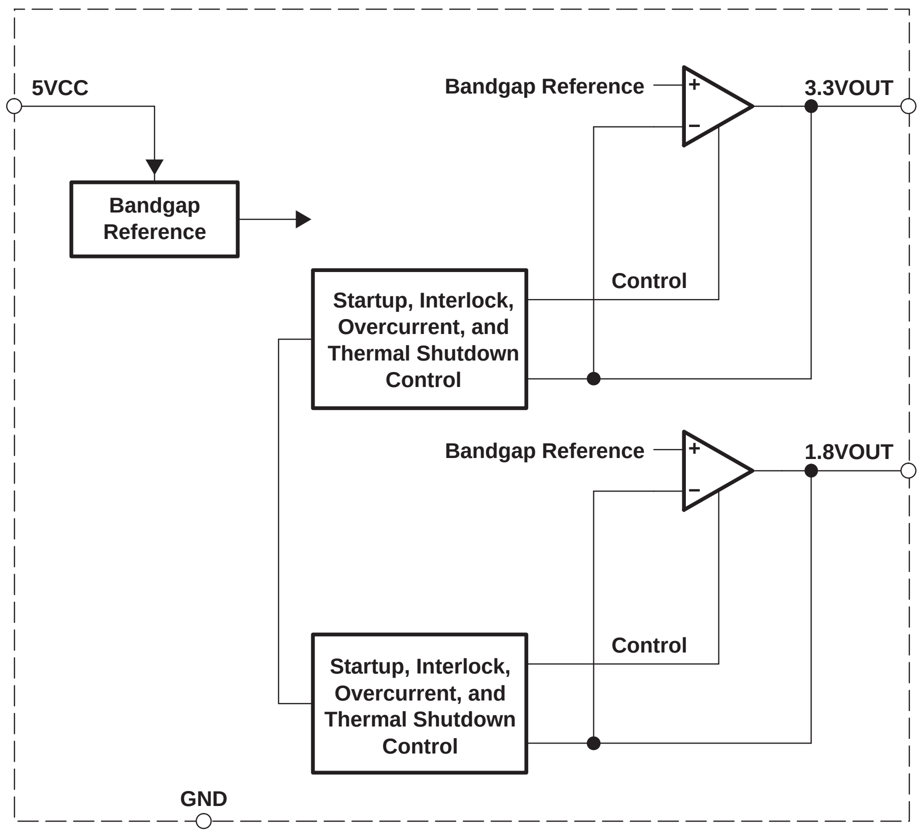


description

The TPPM0110 is a power source intended for use in systems that have a single 5-V input source and require dual, linearly-regulated, low-dropout voltage sources. The outputs must track within 2 V of each other during all conditions and modes of operation. Each output is protected against overcurrent conditions. In the event that one of the outputs is shorted to ground, the other output must maintain a voltage output differential of less than 2 V compared to the output with the abnormal condition.

The 3.3-V ± 3% regulated output is capable of driving loads of 1.5 A, and the 1.8-V ± 2% regulated output is capable of driving loads of 300 mA under all normal operating conditions. The device is available in a PowerPAD™ thermally-enhanced package for efficient heat management, and requires a copper plane to dissipate the heat.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
NC	1−3, 5, 7, 9−12 13−17† 18,9	I	No connection
3.3VOUT	4	O	3.3-V regulated output
5VCC	6	I	5-V input
1.8VOUT	8	O	1.8-V regulated output
GND	20	I	Ground

† These terminals are to be used for test purposes only, and are not connected in system applications. No signal traces should be connected to these terminals.

Table 1. Input Selection‡

INPUT CONDITION	3.3VOUT CONDITION		1.8VOUT CONDITION	
	$V_{(3.3VOUT)}$	$I_{(3.3VOUT)}$	$V_{(1.8VOUT)}$	$I_{(1.8VOUT)}$
Power up 0 to 5 V	Within 2 V of 1.8VOUT	0 to overcurrent limit	0 to 1.8 V	0 to overcurrent limit
5 V	3.3V ±3%	0 to 1.5 A	1.8 V ±2%	0 to 300 mA
Power down 5 V to 0	Within 2 V of 1.8VOUT	1.5 A to 0	1.8 V to 0	300 mA to 0
5 V	0 V	Up to 5.4 A	1.8 V	0 to 300 mA
5 V	Less than 2 V	Don’t care	0 V	Up to 1.08 A
0 V	Within 2 V of 1.8VOUT	Don’t care	1.8 V to 0	Don’t care

‡ See Figures 2, 3, and 4.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)§

5-V input, $V_{(5VCC)}$ (see Notes 1 and 2) . . . . 7 V
3.3-V output current limit, $I_{L(3.3VOUT)}$ . . . . 5.4 A
1.8-V output current limit, $I_{L(1.8VOUT)}$ . . . . 1.08 A
Continuous power dissipation, P_D (see Note 3) . . . . 3.8 W
Electrostatic discharge susceptibility, $V_{(HBMESD)}$ . . . . 2 kV
Operating ambient temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −55°C to 150°C
Lead temperature (soldering, 10 sec), $T_{(LEAD)}$ . . . . 260°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage values on these terminals should not be below –0.5 V.
3. Assumed correct thermal management technique implementation and ambient temperature of 25°C.

recommended operating conditions

		MIN	TYP	MAX	UNIT
5-V input, $V_{(5VCC)}$		4.7		5.3	V
Load capacitance, C_L	10 mΩ < $ESR_{(CL)}$ < 1 Ω			100	µF
Output load current, I_O	3.3VOUT	0		1.5	A
	1.8VOUT	0		300	mA
Ambient temperature, T_A		0		55	°C

electrical characteristics, T_A = 0°C to 55°C, C_L = 100 µF, $V_{(5VCC)}$ = 5 V (unless otherwise noted)

The operating ratings specified below is interpreted as conditions that do not degrade the device's parametric or functional specifications for the life of the product.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(5VCC)}$	Input voltage			4.7	5	5.3	V
$I_{(Q)}$	Quiescent supply current		$I_{O(3.3VOUT)}$ = 1.2 A and $I_{O(1.8VOUT)}$ = 300 mA		1		mA
			With no loads on outputs		600		µA
I_O	Output load current		3.3VOUT = 3.3 V ±3%		1.5		A
			1.8VOUT = 1.8 V ±2%		300		mA
$V_{(3.3VOUT)}$	3.3-V output		I_O = 1 mA to 1.2 A	3.23	3.33	3.43	V
$V_{(1.8VOUT)}$	1.8-V output		I_O = 1 mA to 250 mA	1.78	1.82	1.85	V
$V_{(DO)}$	Regulator drop-out voltage	3.3VOUT	I_O < 1.2 A			1	V
		1.8VOUT	I_O < 250 mA			2.5	
$I_{(3.3VOUT)OC}$	Overcurrent protection		3.3VOUT, I_L↑, See Note 4	2.25	3	5.4	A
			Hysteresis		500		mA
$I_{(1.8VOUT)OC}$	Overcurrent protection		1.8VOUT, See Note 4	0.45	0.6	1.08	A
			Hysteresis		200		mA
C_L	Load capacitance for both regulated outputs					100	µF
$ESR_{(CL)}$	Equivalent series resistance					1	Ω
V_{th}	Threshold voltage		5 V ↓, $I_{O(3.3VOUT)}$= 1.2 A, $I_{O(1.8VOUT)}$ = 250 mA	3.4		4.2	V
			Hysteresis		250		mV
T_{TSD}†	Thermal shutdown hysteresis		Temperature ↑	150		180	°C
			Hysteresis		15		

† Design targets only. Not tested in production.

NOTE 4: In the event of an overcurrent condition, the output should be a constant current limit such that the current never exceeds 360% of $I_{O(TYP)}$. Once the overcurrent condition is removed, the device returns to within the specified regulation limits.

electrical characteristics, T_A = 0°C to 55°C, C_L = 100 µF, $V_{(5VCC)}$ = 5 V (unless otherwise noted)†

The following parametric requirements are applicable to both 3.3VOUT and 1.8VOUT when subjected to these transient tests.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OTL)}$	Output transient voltage limit	Voltage that load step can affect nominal output voltage (see Note 5)	−3%		3%	
$I_{O(STEP)}$	Output load step current	See Note 5	0		$I_{O(TYP)}$	A
$I_{O(SLEW)}$	Output load step current slew rate	See Note 5 and 6			8	A/µs
$t_{(STEP)}$	Output transient time limit	See Note 5		10		µs
	Power up overshoot	Maximum voltage overshoot allowed on either output when component begins regulation. Voltage transient time limit is $t_{(STEP)}$ (see Note 5)			7	%

† Design targets only. Not tested in production..

NOTES: 5. Both outputs must maintain voltage regulation within ±3% of nominal, for a load step from 0 to $I_{O(TYP)}$ and from $I_{O(TYP)}$ to 0 A with a current slew rate of 8A/ms. Load may be toggled at a rate of 20 kHz typical. The outputs must return to the specified regulation limits within the specified time of 10 µs (typical).

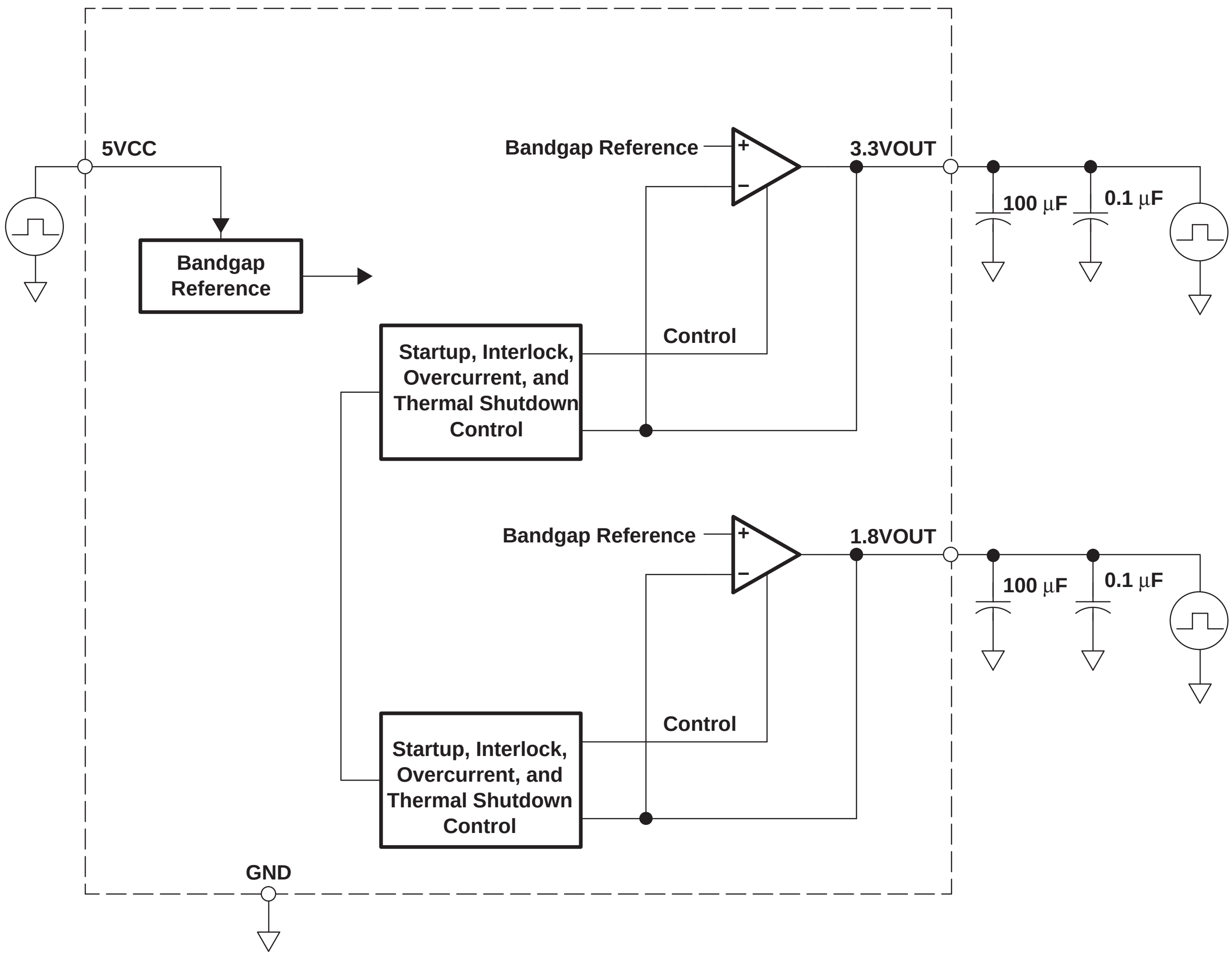
6. Both linear regulators must be capable of regulating small ESR ceramic capacitors or aluminum electrolytic capacitors (see ESR specification).

thermal characteristics

PARAMETER			MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal impedance, junction-to-case				8	°C/W
$R_{\theta JA}$	Thermal impedance, junction-to-ambient	See Note 7			33	°C/W

NOTE 7: See JEDEC PCB specifications for high-K and correct implementation for 150 LFM air flow.

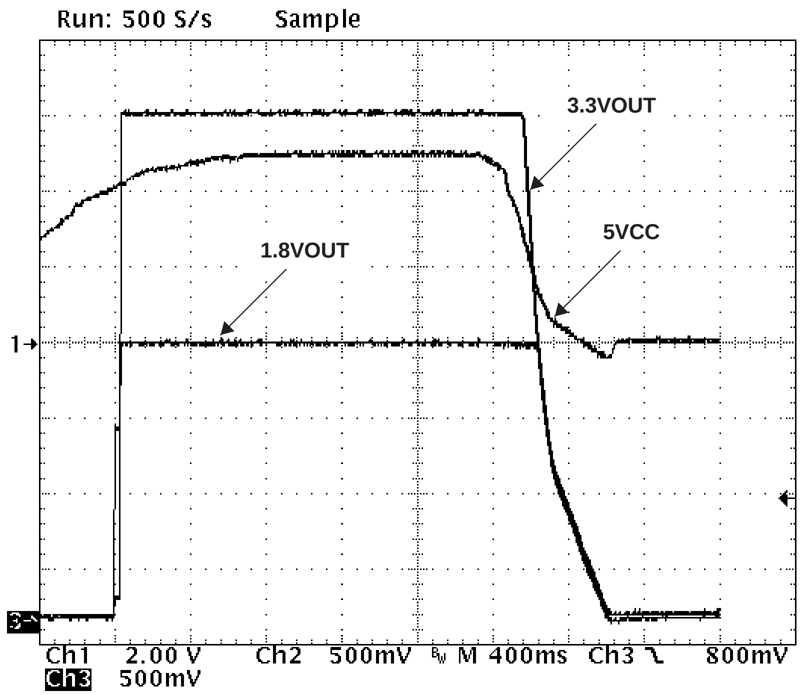
TYPICAL CHARACTERISTICS



NOTE: The 100-µF capacitor has: ESL = 3 nH and ESR = 0.5 Ω to 1 Ω.
Testing circuit includes 100-µF aluminum capacitors which may be replaced with 10-µF ceramic capacitors. Both capacitors must have equivalent series inductance ESL < 3 nH and equivalent series resistance ESR < 1 Ω.

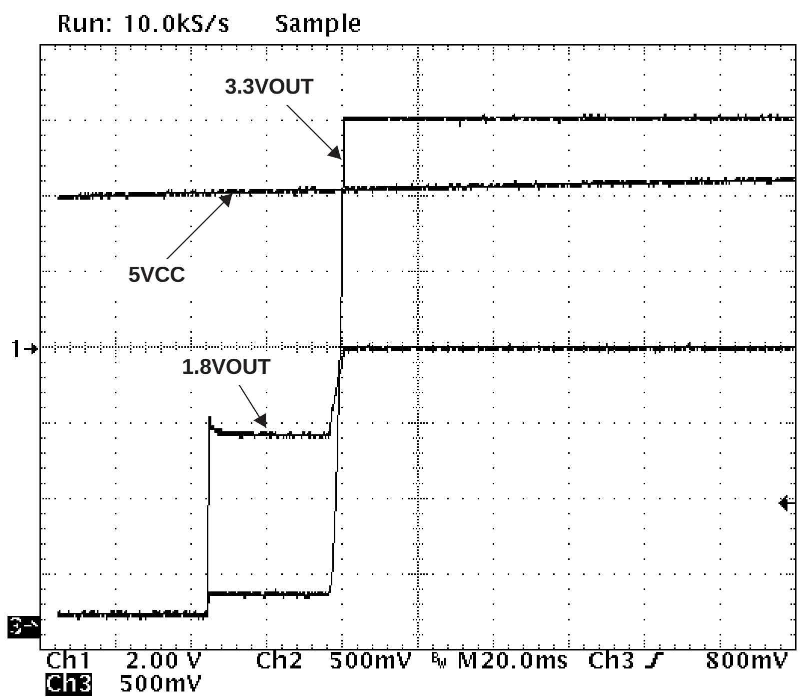
Figure 1. Test Circuit

TYPICAL CHARACTERISTICS



NOTE: The outputs track within 2 V in the power-up and power-down sequence.

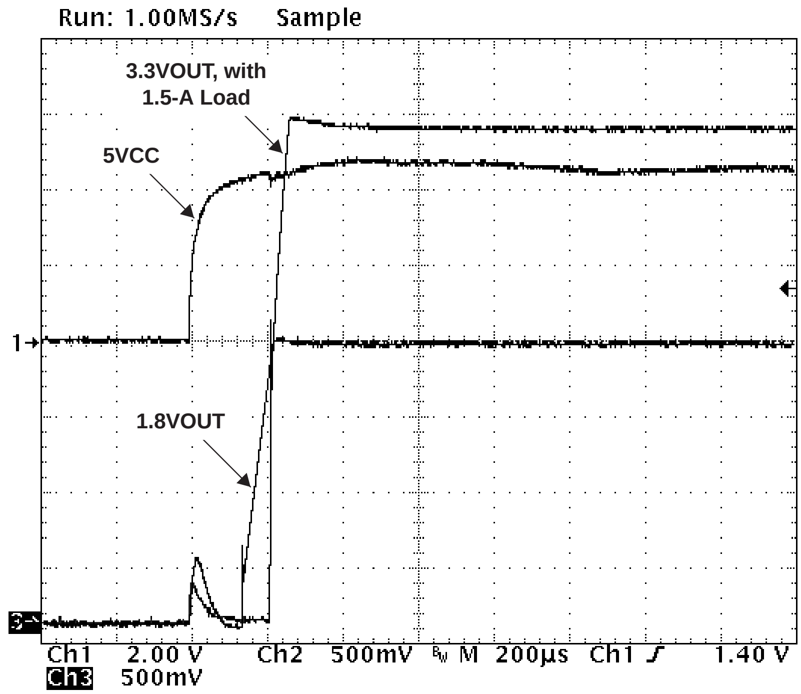
Figure 2. Power-Up and Power-Down Sequence



NOTE: The outputs track within 2 V in the power-up sequence.

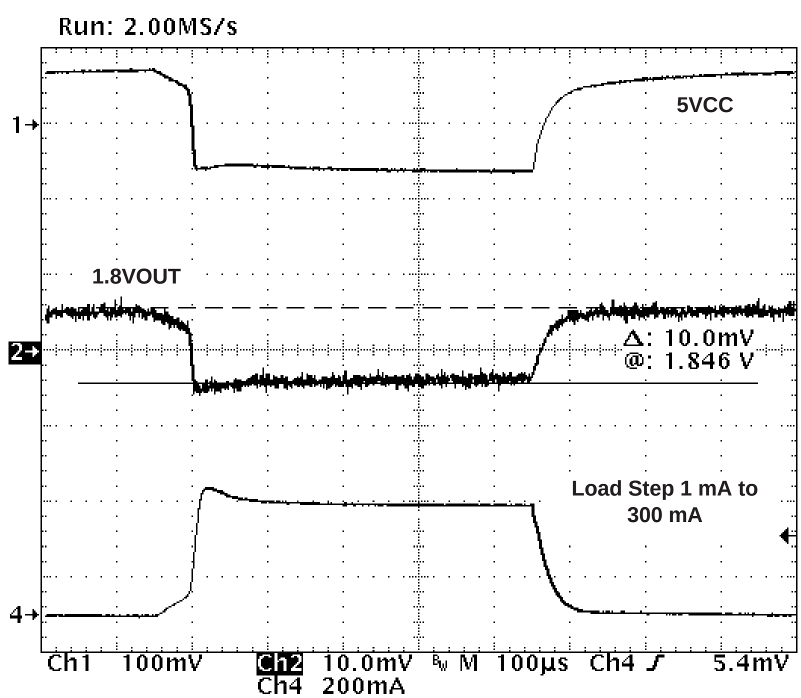
Figure 3. Power-Up Sequence

TYPICAL CHARACTERISTICS



NOTE: The power-up sequence is for an output with 1.5 A on 3.3VOUT.

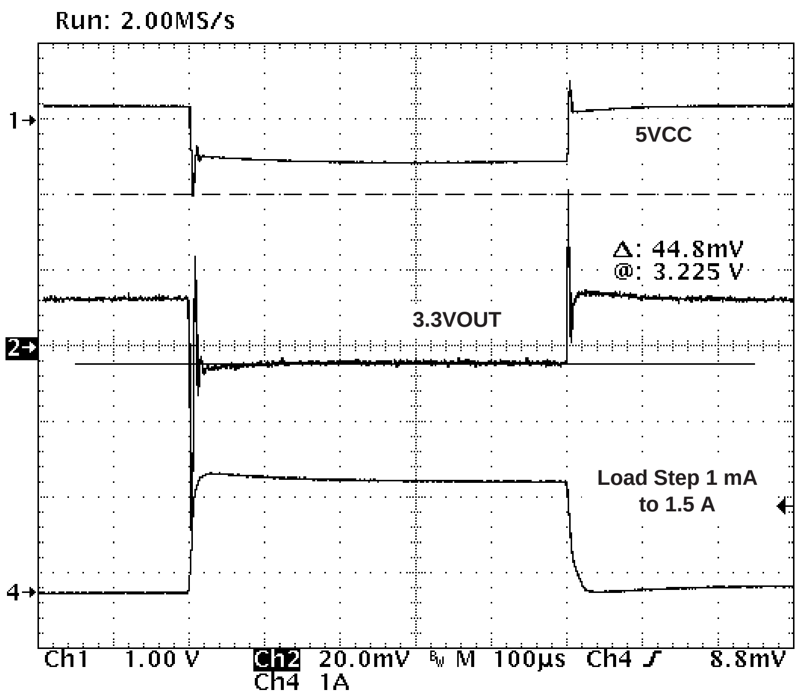
Figure 4. Power-Up Sequence



NOTE: Load regulation on 1.8VOUT with a load step of 1 mA to 300 mA.

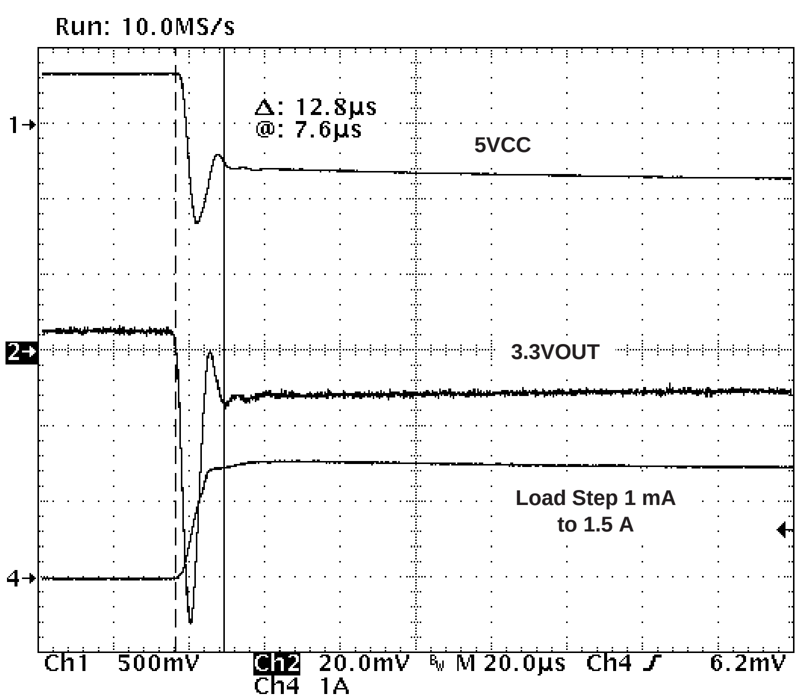
Figure 5. Load Regulation on 1.8VOUT

TYPICAL CHARACTERISTICS



NOTE: Load regulation on 3.3VOUT with a load step of 1 mA to 1.5 A

Figure 6. Load Regulation on 3.3VOUT



NOTE: Output settling time on 3.3VOUT due to load regulation step of 1 mA to 1.5 A

Figure 7. Settling Time Due to Load Regulation on 3.3VOUT

TYPICAL THERMAL CHARACTERISTICS

To ensure reliable operation of the device, the junction temperature of the output device must be within the safe operating area (SOA). This is achieved by providing a means to dissipate the heat generated from the junction of the output structure. There are two components that contribute to thermal resistance. They consist of two paths in series. The first is the junction-to-case thermal resistance, $R_{\theta JC;}$ the second is the case-to-ambient thermal resistance, $R_{\theta CA}$. The overall junction-to-ambient thermal resistance, $R_{\theta JA}$, is determined by:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

The ability to efficiently dissipate the heat from the junction is a function of the package style and board layout incorporated in the application. The operating junction temperature is determined by the operating ambient temperature, T_A, and the junction power dissipation, P_J.

The junction temperature, T_J, is determined by the following thermal equation:

$$T_J = T_A + P_J (R_{\theta JC}) + P_J (R_{\theta CA})$$

$$T_J = T_A + P_J (R_{\theta JA})$$

This particular application uses the 20-pin DWP power pad package with a standard lead frame with a dedicated ground terminal. Using a multilayer printed-circuit board (PCB), the power pad is mounted as recommended in the TI packaging application. The power pad is electrically connected to the ground plane of the board through a dedicated ground pin and the die mount power pad. This provides a means for heat spreading through the copper plane associated within the PCB (ground layer). The thermal resistance from junction to ambient, $R_{\theta JA}$, is dependent of several factors, the implemented method of package attachment to the heat spreading material and the air flow in the system application.

APPLICATION INFORMATION

packaging

To maximize the efficiency of this package for application on a single layer or multilayer PCB, certain guidelines must be followed.

The following information is to be used as a guideline only. For further information, refer to the PowerPAD concept implementation document.

multilayer PCB

The following are guidelines for mounting the PowerPAD IC on a multilayer PCB with a ground plane**.**

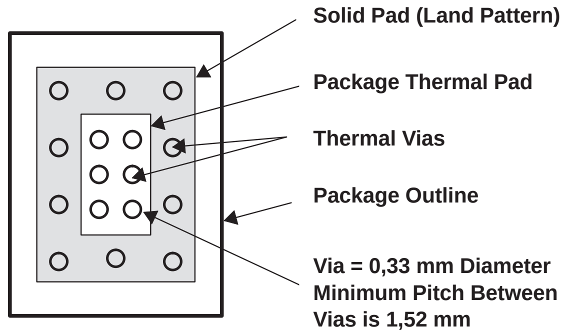


Figure 8. Package and Land Configuration for a Multilayer PCB

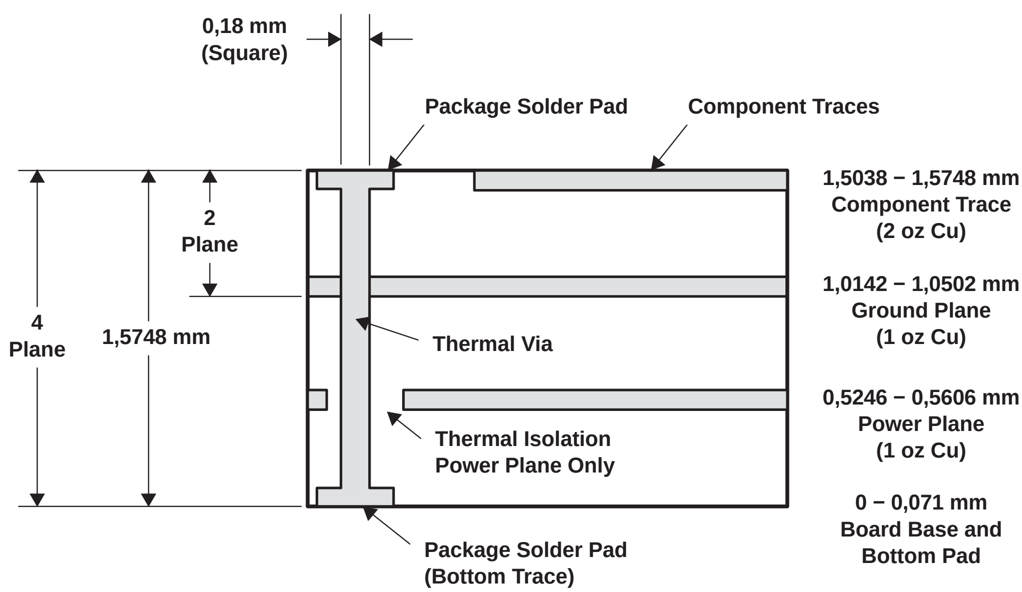


Figure 9. Multilayer Board (Side View)

APPLICATION INFORMATION

In a multilayer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors (die area, number of thermal vias, thickness of copper, etc.). Consult the PowerPAD Thermally Enhanced Package Technical Brief.

single layer PCB

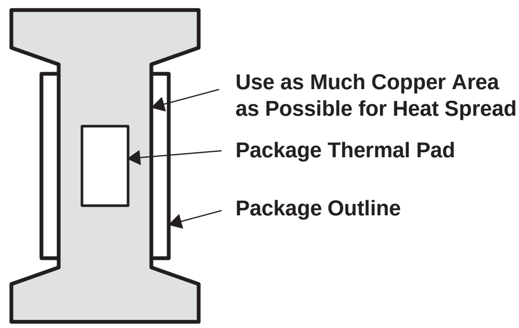
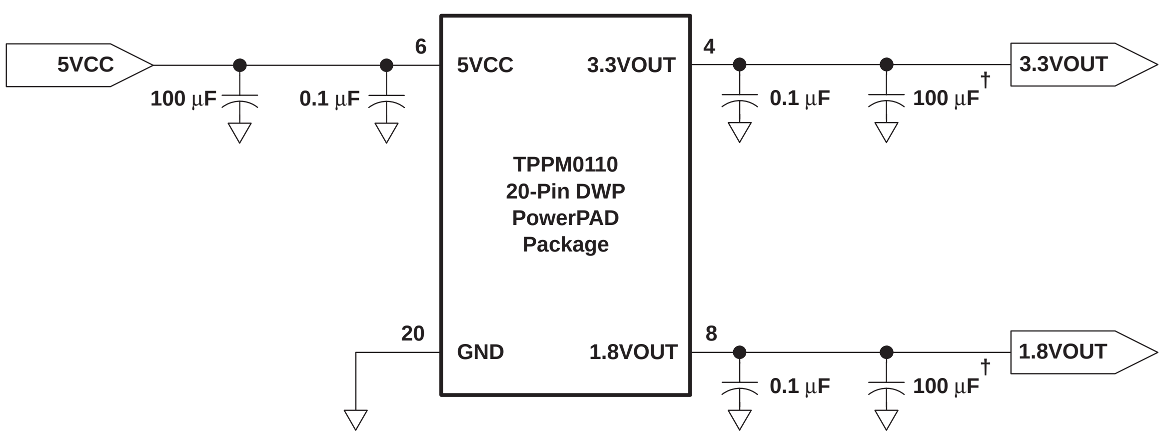


Figure 10. Land Configuration for Single-Layer PCB

Layout recommendation is to utilize as much copper area for the power management section of a single-layer board as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low thermal impedance attachment method (solder paste or thermal-conductive epoxy). In both of these cases, it is advisable to use as much copper traces as possible to dissipate the heat.

IMPORTANT

If this attachment method is not implemented correctly, this product will not operate efficiently. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.



† It is recommended that the capacitors on the outputs (100 μF) have a low ESR < 1 Ω.
These stabilizing capacitors must be placed in close proximity of their corresponding output terminals for optimal performance.

Figure 11. Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPPM0110DWP	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TPPM0110	Samples
TPPM0110DWPR	ACTIVE	SO PowerPAD	DWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TPPM0110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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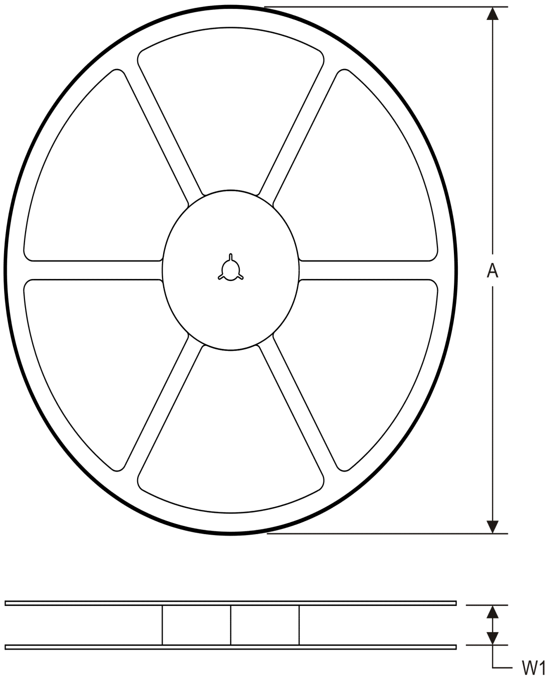
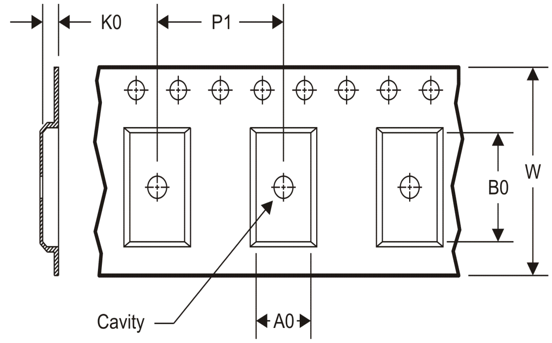
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



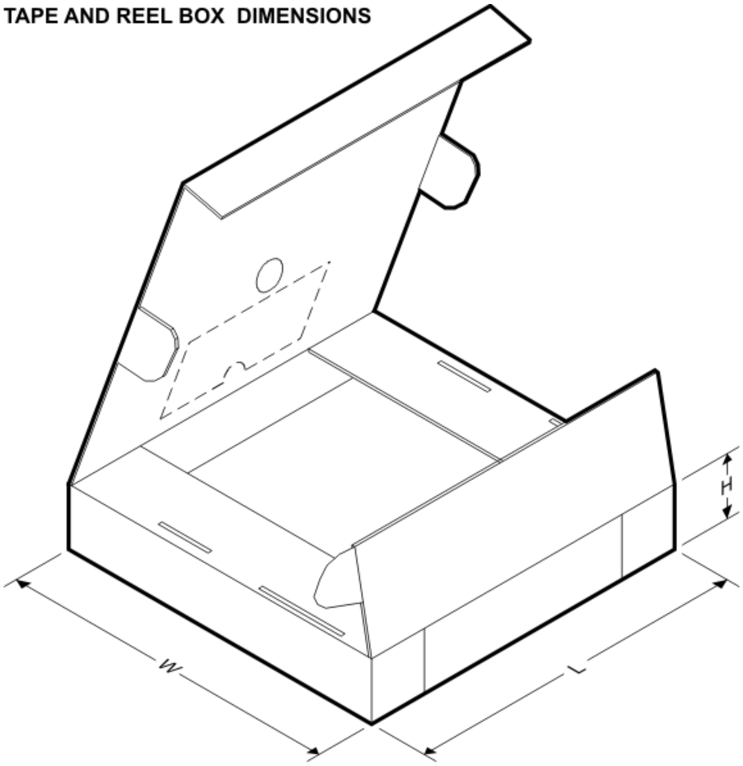
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPPM0110DWPR	SO Power PAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

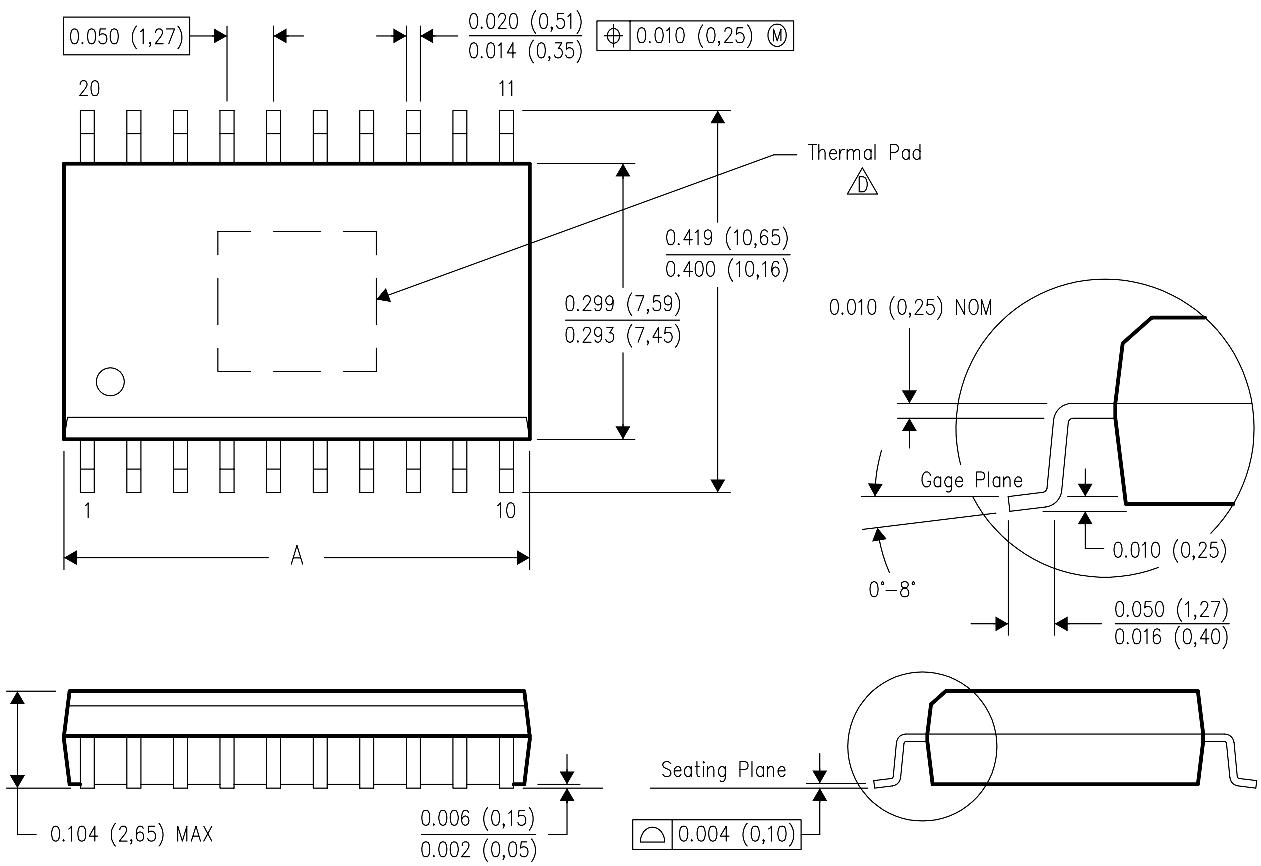


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPPM0110DWPR	SO PowerPAD	DWP	20	2000	367.0	367.0	45.0

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

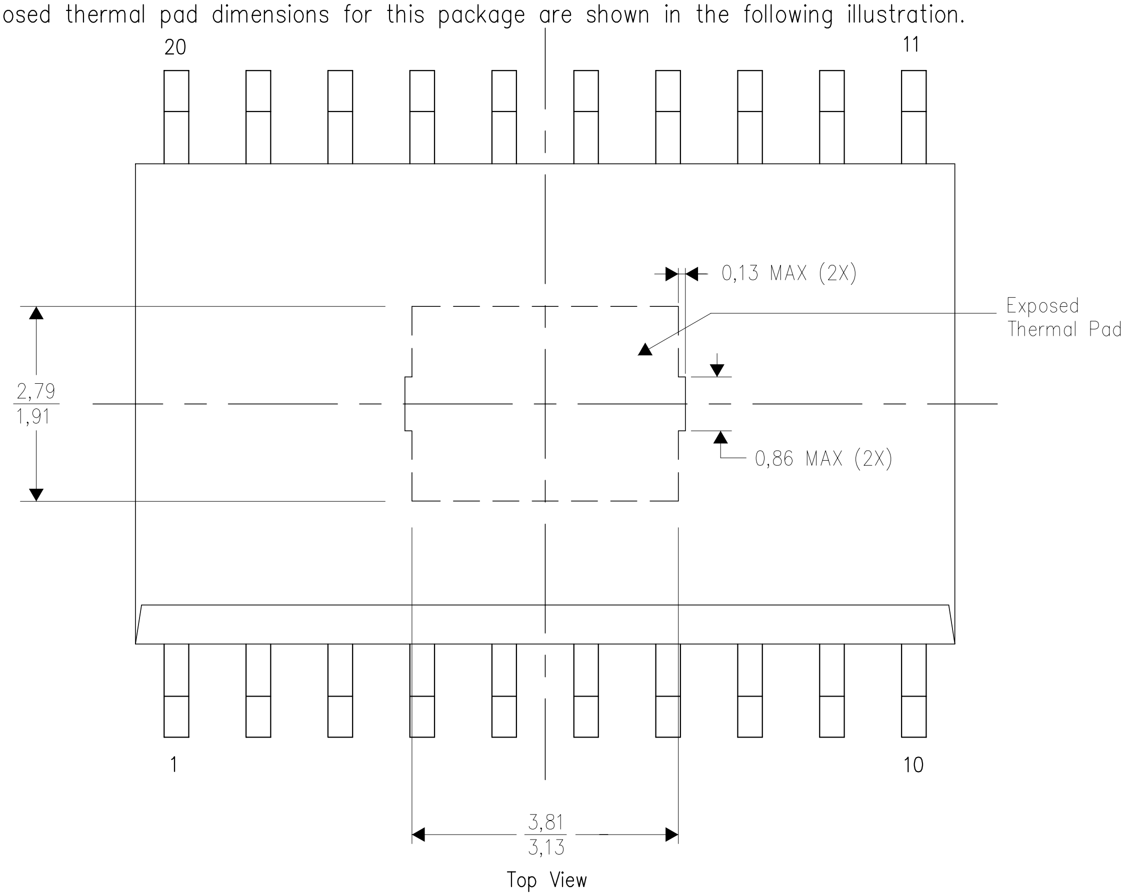
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

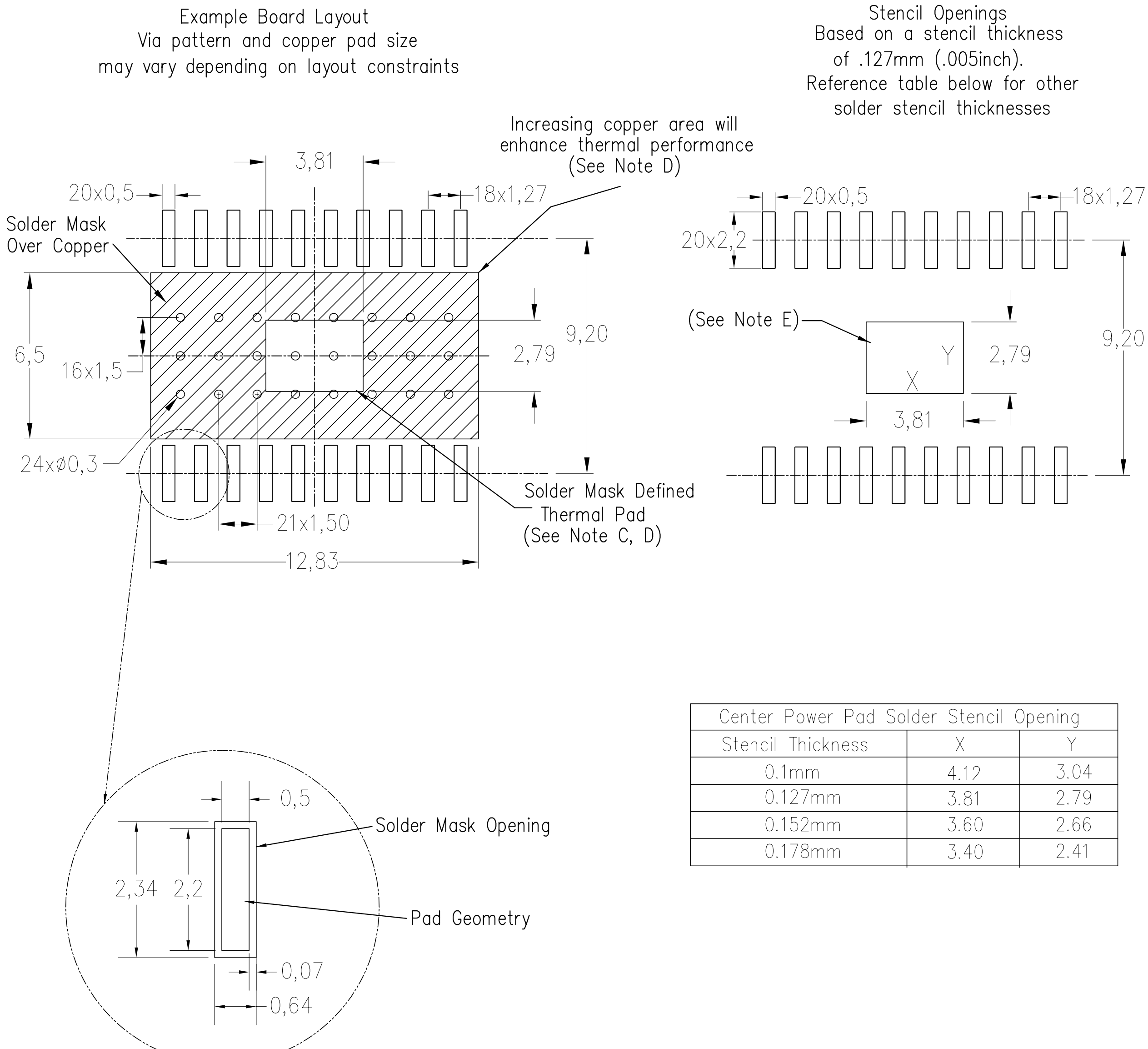


Exposed Thermal Pad Dimensions

4206325–4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.12	3.04
0.127mm	3.81	2.79
0.152mm	3.60	2.66
0.178mm	3.40	2.41

4208286–3/B 12/10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

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