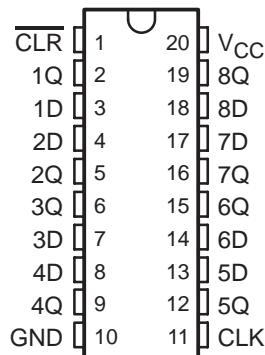
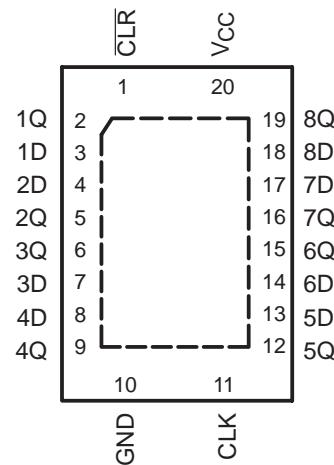


- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

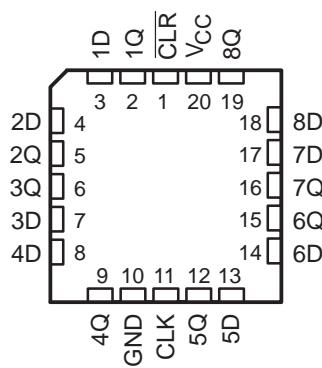
SN54LV273A . . . J OR W PACKAGE
SN74LV273A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV273A . . . RGY PACKAGE
(TOP VIEW)



SN54LV273A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The 'LV273A devices are octal D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	SN74LV273ARGYR	LV273A
	SOIC – DW	Tube of 25	LV273A
		Reel of 2000	SN74LV273ADWR
	SOP – NS	Reel of 2000	SN74LV273ANSR
	SSOP – DB	Reel of 2000	SN74LV273ADBR
	TSSOP – PW	Tube of 70	SN74LV273APW
		Reel of 2000	SN74LV273APWR
		Reel of 250	SN74LV273APWT
-55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LV273ADGVR
	CDIP – J	Tube of 20	SNJ54LV273AJ
		Tube of 85	SNJ54LV273AW
	LCCC – FK	Tube of 55	SNJ54LV273AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LV273A, SN74LV273A OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS399J – APRIL 1998 – REVISED APRIL 2005

description/ordering information (continued)

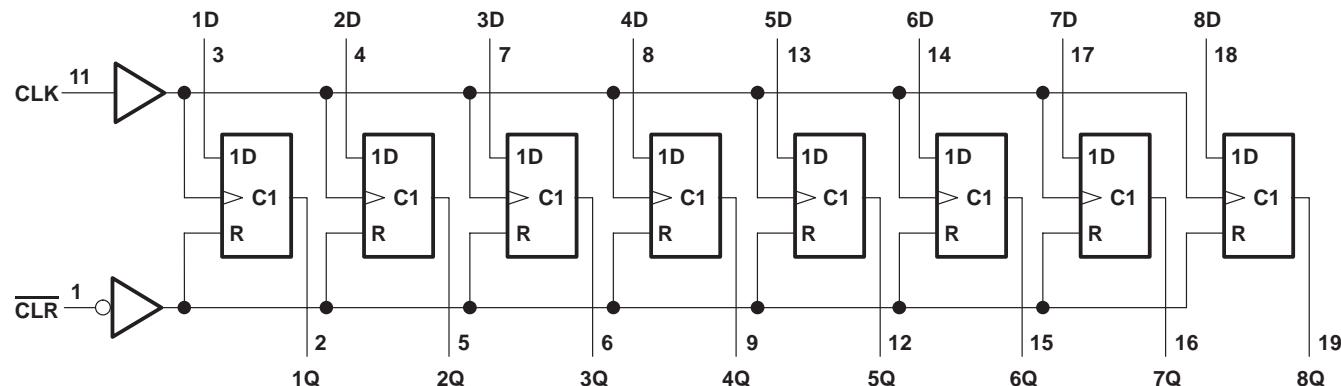
These devices are positive-edge-triggered flip-flops with direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

**SN54LV273A, SN74LV273A
OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

SCLS399J – APRIL 1998 – REVISED APRIL 2005

recommended operating conditions (see Note 5)

			SN54LV273A		SN74LV273A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5			V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5			V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	V _{CC} × 0.3			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	V _{CC} × 0.3			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	V _{CC} × 0.3			
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50			µA
		V _{CC} = 2.3 V to 2.7 V	-2	-2			mA
		V _{CC} = 3 V to 3.6 V	-6	-6			
		V _{CC} = 4.5 V to 5.5 V	-12	-12			
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50			µA
		V _{CC} = 2.3 V to 2.7 V	2	2			mA
		V _{CC} = 3 V to 3.6 V	6	6			
		V _{CC} = 4.5 V to 5.5 V	12	12			
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V	200	200			ns/V
		V _{CC} = 3 V to 3.6 V	100	100			
		V _{CC} = 4.5 V to 5.5 V	20	20			
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV273A			SN74LV273A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 µA	2 V to 5.5 V	V _{CC} - 0.1			V _{CC} - 0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 µA	2 V to 5.5 V		0.1		0.1			V
	I _{OL} = 2 mA	2.3 V		0.4		0.4			
	I _{OL} = 6 mA	3 V		0.44		0.44			
	I _{OL} = 12 mA	4.5 V		0.55		0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1		±1			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		20		20			µA
I _{off}	V _I or V _O = 0 to 5.5 V	0		5		5			µA
C _i	V _I = V _{CC} or GND	3.3 V		2		2			pF

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV273A		SN74LV273A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	6.5	7	7			ns
		CLK high or low	7	8.5	8.5			
t_{SU}	Setup time, data before CLK^\uparrow	Data	8.5	10.5	10.5			ns
		CLR inactive	4	4	4			
t_H	Hold time, data after CLK^\uparrow		0.5	1	1			ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV273A		SN74LV273A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5	6	6			ns
		CLK high or low	5	6.5	6.5			
t_{SU}	Setup time, data before CLK^\uparrow	Data	5.5	6.5	6.5			ns
		CLR inactive	2.5	2.5	2.5			
t_H	Hold time, data after CLK^\uparrow		1	1	1			ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

		$T_A = 25^\circ\text{C}$		SN54LV273A		SN74LV273A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CLR low	5	5	5			ns
		CLK high or low	5	5	5			
t_{SU}	Setup time, data before CLK^\uparrow	Data	4.5	4.5	4.5			ns
		CLR inactive	2	2	2			
t_H	Hold time, data after CLK^\uparrow		1	1	1			ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			UNIT
				MIN	TYP	MAX	
f_{max}			$C_L = 15 \text{ pF}$	55*	95*		MHz
			$C_L = 50 \text{ pF}$	45	75	40	
t_{pd}	CLK	Q	$C_L = 15 \text{ pF}$	10.4*	18.3*	1* 20.5*	ns
t_{PHL}	\overline{CLR}	Q		10.3*	19*	1* 21*	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$	12.9	22.1	1 25	ns
t_{PHL}	\overline{CLR}	Q		13.1	22.8	1 25.5	
$t_{sk(o)}$					2		2

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**SN54LV273A, SN74LV273A
OCTAL D-TYPE FLIP-FLOPS
WITH CLEAR**

SCLS399J – APRIL 1998 – REVISED APRIL 2005

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV273A	SN74LV273A	UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	75*	140*		65*	65	MHz
			$C_L = 50 \text{ pF}$	50	110		45	45	
t_{pd}	CLK	Q	$C_L = 15 \text{ pF}$	7.1*	13.6*		1*	16*	ns
t_{PHL}	\overline{CLR}	Q		6.9*	13.6*		1*	16*	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$	9.1	17.1		1	19.5	ns
t_{PHL}	\overline{CLR}	Q		8.7	17.1		1	19.5	
$t_{sk(o)}$					1.5			1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV273A	SN74LV273A	UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	120*	205*		100*	100	MHz
			$C_L = 50 \text{ pF}$	80	160		70	70	
t_{pd}	CLK	Q	$C_L = 15 \text{ pF}$	4.8*	9*		1*	10.5*	ns
t_{PHL}	\overline{CLR}	Q		4.7*	8.5*		1*	10*	
t_{pd}	CLK	Q	$C_L = 50 \text{ pF}$	6.2	11		1	12.5	ns
t_{PHL}	\overline{CLR}	Q		6	10.5		1	12	
$t_{sk(o)}$					1			1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 6)

PARAMETER	SN74LV273A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.4	-0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage		0.99		V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

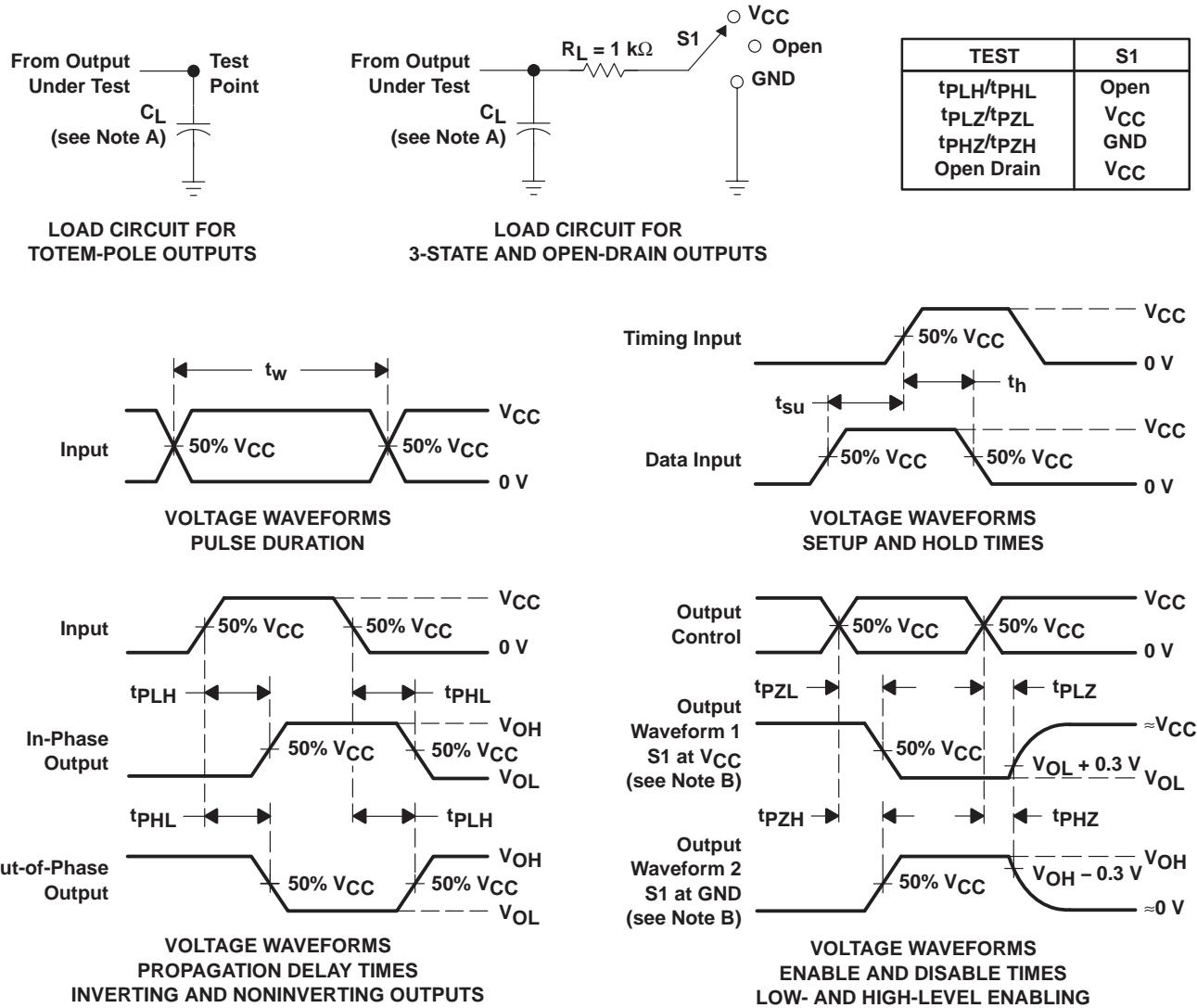
PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
		3.3 V	15.9	
C_{pd} Power dissipation capacitance	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	5 V	17.1	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV273ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADB RG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADGV RG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV273ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LV273ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV273AZQNR	ACTIVE	BGA MI CROSTA R JUNI OR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

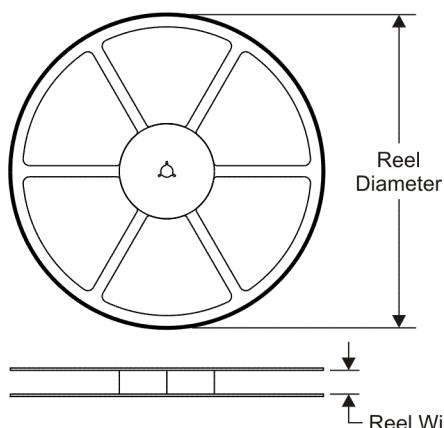
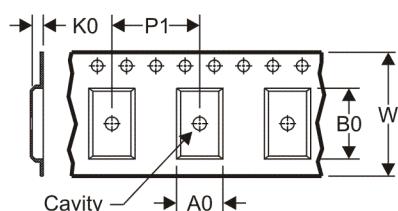
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

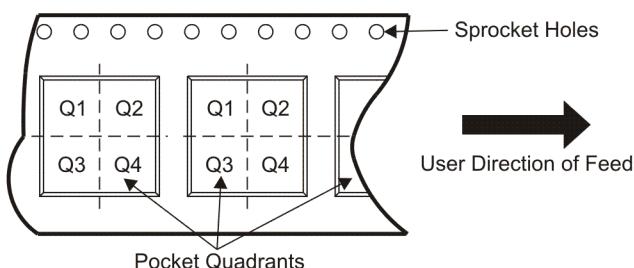
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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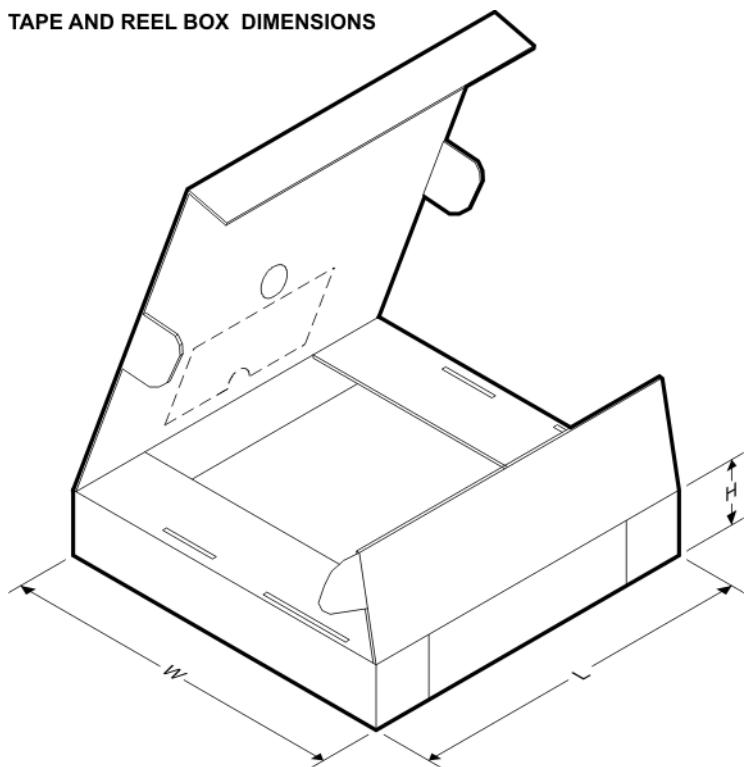
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV273ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV273ADGVR	TVSOP	DGV	20	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LV273ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LV273ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LV273APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV273ARGYR	VQFN	RGY	20	3000	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LV273AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.5	8.0	12.0	Q1
SN74LV273AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1

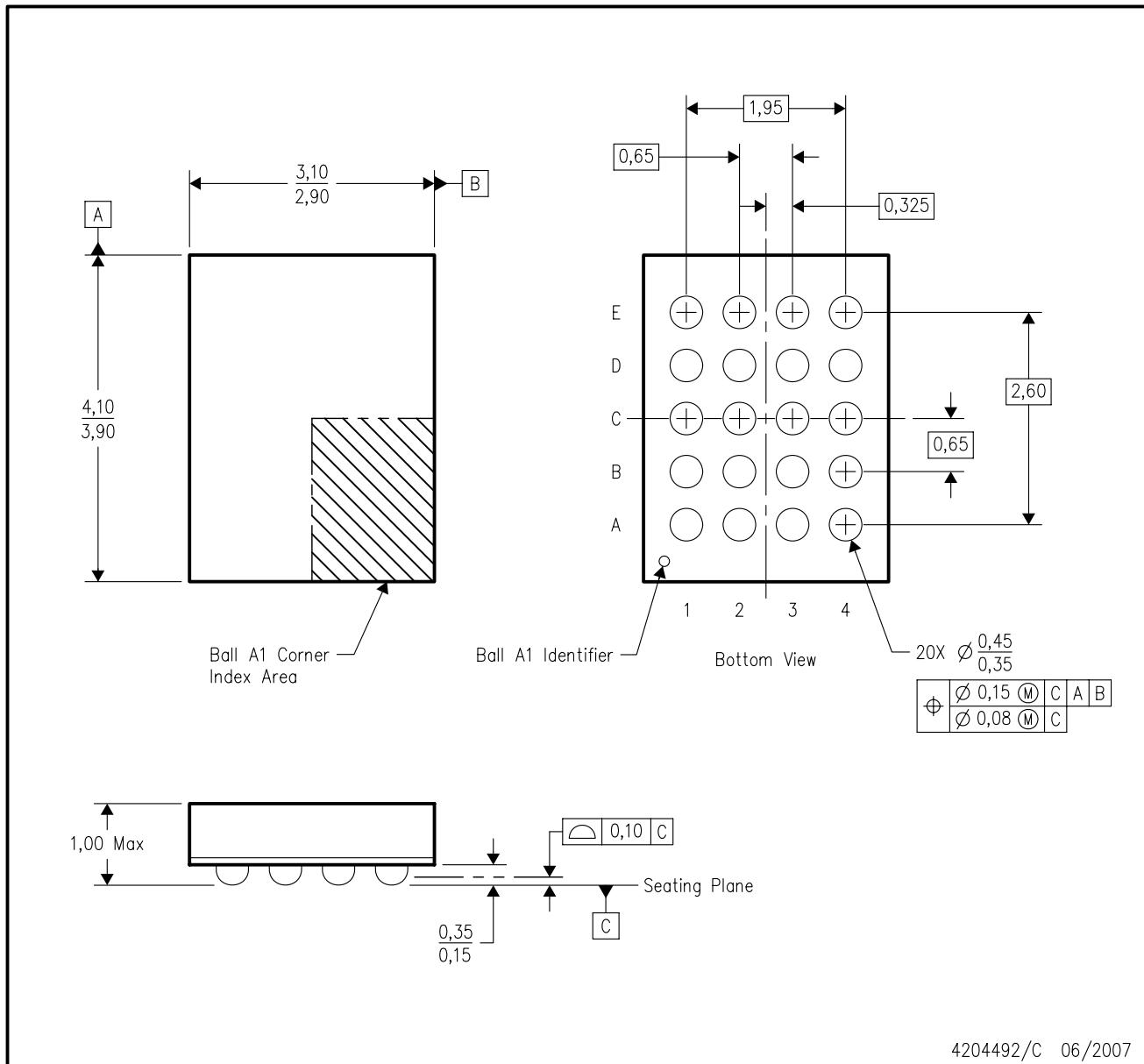
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV273ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LV273ADGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74LV273ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LV273ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LV273APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74LV273ARGYR	VQFN	RGY	20	3000	190.5	212.7	31.8
SN74LV273AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	346.0	346.0	29.0
SN74LV273AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	340.5	338.1	20.6

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



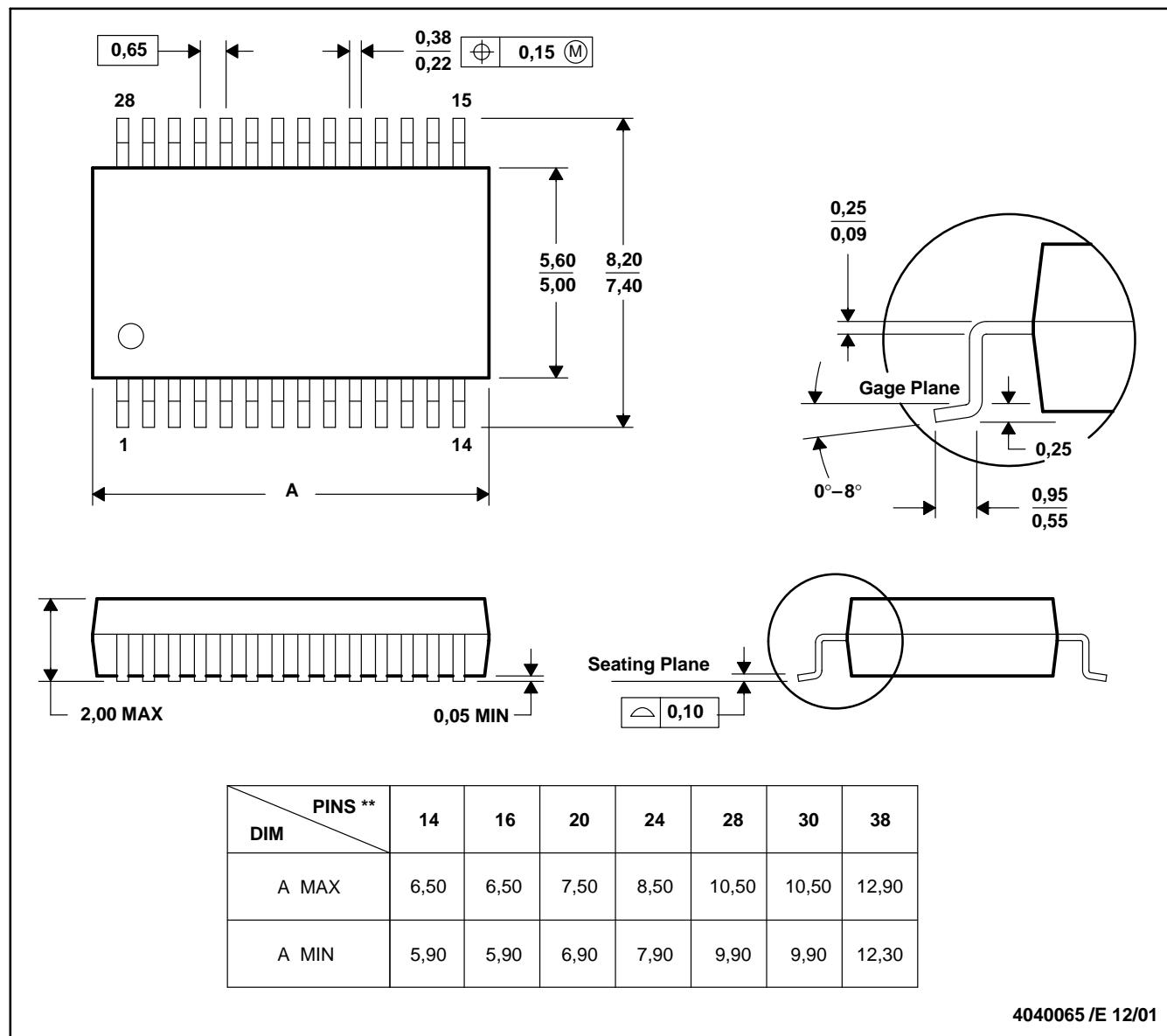
4204492/C 06/2007

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Falls within JEDEC MO-285 variation BC-2.
 - This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

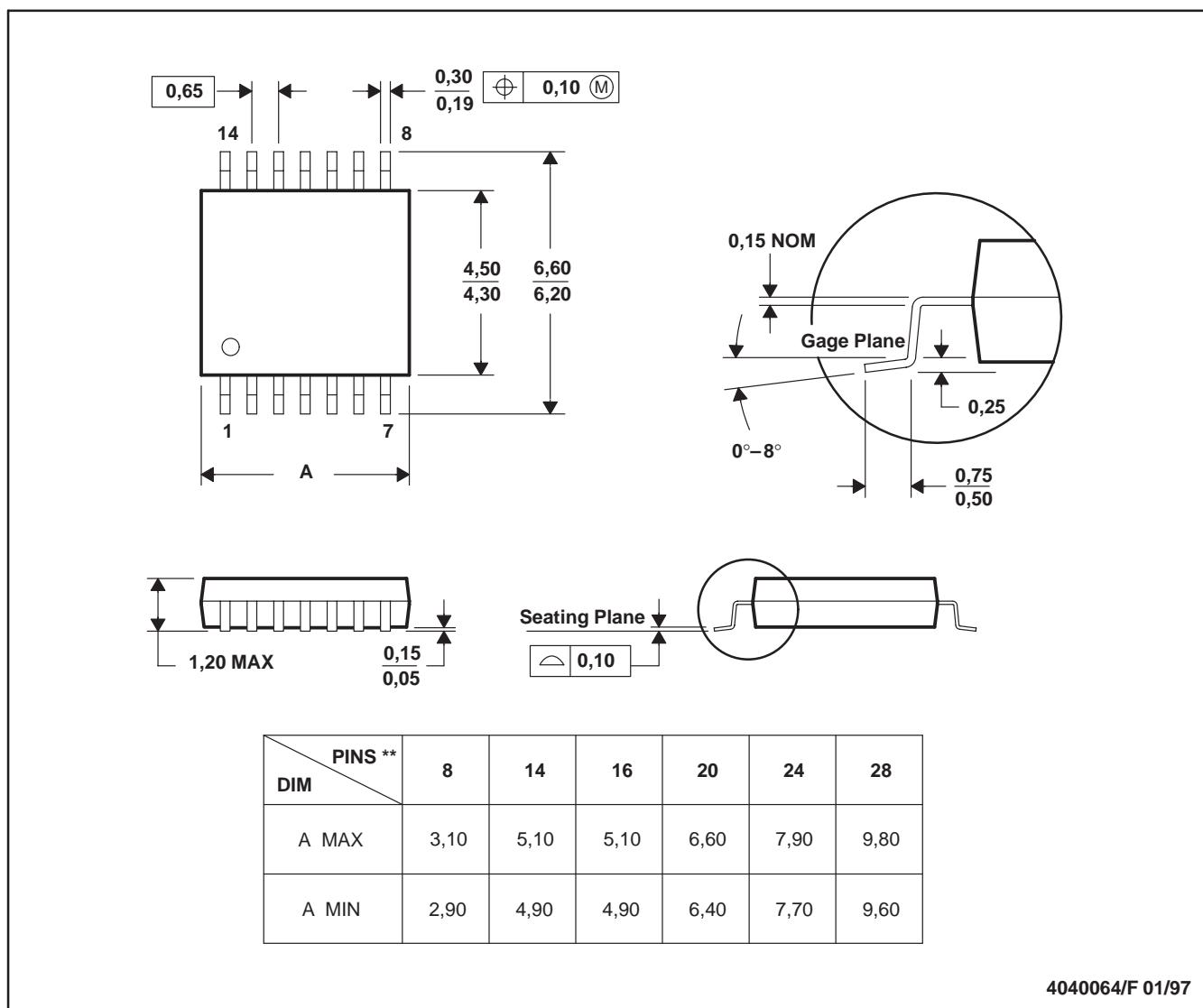


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



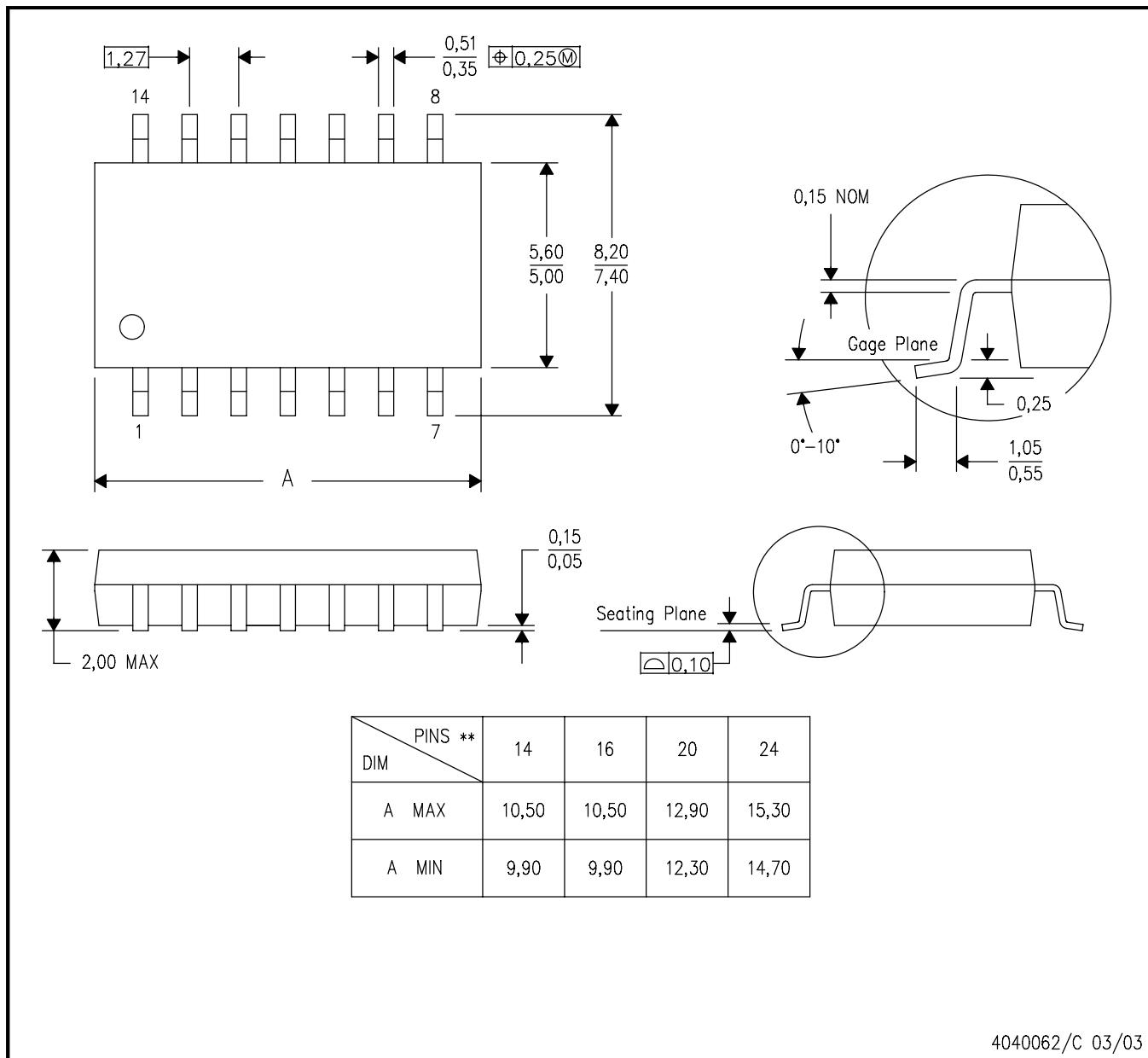
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



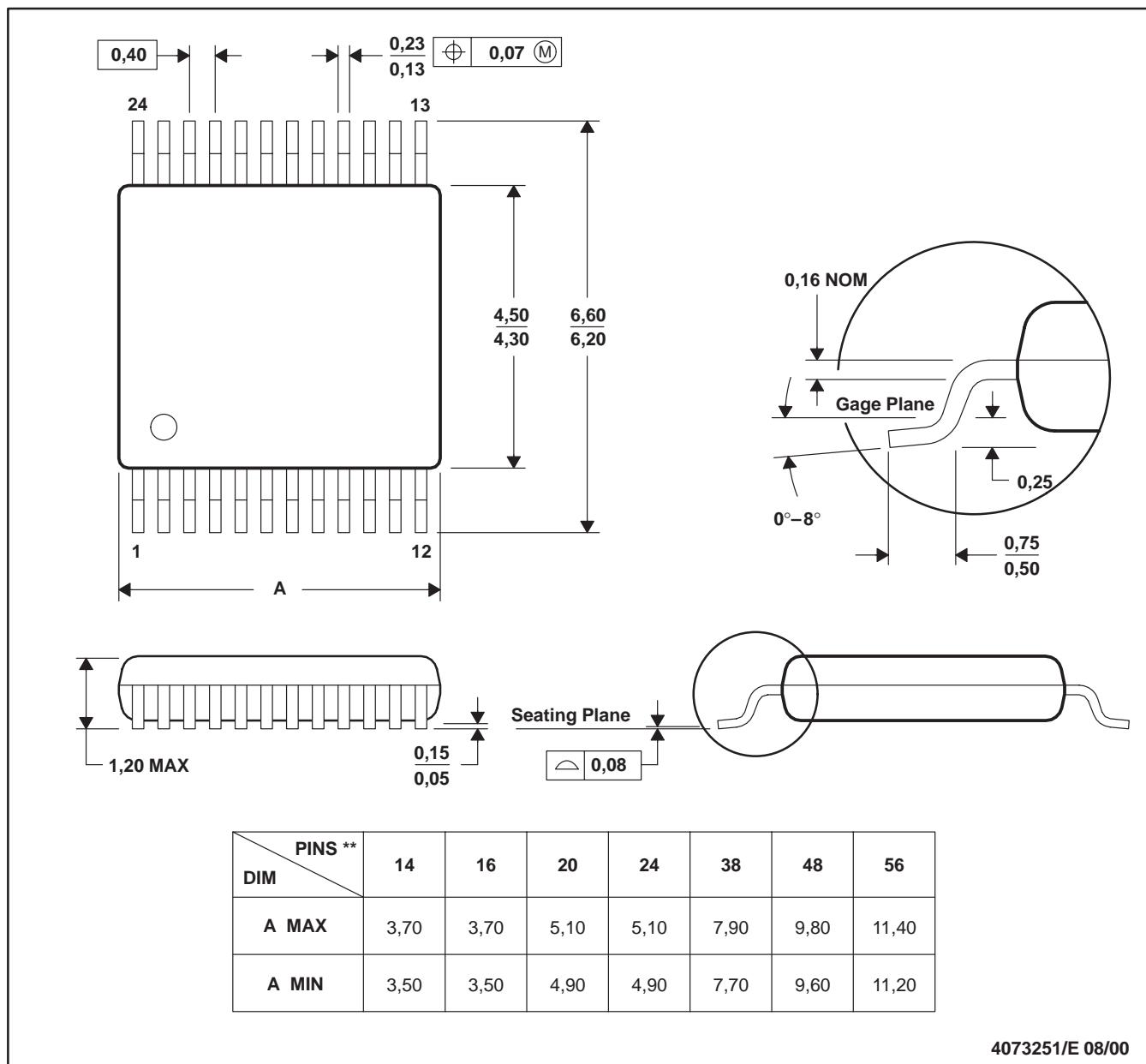
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

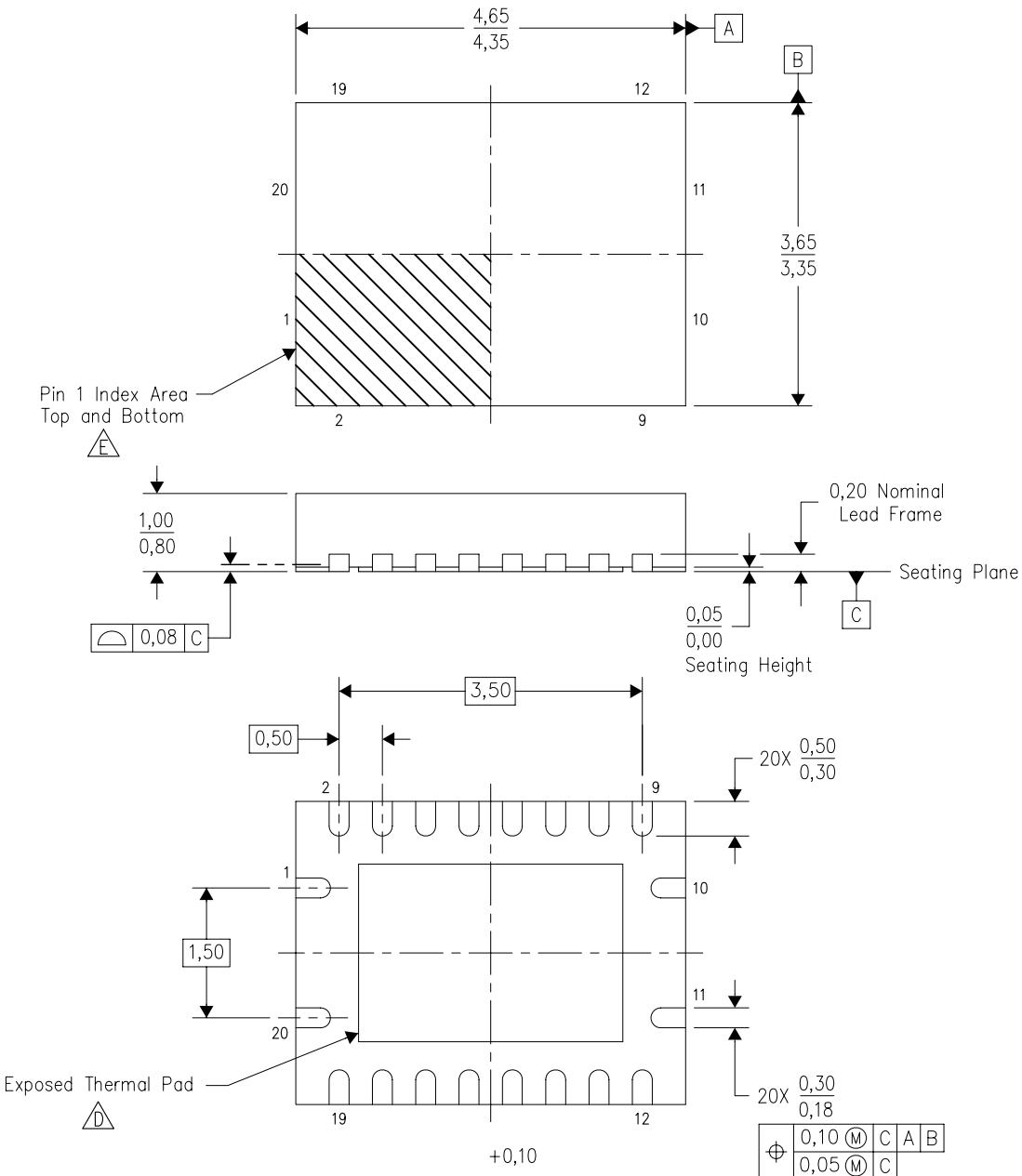
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-4/H 06/2009

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

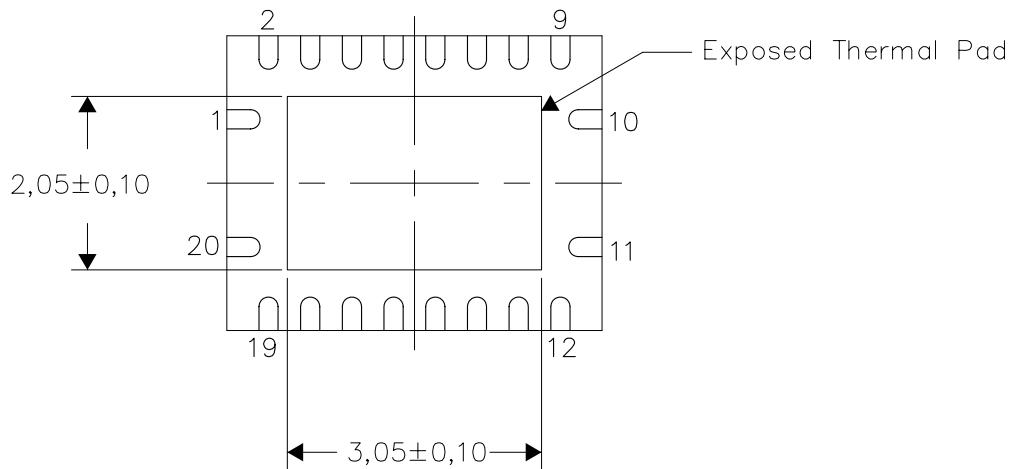
F. Package complies to JEDEC MO-241 variation BC.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

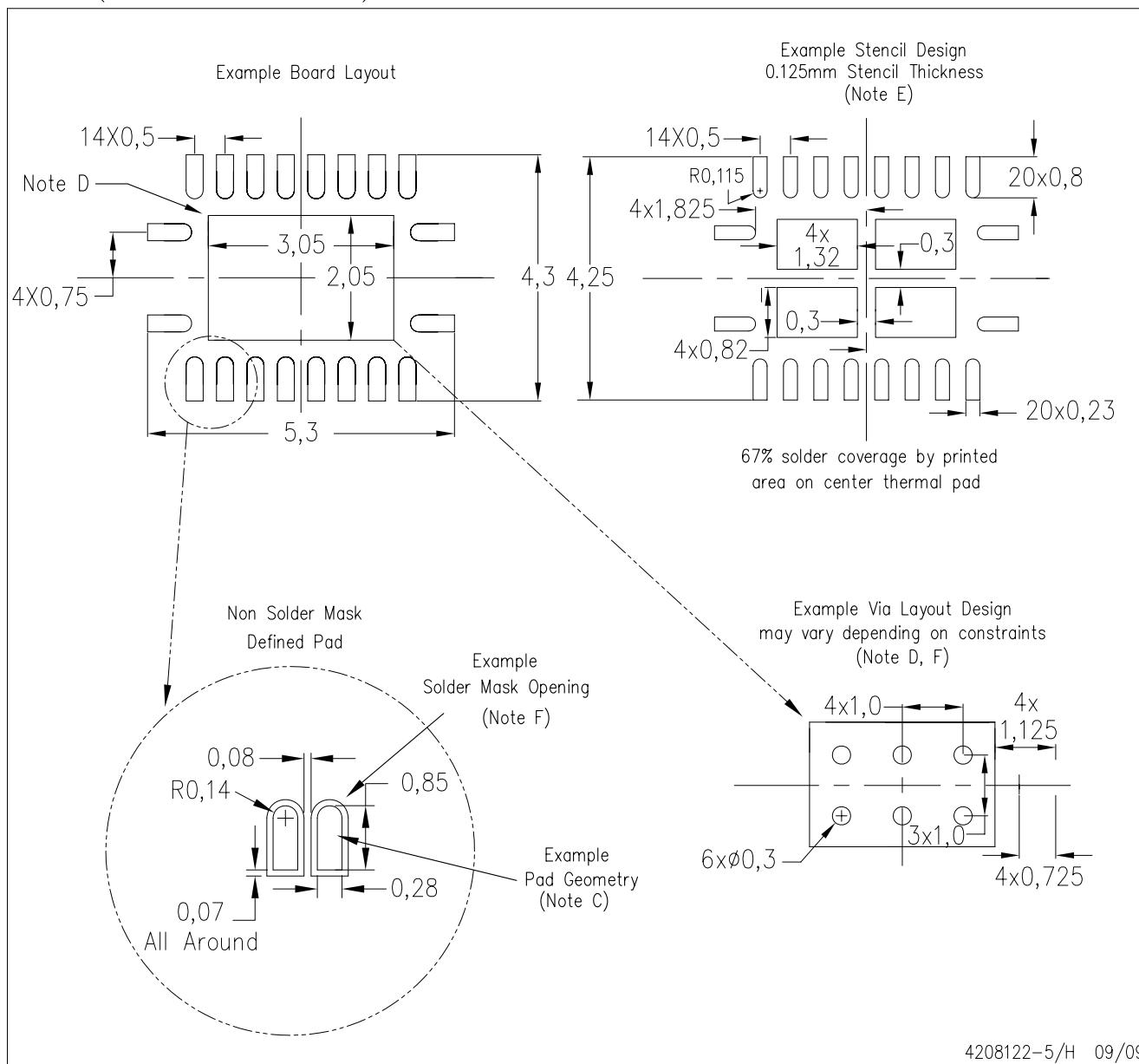


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

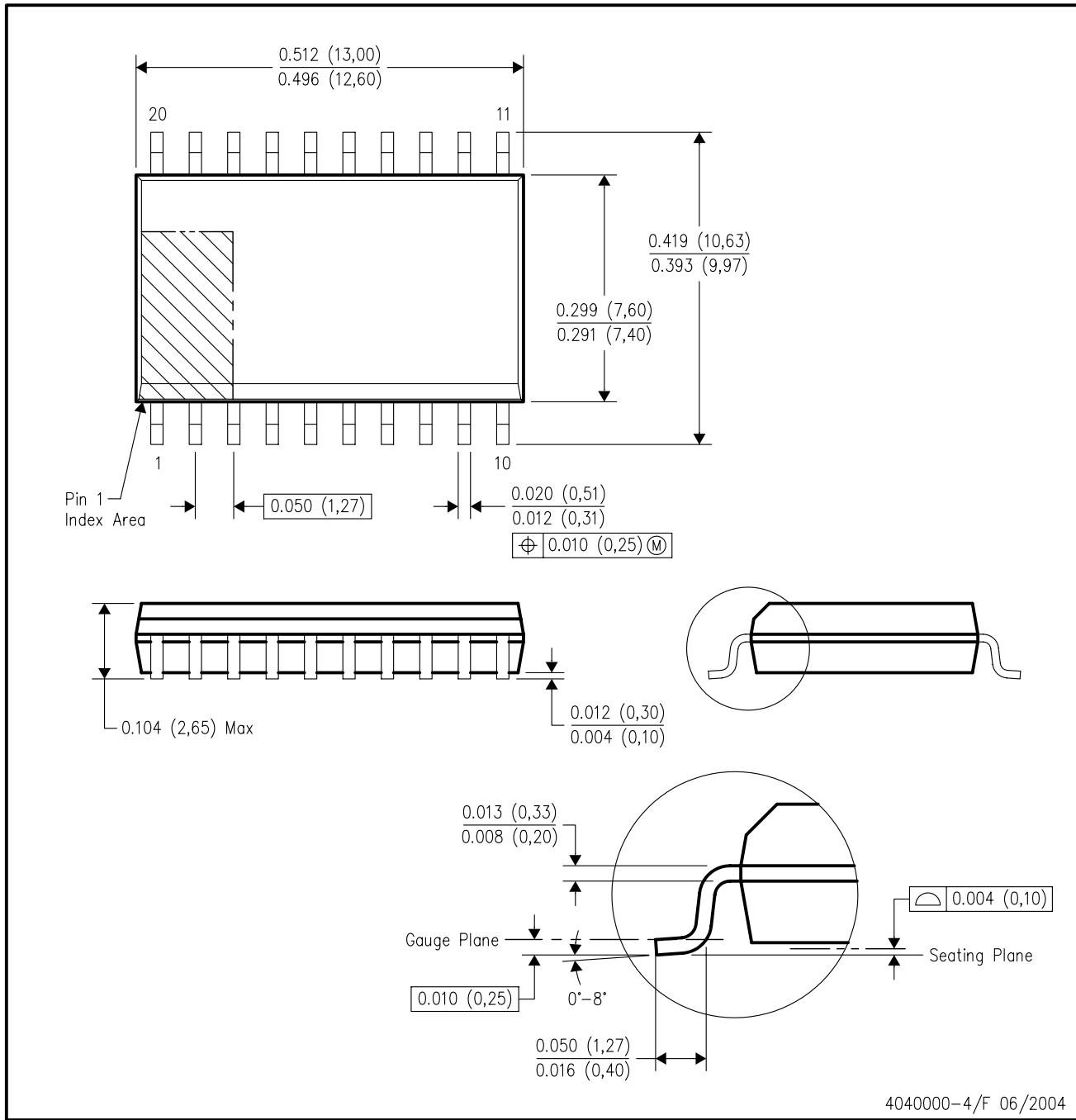
RGY (R-PVQFN-N20)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

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