

# Factory Programmable Quad PLL Clock Generator with VCXO

## Features

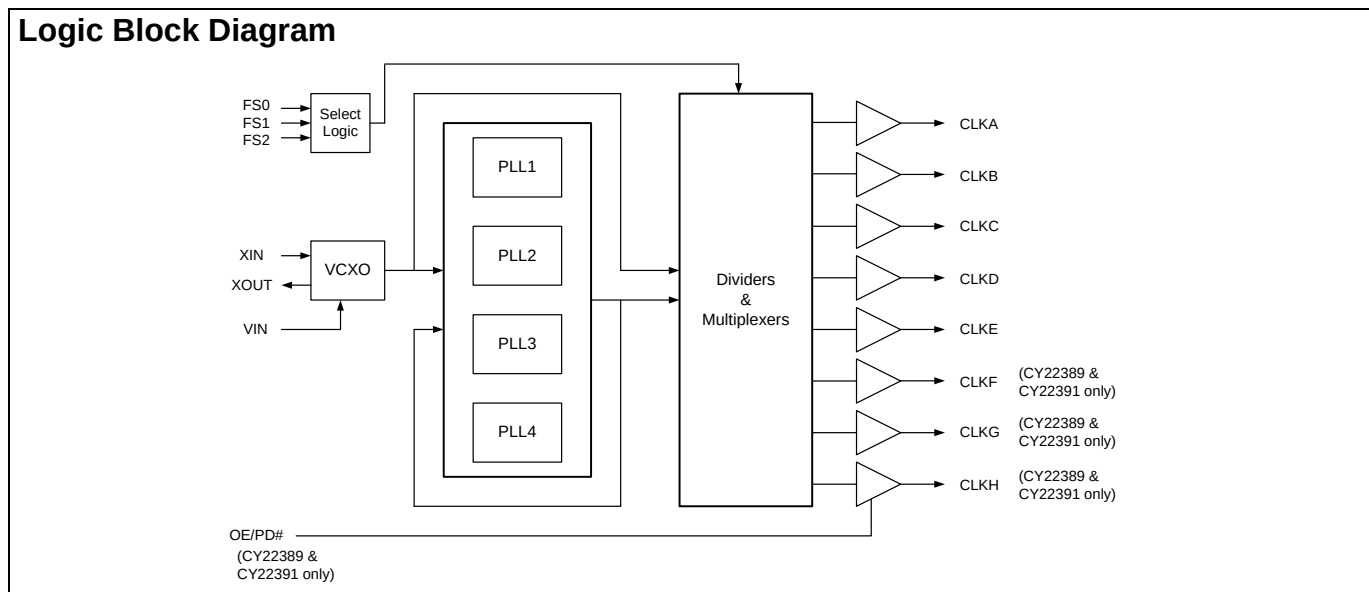
- Fully integrated phase-locked loops (PLLs)
- QFN package
- 40% smaller than 20-pin TSSOP
- 22% smaller than 16-pin TSSOP
- Selectable Output Frequency
- Programmable Output Frequencies
- Output Frequency Range of 5–166 MHz
- Input Frequency Range
- Crystal: 10–30 MHz
- External Reference: 1–100 MHz
- Analog VCXO

- 16-/20-pin TSSOP and 32-pin QFN packages
- 3.3V operation with 2.5V output buffer option

## Benefits

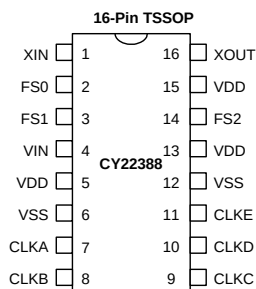
- Meets most Digital Set Top Box, DVD Recorder, and DTV application requirements
- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Integration eliminates the need for external loop filter components
- Meets critical timing requirements in complex system designs
- Enables application compatibility
- Complete VCXO solution with  $\pm 120$  ppm (typical pull range)

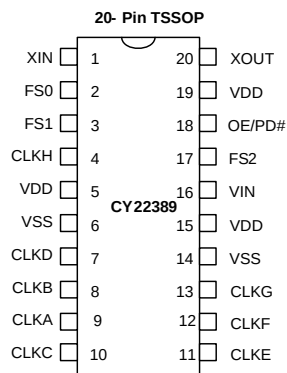
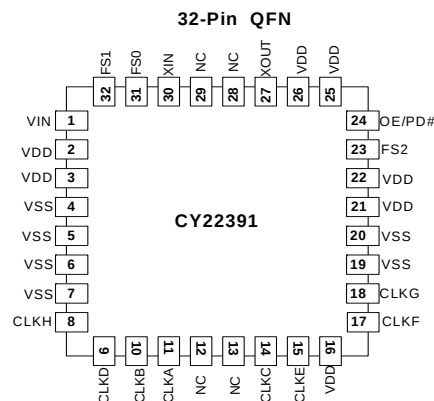
## Logic Block Diagram



## Pinouts

**Figure 1. Pin Diagram - 16-Pin TSSOP CY22388**



**Figure 2. Pin Diagram - 20-Pin TSSOP CY22389**

**Figure 3. Pin Diagram - 32-Pin TSSOP CY22391**


## Pin Definitions

| Pin Name | Pin Number   |              |                    | Pin Description                                                                  |
|----------|--------------|--------------|--------------------|----------------------------------------------------------------------------------|
|          | 16-Pin TSSOP | 20-Pin TSSOP | 32-Pin QFN         |                                                                                  |
| XIN      | 1            | 1            | 30                 | Crystal Input or Reference Clock Input                                           |
| XOUT     | 16           | 20           | 27                 | Crystal Output (No connect if external clock is used)                            |
| CLKA     | 7            | 9            | 11                 | Clock Output                                                                     |
| CLKB     | 8            | 8            | 10                 | Clock Output                                                                     |
| CLKC     | 9            | 10           | 14                 | Clock Output                                                                     |
| CLKD     | 10           | 7            | 9                  | Clock Output                                                                     |
| CLKE     | 11           | 11           | 15                 | Clock Output                                                                     |
| CLKF     | n/a          | 12           | 17                 | Clock Output                                                                     |
| CLKG     | n/a          | 13           | 18                 | Clock Output                                                                     |
| CLKH     | n/a          | 4            | 8                  | Clock Output                                                                     |
| FS0      | 2            | 2            | 31                 | Frequency Select 0                                                               |
| FS1      | 3            | 3            | 32                 | Frequency Select 1                                                               |
| FS2      | 14           | 17           | 23                 | Frequency Select 2                                                               |
| OE/PD#   | n/a          | 18           | 24                 | Programmable control pin: Output Enable (active-high) or Power Down (active-low) |
| VIN      | 4            | 16           | 1                  | Analog Control Input for VCXO                                                    |
| VDD      | 5,13,15      | 5,15,19      | 2,3,16,21,22,25,26 | Voltage Supply                                                                   |
| VSS      | 6,12         | 6,14         | 4,5,6,7,19,20      | Ground                                                                           |
| NC       | n/a          | n/a          | 12,13,28,29        | No Connect.                                                                      |

## General Description

The CY22388 family of devices has an Analog VCXO (Voltage Controlled Crystal Oscillator), 4 PLLs, up to 8 clock outputs and frequency selection capabilities. The frequency selects do not modify any PLL frequency. Instead they allow the user to choose between up to 8 different output divider selections depending on the clock and package configuration. This is illustrated in the following Frequency Selection tables and Functional Block Diagram.

There is one programmable OE/PD#. The OE/PD# pin can be programmed as either an output enable pin or a power down pin. The OE function can be programmed to disable a selected set of outputs when low, leaving the remaining outputs running. Full-chip power down disable all outputs and the PLLs and most of the active circuitry when low.

### Factory-Programmable CY22388/89/91

Factory programming is available for high- or low-volume manufacturing by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. Once the request has been processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

## PLLs

The advantage of having four PLLs is that a single device can generate up to four independent frequencies from a single crystal. Generally a design may require up to four oscillators to accomplish what could be done with a single CY22388.

Each PLL is independent and can be configured to generate a VCO (Voltage Controlled Oscillator) frequency between 62.5 MHz and 250 MHz. Each PLL can then in turn be divided down with post dividers to generate the clock output frequency of the user's choice. The output divider allows each clock output to be divided by 1, 2, 3, 4, 5, 6, 8, 9, 10, 12 or 15. The PLL maximum is reduced to 166 MHz in divide by 1 mode due to output buffer limitations.

Outputs that allow frequency switching perform the transition free of glitches. A glitch is defined as a high or low time shorter than half the smaller of the two periods being switched between. Extended low time (even many cycles in duration) is acceptable.

Selected clock outputs are capable of being powered off a separate 2.5V supply. This allows for driving lower voltage swing inputs. The CY22388/89/91 device still requires 3.3V to power the oscillator and all other internal PLL circuitry. For the 2.5V output option please refer to the CY22388 Application Note. Selected clocks and pinout diagrams are explained in this application note.

Clock D can obtain its output from either the reference source or PLL1/N1 with N1 being defined as the output divider for PLL1. Clock H is defined as a copy of clock D. Clock D is only available from PLL1/N1 on the 16-pin package.

For CY22388, CLKB and CLKC have related frequencies. For CY22389 and CY22391, CLKD and CLKF have related frequencies, CLKA and CLKB have related frequencies, and CLKC and CLKE have related frequencies. Related frequencies come from the same PLL but can have different divider values.

In order to minimize PPM (Parts Per Million) error on the clock outputs, a user must choose a crystal reference frequency that is a common multiple of the desired PLL frequencies. While this would be the ideal situation, this is not always the case and the PLLs have high-resolution counters internally to help minimize frequency deviation from the desired frequency.

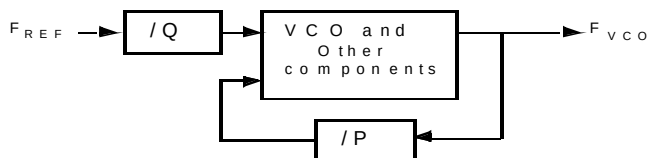
PLL VCO frequencies are generated by the following equation:  

$$F_{VCO} = F_{REF} * (P / Q)$$

Where  $F_{REF}$  is the reference input frequency, P is the PLL feedback divider and Q is the reference input divider.

A PLL is a feedback system where the VCO frequency divided by P and reference frequency divided by Q are constantly being compared and the VCO frequency is adjusted to achieve a locked state. Figure 3 is a simplified drawing of a PLL.

**Figure 3. PLL system**



## Frequency Select Pin Operation

**Table 1. CY22388 16-pin TSSOP**

| Output Signal | Frequency Selection Lines |
|---------------|---------------------------|
| CLK A         | FS2, FS1, FS0             |
| CLK B         | FS1, FS0                  |
| CLK C & CLK D | S0                        |
| CLK E         | FIXED                     |

**Table 2. CY22389 20-pin TSSOP**

| Output Signal         | Frequency Selection Lines |
|-----------------------|---------------------------|
| CLK A                 | FS2, FS1, FS0             |
| CLK B & CLK C         | FS1, FS0                  |
| CLK D, CLK E, & CLK F | FS0                       |
| CLK G                 | FIXED                     |
| CLK H                 | COPY OF CLK D             |

**Table 3. CY22391 32-pin QFN**

| Output Signal         | Frequency Selection Lines |
|-----------------------|---------------------------|
| CLK A                 | FS2, FS1, FS0             |
| CLK B & CLK C         | FS1, FS0                  |
| CLK D, CLK E, & CLK F | FS0                       |
| CLK G                 | FIXED                     |
| CLK H                 | COPY OF CLK D             |

## Analog VCXO

There are three programmable reference operating modes for the CY22388, CY22389, CY22391 family of devices. The first mode utilizes an external pullable crystal and incorporates an internal Analog VCXO.

The second mode configures the internal crystal oscillator to accept an external driven reference source from 1 to 100 MHz. The input capacitance on the XIN PIN when driven in this mode is 15 pF.

The third mode disables the VCXO input control and sets the internal oscillator to a fixed frequency operation. The load capacitance seen by the external crystal when connected to PINS XIN and XOUT is equal to 12 pF.

One of the key components to the CY22388, CY22389, CY22391 family of devices is the analog VCXO. The VCXO is used to “pull” the reference crystal higher or lower in order to lock the system frequency to an external source. This is ideal for applications where the output frequency needs to track along with an external reference frequency that is constantly shifting.

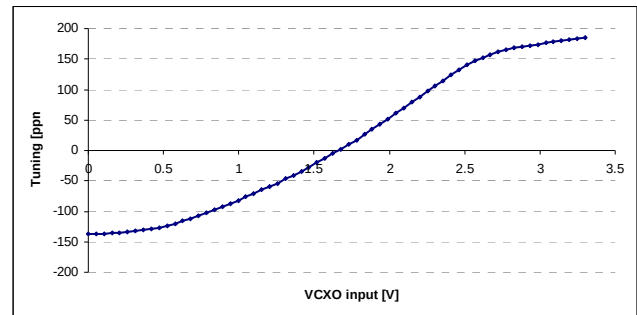
The VCXO is completely analog, so there is infinite resolution on the VCXO pull curve. The Analog to Digital Converter steps that are normally associated with a digital VCXO input is not present in this device. A special pullable crystal must be used in order to have adequate VCXO pull range. Pullable Crystal specifications are included in this data sheet.

Please refer to the CY22388, CY22389, CY22391 Application Note for pullable crystal recommendations outside of the standard industry frequencies given in the Pullable Crystal Specifications.

## VCXO Profile

Figure 4 shows an example of what a VCXO profile looks like. The analog voltage input is on the X-axis and the PPM range is on the Y-axis. An increase in the VCXO input voltage results in a corresponding increase in the output frequency. This has the effect of moving the PPM from a negative to positive offset.

Figure 4. VCXO Profile



## Absolute Maximum Conditions

| Parameter                | Description                       | Condition                | Min  | Max            | Unit  |
|--------------------------|-----------------------------------|--------------------------|------|----------------|-------|
| $V_{DD}/AV_{DD}/V_{DDL}$ | Core Supply Voltage               |                          | -0.5 | 4.6            | V     |
| $V_{IN}$                 | Input Voltage                     | Relative to $V_{SS}$     | -0.5 | $V_{DD} + 0.5$ | VDC   |
| $T_S$                    | Temperature, Storage              | Non-Functional           | -65  | +125           | °C    |
| $ESD_{HBM}$              | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | –              | Volts |
| UL-94                    | Flammability Rating               | V-0 at 1/8 in.           | –    | 10             | ppm   |
| MSL                      | Moisture Sensitivity Level        | QFN package              | 3    |                |       |
|                          |                                   | 16- and 20-pin TSSOP     | 1    |                |       |

## Pullable Crystal Specifications<sup>[1, 3]</sup>

| Parameter   | Description                        | Comments                                              | Min        | Typ. | Max  | Unit     |
|-------------|------------------------------------|-------------------------------------------------------|------------|------|------|----------|
| $F_{NOM}$   | 13.5 MHz and 27 MHz Crystal AT-Cut | Parallel resonance, Fundamental mode                  | See Note 3 |      |      |          |
| $C_{LNOM}$  | Nominal Load Capacitance           | Order crystal at one specific $C_{LNOM}$<br>0 ppm     | 11.4       | 12   | 12.6 | pF       |
| $R_1$       | Equivalent Series Resistance (ESR) | Fundamental mode (CL = Series)                        | –          | –    | 40   | $\Omega$ |
| DL          | Crystal Drive Level                | Nominal $V_{DD}$ at 25C over $\pm 120$ PPM Pull Range | –          | –    | 300  | $\mu W$  |
| $C_0^{[2]}$ | Crystal Shunt Capacitance          |                                                       | 1.5        | 3    | 4.0  | pF       |

### Notes

- Device operates to the following specs, which are guaranteed by design.
- Increased tolerance available from pull range less than  $\pm 120$  PPM.
- Refer to CY22388 Application Note and online software for a list of Approved Crystal Specifications.

## Pullable Crystal Specifications<sup>[1, 3]</sup>

| Parameter          | Description                                      | Comments                                           | Min | Typ. | Max  | Unit |
|--------------------|--------------------------------------------------|----------------------------------------------------|-----|------|------|------|
| $C_1^{[2]}$        | Crystal Motional Capacitance                     |                                                    | 12  | 14   | 16.8 | fF   |
| $F_{3SEPHI}^{[3]}$ | Third Overtone Separation from $3 \cdot F_{NOM}$ | Mechanical Third (High side of $3 \cdot F_{NOM}$ ) | 240 | –    | –    | ppm  |
| $F_{3SEPLO}^{[3]}$ | Third Overtone Separation from $3 \cdot F_{NOM}$ | Mechanical Third (Low side of $3 \cdot F_{NOM}$ )  | –   | –    | –120 | ppm  |

## Recommended Operating Conditions

| Parameter                | Description                                                                                      | Min  | Typ. | Max | Unit |
|--------------------------|--------------------------------------------------------------------------------------------------|------|------|-----|------|
| $V_{DD}/AV_{DD}/V_{DDL}$ | Operating Voltage                                                                                | 3.0  | 3.3  | 3.6 | V    |
| $T_A$                    | Ambient Temperature                                                                              | –10  | –    | 70  | °C   |
| $C_{LOAD}$               | Maximum Load Capacitance                                                                         | –    | –    | 15  | pF   |
| $t_{PU}$                 | Power up time for all $V_{DD}$ s reach minimum specified voltage (power ramps must be monotonic) | 0.05 | –    | 500 | ms   |

## DC Parameters<sup>[4]</sup>

| Parameter      | Description                  | Conditions                                | Min                  | Typ. | Max                  | Unit |
|----------------|------------------------------|-------------------------------------------|----------------------|------|----------------------|------|
| $I_{OH}^{[5]}$ | Output High Current          | $V_{OH} = V_{DD} - 0.5$ , $V_{DD} = 3.3V$ | 12                   | –    | –                    | mA   |
| $I_{OL}^{[5]}$ | Output Low Current           | $V_{OL} = 0.5$ , $V_{DD} = 3.3V$          | 12                   | –    | –                    | mA   |
| $I_{IH}$       | Input High Current           | $V_{IH} = V_{DD}$ , excluding Vin, Xin    | –                    | 5    | 10                   | μA   |
| $I_{IL}$       | Input Low Current            | $V_{IL} = 0V$ , excluding Vin, Xin        | –                    | 5    | 10                   | μA   |
| $V_{IH}$       | Input High Voltage           | FS0/1/2 OE input CMOS levels              | $0.7 \times A_{VDD}$ | –    | –                    | V    |
| $V_{IL}$       | Input Low Voltage            | FS0/1/2 OE input CMOS levels              | –                    | –    | $0.3 \times A_{VDD}$ | V    |
| Parameter      | Description                  | Conditions                                | Min                  | Typ. | Max                  | Unit |
| $V_{VCXO}$     | VIN Input Range              |                                           | 0                    | –    | $A_{VDD}$            | V    |
| $C_{IN}$       | Input Capacitance            | FS0/1/2 and OE Pins only                  | –                    | –    | 7                    | pF   |
| $I_{VDD}$      | Supply Current               | $V_{DD}/AV_{DD}/V_{DDL}$ Current          | –                    | 60   | –                    | mA   |
| $C_{INXIN}$    | Input Capacitance at XIN     | VCXO Disabled External Reference          | –                    | 15   | –                    | pF   |
| $C_{INXTAL}$   | Input Capacitance at Crystal | VCXO Disabled Fixed Freq. Oscillator      | –                    | 12   | –                    | pF   |

## AC Parameters

| Parameter <sup>[4]</sup> | Description                          | Conditions                                                                                                                                                                  | Min | Typ. | Max | Units |
|--------------------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|-------|
| $1/t_1$                  | Output Frequency                     | PLL <sub>minmax</sub> /Divider <sub>maximum</sub>                                                                                                                           | 4.2 | –    | 166 | MHz   |
| DC1                      | Output Duty Cycle (excluding REFOUT) | Duty Cycle is defined in Figure 6; $t_2/t_1$ , 50% of $V_{DD}$<br>External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is $\leq 125$ MHz) | 45  | 50   | 55  | %     |
| DC2                      | Output Duty Cycle                    | Duty Cycle is defined in Figure 6; $t_2/t_1$ , 50% of $V_{DD}$<br>External reference duty cycle between 40% and 60% measured at $V_{DD}/2$ (Clock output is $> 125$ MHz)    | 40  | 50   | 60  | %     |
| DC <sub>REFOUT</sub>     | Output Duty Cycle                    | Duty Cycle is defined in Figure 6; $t_2/t_1$ , 50% of $V_{DD}$<br>(XIN Duty Cycle = 45/55%)                                                                                 | 40  | 50   | 60  | %     |

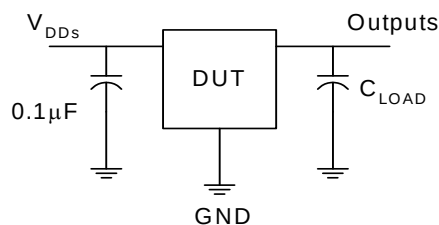
### Notes

- Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.
- Custom Drive level and is available upon request

## AC Parameters (continued)

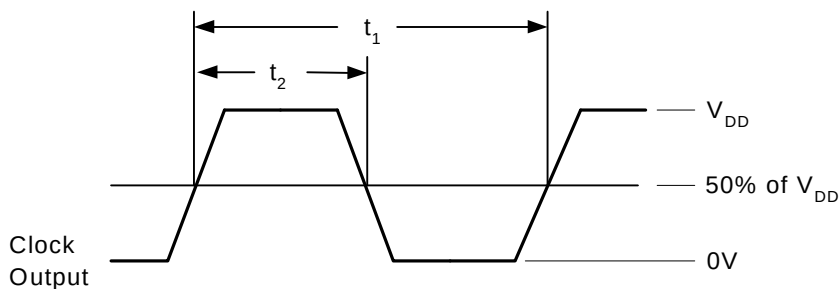
| Parameter <sup>[4]</sup> | Description             | Conditions                                                                                                                                    | Min       | Typ.      | Max | Units |
|--------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----------|-----|-------|
| ER                       | Rising Edge Rate        | Output Clock Edge Rate. Measured from 20% to 80% of $V_{DD}$ . $C_{LOAD} = 15$ pF. See Figure 7.                                              | 0.75      | 1.2       | –   | V/ns  |
| EF                       | Falling Edge Rate       | Output Clock Edge Rate. Measured from 80% to 20% of $V_{DD}$ . $C_{LOAD} = 15$ pF. See Figure 7.                                              | 0.75      | 1.2       | –   | V/ns  |
| $T_9$                    | Clock Jitter            | Period Jitter                                                                                                                                 | –         | $\pm 250$ | –   | ps    |
| $T_{10}$                 | PLL Lock Time           |                                                                                                                                               | –         | 1         | 5   | ms    |
| $f_{\Delta XO}$          | VCXO Crystal Pull Range | Using non-SMD-49 crystal specified in “CY22388 Application Note, ANC0002”<br>Nominal Crystal Frequency Input assumed (0 ppm) at 25°C and 3.3V | $\pm 110$ | $\pm 120$ | –   | ppm   |
|                          |                         | Using SMD-49 crystal specified in “CY22388 Application Note, ANC0002”<br>Nominal Crystal Frequency Input assumed (0 ppm) at 25°C and 3.3V     | $\pm 105$ | $\pm 120$ | –   | ppm   |

**Figure 5. Test and Measurement**

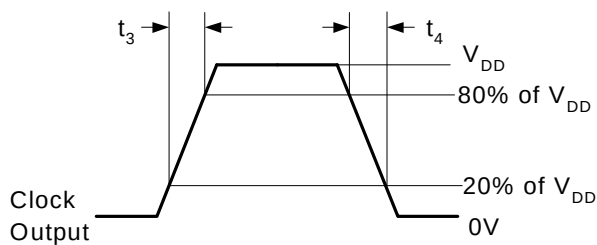


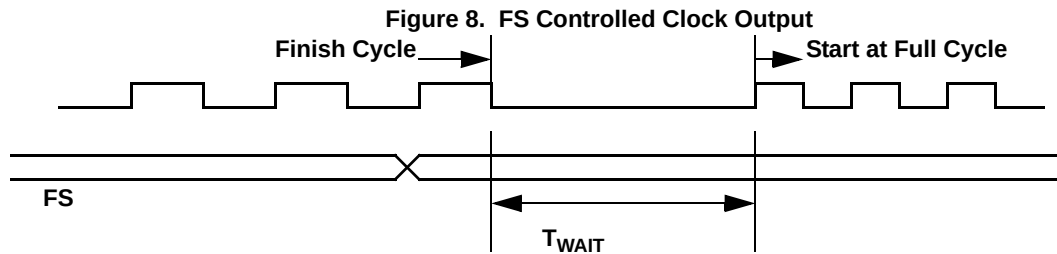
## Voltage and Timing Definitions

**Figure 6. Duty Cycle Definition**



**Figure 7.  $ER = (0.6 \times V_{DD})/t_3$ ,  $EF = (0.6 \times V_{DD})/t_4$**



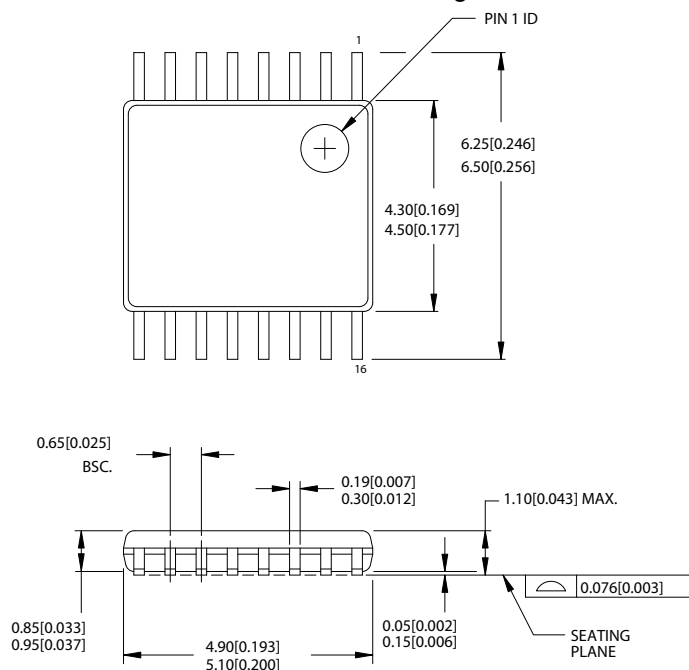


## Ordering Information

| Part Number <sup>[6]</sup>      | Package | Type                               | Production Flow          |
|---------------------------------|---------|------------------------------------|--------------------------|
| <b>Pb-free</b>                  |         |                                    |                          |
| CY22388ZXC-xxx                  | ZZ16    | 16-pin TSSOP                       | Commercial, 0°C to +70°C |
| CY22388ZXC-xxxT                 | ZZ16    | 16-pin TSSOP - Tape and Reel       | Commercial, 0°C to +70°C |
| CY22389ZXC-xxx                  | ZZ20    | 20-pin TSSOP                       | Commercial, 0°C to +70°C |
| CY22389ZXC-xxxT                 | ZZ20    | 20-pin TSSOP - Tape and Reel       | Commercial, 0°C to +70°C |
| CY22391LFXC-xxx <sup>[7]</sup>  | LY32    | 32-pin QFN (Punch)                 | Commercial, 0°C to +70°C |
| CY22391LFXC-xxxT <sup>[7]</sup> | LY32    | 32-pin QFN (Punch) - Tape and Reel | Commercial, 0°C to +70°C |
| CY22391LTXC-xxx                 | LT32    | 32-pin QFN (Saw)                   | Commercial, 0°C to +70°C |
| CY22391LTXC-xxxT                | LT32    | 32-pin QFN (Saw) - Tape and Reel   | Commercial, 0°C to +70°C |

## Package Drawing and Dimensions

**Figure 9. 16-Pin TSSOP 4.40 mm Body ZZ16**

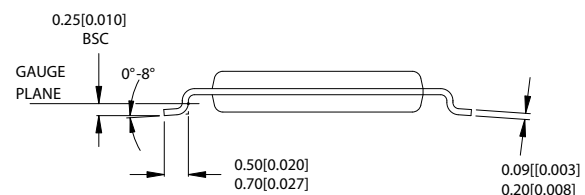


DIMENSIONS IN MM[INCHES] MIN.  
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

| PART #   |                |
|----------|----------------|
| Z16.173  | STANDARD PKG.  |
| ZZ16.173 | LEAD FREE PKG. |

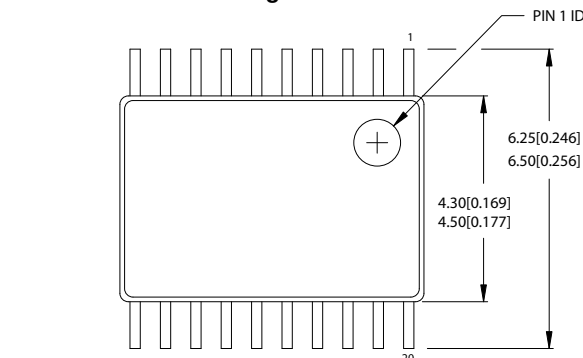


51-85091-A

### Note

- The CY22388ZXC-xxx, CY22389ZXC-xxx, and CY22391LFXC-xxx are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative.
- Not recommended for new designs. The LY32 QFN package transitions to the LT32 QFN.

**Figure 10. 20-Pin Thin Shrunk Small Outline Package (4.40-mm Body) ZZ20**

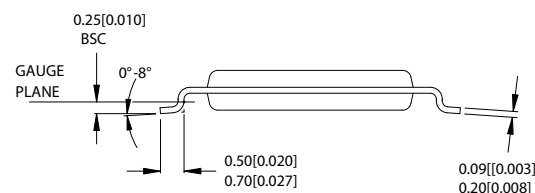
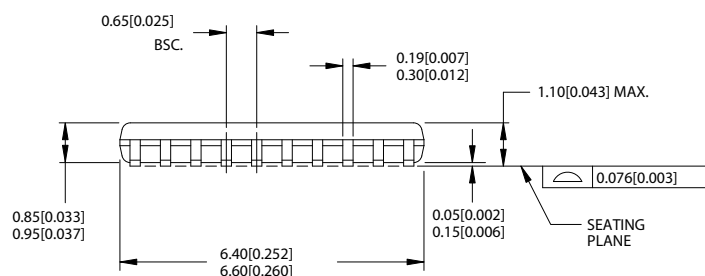


DIMENSIONS IN MM[INCHES] MIN.

MAX.

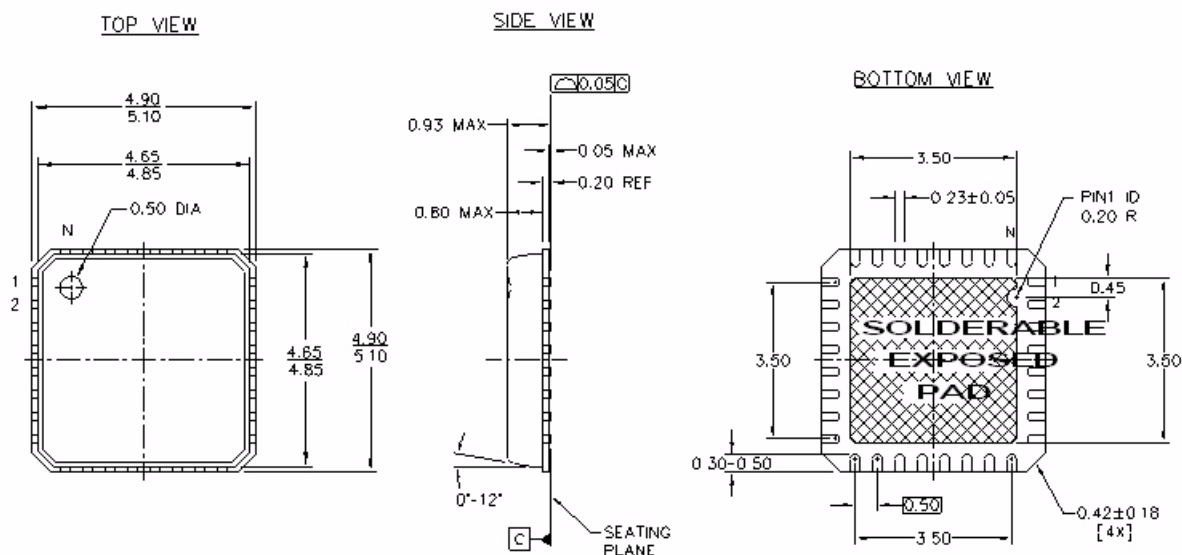
REFERENCE JEDEC MO-153

| PART #                  |
|-------------------------|
| Z20.173 STANDARD PKG.   |
| ZZ20.173 LEAD FREE PKG. |



51-85118-\*A

**Figure 11. 32-Pin Punch QFN (5 x 5 mm) LY32**



**NOTES:**

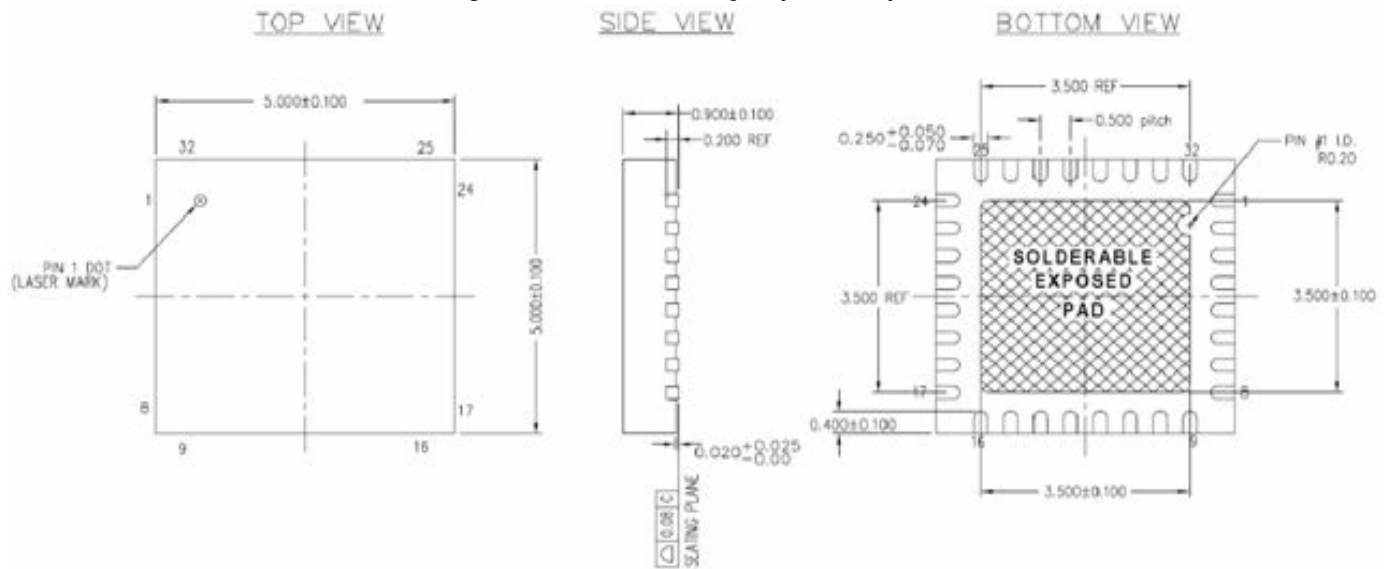
-  HATCH AREA IS SOLDERABLE EXPOSED PAD.
- REFERENCE JEDEC#: MO-220
- PACKAGE WEIGHT: 0.054g
- ALL DIMENSIONS ARE IN MM [MIN/MAX]
- PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF32   | STANDARD    |
| LY32   | PB-FREE     |

51-85188-\*B



**Figure 12. 32-Pin Sawn QFN (5 x 5 mm) LT32**



**NOTES:**

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. PACKAGE WEIGHT: 0.058g
4. DIMENSIONS ARE IN MILLIMETERS

001-30999 \*A

## Document History Page

| Document Title: CY22388, CY22389, CY22391 Factory Programmable Quad PLL Clock Generator with VCXO<br>Document Number: 38-07734 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                                                           | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| **                                                                                                                             | 320458  | RGL             | 03/07/05        | New data sheet Internal setting in VCXO are:XOB/A=110, Offset=1110, Gain=101                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *A                                                                                                                             | 389649  | RGL             | 08/02/05        | Changed R1 value to max. 40Ω<br>Changed DL comments and max. value to 300μW<br>Changed f <sub>ΔXO</sub> min. value to ±110ppm and typ. value to ±120ppm                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| *B                                                                                                                             | 523597  | RGL             | 11/12/06        | Specified a non-SMD-49 and SMD-49 crystal specs in the VCXO Pull Range Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| *C                                                                                                                             | 2632357 | KVM             | 01/13/09        | Updated template.<br>Updated Ordering Information table to add tape & reel part numbers.<br>Added LT32 (saw) QFN package for CY22391, including package drawing.<br>LY32 (punch) QFN package "not recommended for new designs"<br>Added Package column to Ordering Information table and cleaned up package references in captions of the package drawings.<br>Changed document title to spell out each part number in full.<br>Clarified that Power Down (PD#) is active-low: in block diagram, CY22389 pinout and in pin description table. Replaced PDWN and PD with PD#.<br>Changed package diagram 51-85188*A to 51-85188*B. |

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| CAN 2.0b              | <a href="http://psoc.cypress.com/can">psoc.cypress.com/can</a>                           |
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