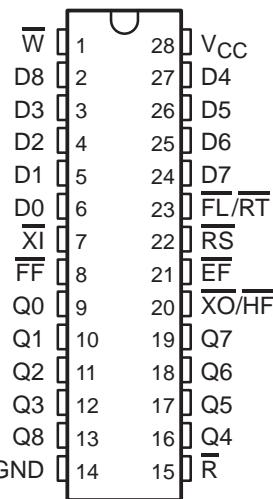
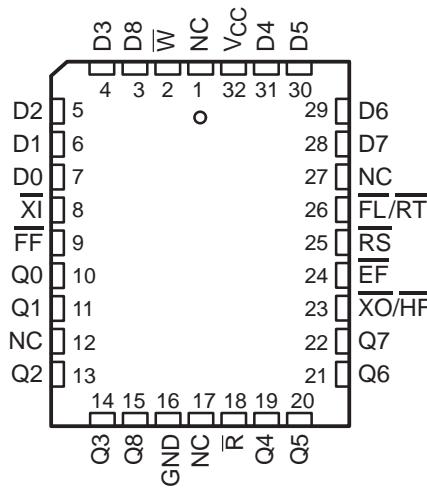


- Reads and Writes Can Be Asynchronous or Coincident
- Organization:
  - SN74ACT7203L – 2048  $\times$  9
  - SN74ACT7204L – 4096  $\times$  9
  - SN74ACT7205L – 8192  $\times$  9
  - SN74ACT7206L – 16383  $\times$  9
- Fast Data Access Times of 15 ns
- Read and Write Frequencies up to 40 MHz
- Bit-Width and Word-Depth Expansion
- Fully Compatible With the IDT7203/7204
- Retransmit Capability
- Empty, Full, and Half-Full Flags
- TTL-Compatible Inputs
- Available in 28-Pin Plastic DIP (NP), Plastic Small-Outline (DV), and 32-Pin Plastic J-Leaded Chip-Carrier (RJ) Packages

DV OR NP PACKAGE  
(TOP VIEW)RJ PACKAGE  
(TOP VIEW)

NC – No internal connection

## description

These devices are constructed with dual-port SRAM and have internal write and read address counters to provide data throughput on a first-in, first-out (FIFO) basis. Write and read operations are independent and can be asynchronous or coincident. Empty and full status flags prevent underflow and overflow of memory, and depth-expansion logic allows combining the storage cells of two or more devices into one FIFO. Word-width expansion is also possible.

Data is loaded into memory by the write-enable ( $\bar{W}$ ) input and unloaded by the read-enable ( $\bar{R}$ ) input. Read and write cycle times of 25 ns (40 MHz) are possible with data access times of 15 ns.

These devices are particularly suited for providing a data channel between two buses operating at asynchronous rates. Applications include use as rate buffers from analog-to-digital converters in data-acquisition systems, temporary storage elements between buses and magnetic or optical memories, and queues for communication systems. A 9-bit-wide data path is provided for the transmission of byte data plus a parity bit or packet-framing information. The read pointer can be reset independently of the write pointer for retransmitting previously read data when a device is not used in depth expansion.

The SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, and SN74ACT7206L are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

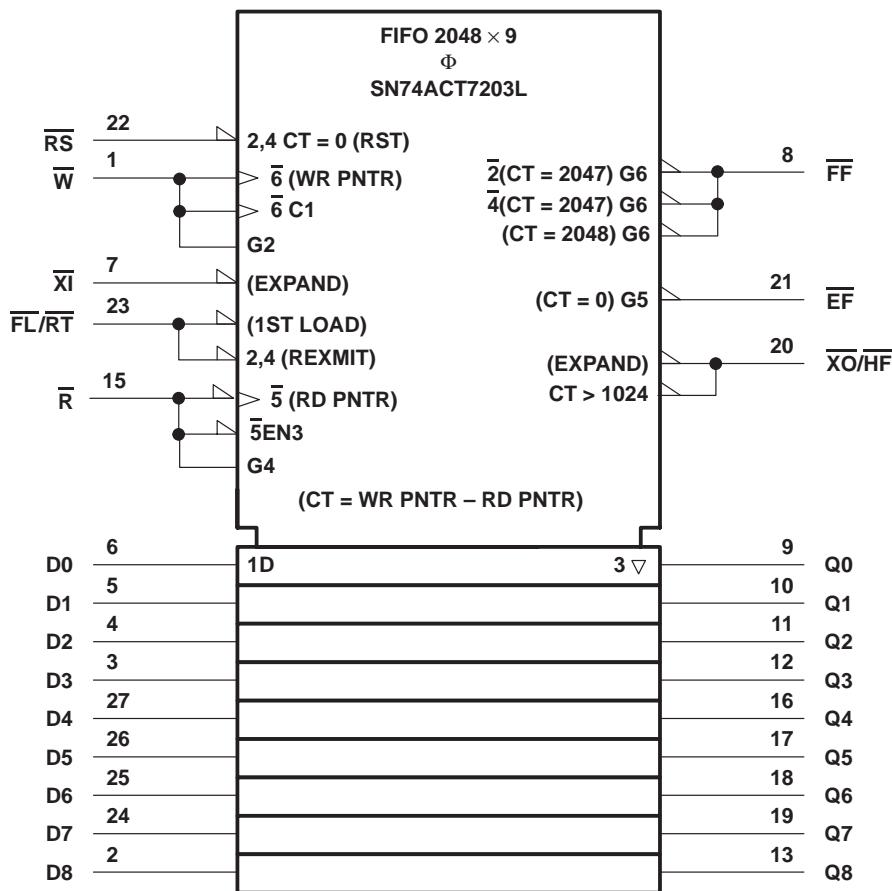
SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L

2048  $\times$  9, 4096  $\times$  9, 8192  $\times$  9, 16384  $\times$  9

ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

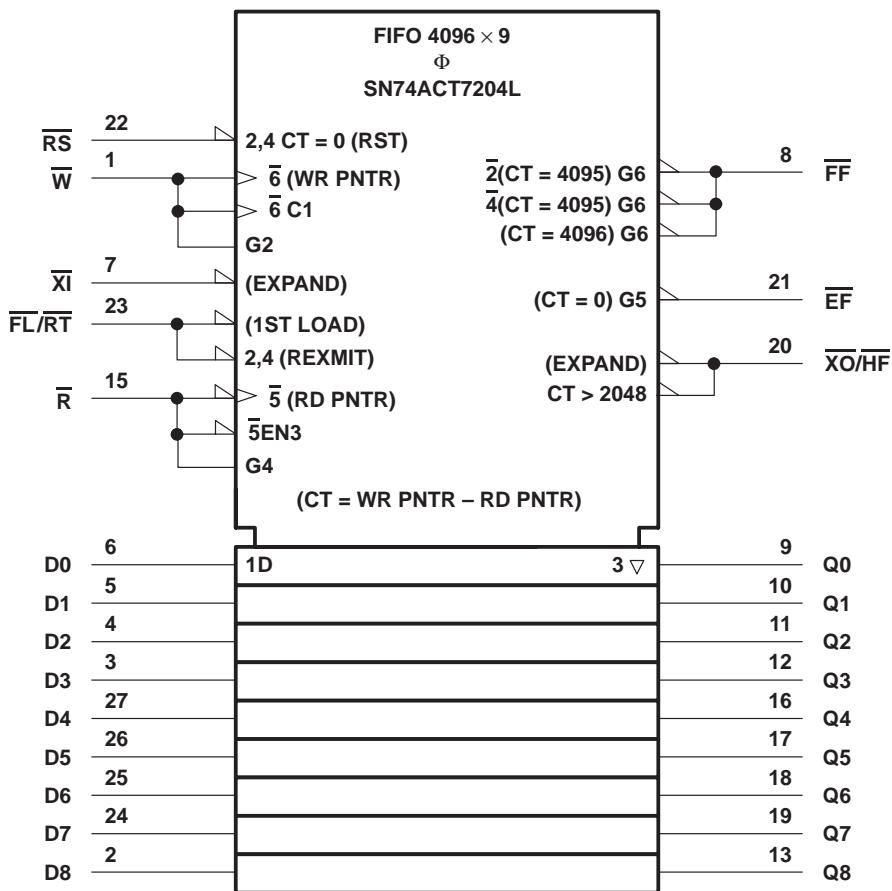
### SN74ACT7203L logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DV and NP packages.

## SN74ACT7204L logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DV and NP packages.

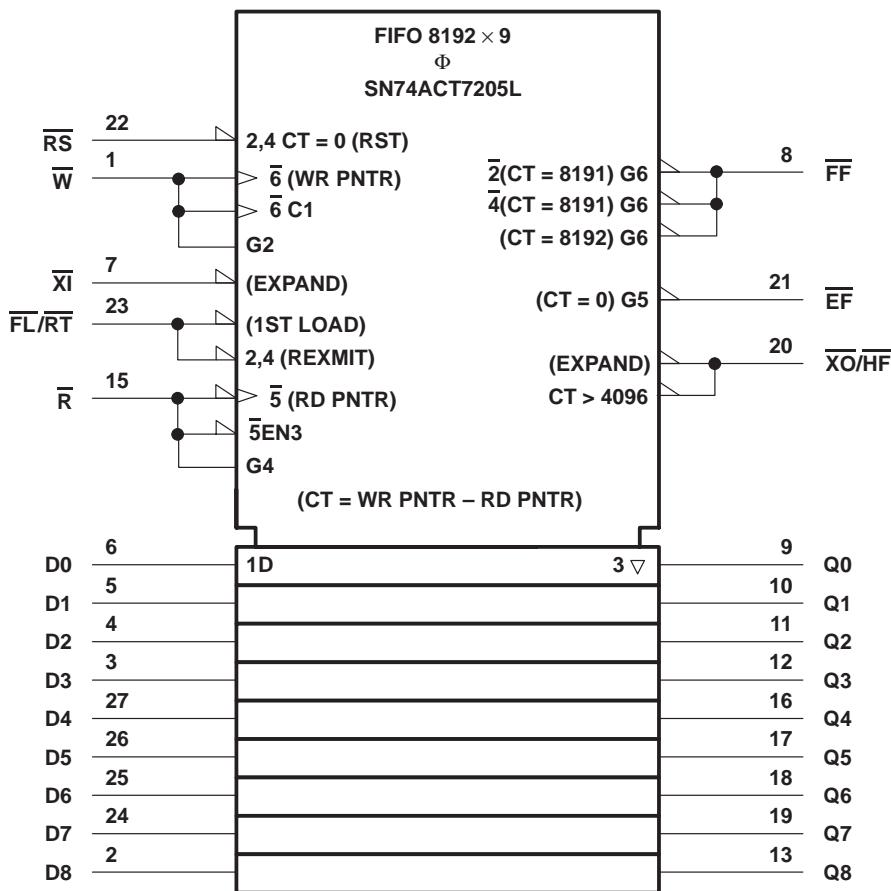
SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L

2048  $\times$  9, 4096  $\times$  9, 8192  $\times$  9, 16384  $\times$  9

ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

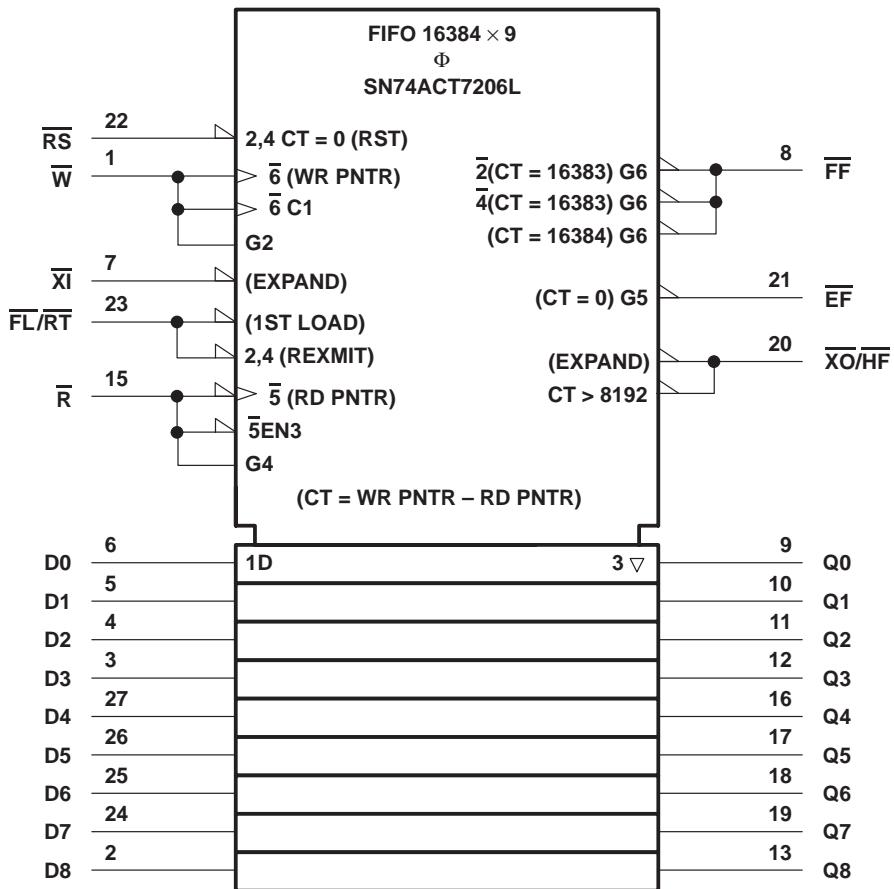
### SN74ACT7205L logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DV and NP packages.

## SN74ACT7206L logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DV and NP packages.

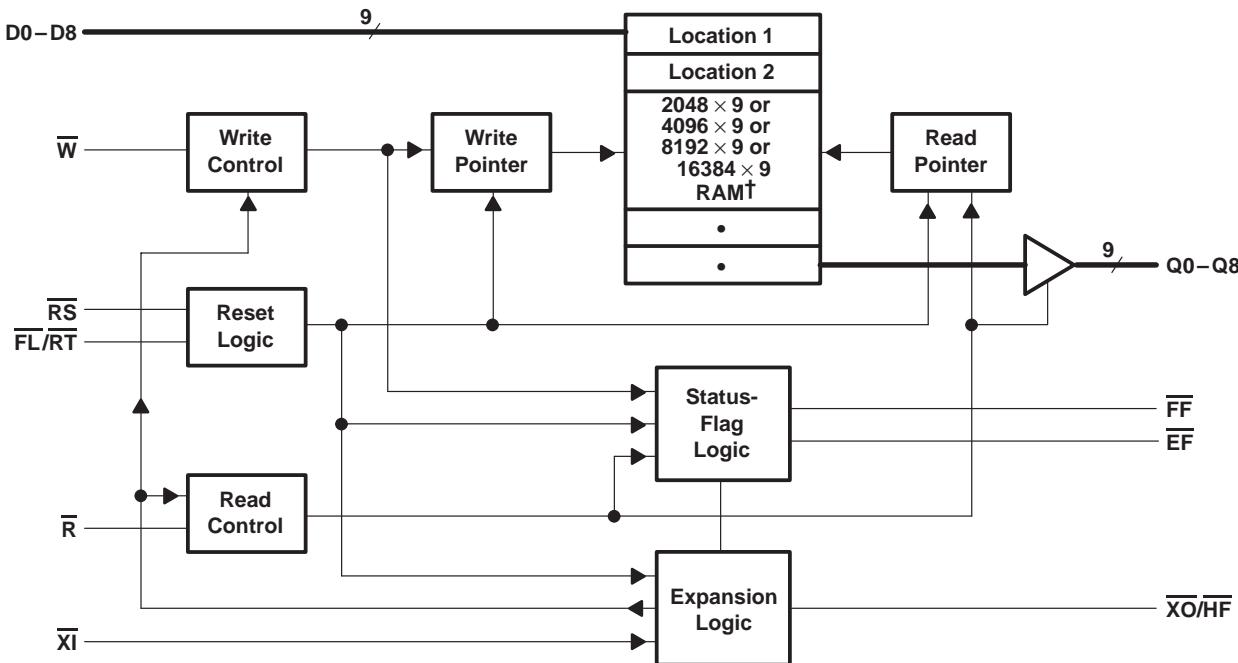
# SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L

2048  $\times$  9, 4096  $\times$  9, 8192  $\times$  9, 16384  $\times$  9

## ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS226A - FEBRUARY 1993 - REVISED SEPTEMBER 1995

### functional block diagram



† 2048  $\times$  9 for SN74ACT7203L; 4096  $\times$  9 for SN74ACT7204L; 8192  $\times$  9 for SN74ACT7205L; 16384  $\times$  9 for SN74ACT7206L

RESET AND RETRANSMIT FUNCTION TABLE  
(single-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS			FUNCTION
RS	FL/RT	XI	READ POINTER	WRITE POINTER	EF	FF	XO/HF	
L	X	L	Location zero	Location zero	L	H	H	Reset device
H	L	L	Location zero	Unchanged	X	X	X	Retransmit
H	H	L	Increment if EF high	Increment if FF high	X	X	X	Read/write

RESET AND FIRST-LOAD FUNCTION TABLE  
(multiple-device depth; single-or multiple-device width)

INPUTS			INTERNAL TO DEVICE		OUTPUTS		FUNCTION
RS	FL/RT	XI	READ POINTER	WRITE POINTER	EF	FF	
L	L	‡	Location zero	Location zero	L	H	Reset first device
L	H	‡	Location zero	Location zero	L	H	Reset all other devices
H	X	‡	X	X	X	X	Read/write

‡ XI is connected to XO/HF of the previous device in the daisy chain (see Figure 15).

## Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
D0–D8	I	Data inputs
$\overline{EF}$	O	Empty-flag output. $\overline{EF}$ is low when the read pointer is equal to the write pointer, inhibiting any operation initiated by a read cycle. When the FIFO is empty, a data word can be read automatically at Q0–Q8 by holding $\overline{R}$ low when loading the data word with a low-level pulse on $\overline{W}$ .
$\overline{FF}$	O	Full-flag output. $\overline{FF}$ is low when the write pointer is one location less than the read pointer, indicating that the device is full and inhibiting any operation initiated by a write cycle. $\overline{FF}$ goes low when the number of writes after reset exceeds the number of reads by 2048 for the SN74ACT7203L, 4096 for the SN74ACT7204L, 8192 for the SN74ACT7205L, and 16384 for the SN74ACT7206L. When the FIFO is full, a data word can be written automatically into memory by holding $\overline{W}$ low while reading out another data word with a low-level pulse on $\overline{R}$ .
$\overline{FL/RT}$	I	First-load/retransmit input. $\overline{FL/RT}$ performs two separate functions. When cascading two or more devices for word-depth expansion, $\overline{FL/RT}$ is tied to ground on the first device in the daisy chain to indicate that it is the first device loaded and unloaded; it is tied high on all other devices in the depth-expansion chain. A device is not used in depth expansion when its expansion-in ( $\overline{XI}$ ) input is tied to ground. In that case, $\overline{FL/RT}$ acts as a retransmit enable. A retransmit operation is initiated when $\overline{FL/RT}$ is pulsed low. This sets the internal read pointer to the first location and does not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be at a high logic level during the low-level $\overline{FL/RT}$ retransmit pulse. Retransmit should be used only when less than 2048/4096 writes are performed between resets; otherwise, an attempt to retransmit can cause the loss of unread data. The retransmit function can affect $\overline{XO/HF}$ depending on the relative locations of the read and write pointers.
GND		Ground
Q0–Q8	O	Data outputs. Q0–Q8 are in the high-impedance state when $\overline{R}$ is high or the FIFO is empty.
$\overline{R}$	I	Read-enable input. A read cycle begins on the falling edge of $\overline{R}$ if $\overline{EF}$ is high. This activates Q0–Q8 and shifts the next data value to this bus. The data outputs return to the high-impedance state as $\overline{R}$ goes high. As the last stored word is read by the falling edge of $\overline{R}$ , $\overline{EF}$ transitions low but Q0–Q8 remain active until $\overline{R}$ returns high. When the FIFO is empty, the internal read pointer is unchanged by a pulse on $\overline{R}$ .
$\overline{RS}$	I	Reset input. A reset is performed by taking $\overline{RS}$ low. This initializes the internal read and write pointers to the first location and sets $\overline{EF}$ low, $\overline{FF}$ high, and $\overline{HF}$ high. Both $\overline{R}$ and $\overline{W}$ must be held high for a reset during the window shown in Figure 7. A reset is required after power up before a write operation can take place.
VCC		Supply voltage
$\overline{W}$	I	Write-enable input. A write cycle begins on the falling edge of $\overline{W}$ if $\overline{FF}$ is high. The value on D0–D8 is stored in memory as $\overline{W}$ returns high. When the FIFO is full, $\overline{FF}$ is low inhibiting $\overline{W}$ from performing any operation on the device.
$\overline{XI}$	I	Expansion-in input. $\overline{XI}$ performs two functions. $\overline{XI}$ is tied to ground to indicate that the device is not used in depth expansion. When the device is used in depth expansion, $\overline{XI}$ is connected to the expansion-out ( $\overline{XO}$ ) output of the previous device in the depth-expansion chain.
$\overline{XO/HF}$	O	Expansion-out/half-full-flag output. $\overline{XO/HF}$ performs two functions. When the device is not used in depth expansion (i.e., when $\overline{XI}$ is tied to ground), $\overline{XO/HF}$ indicates when half the memory locations are filled. After half of the memory is filled, the falling edge on $\overline{W}$ for the next write operation drives $\overline{XO/HF}$ low. $\overline{XO/HF}$ remains low until a rising edge of $\overline{R}$ reduces the number of words stored to exactly half of the total memory. When the device is used in depth expansion, $\overline{XO/HF}$ is connected to $\overline{XI}$ of the next device in the daisy chain. $\overline{XO/HF}$ drives the daisy chain by sending a pulse to the next device when the previous device reaches the last memory location.

**SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L  
 2048 × 9, 4096 × 9, 8192 × 9, 16384 × 9  
 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES**

SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1) .....	–0.5 V to 7 V
Input voltage range (any input), $V_I$ .....	–0.5 V to 7 V
Continuous output current, $I_O$ .....	50 mA
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range, $T_A$ .....	0°C to 70°C
Storage temperature range, $T_{STG}$ .....	–55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$\overline{X_1}$	2.6		V
		Other inputs	2		
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			–2	mA
$I_{OL}$	Low-level output current			8	mA
$T_A$	Operating free-air temperature	0		70	°C

**electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 5.5$  V  
 (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = –2$ mA	2.4		V
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 8$ mA		0.4	V
$I_{OZH}$	$V_O = V_{CC}$ , $\overline{R} \geq V_{IH}$		$\pm 10$	$\mu A$
$I_{OZL}$	$V_O = 0.4$ V, $\overline{R} \geq V_{IH}$		$\pm 10$	$\mu A$
$I_I$	$V_I = 0$ to 5.5 V	–1	1	$\mu A$
$I_{CC1}^{\ddagger}$	$f_{clock} = 20$ MHz		120	mA
$I_{CC2}^{\ddagger}$	$\overline{R}$ , $\overline{W}$ , $\overline{RS}$ , and $\overline{FL/RT}$ at $V_{IH}$		12	mA
$I_{CC3}^{\ddagger}$	$V_I = V_{CC} – 0.2$ V		2	mA
$C_i^{\$}$	$V_I = 0$ , $T_A = 25^\circ C$ , $f = 1$ MHz		10	pF
$C_o^{\$}$	$V_O = 0$ , $T_A = 25^\circ C$ , $f = 1$ MHz		10	pF

†  $I_{CC1}$  = supply current;  $I_{CC2}$  = standby current;  $I_{CC3}$  = power-down current.  $I_{CC}$  measurements are made with outputs open (only capacitive loading).

§ This parameter is sampled and not 100% tested.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L**  
 $2048 \times 9, 4096 \times 9, 8192 \times 9, 16384 \times 9$   
**ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES**  
SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	FIGURE	'ACT7203L-15 'ACT7204L-15 'ACT7205L-15 'ACT7206L-15		'ACT7203L-25 'ACT7204L-25 'ACT7205L-25 'ACT7206L-25		'ACT7203L-50 'ACT7204L-50 'ACT7205L-50 'ACT7206L-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{clock}$	Clock frequency, $\bar{R}$ or $\bar{W}$		40		28.5		15	MHz
$t_{c(R)}$	Cycle time, read	1(a)	25	35	65			ns
$t_{c(W)}$	Cycle time, write	1(b)	25	35	65			ns
$t_{c(RS)}$	Cycle time, reset	7	25	35	65			ns
$t_{c(RT)}$	Cycle time, retransmit	4	25	35	65			ns
$t_{w(RL)}$	Pulse duration, $\bar{R}$ low	1(a)	15	25	50			ns
$t_{w(WL)}$	Pulse duration, $\bar{W}$ low	1(b)	15	25	50			ns
$t_{w(RH)}$	Pulse duration, $\bar{R}$ high	1(a)	10	10	15			ns
$t_{w(WH)}$	Pulse duration, $\bar{W}$ high	1(b)	10	10	15			ns
$t_{w(RT)}$	Pulse duration, $\bar{FL}/\bar{RT}$ low	4	15	25	50			ns
$t_{w(RS)}$	Pulse duration, $\bar{RS}$ low	7	15	25	50			ns
$t_{w(XIL)}$	Pulse duration, $\bar{XI}$ low	10	15	25	50			ns
$t_{w(XIH)}$	Pulse duration, $\bar{XI}$ high	10	10	10	10			ns
$t_{su(D)}$	Setup time, data before $\bar{W}^\uparrow$	1(b), 6	11	15	30			ns
$t_{su(RT)}$	Setup time, $\bar{R}$ and $\bar{W}$ high before $\bar{FL}/\bar{RT}^\uparrow\uparrow$	4	15	25	50			ns
$t_{su(RS)}$	Setup time, $\bar{R}$ and $\bar{W}$ high before $\bar{RS}^\uparrow\uparrow$	7	15	25	50			ns
$t_{su(XI-R)}$	Setup time, $\bar{XI}$ low before $\bar{R}^\downarrow$	10	10	10	15			ns
$t_{su(XI-W)}$	Setup time, $\bar{XI}$ low before $\bar{W}^\downarrow$	10	10	10	15			ns
$t_h(D)$	Hold time, data after $\bar{W}^\uparrow$	1(b), 6	0	0	5			ns
$t_h(E-R)$	Hold time, $\bar{R}$ low after $\bar{EF}^\uparrow$	5, 11	15	25	50			ns
$t_h(F-W)$	Hold time, $\bar{W}$ low after $\bar{FF}^\uparrow$	6, 12	15	25	50			ns
$t_h(RT)$	Hold time, $\bar{R}$ and $\bar{W}$ high after $\bar{FL}/\bar{RT}^\uparrow$	4	10	10	15			ns
$t_h(RS)$	Hold time, $\bar{R}$ and $\bar{W}$ high after $\bar{RS}^\uparrow$	7	10	10	15			ns

† These values are characterized but not currently tested.

**SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L****2048 × 9, 4096 × 9, 8192 × 9, 16384 × 9****ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES**

SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 13)**

PARAMETER	FIGURE	'ACT7203L-15		'ACT7203L-25		'ACT7203L-50		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
$t_a$	Access time, $\overline{R} \downarrow$ or $\overline{EF} \uparrow$ to data out valid	1(a), 3, 5		15		25		50	ns
$t_{v(RH)}$	Valid time, data out valid after $\overline{R} \uparrow$	1(a)		5		5		5	ns
$t_{en(R-QX)}$	Enable time, $\overline{R} \downarrow$ to Q outputs at low impedance <sup>†</sup>	1(a)		5		5		10	ns
$t_{en(W-QX)}$	Enable time, $\overline{W} \uparrow$ to Q outputs at low impedance <sup>†‡</sup>		5		5		15	ns	
$t_{dis(R)}$	Disable time, $\overline{R} \uparrow$ to Q outputs at high impedance <sup>†</sup>	1(a)		15		18		30	ns
$t_w(FH)$	Pulse duration, $\overline{FF}$ high in automatic-write mode	6		15		25		45	ns
$t_w(EH)$	Pulse duration, $\overline{EF}$ high in automatic-read mode		5		15		25	45	ns
$t_{pd(W-F)}$	Propagation delay time, $\overline{W} \downarrow$ to $\overline{FF}$ low	2		15		25		45	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{R} \uparrow$ to $\overline{FF}$ high	2, 6, 12		15		25		45	ns
$t_{pd(RS-F)}$	Propagation delay time, $\overline{RS} \downarrow$ to $\overline{FF}$ high	7		25		35		65	ns
$t_{pd(RS-HF)}$	Propagation delay time, $\overline{RS} \downarrow$ to $\overline{XO/HF}$ high	7		25		35		65	ns
$t_{pd(W-E)}$	Propagation delay time, $\overline{W} \uparrow$ to $\overline{EF}$ high	3, 5, 11		15		25		45	ns
$t_{pd(R-E)}$	Propagation delay time, $\overline{R} \downarrow$ to $\overline{EF}$ low	3		15		25		45	ns
$t_{pd(RS-E)}$	Propagation delay time, $\overline{RS} \downarrow$ to $\overline{EF}$ low	7		25		35		65	ns
$t_{pd(W-HF)}$	Propagation delay time, $\overline{W} \downarrow$ to $\overline{XO/HF}$ low	8		25		35		65	ns
$t_{pd(R-HF)}$	Propagation delay time, $\overline{R} \uparrow$ to $\overline{XO/HF}$ high	8		25		35		65	ns
$t_{pd(R-XOL)}$	Propagation delay time, $\overline{R} \downarrow$ to $\overline{XO/HF}$ low	9		15		25		50	ns
$t_{pd(W-XOL)}$	Propagation delay time, $\overline{W} \downarrow$ to $\overline{XO/HF}$ low	9		15		25		50	ns
$t_{pd(R-XOH)}$	Propagation delay time, $\overline{R} \uparrow$ to $\overline{XO/HF}$ high	9		15		25		50	ns
$t_{pd(W-XOH)}$	Propagation delay time, $\overline{W} \uparrow$ to $\overline{XO/HF}$ high	9		15		25		50	ns
$t_{pd(RT-FL)}$	Propagation delay time, $\overline{FL/RT} \downarrow$ to HF, EF, FF valid	4		25		35		65	ns

<sup>†</sup> These values are characterized but not currently tested.<sup>‡</sup> Only applies when data is automatically read

PARAMETER MEASUREMENT INFORMATION

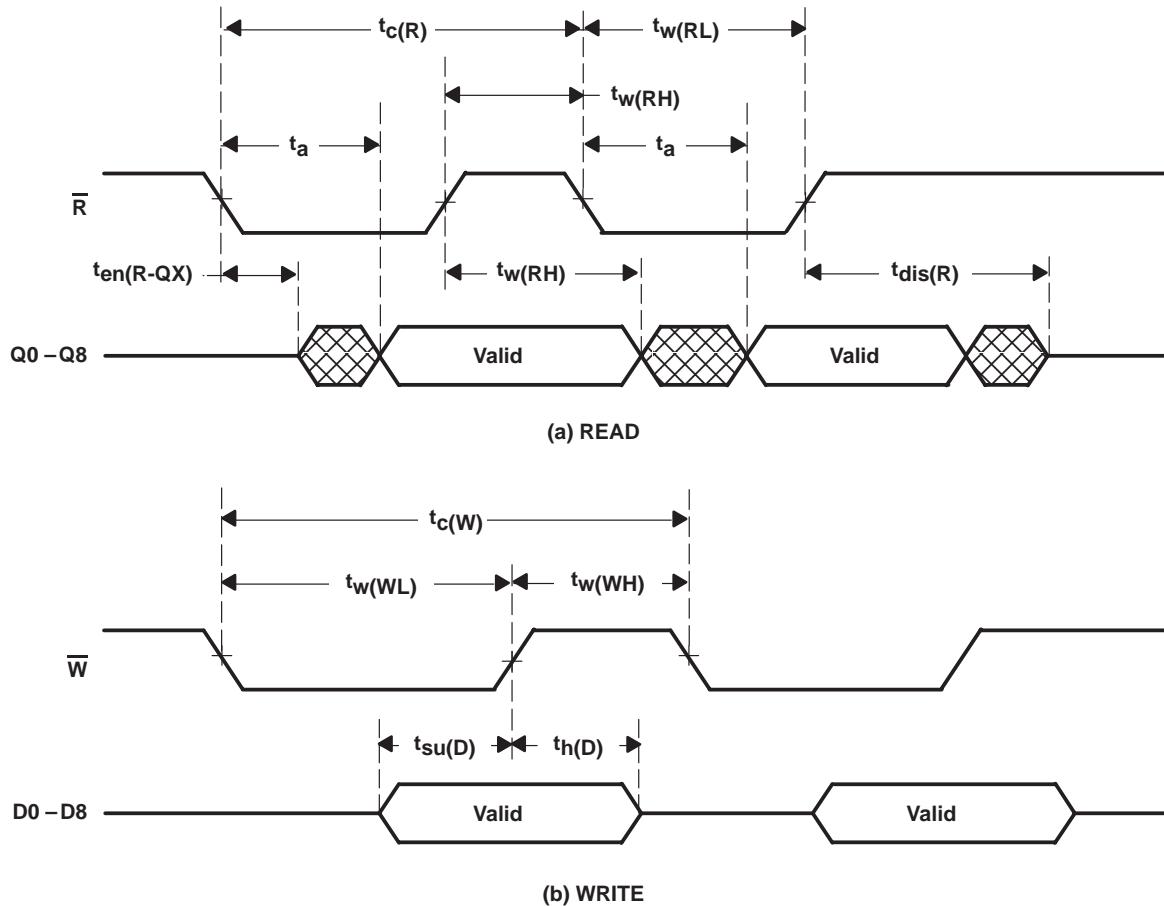


Figure 1. Asynchronous Waveforms

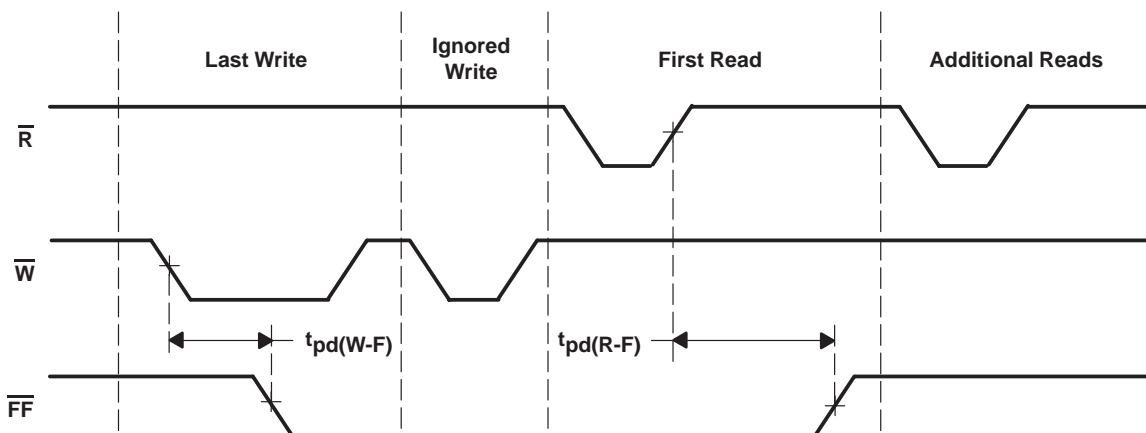


Figure 2. Full-Flag Waveforms

## PARAMETER MEASUREMENT INFORMATION

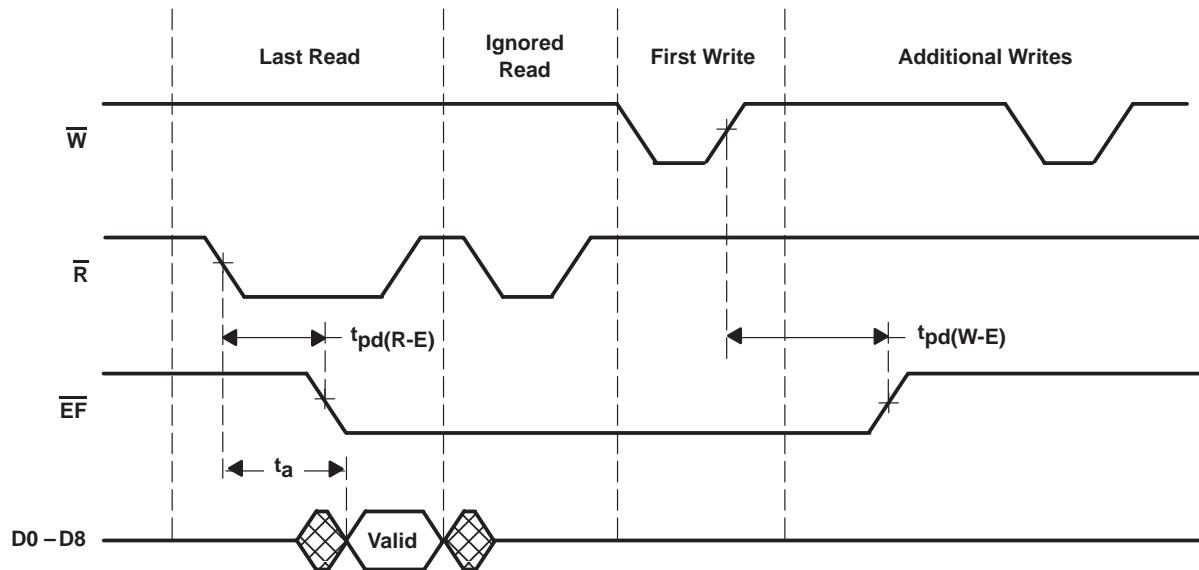
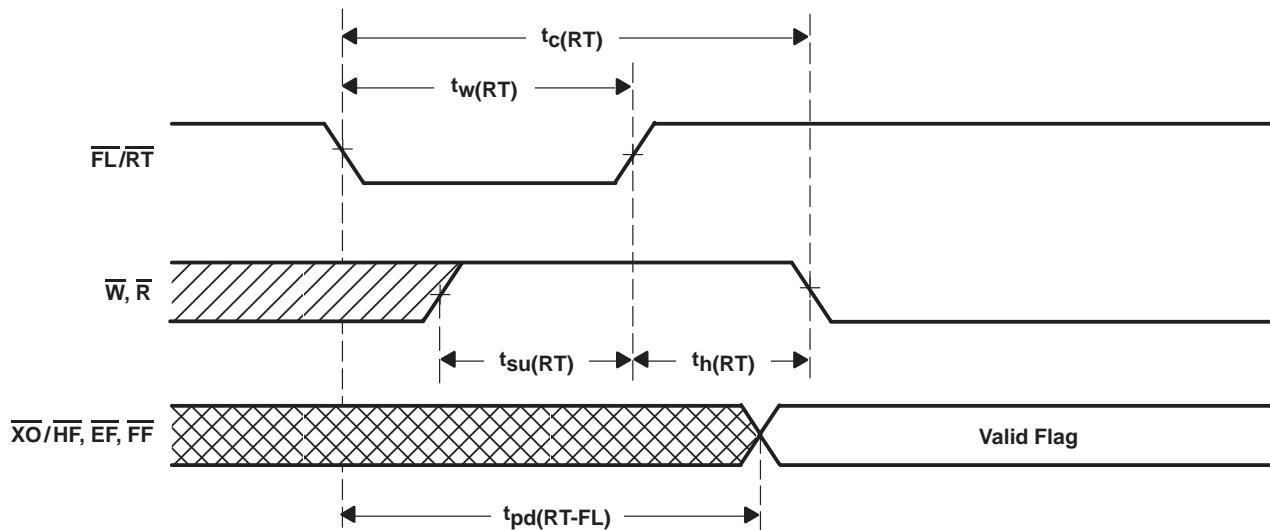


Figure 3. Empty-Flag Waveforms



NOTE A: The  $\overline{EF}$ ,  $\overline{FF}$ , and  $\overline{XO/HF}$  status flags are valid after completion of the retransmit cycle.

Figure 4. Retransmit Waveforms

PARAMETER MEASUREMENT INFORMATION

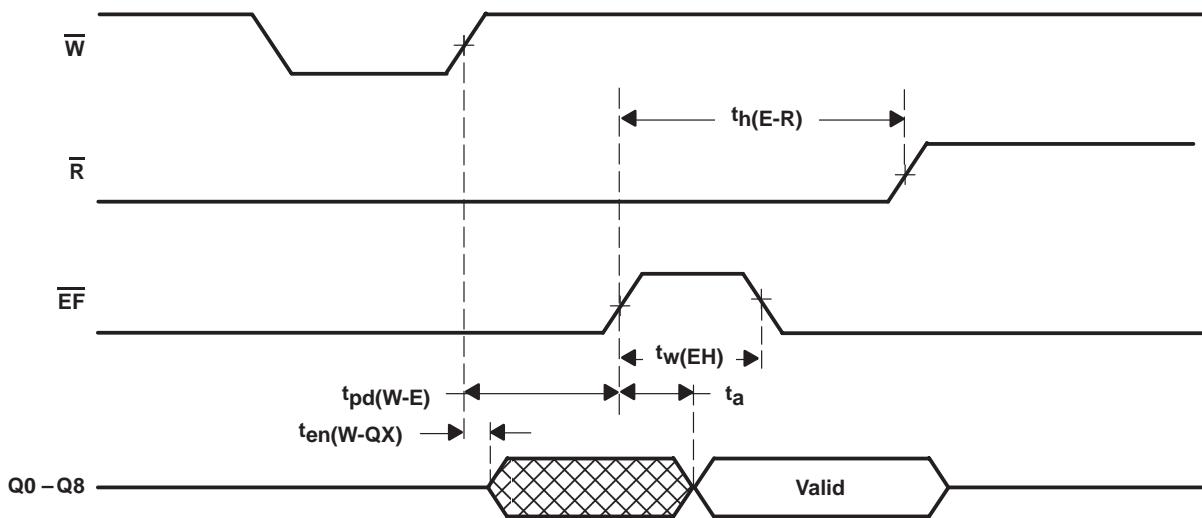


Figure 5. Automatic-Read Waveforms

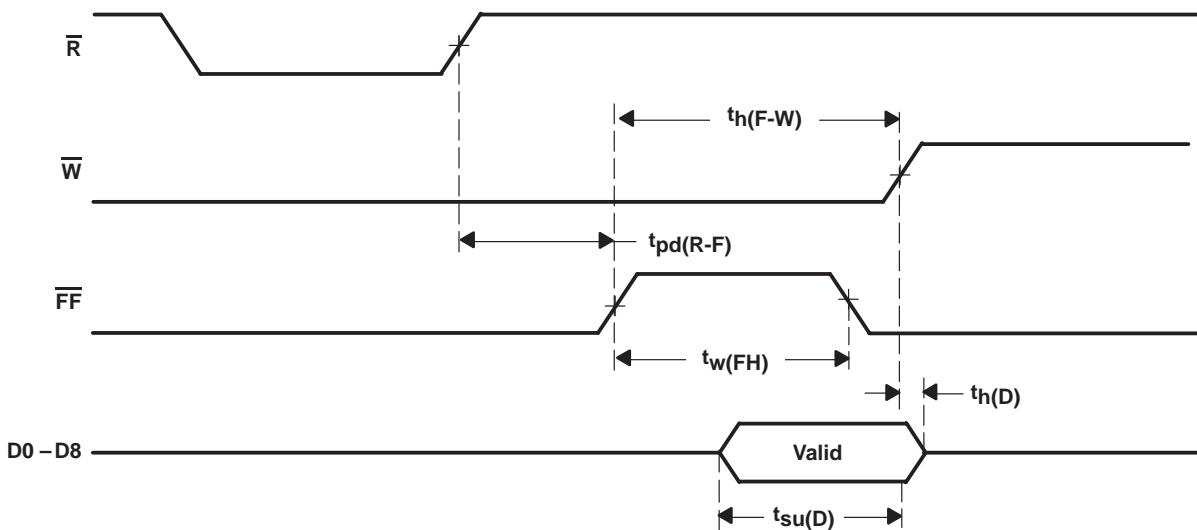


Figure 6. Automatic-Write Waveforms

SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L

2048  $\times$  9, 4096  $\times$  9, 8192  $\times$  9, 16384  $\times$  9

ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS226A - FEBRUARY 1993 - REVISED SEPTEMBER 1995

### PARAMETER MEASUREMENT INFORMATION

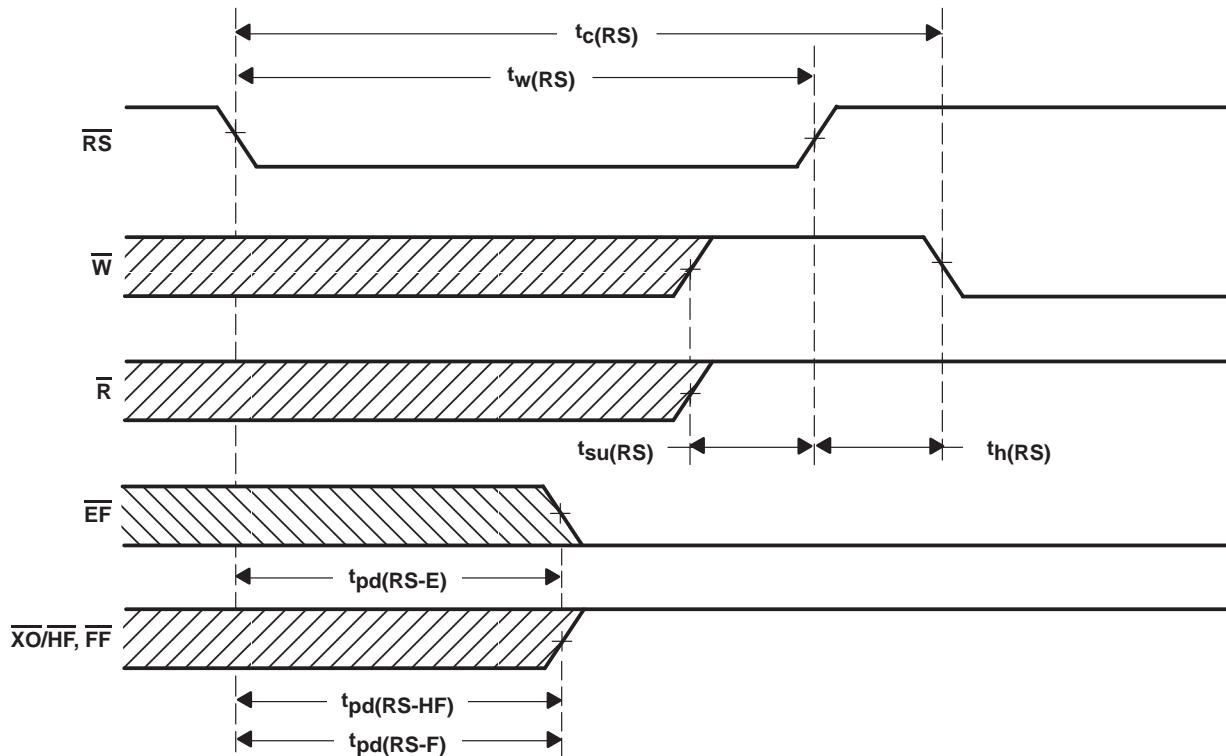


Figure 7. Master-Reset Waveforms

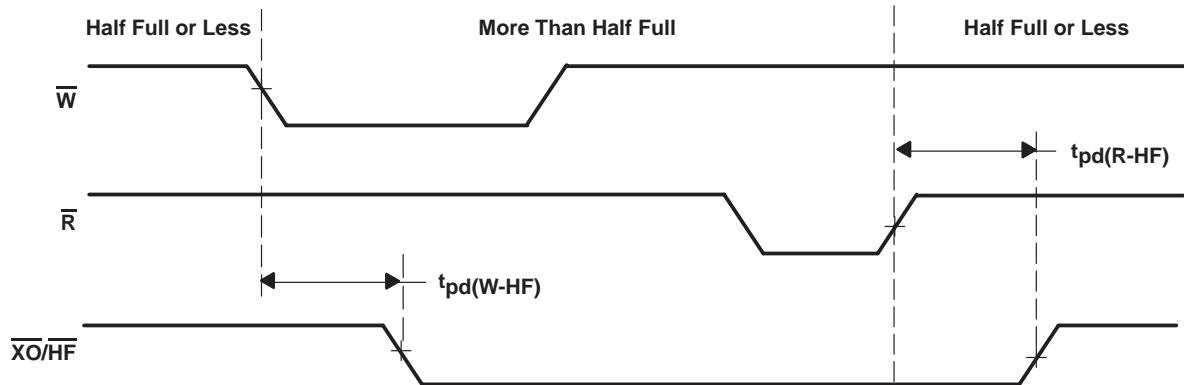


Figure 8. Half-Full Flag Waveforms

PARAMETER MEASUREMENT INFORMATION

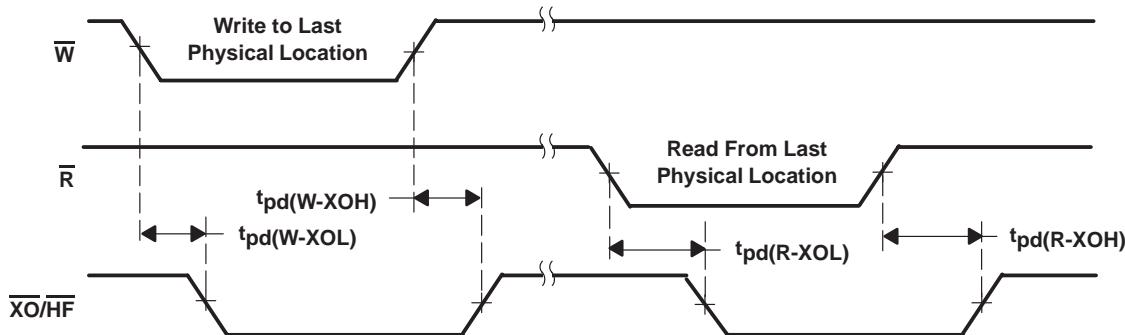


Figure 9. Expansion-Out Waveforms

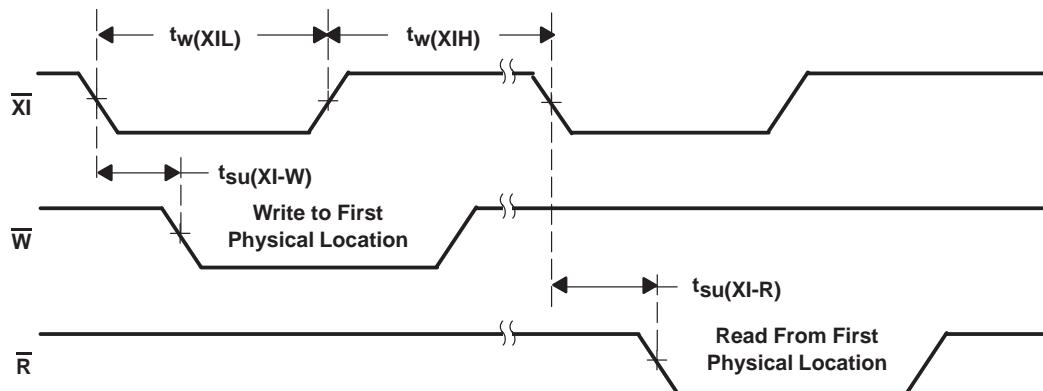


Figure 10. Expansion-In Waveforms

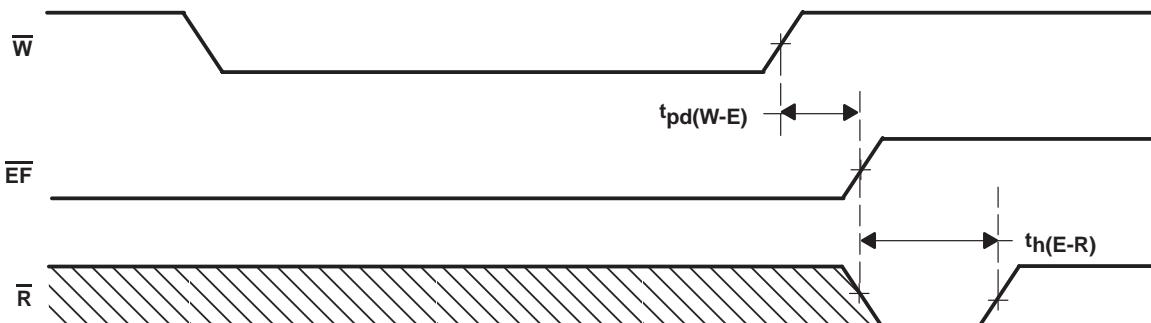


Figure 11. Minimum Timing for an Empty-Flag Coincident-Read Pulse

SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L

2048  $\times$  9, 4096  $\times$  9, 8192  $\times$  9, 16384  $\times$  9

ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

---

#### PARAMETER MEASUREMENT INFORMATION

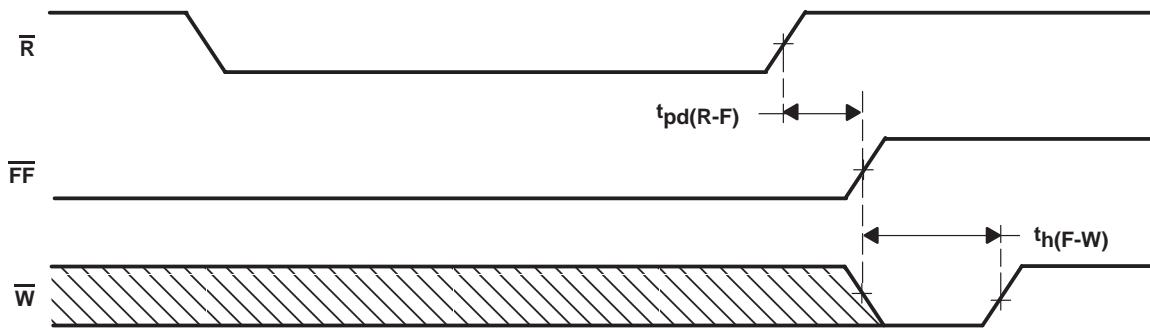
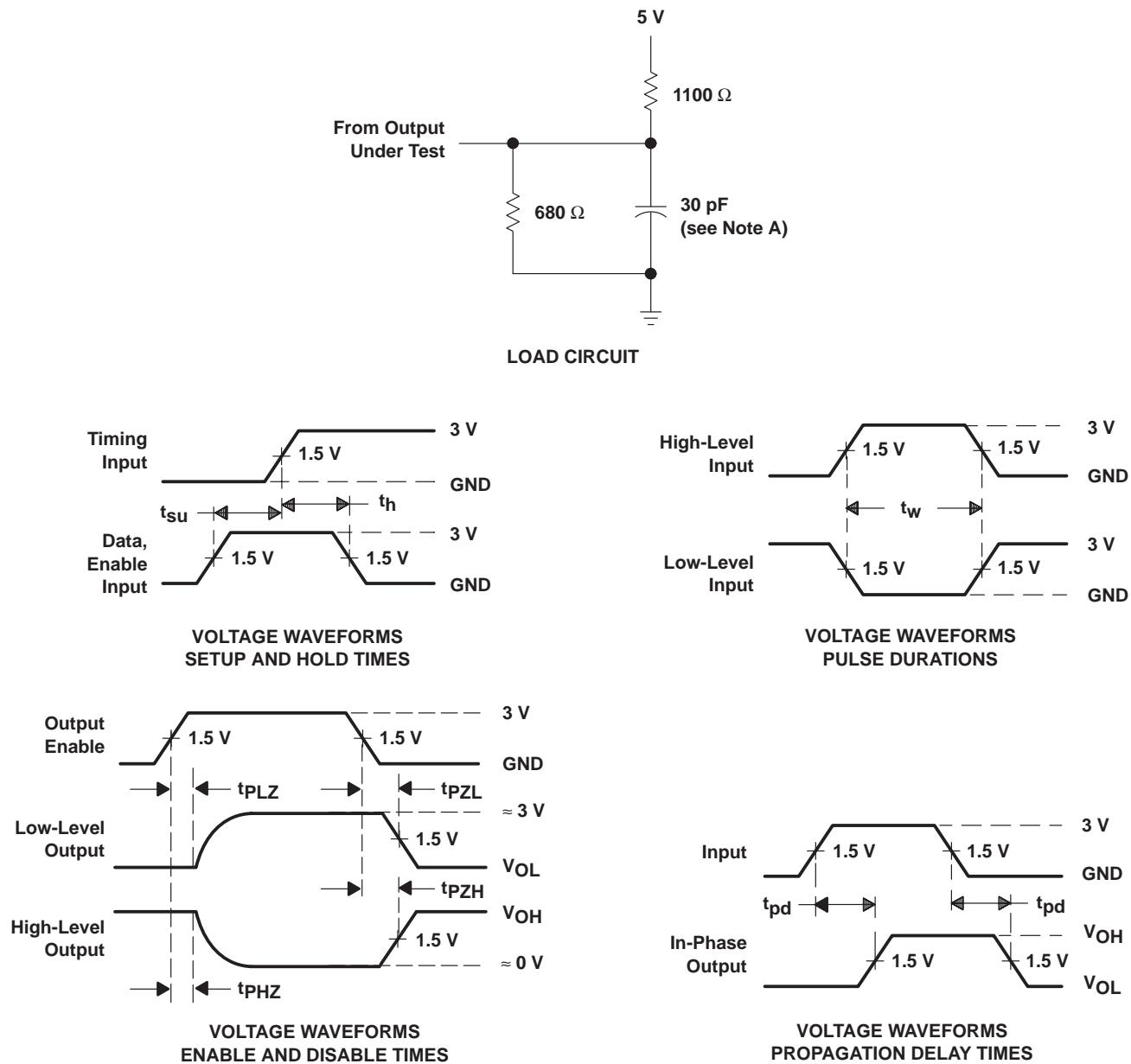


Figure 12. Minimum Timing for a Full-Flag Coincident-Write Pulse

PARAMETER MEASUREMENT INFORMATION



NOTE A: Includes probe and jig capacitance

Figure 13. Load Circuit and Voltage Waveforms

## APPLICATION INFORMATION

Combining two or more devices to create one FIFO with a greater number of memory bits is accomplished in two different ways. Width expansion increases the number of bits in each word by connecting FIFOs with the same depth in parallel. Depth expansion uses the built-in expansion logic to daisy-chain two or more devices for applications requiring more than 2048, 4096, 8192, or 16384 words of storage. Width expansion and depth expansion can be used together.

### width expansion

Word-width expansion is achieved by connecting the corresponding input control to multiple devices with the same depth. Status flags ( $\overline{EF}$ ,  $\overline{FF}$ , and  $\overline{HF}$ ) can be monitored from any one device. Figure 14 shows two FIFOs in a width-expansion configuration. Both devices have their expansion-in ( $XI$ ) inputs tied to ground. This disables the depth-expansion function of the device, allowing the first-load/retransmit ( $\overline{FL}/\overline{RT}$ ) input to function as a retransmit ( $\overline{RT}$ ) input and the expansion-out/half-full ( $\overline{XO}/\overline{HF}$ ) output to function as a half-full ( $\overline{HF}$ ) flag.

### depth expansion

The SN74ACT7203L/7204L/7205L/7206L are easily expanded in depth. Figure 15 shows the connections used to depth expand three SN74ACT7203L/7204L/7205L/7206L devices. Any depth can be attained by adding additional devices to the chain. The SN74ACT7203L/7204L/7205L/7206L operate in depth expansion under the following conditions:

- The first device in the chain is designated by connecting  $\overline{FL}$  to ground.
- All other devices have their  $\overline{FL}$  inputs at a high logic level.
- $\overline{XO}$  of each device must be connected to  $\overline{XI}$  of the next device.
- External logic is needed to generate a composite  $\overline{FF}$  and  $\overline{EF}$ . All  $\overline{FF}$  outputs must be ORed together, and all  $\overline{EF}$  outputs must be ORed together.
- $\overline{RT}$  and  $\overline{HF}$  functions are not available in the depth-expanded configuration.

### combined depth and width expansion

Both expansion techniques can be used together to increase depth and width. This is done by creating depth-expanded units and then connecting them in a width-expanded configuration (see Figure 16).

## APPLICATION INFORMATION

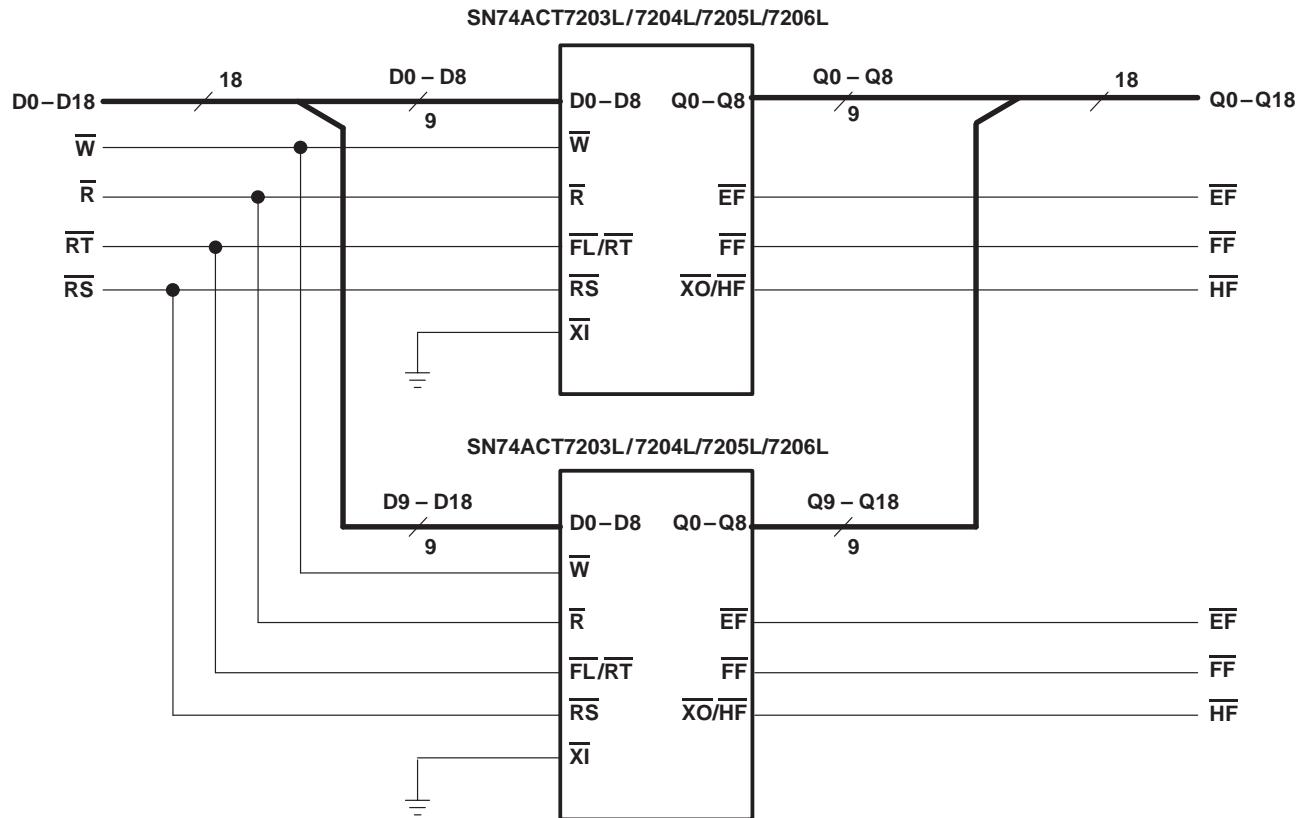


Figure 14. Word-Width Expansion: 2048/4096 Words  $\times$  18 Bits

SN74ACT7203L, SN74ACT7204L, SN74ACT7205L, SN74ACT7206L

2048  $\times$  9, 4096  $\times$  9, 8192  $\times$  9, 16384  $\times$  9

ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

SCAS226A – FEBRUARY 1993 – REVISED SEPTEMBER 1995

## APPLICATION INFORMATION

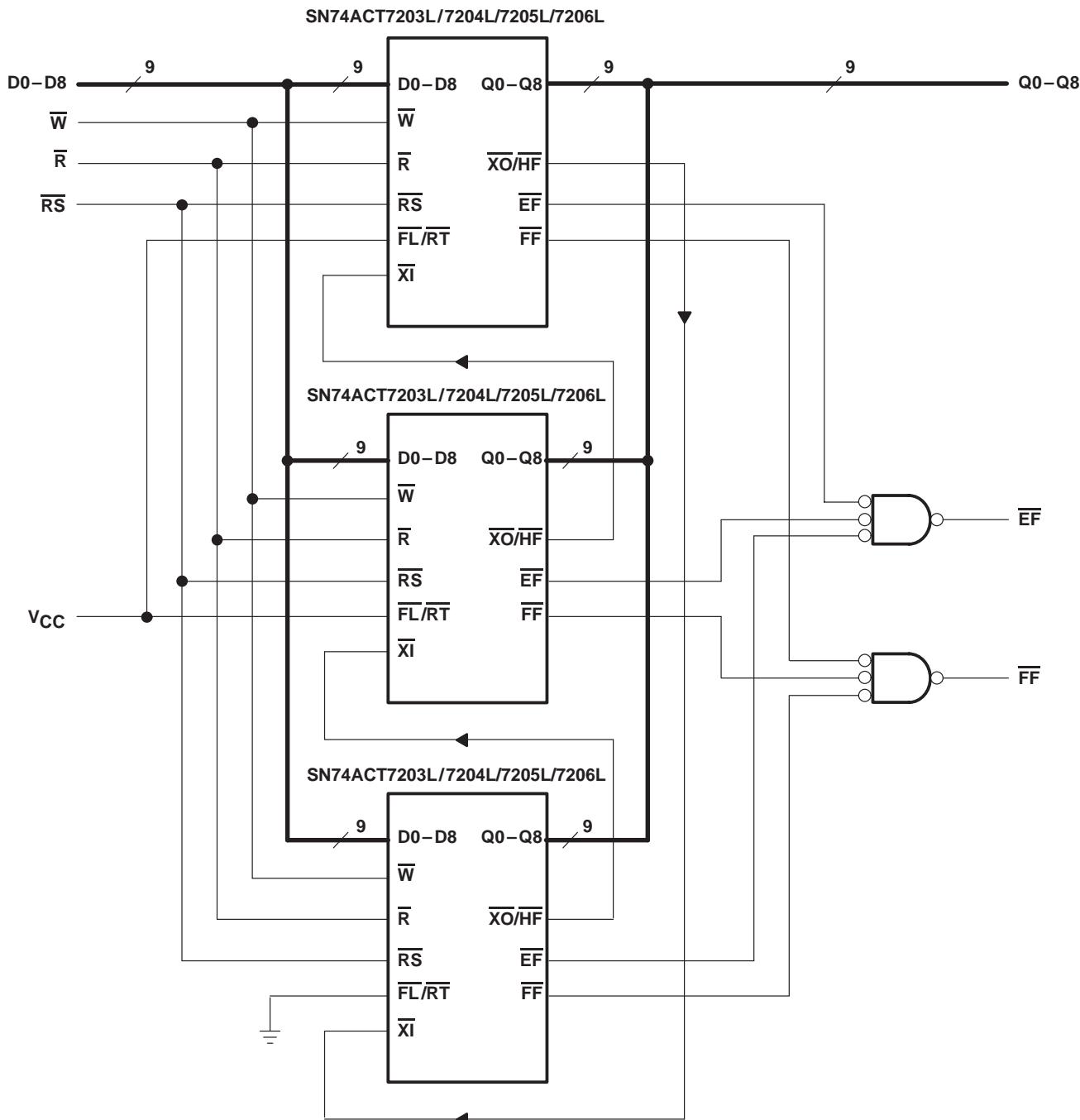


Figure 15. Word-Depth Expansion: 6144/12288/24576/49152 Words  $\times$  9 Bits

## APPLICATION INFORMATION

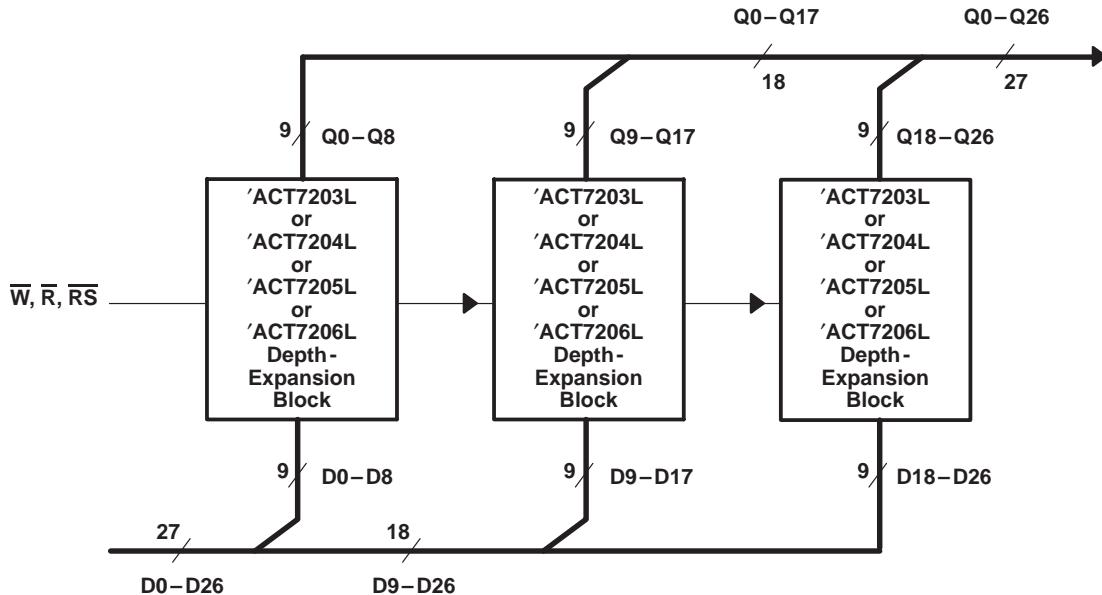


Figure 16. Word-Depth Plus Word-Width Expansion

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ACT7203L15NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7203L15RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7203L25NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7203L25RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7203L50NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7203L50RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7204L15NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7204L15RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7204L20NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7204L20RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7204L25NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7204L25RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7204L35NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7204L35RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7204L50NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7204L50RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7205L15NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7205L15RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7205L25NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7205L25RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7205L25RJR	DEPRECATED	PLCC	RJ	0		TBD	Call TI	Call TI
SN74ACT7205L50NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7205L50RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7206L15RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7206L25RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI
SN74ACT7206L50NP	DEPRECATED	PDIP	NP	28		TBD	Call TI	Call TI
SN74ACT7206L50RJ	DEPRECATED	PLCC	RJ	32		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**DEPRECATED:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	amplifier.ti.com	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	dataconverter.ti.com	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	dsp.ti.com	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	interface.ti.com	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	logic.ti.com	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	power.ti.com	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	microcontroller.ti.com	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated