# **Power MOSFET** 20 Amps, 30 Volts, N-Channel DPAK

This logic level vertical power MOSFET is a general purpose part that provides the "best of design" available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain—to—source diode has a ideal fast but soft recovery.

#### **Features**

- Pb-Free Packages are Available
- Ultra-Low R<sub>DS(on)</sub>, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for use in Bridge Circuits
- I<sub>DSS</sub> and V<sub>DS(on)</sub> Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0

### **Typical Applications**

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many Applications

### **MAXIMUM RATINGS** (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	30	Vdc
Gate-to-Source Voltage - Continuous - Non-Repetitive (t <sub>p</sub> ≤10 ms)	V <sub>GS</sub> V <sub>GS</sub>	±20 ±24	Vdc
$ \begin{array}{lll} & \text{Drain Current} \\ & - \text{ Continuous } @ \text{ T}_{A} = 25^{\circ}\text{C} \\ & - \text{ Continuous } @ \text{ T}_{A} = 100^{\circ}\text{C} \\ & - \text{ Single Pulse } (t_{p} \! \leq \! 10  \mu\text{s}) \end{array} $	I <sub>D</sub> I <sub>D</sub> I <sub>DM</sub>	20 16 60	Adc Apk
Total Power Dissipation @ T <sub>A</sub> = 25°C  Derate above 25°C  Total Power Dissipation @ T <sub>C</sub> = 25°C (Note 1)	P <sub>D</sub>	74 0.6 1.75	W W/°C W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ( $V_{DD} = 30$ Vdc, $V_{GS} = 5$ Vdc, $L = 1.0$ mH, $I_{L(pk)} = 24$ A, $V_{DS} = 34$ Vdc)	E <sub>AS</sub>	288	mJ
Thermal Resistance  – Junction-to-Case  – Junction-to-Ambient  – Junction-to-Ambient (Note 1)	$egin{array}{l} R_{ hetaJC} \ R_{ hetaJA} \ R_{ hetaJA} \end{array}$	1.67 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T∟	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

 When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.

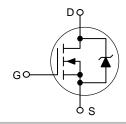


# ON Semiconductor®

http://onsemi.com

20 A, 30 V,  $R_{DS(on)}$  = 27 m $\Omega$ 

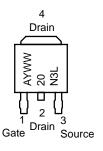
#### N-Channel



#### MARKING DIAGRAMS

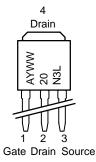


DPAK CASE 369C STYLE 2





DPAK-3 CASE 369D STYLE 2



 20N3L
 = Device Code

 A
 = Assembly Location

 Y
 = Year

 WW
 = Work Week

dimensions section on page 2 of this data sheet.

ORDERING INFORMATION
See detailed ordering and shipping information in the package

# **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

Chara	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 2) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 µAdc) Temperature Coefficient (Positive)			30 -	- 43	_ _	Vdc mV/°C
Zero Gate Voltage Drain Current $(V_{DS} = 30 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 30 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$		I <sub>DSS</sub>	_ _	- -	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)			-	-	±100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (Note 2) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)		V <sub>GS(th)</sub>	1.0 -	1.6 5.0	2.0	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2) $ (V_{GS} = 4.0 \text{ Vdc}, I_D = 10 \text{ Adc}) $ $ (V_{GS} = 5.0 \text{ Vdc}, I_D = 10 \text{ Adc}) $			- -	28 23	31 27	mΩ
Static Drain-to-Source On-Voltage (Note 2) $ (V_{GS} = 5.0 \text{ Vdc}, I_D = 20 \text{ Adc}) $ $ (V_{GS} = 5.0 \text{ Vdc}, I_D = 10 \text{ Adc}, T_J = 150^{\circ}\text{C}) $			- -	0.48 0.40	0.54 –	Vdc
Forward Transconductance (Note 2) (V <sub>DS</sub> = 5.0 Vdc, I <sub>D</sub> = 10 Adc)		9FS	_	21	_	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc},$	C <sub>iss</sub>	-	1005	1260	pF
Output Capacitance	f = 1.0  MHz	C <sub>oss</sub>	_	271	420	
Transfer Capacitance		C <sub>rss</sub>	_	87	112	
SWITCHING CHARACTERISTICS (No	te 3)					T
Turn-On Delay Time	(V <sub>DD</sub> = 20 Vdc, I <sub>D</sub> = 20 Adc,	t <sub>d(on)</sub>	_	17	25	ns
Rise Time	$V_{GS} = 5.0 \text{ Vdc},$	t <sub>r</sub>	_	137	160	
Turn-Off Delay Time	$R_G = 9.1 \Omega$ ) (Note 2)	t <sub>d(off)</sub>	-	38	45	
Fall Time		t <sub>f</sub>	_	31	40	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 15 Adc,	Q <sub>T</sub>	_	13.8	18.9	nC
	V <sub>GS</sub> = 10 Vdc) (Note 2)	Q <sub>1</sub>	_	2.8	-	
		$Q_2$	_	6.6	_	
SOURCE-DRAIN DIODE CHARACTE	RISTICS		_	_	1	
Forward On–Voltage	$(I_S = 20 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 2)}$ $(I_S = 20 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	$V_{SD}$	_ _	1.0 0.9	1.15 -	Vdc
Reverse Recovery Time		t <sub>rr</sub>	-	23	-	ns
	$(I_S = 15 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$	ta	-	13	-	
	$dI_{S}/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 2)}$	t <sub>b</sub>	-	10	-	
Reverse Recovery Stored Charge		$Q_{RR}$	_	0.017	_	μC

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>	
NTD20N03L27	DPAK	75 Units/Rail	
NTD20N03L27G	DPAK (Pb–Free)	75 Units/Rail	
NTD20N03L27-1	DPAK-3	75 Units/Rail	
NTD20N03L27-1G	DPAK (Pb-Free)	75 Units/Rail	
NTD20N03L27T4	DPAK	2500 Tape & Reel	
NTD20N03L27T4G	DPAK (Pb-Free)	2500 Tape & Reel	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

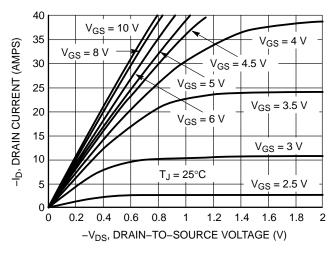


Figure 1. On-Region Characteristics

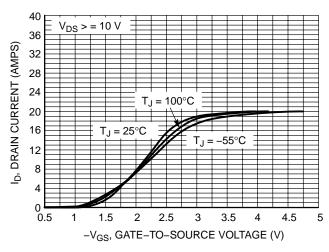


Figure 2. Transfer Characteristics

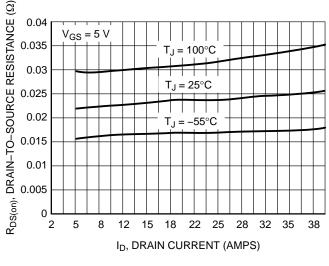


Figure 3. On-Resistance vs. Drain Current and **Temperature** 

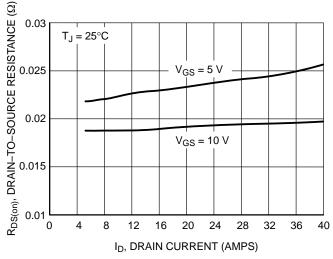


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage** 

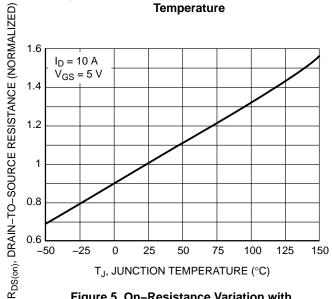


Figure 5. On-Resistance Variation with **Temperature** 

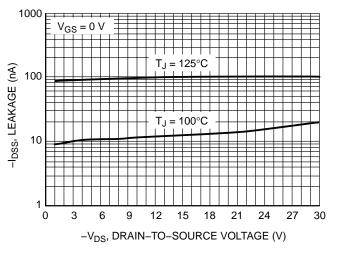


Figure 6. Drain-to-Source Leakage Current vs. Voltage

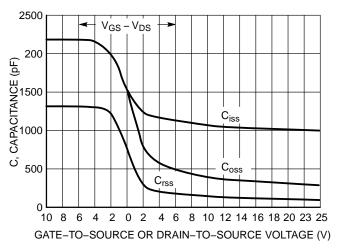


Figure 7. Capacitance Variation

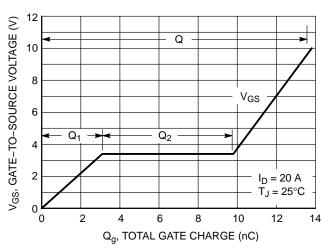


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

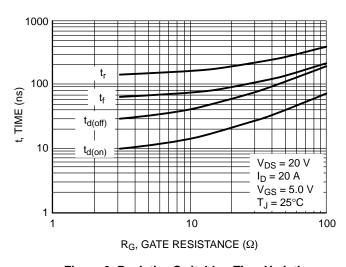


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

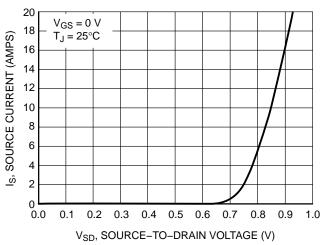


Figure 10. Diode Forward Voltage vs. Current

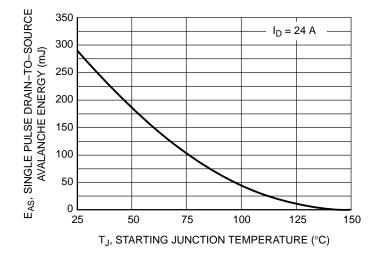
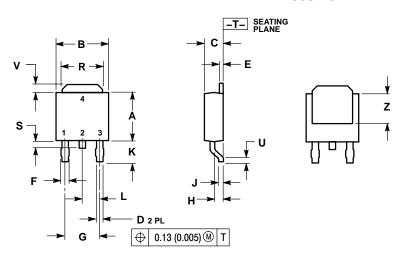


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

# **PACKAGE DIMENSIONS**

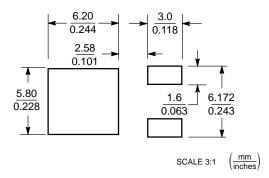
### **DPAK** CASE 369C-01 ISSUE O



	INCHES		MILLIMETE	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020		0.51	
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

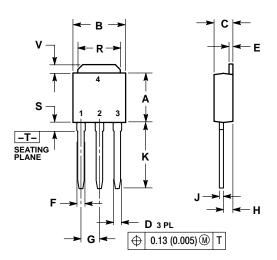
# **SOLDERING FOOTPRINT\***

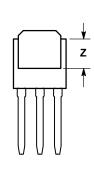


<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

DPAK-3 CASE 369D-01 ISSUE B





- NOTES:
  1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090	.090 BSC		2.29 BSC	
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
K	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
٧	0.035	0.050	0.89	1.27	
Ζ	0.155		3.93		

STYLE 2: PIN 1. GATE

- 2. DRAIN
- 3 SOURCE
- DRAIN

ON Semiconductor and was are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its partnif rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA **Phone**: 480–829–7710 or 800–344–3860 Toll Free USA/Canada **Fax**: 480–829–7709 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.