

MX88L250EC-X MX88L250EC-S MX88L250EC-D Data Sheet

Table of Contentsd

TABLE OF CONTENTSD	2
GENERAL DESCRIPTION	4
APPLICATIONS	4
FEATURES	4
GENERAL FEATURES	4
INPUT	4
OUTPUT	5
CPU INTERFACE	5
POWER	5
CHIP BLOCK DIAGRAM	6
SYSTEM BLOCK DIAGRAM FOR LCD MONITOR (TTL AND PANELLINK / LVDS INTERFACED)	7
ANALOG INTERFACE LCD MONITOR	7
DIGITAL INTERFACE LCD MONITOR	7
MX88L250EC-X, MX88L250EC-S 128P PIN CONFIGURATIONS	8
MX88L250EC-D 160P PIN CONFIGURATIONS	9
GENERAL DESCRIPTION	10
VIP (VIDEO INPUT PROCESSOR) FUNCTION DESCRIPTION	10
VOP (VIDEO OUTPUT PROCESSOR) FUNCTION DESCRIPTION	10
BIU (BUS INTERFACE UNIT) FUNCTION DESCRIPTION	10
PIN DESCRIPTION	11
CPU INTERFACE PINS: (8 / 16 PINS)	11
INPUT INTERFACE PINS: (29 / 53 PINS)	11
LCD INTERFACE PINS: (53 PINS)	12
INTERNAL VCG INTERFACE PINS: (2 PINS)	13
OTHER INTERFACE PINS: (6 PINS)	13
EXTERNAL CLOCK INPUT INTERFACE PINS: (2 PIN)	14
POWER PINS: (28 PINS) DUAL POWER 3.3 / 2.5 VOLTS, 5 VOLT TOLERANT INPUTS	14
AC CHARACTERISTICS	15
1. INPUT SIGNAL	15
2. OUTPUT SIGNAL	16
3. DIRECT CPU INTERFACE	17
4. SERIAL BUS INTERFACE	18
5. EXTERNAL CLOCK INPUT INTERFACE	18
DC CHARACTERISTICS	19

MX88L250EC

Revision: 0.03A
2001/10/12

1. ENVIRONMENTAL SPECIFICATION:	19
2. STANDARD DC SPECIFICATION FOR 3.3 VOLTS OPERATION:	19
DIMENSION	20

MX88L250EC

Revision: 0.03A
2001/10/12

General Description

MX88L250EC Series is the Low Cost yet High Performance Solution for Flat Panel Display application. Applying Macronix' s Smartscaling™-2⁺ filter, it provides high quality scaled video image and format conversion capability.

Applications

- XGA/SXGA LCD monitors

Features

General Features

- MX88L250EC-X and MX88L250EC-S are fully Pin to Pin Compatible.
- Convert PC video signal into flat panel display device timing and resolution.
- Built-in Line Buffer to provide Fame-Buffer-Less solution.
- Support Clock, Phase, Horizontal and Vertical position adjustments.
- Support Auto-Tracking and Auto-Position capabilities (SmartTracking™ Technology).
- Support Auto-Gain capability for input image
- Arbitrary scaling from 1 to 32 times with filters (SmartScaling™ – 2⁺ Technology).
- Support Edge Filter control.
- Built-in OSD generator with 64 ROM /128 programmable RAM fonts, mixer with Color Palette, Color Key and Alpha Blending.
- Provide 90-degree Rotation for internal OSD to support Portrait direction display.
- On-chip Digital Brightness and Contrast adjustments.
- On-chip Digital Gamma Correction for panel compensation.
- Support Temporal Dithering capability to make 18 bit video as good as 24 bit quality.
- Support “Test mode” function which internally generates some test patterns, including gray, saw, and cross talk, for output.

Input

- MX88L250EC-X supports Single port 24bit, PC video up to XGA operation mode.
- MX88L250EC-S supports Single port 24bit, PC video up to SXGA operation mode.

MX88L250EC

Revision: 0.03A
2001/10/12

- MX88L250EC-D supports Dual port 48bit, PC video up to SXGA operation mode
- Support Composite Sync. input.
- Support H/V Sync. Polarity and Pulse Width information for mode detection.
- Support H/V Sync. Interrupt for power management requirement.

Output

- Support TFT LCD panel in following resolution and frequency.

Resolution	800x600	1024x768	1280x1024
Horizontal frequency (KHz)	20 ~ 55	20 ~ 70	80
Vertical frequency (Hz)	50 ~ 75	50 ~ 75	75
Dot clock (MHz)	32.5 ~ 60	25 ~ 80	140

- Single (18/24) and Dual (36/48) bit RGB data output.
- Support Inverse, Delay and Frequency adjustments for LCD panel clock.
- Support programmable H/V sync. and LDTG timing for LCD panel.
- Support two PWM outputs

CPU Interface

- Support Direct Bus 8 bit interface (*MX88L250EC-D only*)
- Support Two/Three-Wire Serial Bus interface.
- Support Double Buffer Register capability.

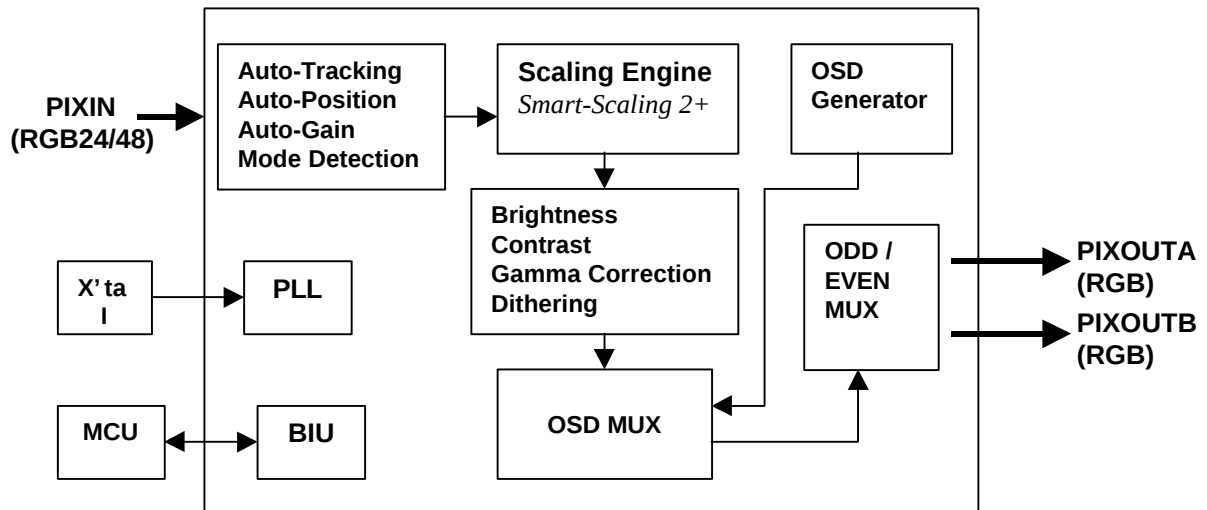
Power

- Power Supplier: Dual Power 3.3/2.5 volts, 5V tolerant inputs.
- Power Consumption: less than 1W.

MX88L250EC

Revision: 0.03A
2001/10/12

Chip Block Diagram

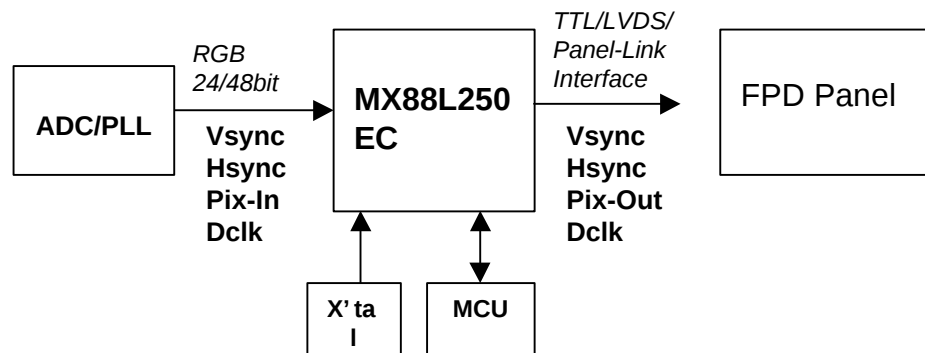


MX88L250EC

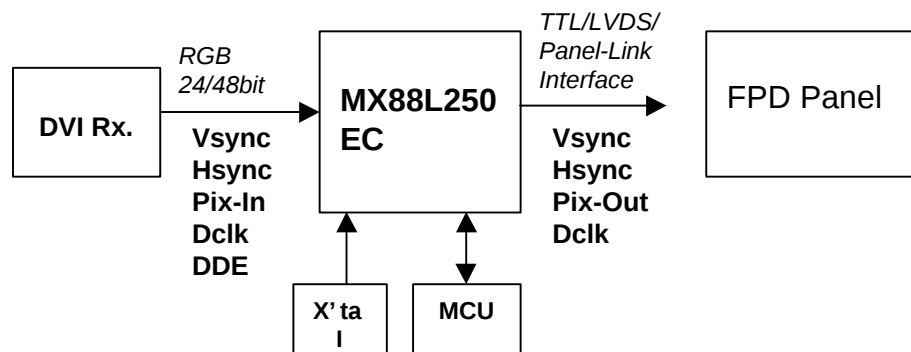
Revision: 0.03A
2001/10/12

System Block Diagram for LCD monitor (TTL and PanelLink / LVDS Interfaced)

Analog Interface LCD monitor



Digital Interface LCD monitor



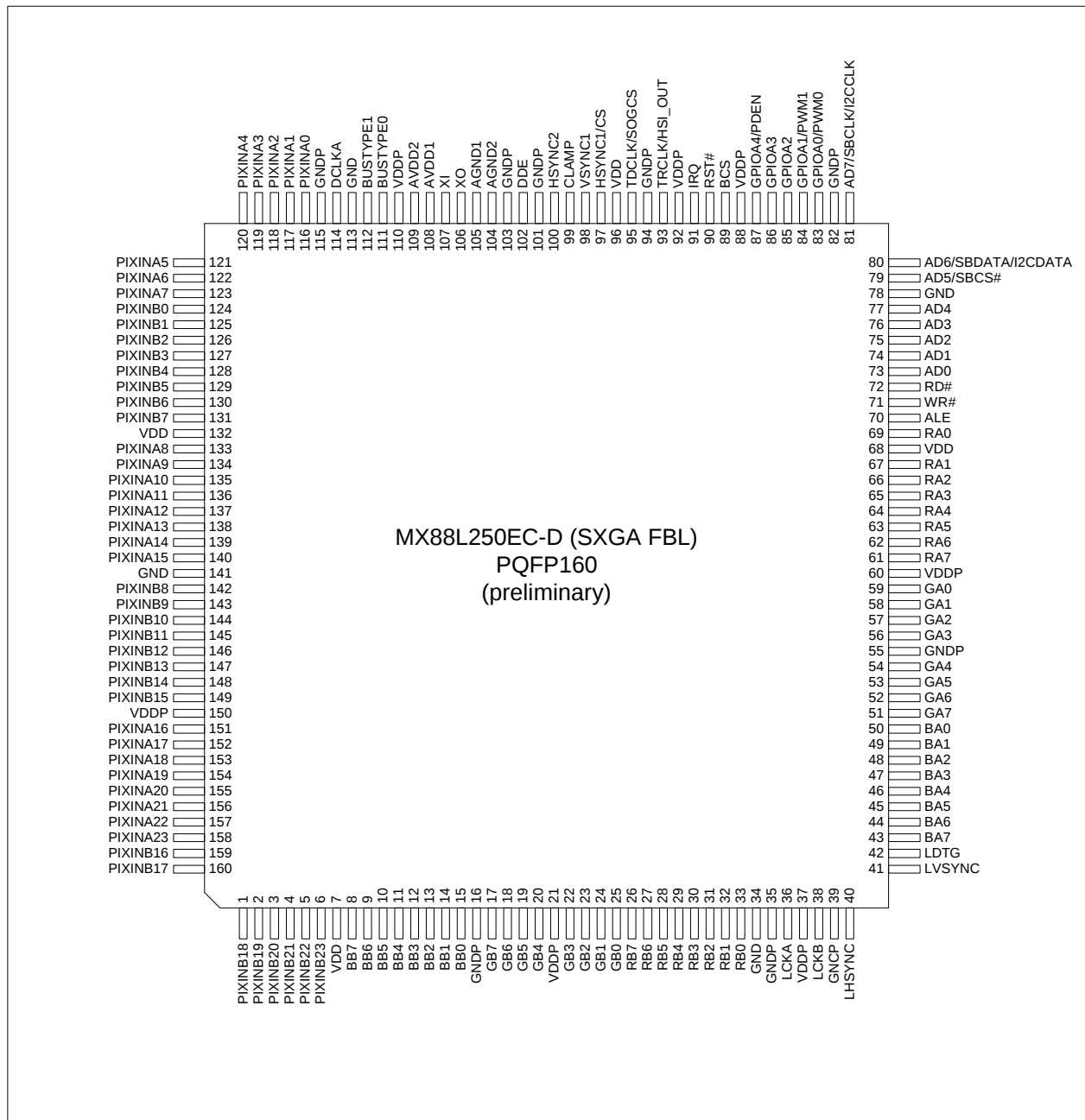
Revision: 0.03A
2001/10/12

MX88L250EC-X (XGA FBL)
MX88L250EC-S (SXGA FBL)
PQFP128
(preliminary)

MX88L250EC

Revision: 0.03A
2001/10/12

MX88L250EC-D 160p Pin Configurations



General Description

There are three major portions in this chip which include VIP (Video Input Processor), VOP (Video Output Processor) and BIU (CPU Bus Interface Unit). Following is the block and description of these portions.

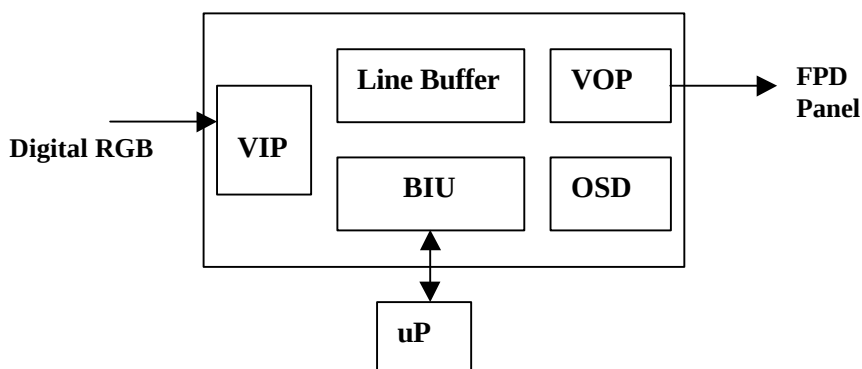


Fig. Chip Level Block Diagram

VIP (Video Input Processor) Function Description

VIP is a video input process unit which receives digital data from ADC or digital input then process it to line buffer for VOP. It supports mode detection, auto-position, auto-gain, auto-tracking function for ADC modification.

VOP (Video Output Processor) Function Description

VOP is a Video Output Process unit which reads data from line buffer and then process it to flat panel display.

With Line Buffers and Scale- up logic based on proprietary Smartscaling™ -2+ algorithm, it can enlarge image smoothly. Furthermore, it provides many adjusting functions like programmable Brightness and Contrast control, programmable GAMMA table, programmable Dithering control, and OSD MUX to adjust the output quality. It also provides Single/Dual output to cope with different flat panels display device.

BIU (Bus Interface Unit) Function Description

BIU is a bus interface unit between the host CPU and MX88L250 which supports two bus types: Direct and Serial Bus.

MX88L250EC

Revision: 0.03A
2001/10/12

Pin Description

CPU Interface Pins: (8 / 16 pins)

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
RST#		I	77	90	System reset.
AD[7:0]		IO	X	81-79 77-73	Multiplexed low order address and data bus
SBCLK / AD7		I	68	81	Two/Three-Wire Serial Bus Clock (share with AD7)
SBDATA / AD6		IO	67	80	Two/Three-Wire Serial Bus Data (share with AD6)
SBCS# / AD5		I	66	79	Three-Wire Serial Bus CS# (low active) (share with AD5)
BCS		I	76	89	Bus Select, Active high.
ALE		I	X	70	Address Latch Enable for 8051 Bus.
WR#		I	X	71	Memory Write Strobe for direct bus
RD#		I	X	72	Memory Read Strobe for direct bus
BUSTYPE1		I	99	112	Bus type bit 1
BUSTYPE0		I	98	111	Bus type bit 0 (NC for MX88L250EC-S & -X)
IRQ		O	78	91	Interrupt request

Input Interface Pins: (29 / 53 pins)

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
PIXINA 0-7		I	103-110	116-123	Input data R0-R7
PIXINA 8-15		I	112-115 117-120	133-140	Input data G0-G7

MX88L250EC

Revision: 0.03A
2001/10/12

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
PIXINA 16-23		I	122-128 1	151-158	Input data B0-B7
PIXINB 0-7		I	X	124-131	Input data R0-R7
PIXINB 8-15		I	X	142-149	Input data G0-G7
PIXINB 16-23		I	X	159-160 1-6	Input data B0-B7
HSYNC1/CS		I	84	97	Hsync input1 (for mode detection)
HSYNC2		I	87	100	Hsync input2 (for screen position & sampling use)
VSYNC1		I	85	98	Vsync input
DDE		I	89	102	Digital Data enable
DCLKA		I	101	114	Input dot clock1

LCD Interface Pins: (53 pins)

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
RA[7:0]	4 mA	O	64 62-56	69 67-61	RED DATA (Odd),
GA[7:0]	4 mA	O	54-51 49-46	59-56 54-51	GREEN DATA (Odd),
BA[7:0]	4 mA	O	45-38	50-43	BLUE DATA (Odd),
RB[7:0]	4 mA	O	28-21	33-26	RED DATA (Even).
GB[7:0]	4 mA	O	20-17 15-12	25-22 20-17	GREEN DATA (Even).
BB[7:0]	4 mA	O	10-3	15-8	BLUE DATA (Even),
LVSYNC	8 mA	O	36	41	VSYNC output for LCD display.

MX88L250EC

Revision: 0.03A
2001/10/12

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
LHSYNC	8 mA	O	35	40	HSYNC output for LCD display.
LDTG	8 mA	O	37	42	Data Enable output for LCD display.
LCKA	16 mA	O	31	36	Odd data clock output for LCD display
LCKB	16 mA	O	33	38	Even data clock output for LCD display.

Internal VCG Interface Pins: (2 pins)

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
XI		I	94	107	Analog pad for Reference Frequency Input for internal oscillator. (3.3 V)
XO		O	93	106	Analog pad for Reference Frequency Output for internal oscillator. (3.3V)

Other Interface Pins: (6 pins)

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
GPIOA0 / PWM0	2 mA	IO	70	83	Pulse width Modulation 0 Output, share with general IO 0
GPIOA1 / PWM1	2 mA	IO	71	84	Pulse width Modulation 1 Output, share with general IO 1
GPIOA2	2 mA	IO	72	85	General IO 2
GPIOA3	2 mA	IO	73	86	General IO 3
GPIOA4 / PDEN	2 mA	IO	74	87	PDEN output for ADC Shared with general IO 4
Clamp		O	86	99	Clamp output for ADC

MX88L250EC

Revision: 0.03A
2001/10/12

External Clock Input Interface Pins: (2 pin)

Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
TRCLK / HS1_OUT		I O	80	93	External RCLK input (share with HS_OUT)
TDCLK / SOGCS		I	82	95	External DCLK input. (share with SOGCS)

Power Pins: (28 pins) dual power 3.3 / 2.5 Volts, 5 Volt tolerant inputs

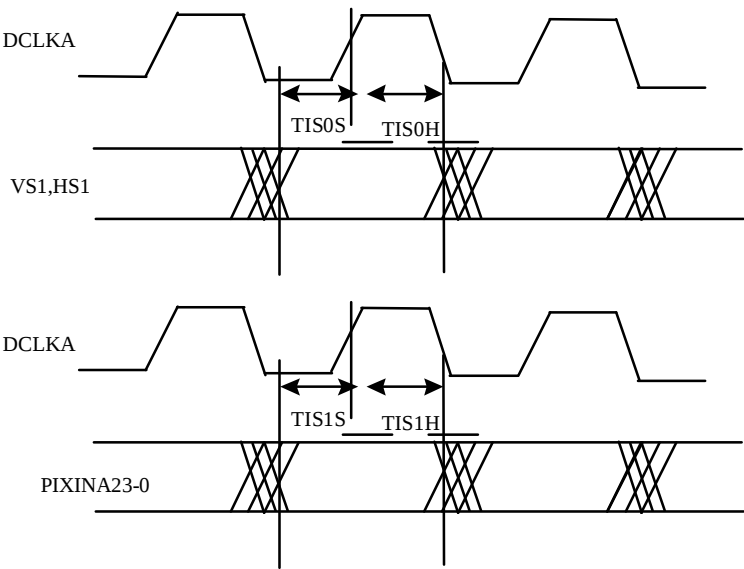
Pin Name	Drive	I/O	Pin No. (L250EC-X) (L250EC-S) 128 pin	Pin No. (L250EC-D) 160 pin	DESCRIPTION
VDD			2,63,83, 111,	7,68,96, 132,	Core Power 2.5 V
GND			29,65, 100,116	34,78,113, 141,	Core GND
VDDP			16,32,55 ,75,79,9 7,121	21,37,60, 88,92,110, 150,	PAD Power 3.3 V
GNDP			11,30,34 ,50,69,8 1,88,90, 102,	16,35,39, 55,82,94, 101,103, 115,	PAD GND
AVDD1 / AVDD2			95,96	108,109	Analog Power 2.5 V
AGND1 / AGND2			91,92	104,105	Analog GND

Remark:

1. All the input loading is 5pf
2. Driving capability is measured under 20pf loading
3. LCKA driving capability is measured under 30pf loading

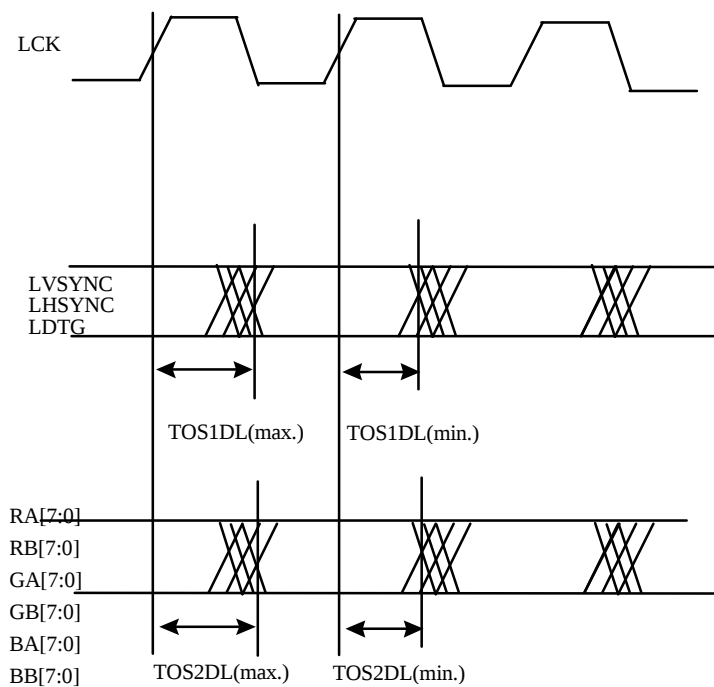
AC Characteristics

1. Input signal



Symbol	Parameter	Min.	Max.	Unit
TIS0S, TIS0H	Setup time	2		ns
TIS1S, TIS1H	Hold time	2		ns

2. Output signal

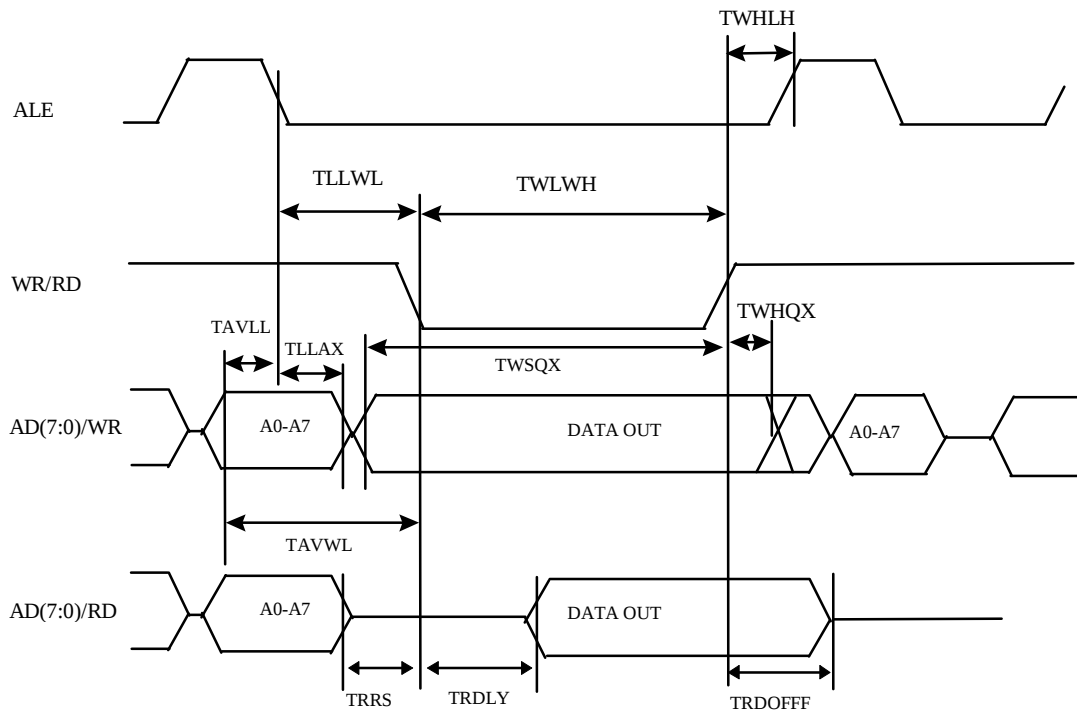


Symbol	Parameter	Min.	Max.	Unit
TOS1DL	Output LHSYNC, LVSYNC, LDTG output delay	1	5	ns
TOS2DL	Output Pixel Signal output delay	1	5	ns

MX88L250EC

Revision: 0.03A
2001/10/12

3. Direct CPU Interface



Symbol	Parameter	Min.	Max.	Unit
TAVLL	Address Valid to ALE Low	2		ns
TLLAX	Address Hold After ALE Low	1		ns
TWLWH	WR Pulse Width	30		ns
TWSQX	Data Setup Before WR	10		ns
TWHQX	Data Hold After WR	0		ns
TWHLH	WR/RD High to ALE High	0		ns
TRDLY	Data delay after RD Low	10	35	ns
TRDOFF	Data off delay after RD High	0	7	ns

4. Serial Bus Interface

Symbol	Parameter	Min.	Max.	Unit
Tcsck	CS to CLK Start	0		ns
Tckcs	CLK to CS high	20		ns
Tds	Data setup time versus CLK	10.1		ns
Tdh	Data hold time versus CLK	20		ns
Tdd	Data delay time	14	18	ns

5. External Clock Input Interface

Symbol	Parameter	Min.	Max.	Unit
Fclk	Maximum TDCLK input frequency		80	MHz
Fpw	Minimum pulse width	3		ns

DC characteristics

1. Environmental specification:

Rating	Value	Unit
Ambient Operating Temperature	0 to 70	°C
Storage Temperature	-55 to 125	°C
Maximum Junction Temperature	125	°C
Maximum Case Temperature	100	°C

2. Standard DC Specification for 3.3 Volts Operation:

(Ta=0°C to 70°C, VCC=3V to 3.6V)

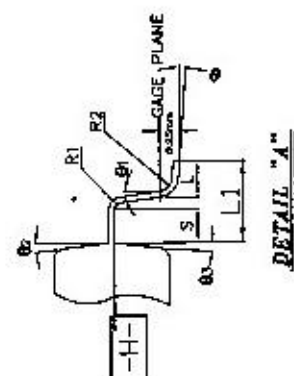
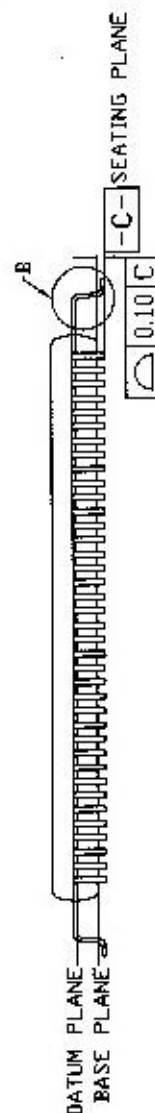
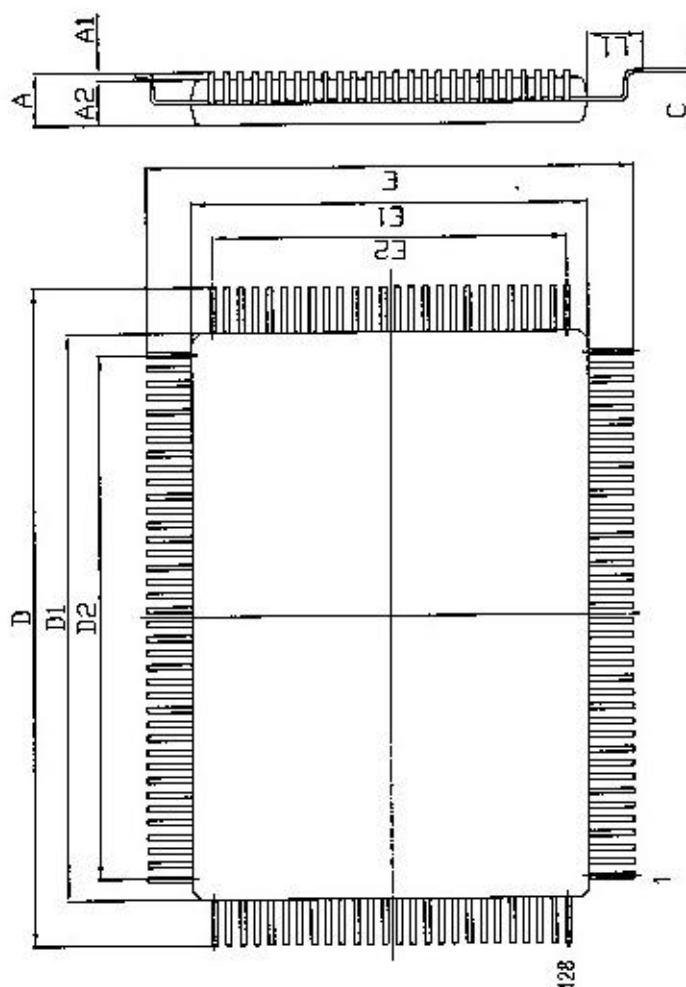
Symbol	Parameter	Min	Max	Unit	Conditions
VOH	Output High Voltage	2.4		V	
VOL	Output Low Voltage		0.4	V	
VIH	Input High Voltage	2.0		V	
VIL	Input Low Voltage		0.8	V	
RPU	I/O Pull-up Resistance	100	300	KOhm	
RPD	I/O Pull-down Resistance	50	150	KOhm	
ILI	Input Leakage Current	-10	+10	μ A	
ILO	Output Leakage Current	-20	+20	μ A	

MX88L250EC

Revision: 0.03A
2001/10/12

Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Max	
A	—	—	0.134	—	—	3.40
A1	0.010	—	—	0.25	—	—
A2	0.098	0.107	0.114	2.50	2.72	2.90
b	0.007	0.008	0.011	0.17	0.20	0.27
C	0.004	0.006	0.009	0.11	0.15	0.23
D	0.913 BSC.			23.20 BSC.		
D1	0.787 BSC.			20.00 BSC.		
D2	0.728 REF			18.50 REF		
E	0.677 BSC.			17.20 BSC.		
E1	0.551 BSC.			14.00 BSC.		
E2	0.492 REF			12.50 REF		
e	0.020 BSC.			0.50 BSC.		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 REF			1.60 REF		
S	0.008	—	—	0.20	—	—
R1	0.005	—	—	0.13	—	—
R2	0.005	—	0.012	0.13	—	0.30
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2	7° REF			7° REF		
θ3	15° REF			15° REF		

REFERENCE DOCUMENT: JEDEC SPEC MO-022



MAC 宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 610-0211.4	
TITLE PACKAGE OUTLINE DIMENSION FOR QFP (28 pins, 20mm) (3.2mm FOOTPRINT)		TOLERANCE DIMENSION ANGLE	
DRAWN C.L.Chang	APPROVED Dennis Chang	DATE 02-22-01	REVISION 0