Inductorless Liquid Lens Driver

Features

- Drives capacitive loads up to 200pF
- Programmable drive amplitude (compatible with $40V_{RMS}$ to $60V_{RMS}$ lenses)
- On-chip boost converter
- No external inductor
- I²C interface
- Low operating current (≤20mA)
- Low standby current (≤1.0µA)
- Controlled drive edge reduces EMI
- 10-Lead 4x4mm DFN Package

Applications

- Cell phone cameras
- PDA and ultracompact cameras
- Bar code readers
- Web and laptop cameras

General Description

The HV892 liquid lens driver is controlled via an I²C interface, is capable of driving capacitive loads of up to 200pF, and is compatible with $40V_{RMS}$ to $60V_{RMS}$ lenses.

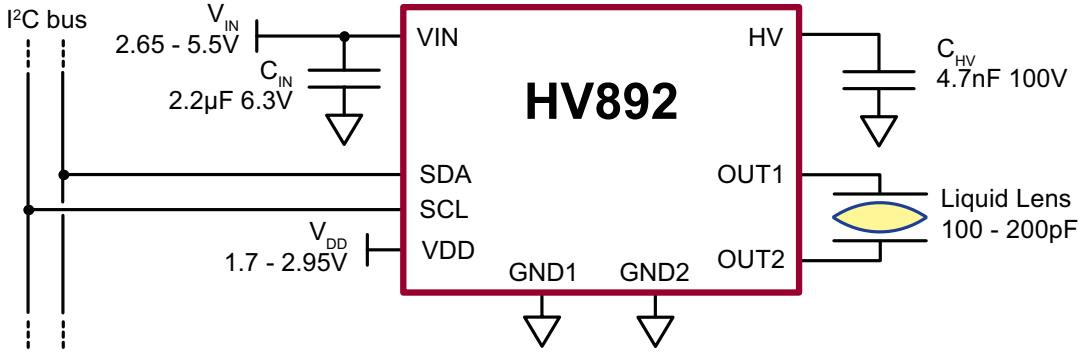
A single byte (AMP) written to the HV892 controls the operation of the driver. Setting AMP = 01h to FFh controls output amplitude in 255 monotonic steps. Setting AMP = 00h causes the HV892 to go into low power standby mode, consuming less than 1.0µA. When active, the HV892 draws less than 20mA.

A charge pump boost converter integrated on-chip provides the high voltage necessary for driving the lens. No external inductors or diodes are needed. Two ceramic chip capacitors are the only external components required for a complete lens driver circuit.

An H-bridge output stage provides AC drive to the lens, allowing the use of a single high voltage boost converter while providing alternating polarity to the lens. Controlled rising and falling edges on the drive waveform reduces EMI.

The HV892 is offered in a 10-Lead 4x4mm DFN package.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV892K7-G	10-Lead DFN (4x4)	3000/Reel

-G indicates package is RoHS compliant ('Green')

ESD Sensitive Device

Absolute Maximum Ratings

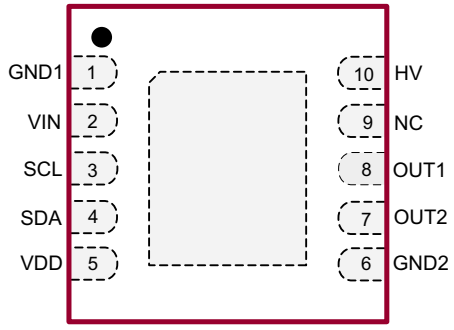
Parameter	Value
V_{IN}, V_{DD}	-0.5V to +6.5V
SDA, SCL	-0.5V to +6.5V
Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	$R_{\theta ja}$
10-Lead DFN (4x4)	44°C/W

Pin Configuration



10-Lead DFN
(top view)

Note:
Pads are at the bottom of the package. Center heat slug is at ground potential

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
___ = "Green" Packaging

Package may or may not include the following marks: Si or

10-Lead DFN

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{IN}	Supply voltage	2.65	-	5.50	V	---
V_{DD}	I²C logic level reference	1.70	-	2.95	V	---
t_{VIN}	Time for V_{IN} to ramp to 90%[1]	-	-	2.0	ms	---
C_{IN}	Supply bypass capacitor	-	2.2	-	µF	---
C_{HV}	High voltage storage capacitor	24	-	-	x C_{LOAD}	100V rating
C_{LOAD}	Load (lens) capacitance	100	150	200	pF	---
f_{SCL}	I²C clock	-	-	400	kHz	---
T_A	Ambient temperature	-25	-	+85	°C	---

Notes:

1. *To assure the driver powers up in standby state. No damage will occur if ramped up slower.*

Electrical Specifications *(Over recommended operating conditions @ T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{IN}	V_{IN} supply current	-	-	500	nA	AMP = 00h, SDA = V_{DD}, SCL = V_{DD}
		-	8.0	20	mA	AMP = FFh, SDA = V_{DD}, SCL = V_{DD}
I_{DD}	V_{DD} supply current	-	-	500	nA	AMP = 00h, SDA = V_{DD}, SCL = V_{DD}
		-	9.0	12	µA	AMP = FFh, SDA = V_{DD}, SCL = V_{DD}
HV	Output voltage of internal boost converter	71	75	79	V	C_{LOAD} = 0pF

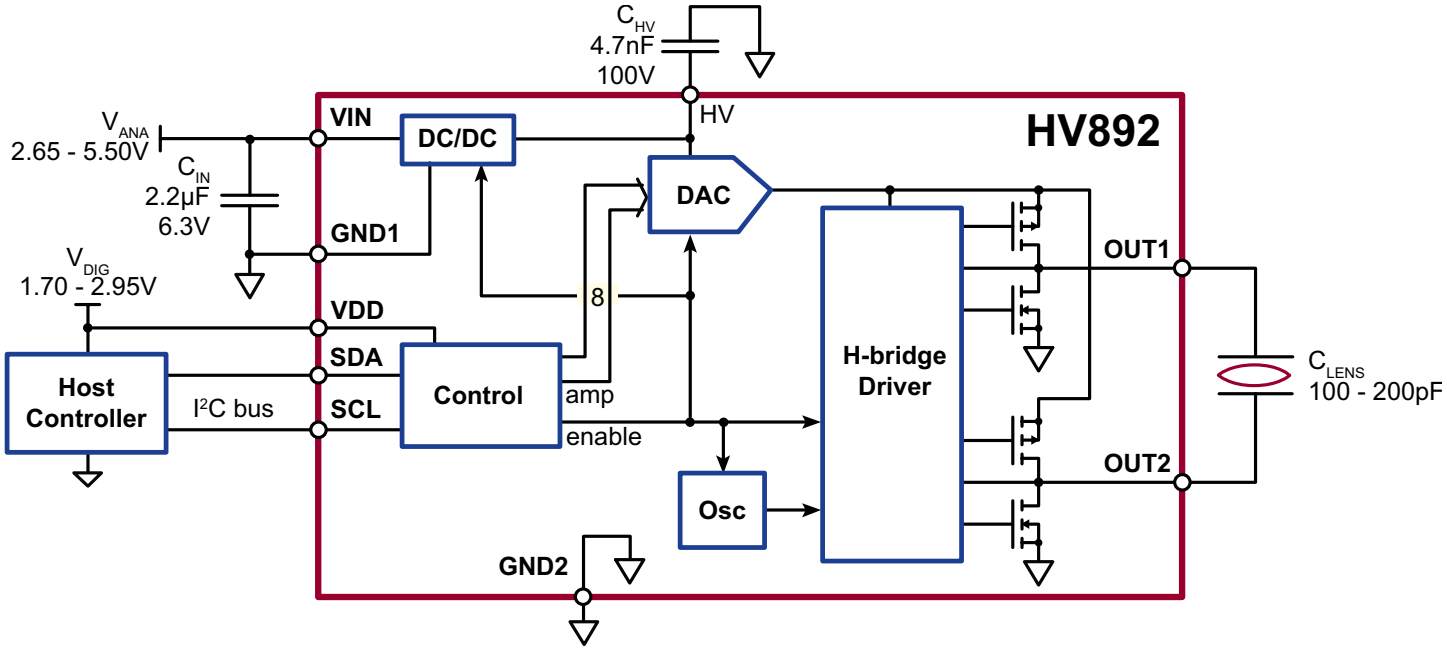
Electrical Specifications *(cont.)(Over recommended operating conditions @ T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{OUT(AC)}$	AC output voltage	-	0	-	V_{RMS}	AMP = 00h
		9.0	10	11		AMP = 01h
		58.5	62.0	65.5		AMP = FFh
$V_{OUT(DC)}$	DC output offset voltage	-2.0	0	+2.0	V	---
DNL	Differential non-linearity (guaranteed monotonic)	-1.0	-	+1.0	LSB	---
f_{OUT}	Output frequency	1.0	1.5	2.0	kHz	---
D_X	Transition time (fraction of period)	-	4.7	-	%	---
dV/dt	Output slope	-	4.7	-	V/µs	C_{LOAD} = 150pF, V_{IN} = 3.8V
t_{SU}	Startup time to 90% amplitude[1]	-	-	20	ms	AMP = 00h → FFh, C_{HV} = 4.7nF
t_A	Amplitude response time[1]	-	-	5.0	ms	Over any 1-step AMP increment or decrement (except 00h)
V_{IL}	Logic low input voltage	-	-	0.30	x V_{DD}	---
V_{IH}	Logic high input voltage	0.7	-	-	x V_{DD}	---
V_{OL}	Logic low output voltage	-	-	0.2	x V_{DD}	I_{LOAD} = 3.0mA
I_L	Logic low input current	-	-	10	µA	V_{DD} = 1.70 - 2.95V
I_H	Logic high input current	-	-	10	µA	V_{DD} = 1.70 - 2.95V
C_{LI}	Logic input capacitance	-	-	10	pF	V_{DD} = 1.70 - 2.95V, grounded or open

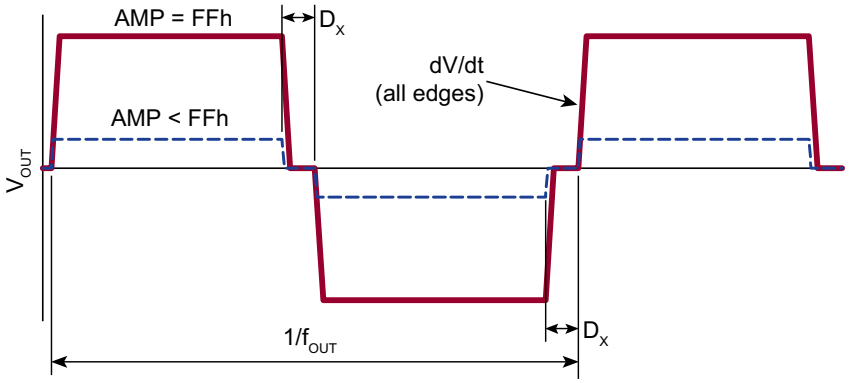
Notes:

1. *Measured from the rising edge of the I²C acknowledge bit that terminates transmission of the AMP data byte.*

Block Diagram and Typical Application



Output Waveform



Applications Information

I²C

The HV892 is a write-only fast mode I²C device. Logic voltages are referenced to V_{DD}.

Address

The HV892 recognizes a 7-bit address. The device is pre-programmed with an I²C address of 0100011b. For other addresses, please contact the factory.

Data

A single byte written to the HV892 controls the operation of the lens driver. See the Command Table below. The MSB is clocked-in first.

Command Table

AMP	Description
00h	Low power standby mode. When in standby mode, the internal boost converter and H-bridge oscillator are shut down, and the OUT pins are held at ground. Any AMP value other than 00h brings the HV892 out of standby mode. The time it takes the HV892 to exit standby mode and achieve full output amplitude is less than 20ms with a 4.7nF capacitor on the HV pin. Faster startup times may be achieved by lowering C_{HV} at the expense of possible waveform distortion.
01h-FFh	Controls output amplitude according to: $V_{OUT(RMS)} = 9.8V_{RMS} + AMP \bullet 205mV_{RMS}$

Supplies

V_{IN} should be ramped up in less than 2.0ms to assure the driver starts-up in standby mode. If brought up slower, the driver may not start-up in standby mode, with output amplitude at an indeterminate level. In this case, writing AMP = 00h brings the driver to standby mode. No damage will occur if ramped slower than 2.0ms.

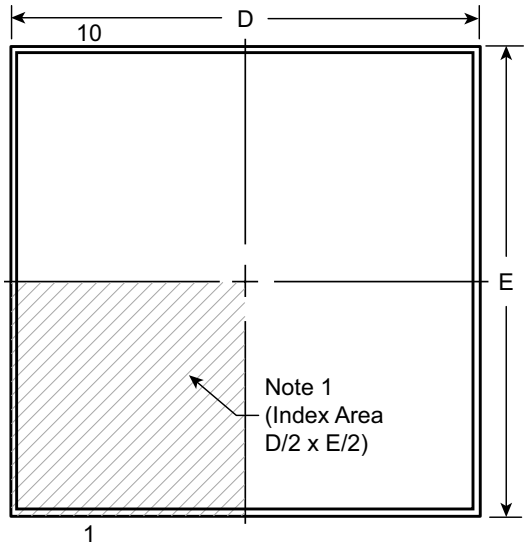
Pin Functions

Pin	Name	Description
1	GND1	Ground for the DC–DC converter. Connect GND1 and GND2 together close to the IC.
2	VIN	Input voltage. Bypass with a 2.2µF capacitor to GND1.
3	SCL	Clock for the I²C interface. The HV892 is a Fast Mode device (f_{SCL} ≤ 400kHz).
4	SDA	Serial data for the I²C interface. The HV892 is a write-only device, with a single 8-bit command byte (AMP, see page 4).
5	VDD	Externally supplied reference voltage for the I²C logic levels. Connect to the I²C bus supply.
6	GND2	Ground for the IC except the DC-DC converter. Connect GND1 and GND2 together close to the IC.
7	OUT2	Outputs of the H-bridge driver. The liquid lens connects between these two pins. When disabled (AMP = 00h), both of these outputs are held at ground.
8	OUT1	
9	NC	Not connected.
10	HV	High voltage DC output of the internal boost converter. Connect a 4.7nF, 100V ceramic capacitor to ground close to the IC.

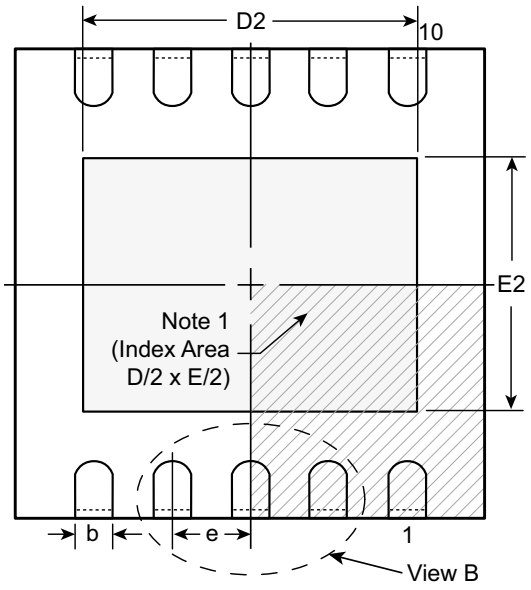
Exposed backside pad is at ground potential and should be connected to circuit ground.

10-Lead DFN Package Outline (K7)

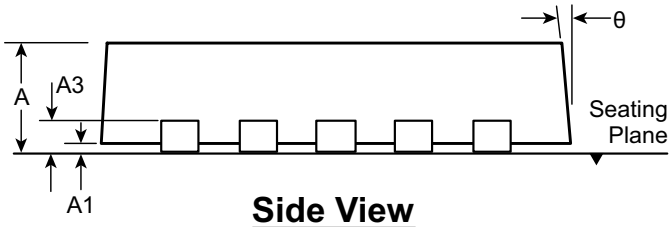
4.00x4.00mm body, 0.80mm height (max), 0.65mm pitch



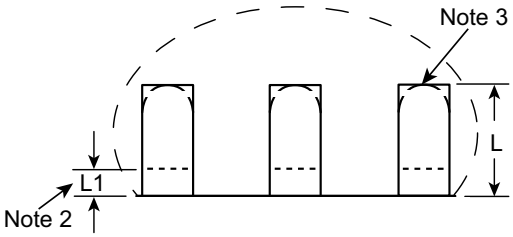
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.25	3.85*	2.80	3.85*	2.30	0.65 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.30	4.00	-	4.00	-		0.40	-	-
	MAX	0.80	0.05		0.35	4.15*	3.50	4.15*	2.80		0.50	0.15	14°

JEDEC Registration MO-229, Variation WGGC, Issue C, Aug. 2003.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
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