

# 16-Kbit (2 K × 8) AutoStore™ nvSRAM

## Features

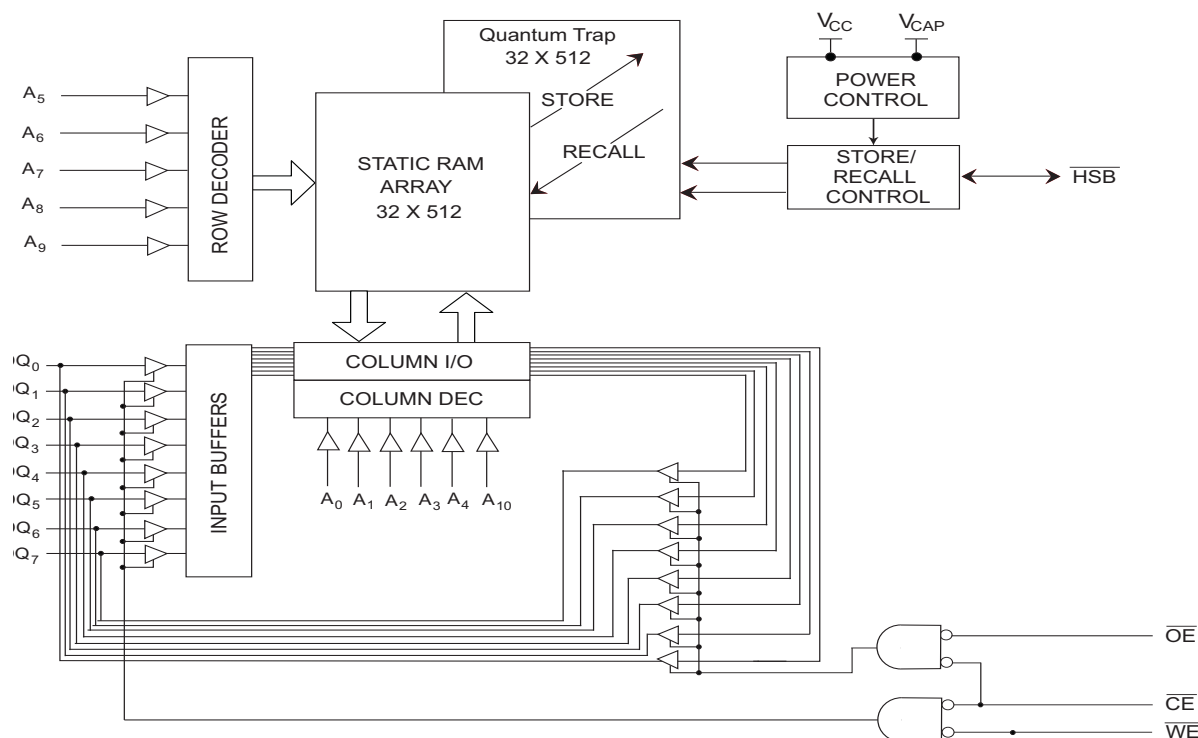
- 25 ns and 45 ns access times
- Hands off automatic STORE on power-down with external 68  $\mu$ F capacitor
- STORE to QuantumTrap™ nonvolatile elements is initiated by software, hardware, or AutoStore™ on power-down
- RECALL to SRAM initiated by software or power-up
- Unlimited read, write, and RECALL cycles
- 1,000,000 STORE cycles to QuantumTrap
- 100 year data retention to QuantumTrap
- Single 5 V  $\pm$ 10% operation
- Commercial and industrial temperatures
- 28-pin 300 mil and (330 mil) Small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

## Functional Description

The Cypress STK22C48 is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. A hardware STORE is initiated with the HSB pin.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

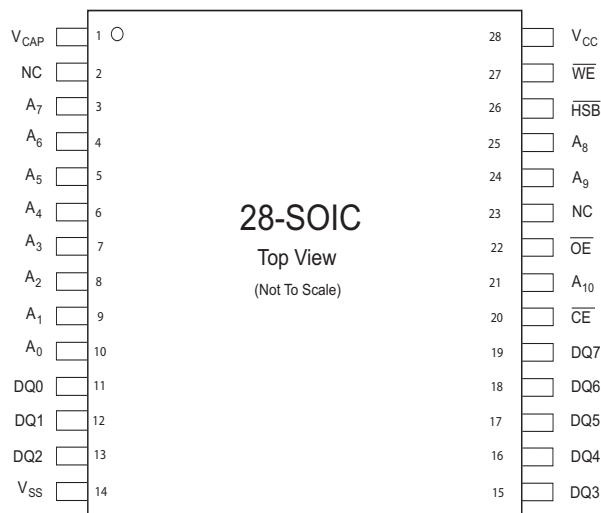


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## Pin Configurations

**Figure 1. Pin Diagram - 28-pin SOIC**



**Table 1. Pin Definitions**

| Pin Name         | Alt            | IO Type         | Description   |
|------------------|----------------|-----------------|---|
| $A_0$ – $A_{10}$ |                | Input           | <b>Address inputs.</b> Used to select one of the 2,048 bytes of the nvSRAM.   |
| DQ0–DQ7          |                | Input or output | <b>Bidirectional data IO lines.</b> Used as input or output lines depending on operation.   |
| $\overline{WE}$  | $\overline{W}$ | Input           | <b>Write enable input, active LOW.</b> When the chip is enabled and $\overline{WE}$ is LOW, data on the IO pins is written to the specific address location.  |
| $\overline{CE}$  | $\overline{E}$ | Input           | <b>Chip enable input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.  |
| $\overline{OE}$  | $\overline{G}$ | Input           | <b>Output enable, active LOW.</b> The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the IO pins to tri-state.  |
| $V_{SS}$         |                | Ground          | <b>Ground for the device.</b> The device is connected to ground of the system.  |
| $V_{CC}$         |                | Power supply    | <b>Power supply inputs to the device.</b>   |
| $\overline{HSB}$ |                | Input or output | <b>Hardware Store Busy (HSB).</b> When LOW, this output indicates a Hardware Store is in progress. When pulled low external to the chip, it initiates a nonvolatile STORE operation. A weak internal pull-up resistor keeps this pin high if not connected (connection optional). |
| $V_{CAP}$        |                | Power supply    | <b>AutoStore capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.   |
| NC               |                | No connect      | <b>No connect.</b> This pin is not connected to the die.  |

## Device Operation

The STK22C48 nvSRAM is made up of two functional components paired in the same physical cell. These are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture enables the storage and recall of all cells in parallel. During the STORE and RECALL operations, SRAM Read and Write operations are inhibited. The STK22C48 supports unlimited reads and writes similar to a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to one million STORE operations.

## SRAM Read

The STK22C48 performs a Read cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are LOW while WE and HSB are HIGH. The address specified on pins A<sub>0-10</sub> determines the 2,048 data bytes accessed. When the Read is initiated by an address transition, the outputs are valid after a delay of t<sub>AA</sub> (Read cycle 1). If the Read is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs are valid at t<sub>ACE</sub> or at t<sub>DOE</sub>, whichever is later (Read cycle 2). The data outputs repeatedly respond to address changes within the t<sub>AA</sub> access time without the need for transitions on any control input pins, and remains valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought HIGH, or WE or HSB is brought LOW.

## SRAM Write

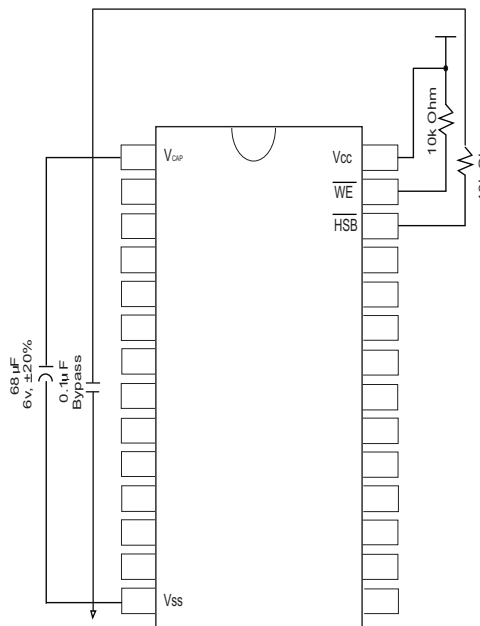
A Write cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are LOW and HSB is HIGH. The address inputs must be stable prior to entering the Write cycle and must remain stable until either  $\overline{CE}$  or WE goes HIGH at the end of the cycle. The data on the common I/O pins DQ<sub>0-7</sub> are written into the memory if it has valid t<sub>SD</sub>, before the end of a WE controlled Write or before the end of an  $\overline{CE}$  controlled Write. Keep  $\overline{OE}$  HIGH during the entire Write cycle to avoid data bus contention on common I/O lines. If  $\overline{OE}$  is left LOW, internal circuitry turns off the output buffers t<sub>HZWE</sub> after WE goes LOW.

## AutoStore Operation

During normal operation, the device draws current from V<sub>CC</sub> to charge a capacitor connected to the V<sub>CAP</sub> pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V<sub>CC</sub> pin drops below V<sub>SWITCH</sub>, the part automatically disconnects the V<sub>CAP</sub> pin from V<sub>CC</sub>. A STORE operation is initiated with power provided by the V<sub>CAP</sub> capacitor.

Figure 2 shows the proper connection of the storage capacitor (V<sub>CAP</sub>) for automatic store operation. A charge storage capacitor between 68  $\mu$ F and 220  $\mu$ F ( $\pm 20\%$ ) rated at 6 V should be

**Figure 2. AutoStore Mode**

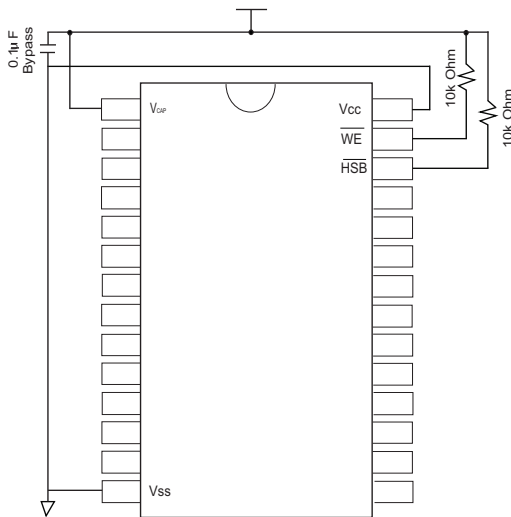


In system power mode, both V<sub>CC</sub> and V<sub>CAP</sub> are connected to the +5 V power supply without the 68  $\mu$ F capacitor. In this mode, the AutoStore function of the STK22C48 operates on the stored system charge as power goes down. The user must, however, guarantee that V<sub>CC</sub> does not drop below 3.6 V during the 10 ms STORE cycle.

To prevent unneeded STORE operations, automatic STORES and those initiated by externally driving HSB LOW are ignored, unless at least one WRITE operation takes place since the most recent STORE or RECALL cycle. An optional pull-up resistor is shown connected to HSB. This is used to signal the system that the AutoStore cycle is in progress.

## AutoStore Inhibit mode

If an automatic STORE on power loss is not required, then V<sub>CC</sub> is tied to ground and +5 V is applied to V<sub>CAP</sub> (Figure 3 on page 5). This is the AutoStore Inhibit mode, where the AutoStore function is disabled. If the STK22C48 is operated in this configuration, references to V<sub>CC</sub> are changed to V<sub>CAP</sub> throughout this data sheet. In this mode, STORE operations are triggered with the HSB pin. It is not permissible to change between these three options "on the fly".

**Figure 3. AutoStore Inhibit Mode**


## Hardware STORE (HSB) Operation

The STK22C48 provides the  $\overline{\text{HSB}}$  pin for controlling and acknowledging the STORE operations. The  $\overline{\text{HSB}}$  pin is used to request a hardware STORE cycle. When the  $\overline{\text{HSB}}$  pin is driven LOW, the STK22C48 conditionally initiates a STORE operation after  $t_{\text{DELAY}}$ . An actual STORE cycle only begins if a Write to the SRAM takes place since the last STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, while the STORE (initiated by any means) is in progress. Pull-up this pin with an external 10 K ohm resistor to  $V_{\text{CAP}}$  if  $\overline{\text{HSB}}$  is used as a driver.

SRAM Read and Write operations, that are in progress when  $\overline{\text{HSB}}$  is driven LOW by any means, are given time to complete before the STORE operation is initiated. After  $\overline{\text{HSB}}$  goes LOW, the STK22C48 continues SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM Read operations take place. If a Write is in progress when  $\overline{\text{HSB}}$  is pulled LOW, it allows a time,  $t_{\text{DELAY}}$  to complete. However, any SRAM Write cycles requested after  $\overline{\text{HSB}}$  goes LOW are inhibited until  $\overline{\text{HSB}}$  returns HIGH.

During any STORE operation, regardless of how it is initiated, the STK22C48 continues to drive the  $\overline{\text{HSB}}$  pin LOW, releasing it only when the STORE is complete. After completing the STORE operation, the STK22C48 remains disabled until the  $\overline{\text{HSB}}$  pin returns HIGH.

If  $\overline{\text{HSB}}$  is not used, it is left unconnected.

## Hardware RECALL (Power Up)

During power-up or after any low power condition ( $V_{\text{CC}} < V_{\text{RESET}}$ ), an internal RECALL request is latched. When  $V_{\text{CC}}$  once again exceeds the sense voltage of  $V_{\text{SWITCH}}$ , a RECALL cycle is automatically initiated and takes  $t_{\text{HRECALL}}$  to complete.

## Data Protection

The STK22C48 protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and Write operations. The low voltage condition is detected when  $V_{\text{CC}}$  is less than  $V_{\text{SWITCH}}$ . If the STK22C48 is in a Write mode (both  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  are low) at power-up after a RECALL or after a STORE, the Write is inhibited until a negative transition on  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  is detected. This protects against inadvertent writes during power-up or brown out conditions.

## Noise Considerations

The STK22C48 is a high speed memory. It must have a high frequency bypass capacitor of approximately 0.1  $\mu\text{F}$  connected between  $V_{\text{CC}}$  and  $V_{\text{SS}}$ , using leads and traces that are as short as possible. As with all high speed CMOS ICs, careful routing of power, ground, and signals reduce circuit noise.

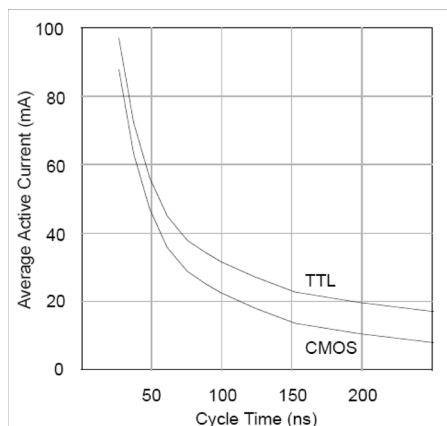
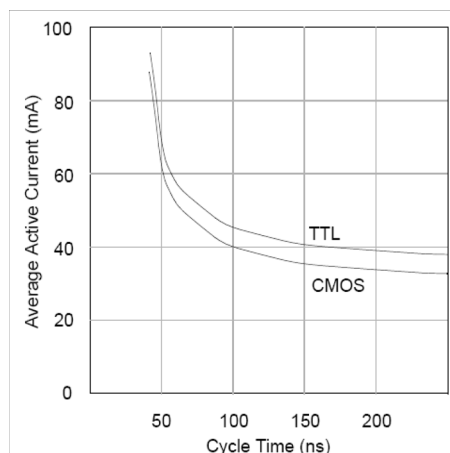
## Hardware Protect

The STK22C48 offers hardware protection against inadvertent STORE operation and SRAM Writes during low voltage conditions. When  $V_{\text{CAP}} < V_{\text{SWITCH}}$ , all externally initiated STORE operations and SRAM Writes are inhibited. AutoStore can be completely disabled by tying  $V_{\text{CC}}$  to ground and applying +5 V to  $V_{\text{CAP}}$ . This is the AutoStore Inhibit mode; in this mode, STORES are only initiated by explicit request using either the software sequence or the  $\overline{\text{HSB}}$  pin.

## Low Average Active Power

CMOS technology provides the STK22C48 the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. Figure 4 on page 6 shows the relationship between  $I_{\text{CC}}$  and Read or Write cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range,  $V_{\text{CC}} = 5.5 \text{ V}$ , 100% duty cycle on chip enable). Only standby current is drawn when the chip is disabled. The overall average current drawn by the STK22C48 depends on the following items:

- The duty cycle of chip enable
- The overall cycle rate for accesses
- The ratio of Reads to Writes
- CMOS versus TTL input levels
- The operating temperature
- The  $V_{\text{CC}}$  level
- I/O loading

**Figure 4. Current Versus Cycle Time (Read)**

**Figure 5. Current Versus Cycle Time (Write)**


## Preventing Store

The STORE function is disabled by holding  $\overline{\text{HSB}}$  high with a driver capable of sourcing 30 mA at a  $V_{\text{OH}}$  of at least 2.2 V, because it must overpower the internal pull-down device. This

**Table 2. Hardware Mode Selection**

| $\overline{\text{CE}}$ | $\overline{\text{WE}}$ | $\overline{\text{HSB}}$ | A10–A0 | Mode              | I/O           | Power                           |
|------------------------|------------------------|-------------------------|--------|-------------------|---------------|---------------------------------|
| H                      | X                      | H                       | X      | Not selected      | Output high Z | Standby                         |
| L                      | H                      | H                       | X      | Read SRAM         | Output data   | Active <sup>[1]</sup>           |
| L                      | L                      | H                       | X      | Write SRAM        | Input data    | Active                          |
| X                      | X                      | L                       | X      | Nonvolatile STORE | Output high Z | $I_{\text{CC2}}$ <sup>[2]</sup> |

### Notes

1. I/O state assumes  $\overline{\text{OE}} \leq V_{\text{IL}}$ . Activation of nonvolatile cycles does not depend on state of  $\overline{\text{OE}}$ .
2. HSB STORE operation occurs only if an SRAM Write is done since the last nonvolatile cycle. After the STORE (if any) completes, the part goes into standby mode, inhibiting all operations until HSB rises.

device drives  $\overline{\text{HSB}}$  LOW for 20 ns at the onset of a STORE. When the STK22C48 is connected for AutoStore operation (system  $V_{\text{CC}}$  connected to  $V_{\text{CC}}$  and a 68  $\mu\text{F}$  capacitor on  $V_{\text{CAP}}$ ) and  $V_{\text{CC}}$  crosses  $V_{\text{SWITCH}}$  on the way down, the STK22C48 attempts to pull HSB LOW. If  $\overline{\text{HSB}}$  does not actually get below  $V_{\text{IL}}$ , the part stops trying to pull HSB LOW and abort the STORE attempt.

## Best Practices

nvSRAM products have been used effectively for over 15 years. While ease of use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. The end product's firmware should not assume that an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on must always program a unique NV pattern (for example, complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power-up boot firmware routines should rewrite the nvSRAM into the desired state. While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, and so on).
- The  $V_{\text{CAP}}$  value specified in this data sheet includes a minimum and a maximum value size. The best practice is to meet this requirement and not exceed the maximum  $V_{\text{CAP}}$  value because the higher inrush currents may reduce the reliability of the internal pass transistor. Customers who want to use a larger  $V_{\text{CAP}}$  value to make sure there is extra store charge should discuss their  $V_{\text{CAP}}$  size selection with Cypress.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Temperature under bias..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  relative to  $V_{SS}$ ..... -0.5 V to 7.0 V

Voltage on input relative to  $V_{SS}$  ..... -0.6 V to  $V_{CC} + 0.5$  V

Voltage on  $DQ_{0-7}$  or  $\overline{HSB}$  ..... -0.5 V to  $V_{CC} + 0.5$  V

Power dissipation ..... 1.0 W

DC output current (1 output at a time, 1 s duration) .... 15 mA

## Operating Range

| Range      | Ambient Temperature | $V_{CC}$       |
|------------|---------------------|----------------|
| Commercial | 0 °C to +70 °C      | 4.5 V to 5.5 V |
| Industrial | -40 °C to +85 °C    | 4.5 V to 5.5 V |

## DC Electrical Characteristics

Over the operating range ( $V_{CC} = 4.5$  V to 5.5 V) [3]

| Parameter                       | Description   | Test Conditions   |            | Min                   | Max                   | Unit     |
|---------------------------------|---|---|------------|-----------------------|-----------------------|----------|
| I <sub>CC1</sub>                | Average V <sub>CC</sub> current   | t <sub>RC</sub> = 25 ns<br>t <sub>RC</sub> = 45 ns<br>Dependent on output loading and cycle rate.<br>Values obtained without output loads.<br>I <sub>OUT</sub> = 0 mA.                            | Commercial | –                     | 85<br>65              | mA<br>mA |
|                                 |   |   | Industrial | –                     | 90<br>65              | mA<br>mA |
| I <sub>CC2</sub>                | Average V <sub>CC</sub> current during STORE                                    | All inputs Do Not Care, V <sub>CC</sub> = Max<br>Average current for duration t <sub>STORE</sub>  |            | –                     | 3                     | mA       |
| I <sub>CC3</sub>                | Average V <sub>CC</sub> current at t <sub>RC</sub> = 200 ns, 5 V, 25 °C typical | WE ≥ (V <sub>CC</sub> – 0.2 V). All other inputs cycling.<br>Dependent on output loading and cycle rate. Values obtained without output loads.  |            | –                     | 10                    | mA       |
| I <sub>CC4</sub>                | Average V <sub>CAP</sub> current during AutoStore cycle                         | All inputs Do Not Care, V <sub>CC</sub> = Max<br>Average current for duration t <sub>STORE</sub>  |            | –                     | 2                     | mA       |
| I <sub>SB1</sub> <sup>[4]</sup> | Average Vcc current (Standby, cycling TTL input levels)                         | t <sub>RC</sub> = 25 ns, $\overline{CE} \geq V_{IH}$<br>t <sub>RC</sub> = 45 ns, $\overline{CE} \geq V_{IH}$  | Commercial | –                     | 25<br>18              | mA<br>mA |
|                                 |   |   | Industrial | –                     | 26<br>19              | mA<br>mA |
| I <sub>SB2</sub> <sup>[4]</sup> | V <sub>CC</sub> standby current   | CE ≥ (V <sub>CC</sub> – 0.2 V). All others V <sub>IN</sub> ≤ 0.2 V or ≥ (V <sub>CC</sub> – 0.2 V).<br>Standby current level after nonvolatile cycle is complete.<br>Inputs are static. f = 0 MHz. |            | –                     | 1.5                   | mA       |
| I <sub>ILK</sub>                | Input leakage current   | V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>  |            | –1                    | +1                    | μA       |
| I <sub>OLK</sub>                | Off state output leakage current  | V <sub>CC</sub> = Max, V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , CE or OE ≥ V <sub>IH</sub> or WE ≤ V <sub>IL</sub>   |            | –5                    | +5                    | μA       |
| V <sub>IH</sub>                 | Input HIGH voltage  |   |            | 2.2                   | V <sub>CC</sub> + 0.5 | V        |
| V <sub>IL</sub>                 | Input LOW voltage   |   |            | V <sub>SS</sub> – 0.5 | 0.8                   | V        |
| V <sub>OH</sub>                 | Output HIGH voltage   | I <sub>OUT</sub> = –4 mA except HSB   |            | 2.4                   | –                     | V        |
| V <sub>OL</sub>                 | Output LOW voltage  | I <sub>OUT</sub> = 8 mA except HSB  |            | –                     | 0.4                   | V        |
| V <sub>BL</sub>                 | Logic ‘0’ voltage on HSB output   | I <sub>OUT</sub> = 3 mA   |            | –                     | 0.4                   | V        |
| V <sub>CAP</sub>                | Storage capacitor   | Between V <sub>CAP</sub> pin and Vss, 6 V rated. 68 μF –10%, +20% nom.  |            | 61                    | 220                   | μF       |

## Data Retention and Endurance

| Parameter | Description                  | Min   | Unit  |
|-----------|------------------------------|-------|-------|
| $DATA_R$  | Data retention               | 100   | Years |
| $NV_C$    | Nonvolatile STORE operations | 1,000 | K     |

### Notes

- $V_{CC}$  reference levels throughout this data sheet refer to  $V_{CC}$  if that is where the power supply connection is made, or  $V_{CAP}$  if  $V_{CC}$  is connected to ground.
- $\overline{CE} \geq V_{IH}$  does not produce standby current levels until any nonvolatile cycle in progress has timed out.



## Capacitance

In the following table, the capacitance parameters are listed.<sup>[5]</sup>

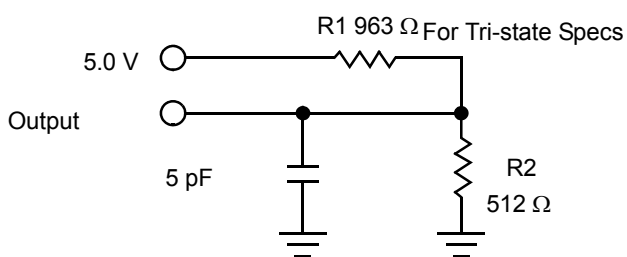
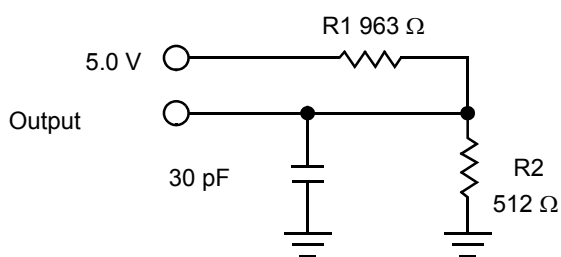
| Parameter        | Description        | Test Conditions  | Max | Unit |
|------------------|--------------------|--|-----|------|
| C <sub>IN</sub>  | Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz,<br>V <sub>CC</sub> = 0 to 3.0 V | 8   | pF   |
| C <sub>OUT</sub> | Output capacitance |  | 7   | pF   |

## Thermal Resistance

In the following table, the thermal resistance parameters are listed.<sup>[5]</sup>

| Parameter       | Description                                 | Test Conditions  | 28-SOIC<br>(300 mil) | 28-SOIC<br>(330 mil) | Unit |
|-----------------|---|--|----------------------|----------------------|------|
| Θ <sub>JA</sub> | Thermal resistance<br>(junction to ambient) | Test conditions follow standard test methods<br>and procedures for measuring thermal<br>impedance, per EIA / JESD51. | TBD                  | TBD                  | °C/W |
| Θ <sub>JC</sub> | Thermal resistance<br>(junction to case)    |  | TBD                  | TBD                  | °C/W |

**Figure 6. AC Test Loads**



## AC Test Conditions

Input pulse levels..... 0 V to 3 V  
 Input rise and fall times (10% to 90%)..... ≤ 5 ns  
 Input and output timing reference levels ..... 1.5 V

### Note

5. These parameters are guaranteed by design and are not tested.



## AC Switching Characteristics

### SRAM Read Cycle

| Parameter         |                      | Description                       | 25 ns |     | 45 ns |     | Unit |
|-------------------|----------------------|-----------------------------------|-------|-----|-------|-----|------|
| Cypress Parameter | Alt                  |                                   | Min   | Max | Min   | Max |      |
| $t_{ACE}$         | $t_{ELQV}$           | Chip enable access time           | –     | 25  | –     | 45  | ns   |
| $t_{RC}^{[6]}$    | $t_{AVAV}, t_{ELEH}$ | Read cycle time                   | 25    | –   | 45    | –   | ns   |
| $t_{AA}^{[7]}$    | $t_{AVQV}$           | Address access time               | –     | 25  | –     | 45  | ns   |
| $t_{DOE}$         | $t_{GLQV}$           | Output enable to data valid       | –     | 10  | –     | 20  | ns   |
| $t_{OHA}^{[7]}$   | $t_{AXQX}$           | Output hold after address change  | 5     | –   | 5     | –   | ns   |
| $t_{LZCE}^{[8]}$  | $t_{ELQX}$           | Chip enable to output active      | 5     | –   | 5     | –   | ns   |
| $t_{HZCE}^{[8]}$  | $t_{EHQZ}$           | Chip disable to output inactive   | –     | 10  | –     | 15  | ns   |
| $t_{LZOE}^{[8]}$  | $t_{GLQX}$           | Output enable to output active    | 0     | –   | 0     | –   | ns   |
| $t_{HZOE}^{[8]}$  | $t_{GHQZ}$           | Output disable to output inactive | –     | 10  | –     | 15  | ns   |
| $t_{PU}^{[9]}$    | $t_{ELICCH}$         | Chip enable to power active       | 0     | –   | 0     | –   | ns   |
| $t_{PD}^{[9]}$    | $t_{EHICCL}$         | Chip disable to power standby     | –     | 25  | –     | 45  | ns   |

### Switching Waveforms

Figure 7. SRAM Read Cycle 1: Address Controlled <sup>[6, 7]</sup>

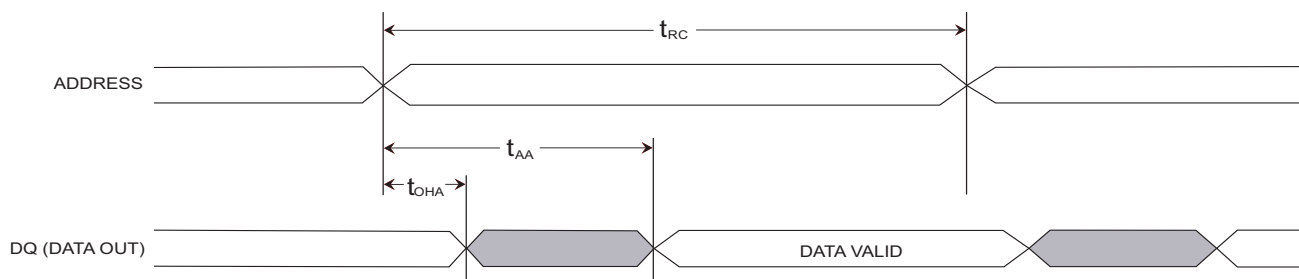
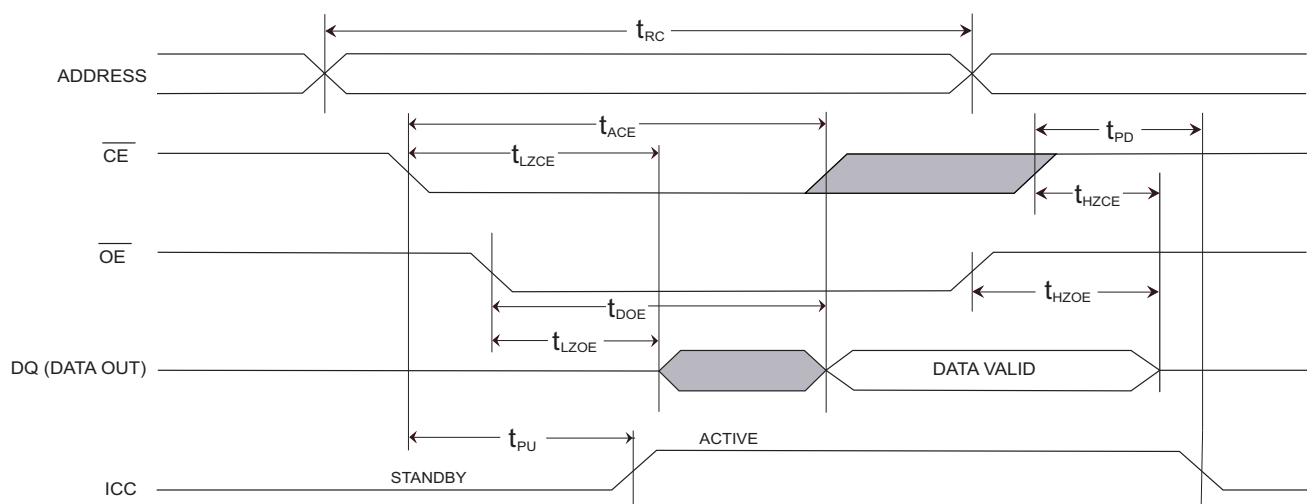


Figure 8. SRAM Read Cycle 2:  $\overline{CE}$  and  $\overline{OE}$  Controlled <sup>[6]</sup>



#### Notes

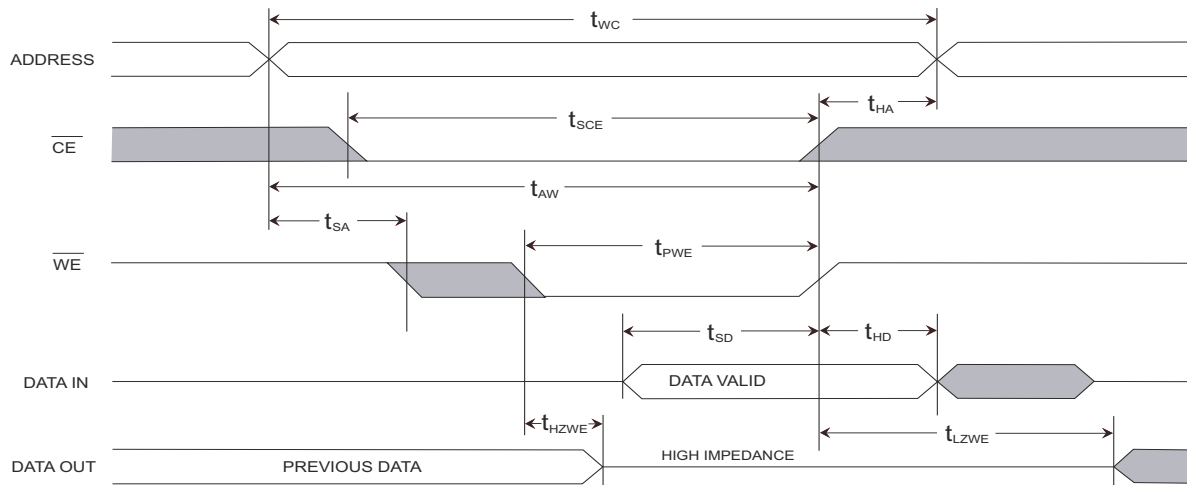
- WE and HSB must be High during SRAM Read cycles.
- Device is continuously selected with CE and OE both Low.
- Measured  $\pm 200$  mV from steady state output voltage.
- These parameters are guaranteed by design and are not tested.

## SRAM Write Cycle

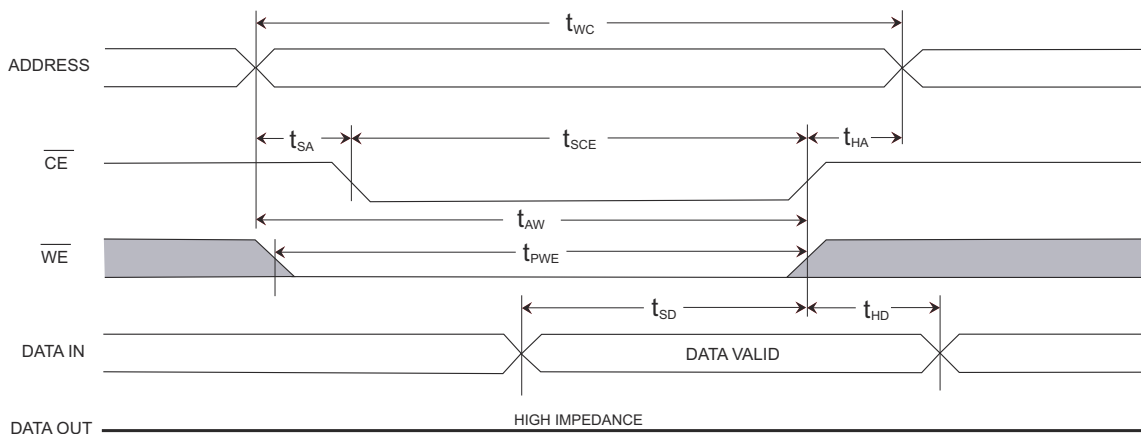
| Parameter             |                         | Description                      | 25 ns |     | 45 ns |     | Unit |
|-----------------------|-------------------------|----------------------------------|-------|-----|-------|-----|------|
| Cypress Parameter     | Alt                     |                                  | Min   | Max | Min   | Max |      |
| $t_{WC}$              | $t_{AVAV}$              | Write cycle time                 | 25    | –   | 45    | –   | ns   |
| $t_{PWE}$             | $t_{WLWH}$ , $t_{WLEH}$ | Write pulse width                | 20    | –   | 30    | –   | ns   |
| $t_{SCE}$             | $t_{ELWH}$ , $t_{ELEH}$ | Chip enable to end of write      | 20    | –   | 30    | –   | ns   |
| $t_{SD}$              | $t_{DVWH}$ , $t_{DVEH}$ | Data setup to end of write       | 10    | –   | 15    | –   | ns   |
| $t_{HD}$              | $t_{WHDX}$ , $t_{EHDX}$ | Data hold after end of write     | 0     | –   | 0     | –   | ns   |
| $t_{AW}$              | $t_{AVWH}$ , $t_{AVEH}$ | Address setup to end of write    | 20    | –   | 30    | –   | ns   |
| $t_{SA}$              | $t_{AVWL}$ , $t_{AVEL}$ | Address setup to start of write  | 0     | –   | 0     | –   | ns   |
| $t_{HA}$              | $t_{WHAX}$ , $t_{EHAX}$ | Address hold after end of write  | 0     | –   | 0     | –   | ns   |
| $t_{HZWE}^{[10, 11]}$ | $t_{WLQZ}$              | Write enable to output disable   | –     | 10  | –     | 14  | ns   |
| $t_{LZWE}^{[10]}$     | $t_{WHQX}$              | Output active after end of write | 5     | –   | 5     | –   | ns   |

## Switching Waveforms

**Figure 9. SRAM Write Cycle 1:  $\overline{WE}$  Controlled** [12, 13]



**Figure 10. SRAM Write Cycle 2:  $\overline{CE}$  Controlled** [12, 13]



### Notes

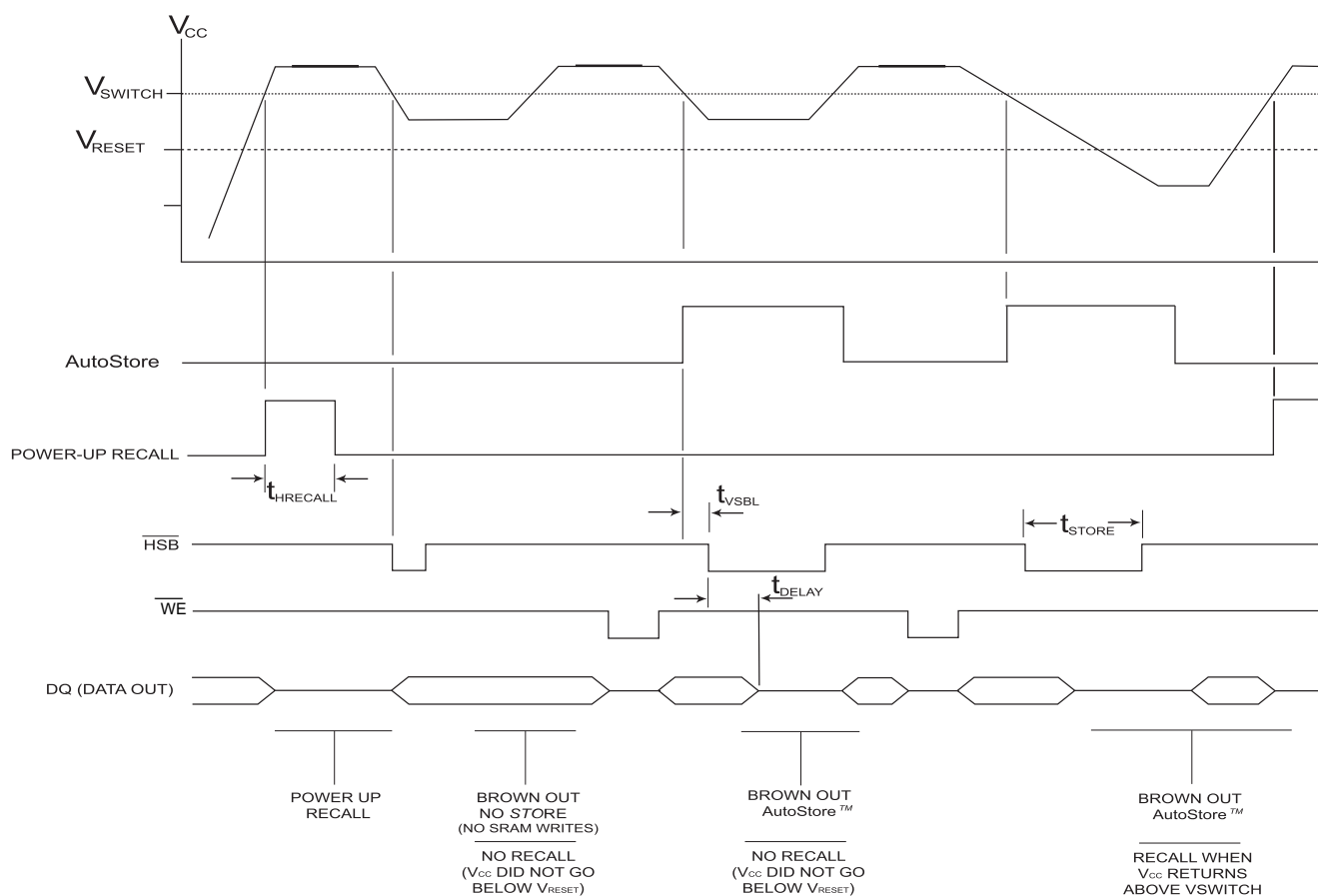
10. Measured  $\pm 200$  mV from steady state output voltage.
11. If  $\overline{WE}$  is Low when  $\overline{CE}$  goes Low, the outputs remain in the high impedance state.
12. HSB must be high during SRAM Write cycles.
13.  $\overline{CE}$  or  $\overline{WE}$  must be greater than  $V_{IH}$  during address transitions.

## AutoStore or Power Up RECALL

| Parameter              | Alt                  | Description                                     | STK22C48 |     | Unit    |
|------------------------|----------------------|---|----------|-----|---------|
|                        |                      |   | Min      | Max |         |
| $t_{HRECALL}^{[14]}$   | $t_{RESTORE}$        | Power Up RECALL duration                        | –        | 550 | $\mu s$ |
| $t_{STORE}^{[15, 16]}$ | $t_{HLHZ}$           | STORE cycle duration                            | –        | 10  | ms      |
| $t_{DELAY}^{[17]}$     | $t_{HLQZ}, t_{BLQZ}$ | Time allowed to complete SRAM cycle             | 1        | –   | $\mu s$ |
| $V_{SWITCH}$           |                      | Low voltage trigger level                       | 4.0      | 4.5 | V       |
| $V_{RESET}$            |                      | Low voltage reset level                         | –        | 3.6 | V       |
| $t_{VSBL}^{[18]}$      |                      | Low voltage trigger ( $V_{SWITCH}$ ) to HSB Low | –        | 300 | ns      |

## Switching Waveform

Figure 11. AutoStore/Power Up RECALL



### Notes

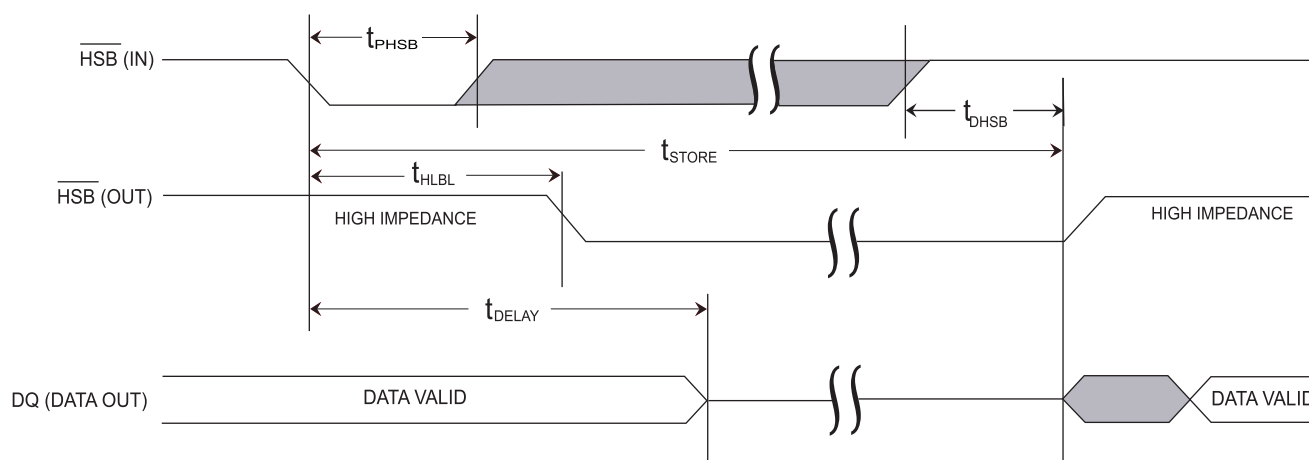
14.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
15. CE and OE low and WE high for output behavior.
16. HSB is asserted low for 1us when  $V_{CAP}$  drops through  $V_{SWITCH}$ . If an SRAM Write has not taken place since the last nonvolatile cycle, HSB is released and no store takes place.
17. CE and OE low for output behavior.
18. HSB must be high during SRAM Write cycles.

## Hardware STORE Cycle

| Parameter                    | Alt                                   | Description                        | STK22C48 |     | Unit |
|------------------------------|---------------------------------------|------------------------------------|----------|-----|------|
|                              |                                       |                                    | Min      | Max |      |
| $t_{\text{DHSB}}^{[19, 20]}$ | $t_{\text{RECOVER}}, t_{\text{HHQX}}$ | Hardware STORE HIGH to inhibit off | –        | 700 | ns   |
| $t_{\text{PHSB}}$            | $t_{\text{HLHX}}$                     | Hardware STORE pulse width         | 15       | –   | ns   |
| $t_{\text{HLBL}}$            |                                       | Hardware STORE LOW to STORE busy   | –        | 300 | ns   |

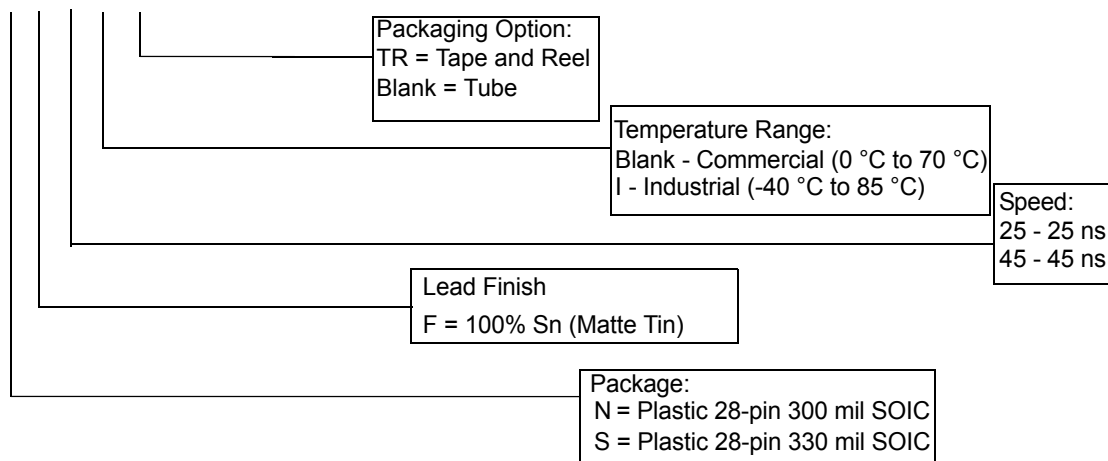
## Switching Waveform

Figure 12. Hardware STORE Cycle



### Notes

19.  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  low and  $\overline{\text{WE}}$  high for output behavior.
20.  $t_{\text{DHSB}}$  is only applicable after  $t_{\text{STORE}}$  is complete.

**Ordering Code Definitions**
**STK22C48 - N F 45 I TR**

**Ordering Information**

These parts are not recommended for new designs. They are in production to support ongoing production programs only.

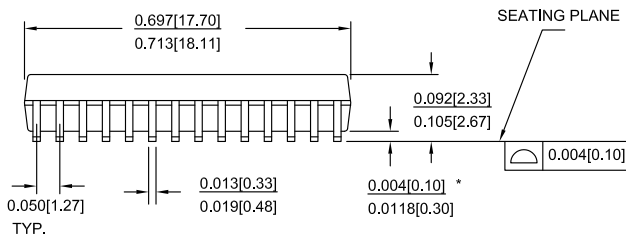
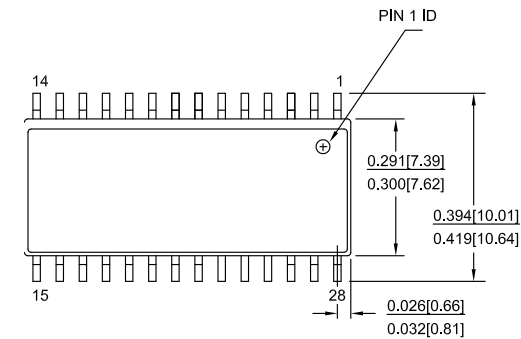
| Speed (ns) | Ordering Code    | Package Diagram | Package Type          | Operating Range |
|------------|------------------|-----------------|-----------------------|-----------------|
| 25         | STK22C48-NF25ITR | 51-85026        | 28-pin SOIC (300 mil) | Industrial      |
|            | STK22C48-NF25I   | 51-85026        | 28-pin SOIC (300 mil) |                 |
|            | STK22C48-SF25ITR | 51-85058        | 28-pin SOIC (330 mil) |                 |
|            | STK22C48-SF25I   | 51-85058        | 28-pin SOIC (330 mil) |                 |
| 45         | STK22C48-NF45TR  | 51-85026        | 28-pin SOIC (300 mil) | Commercial      |
|            | STK22C48-NF45    | 51-85026        | 28-pin SOIC (300 mil) |                 |

All parts are Pb-free. The above table contains Final information. Please contact your local Cypress sales representative for availability of these parts

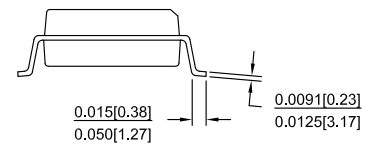
## Package Diagrams

**Figure 13. 28-Pin (300 mil) SOIC (51-85026)**

28 Lead (300 Mil) SOIC – S21

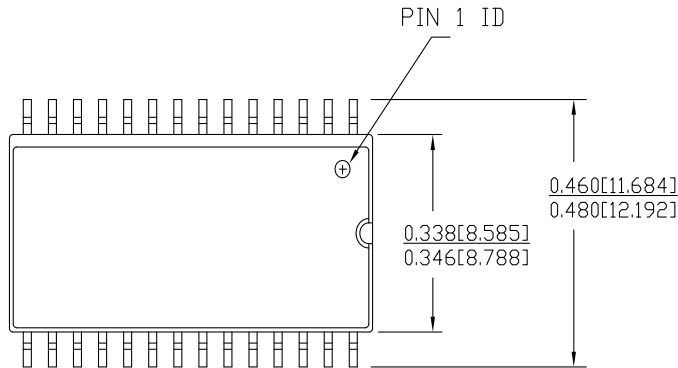


| PART # |                |
|--------|----------------|
| S28.3  | STANDARD PKG.  |
| SZ28.3 | LEAD FREE PKG. |
| SX28.3 | LEAD FREE PKG. |



51-85026 \*H

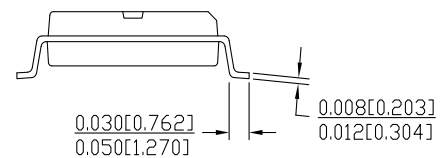
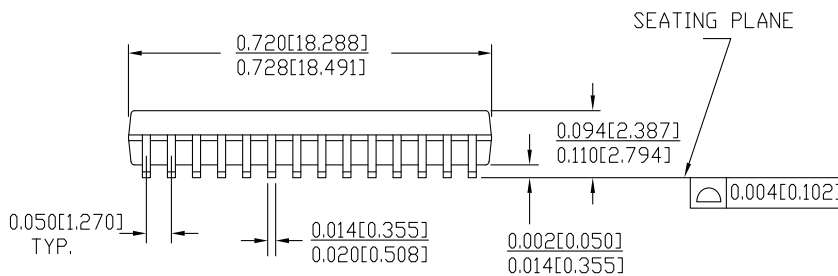
**Figure 14. 28-Pin (330 mil) SOIC (51-85058)**



DIMENSIONS IN INCHES[MM] MIN.  
MAX.

PACKAGE WEIGHT 0.79gms

| PART #  |                |
|---------|----------------|
| S28.33  | STANDARD PKG.  |
| SZ28.33 | LEAD FREE PKG. |



51-85058 \*C

## Document Conventions

### Acronyms

| Acronym | Description                             |
|---------|---|
| CMOS    | Complementary metal oxide semiconductor |
| EIA     | Electronic Industries Alliance          |
| I/O     | Input/output                            |
| nvSRAM  | nonvolatile static random access memory |
| RoHS    | Restriction of hazardous substances     |
| SOIC    | Small outline integrated circuit        |

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| Kb     | 1024 bits       |
| °C     | degree Celsius  |
| Hz     | Hertz           |
| KΩ     | kilo ohms       |
| MHz    | megahertz       |
| μA     | microamperes    |
| μF     | microfarads     |
| μs     | microseconds    |
| mA     | milliamperes    |
| ms     | milliseconds    |
| ns     | nanoseconds     |
| Ω      | ohms            |
| pF     | picofarads      |
| V      | Volts           |
| W      | Watts           |



## Document History Page

| Document Title: STK22C48 16-Kbit (2 K × 8) AutoStore™ nvSRAM<br>Document Number: 001-51000 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Rev.   | ECN No. | Orig. of Change | Submission Date | Description of Change  |
| **   | 2625139 | GVCH/PYRS       | 01/30/2009      | New data sheet   |
| *A   | 2826441 | GVCH            | 12/11/2009      | Added following text in the Ordering Information section: "These parts are not recommended for new designs. In production to support ongoing production programs only."<br>Added watermark in PDF stating "Not recommended for new designs. In production to support ongoing production programs only."<br>Added Contents on page 2. |
| *B   | 3037216 | GVCH            | 09/23/2010      | Added <a href="#">Pin Configurations</a> and <a href="#">Pin Definitions</a> table.<br>Updated <a href="#">Package Diagrams</a> .<br>Added <a href="#">Acronyms</a> and units <a href="#">Units of Measure</a> table.<br>Minor edits.  |
| *C   | 3054310 | GVCH/KEER       | 10/11/2010      | Removed inactive parts - STK22C48-NF25, STK22C48-NF25TR, STK22C48-SF25, STK22C48-SF25TR, STK22C48-SF45, STK22C48-SF45TR, STK22C48-NF45I, STK22C48-NF45ITR from Ordering information table.<br>Updated Package diagrams.  |
| *D   | 3189527 | GVCH            | 03/07/2011      | Added watermark in PDF stating "Not recommended for new designs. In production to support ongoing production programs only."   |
| *E   | 3531563 | GVCH            | 02/23/2012      | <a href="#">Package Diagrams</a> : Updated 28-Pin (330 Mil) SOIC package diagram   |
| *F   | 4576271 | GVCH            | 11/24/2014      | Added documentation related hyperlink in page 1<br>Removed pruned parts - STK22C48-NF25ITR, STK22C48-NF25I, STK22C48-SF25ITR, STK22C48-SF25I, STK22C48-NF45TR, STK22C48-NF45<br>Updated package diagram 51-85026*F to 51-85026*H   |

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