

12-Bit to 24-Bit Registered Bus Exchanger with 3-State Outputs

Product Features

- Designed for low voltage operation
- $V_{CC} = 2.3V$ to $3.6V$
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce)
< 0.8V at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- Typical V_{OHV} (Output V_{OH} Undershoot)
< 2.0V at $V_{CC} = 3.3V$, $T_A = 25^\circ C$
- Bus Hold retains last active bus state during 3-state eliminates the need for external pullup resistors
- Industrial operation at $-40^\circ C$ to $+85^\circ C$
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

Product Description

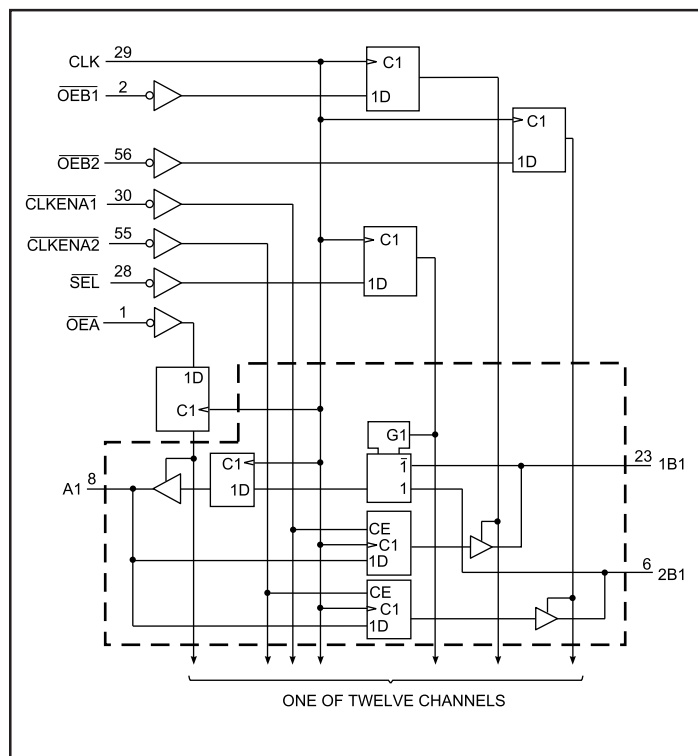
The PI74ALVCH16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAM's and high-speed microprocessors.

Data is stored on the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKENA}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB1}$, and $\overline{OEB2}$).

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Because $\overline{OE}$ is being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock
$\overline{SEL}$	Select (Active Low)
$\overline{CLKEN}$	Clock Enable (Active Low)
A,1B,2B	3-State Outputs
GND	Ground
VCC	Power

Truth Tables⁽¹⁾

Inputs			Outputs	
CLK	$\overline{OEA}$	$\overline{OEB}$	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

Product Pin Configuration

$\overline{OEA}$	1	56	$\overline{OEB2}$
$\overline{OEB1}$	2	55	$\overline{CLKENA2}$
2B3	3	54	2B4
GND	4	53	GND
2B2	5	52	2B5
2B1	6	51	2B6
VCC	7	50	VCC
A1	8	49	2B7
A2	9	48	2B8
A3	10	47	2B9
GND	11	46	GND
A4	12	45	2B10
A5	13	44	2B11
A6	14	43	2B12
A7	15	42	1B12
A8	16	41	1B11
A9	17	40	1B10
GND	18	39	GND
A10	19	38	1B9
A11	20	37	1B8
A12	21	36	1B7
VCC	22	35	VCC
1B1	23	34	1B6
1B2	24	33	1B5
GND	25	32	GND
1B3	26	31	1B4
NC	27	30	$\overline{CLKENA1}$
$\overline{SEL}$	28	29	CLK

A to B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	1B ₀ ⁽²⁾	2B ₀ ⁽²⁾
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

B to A STORAGE ($\overline{OEA} = L$)

Inputs				Outputs A
CLK	$\overline{SEL}$	1B	2B	
X	H	X	X	A0 ⁽²⁾
X	L	X	X	A0 ⁽²⁾
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

Notes:

- H = High Signal Level
L = Low Signal Level
X = Irrelevant
Z = High Impedance
↑ = Transition, Low to High
- Output level before indicated steady state input conditions established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage Range, V_{CC}	–0.5V to 4.6V
Input Voltage Range, V_I : Except	
I/O ports ⁽¹⁾	–0.5V to 4.6V
I/O ports ^(1,2)	–0.5V to $V_{CC} + 0.5V$
Output Voltage Range, V_O ^(1,2)	–0.5V to $V_{CC} + 0.5V$
Input Clamp current, I_{IK} ($V_I < 0$)	–50mA
Output Clamp current, I_{OK} ($V_O < 0$)	–50mA
Continuous Output Current, I_O	±50mA
Continuous Current through each V_{CC} or GND	±100mA
Maximum Power Dissipation:	
A package	1W
V package	1.4W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6V maximum.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3V \pm 10\%$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.3V$ to $2.7V$	1.7			
		$V_{CC} = 2.7V$ to $3.6V$	2.0			
V_{IL}	Input LOW Voltage	$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 2.7V$ to $3.6V$			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	HIGH-level Output Current	$V_{CC} = 2.3V$			–12	mA
		$V_{CC} = 2.7V$			–12	
		$V_{CC} = 3.0V$			–24	
I_{OL}	LOW-level Output Current	$V_{CC} = 2.3V$			12	
		$V_{CC} = 2.7V$			12	
		$V_{CC} = 3.0V$			24	
T_A	Operating Free-Air Temperature		–40		85	°C
$At/\Delta V$	Input Transition Rise or Fall Rate				10	ns/V

(Table Continued)

DC Electrical Characteristics-Continued (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$)

Parameters	Test Conditions	$V_{CC}^{(1)}$	Min.	Typ. ⁽²⁾	Max.	Units
V_{OH}	$I_{OH} = -100\mu\text{A}$	Min. to Max.	$V_{CC} - 0.2$			V
	$I_{OH} = -6\text{mA}$	2.3V	2.0			
	$I_{OH} = -12\text{mA}$	2.3V	1.7			
		2.7V	2.2			
		3.0V	2.4			
	$I_{OH} = -24\text{mA}$	3.0V	2.0			
V_{OL}	$I_{OL} = 100\mu\text{A}$	Min. to Max.			0.2	V
	$I_{OL} = 6\text{mA}$	2.3V			0.4	
	$I_{OL} = 12\text{mA}$	2.3V			0.7	
		2.7V			0.4	
	$I_{OL} = 24\text{mA}$	3.0V			0.55	
I_I	$V_I = V_{CC}$ or GND	3.6V			± 5	μA
I_I (Hold) ⁽³⁾	$V_I = 0.7\text{V}$	2.3V	45			
	$V_I = 1.7\text{V}$		-45			
	$V_I = 0.8\text{V}$	3.0V	75			
	$V_I = 2.0\text{V}$		-75			
	$V_I = 0$ to 3.6V	3.6V			± 500	
$I_{OZ}^{(4)}$	$V_O = V_{CC}$ or GND	3.6V			± 10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6V			40	
ΔI_{CC}	One input at $V_{CC} - 0.6\text{V}$, Other inputs at V_{CC} or GND	3V to 3.6V			750	
C_I Control Inputs	$V_I = V_{CC}$ or GND	3.3V		3.5		pF
C_{IO} A or B Ports	$V_O = V_{CC}$ or GND	3.3V		8.5		

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient and maximum loading.
3. Bus hold maximum dynamic current required to switch the input from one state to another
4. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency			135		135		135	MHz
t_w	Pulse duration, CLK High or Low		3.3		3.3		3.3		ns
t_{SU}	Setup time	A data before CLK $\uparrow$	2.0		2.0		1.7		
		B data before CLK $\uparrow$	2.2		2.1		1.8		
		$\overline{SEL}$ before CLK $\uparrow$	1.6		1.6		1.3		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK $\uparrow$	1.0		1.2		0.9		
		$\overline{OE}$ data before CLK $\uparrow$	1.5		1.6		1.3		
t_H	Hold time	A data after CLK $\uparrow$	0.7		0.6		0.6		
		B data after CLK $\uparrow$	0.7		0.6		1.6		
		$\overline{SEL}$ after CLK $\uparrow$	1.1		0.7		0.7		
		$\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK $\uparrow$	1.0		0.8		1.1		
		$\overline{OE}$ after CLK $\uparrow$	0.8		0.8		0.8		

Switching Characteristics over Operating Range⁽¹⁾

Parameters	From (INPUT)	To (OUTPUT)	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Units
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
f _{MAX}			135		135		135		ns
t _{PD}	CLK	B	1.0	8.2		7.3	1.0	6.2	
		A	1.0	6.4		5.8	1.0	5.0	
t _{EN}		B	1.0	7.9		6.7	1.0	6.1	
		A	1.0	7.6		6.2	1.0	5.9	
t _{DIS}		B	1.0	8.1		6.9	1.0	6.1	
		A	1.0	7.5		6.8	1.0	5.6	

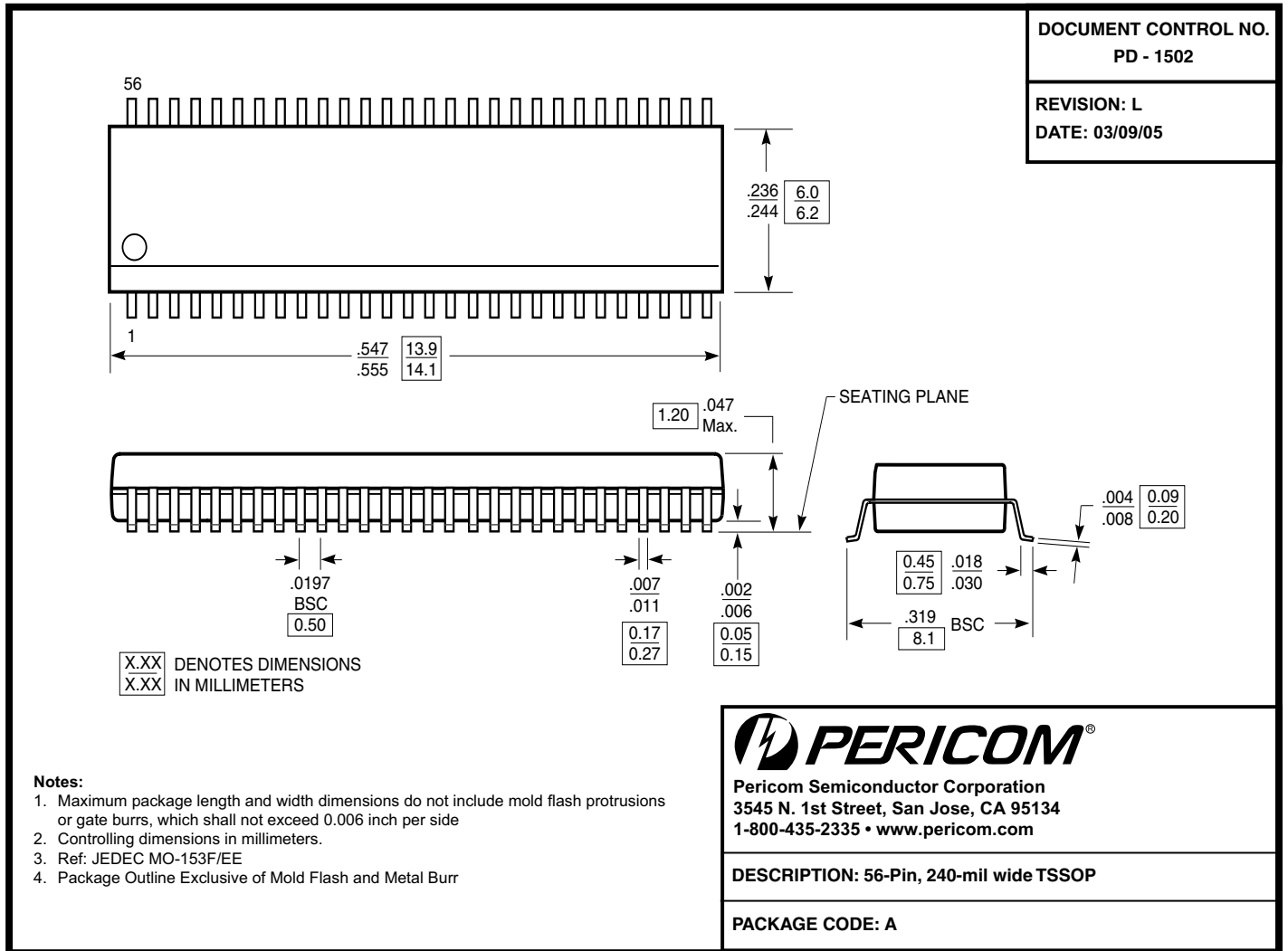
Notes:

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

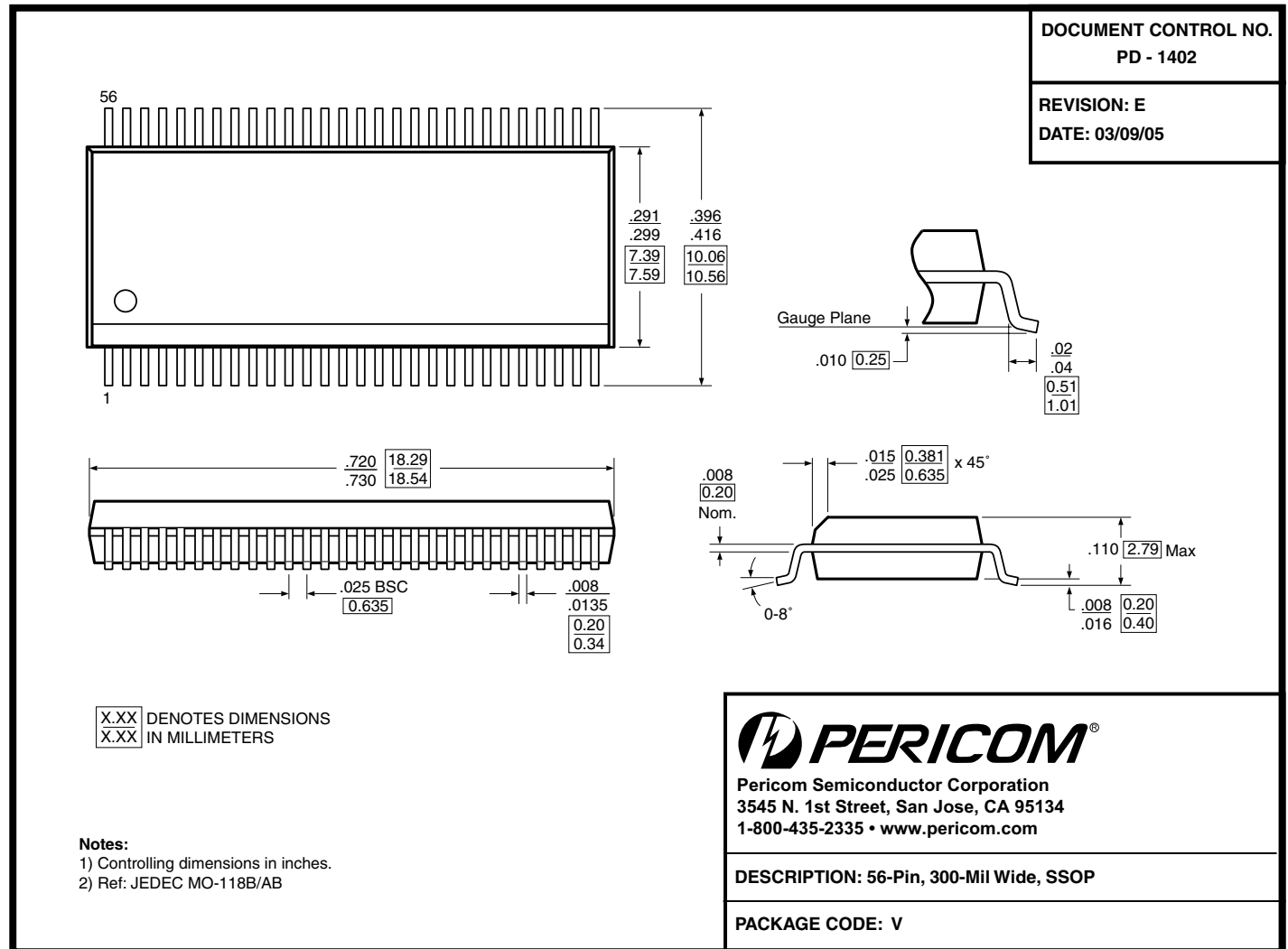
Operating Characteristics, $T_A = 25^\circ C$

Parameter		Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Units
			Typical		
C _{PD} Power Dissipation Capacitance per Exchanger	Outputs Enabled	C _L = 50pF, F = 10 MHz	87	120	pF
	Outputs Disabled		80.5	118	

Packaging Mechanical



Packaging Mechanical



Ordering Information

Ordering Code	Package Code	Package Type
PI74ALVCH16269A	A	56-pin 240 mil wide plastic TSSOP (A)
PI74ALVCH16269V	V	56-pin 300 mil wide plastic SSOP (V)

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- Adding an X suffix = Tape/Reel