

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4071BP, TC4071BF, TC4071BFN

TC4071B QUAD 2 INPUT OR GATE

TC4071B is positive logic OR gates with two inputs respectively. As all the outputs of gates are equipped with the buffer circuits of inverters, the input/output propagation characteristic has been improved and the variation of propagation time caused by increase of load capacity is kept minimum.

(Note) The JEDEC SOP (FN) is not available in Japan.

P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

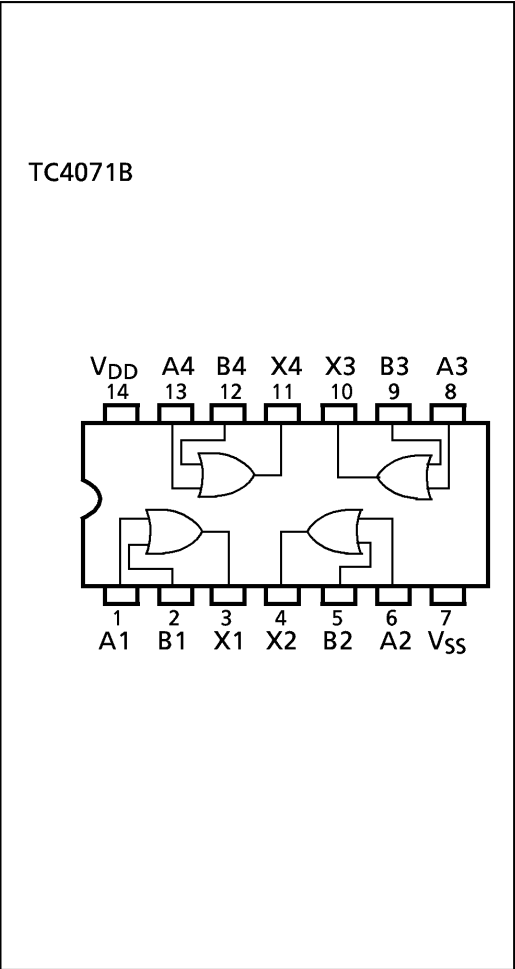
F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

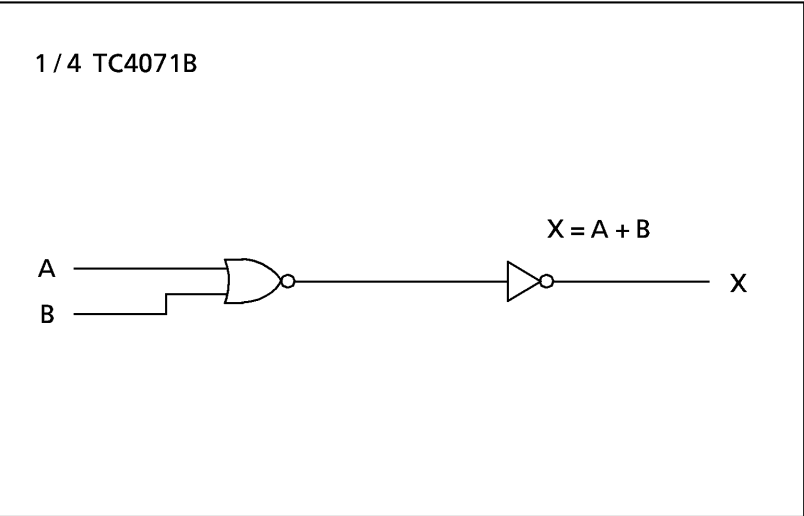
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} – 0.5~V _{SS} + 20	V
Input Voltage	V _{IN}	V _{SS} – 0.5~V _{DD} + 0.5	V
Output Voltage	V _{OUT}	V _{SS} – 0.5~V _{DD} + 0.5	V
DC Input Current	I _{IN}	± 10	mA
Power Dissipation	P _D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T _{opr}	– 40~85	°C
Storage Temperature Range	T _{stg}	– 65~150	°C

PIN ASSIGNMENT (TOP VIEW)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

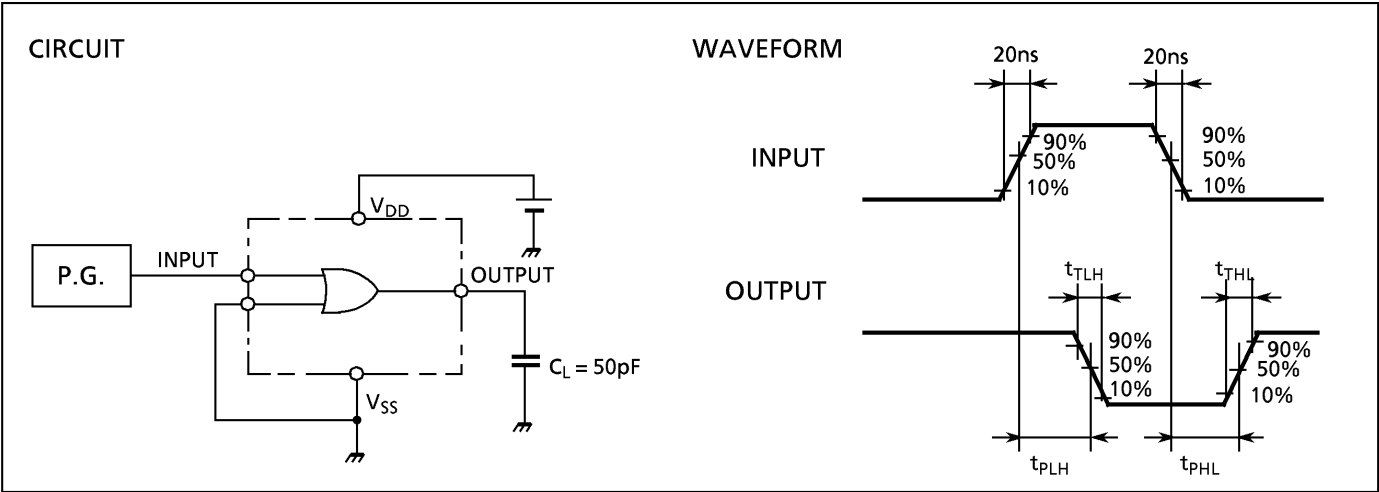
CHARACTERISTIC		SYM- BOL	TEST CONDITION	V _{DD} (V)	- 40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage		V _{OH}	I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.00 10.00 15.00	— — —	4.95 9.95 14.95	— — —	V
Low-Level Output Voltage		V _{OL}	I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5 10 15	— — —	0.05 0.05 0.05	— — —	0.00 0.00 0.00	0.05 0.05 0.05	— — —	0.05 0.05 0.05	
Output High Current		I _{OH}	V _{OH} = 4.6V	5	- 0.61	—	- 0.51	- 1.0	—	- 0.42	—	
			V _{OH} = 2.5V	5	- 2.50	—	- 2.10	- 4.0	—	- 1.70	—	
			V _{OH} = 9.5V	10	- 1.50	—	- 1.30	- 2.2	—	- 1.10	—	
			V _{OH} = 13.5V	15	- 4.00	—	- 3.40	- 9.0	—	- 2.80	—	
			V _{IN} = V _{SS} , V _{DD}									
Output Low Current		I _{OL}	V _{OL} = 0.4V	5	0.61	—	0.51	1.5	—	0.42	—	
			V _{OL} = 0.5V	10	1.50	—	1.30	3.8	—	1.10	—	
			V _{OL} = 1.5V	15	4.00	—	3.40	15.0	—	2.80	—	
			V _{IN} = V _{SS}									
Input High Voltage		V _{IH}	V _{OUT} = 0.5V, 4.5V	5	3.5	—	3.5	2.75	—	3.5	—	V
			V _{OUT} = 1.0V, 9.0V	10	7.0	—	7.0	5.50	—	7.0	—	
			V _{OUT} = 1.5V, 13.5V	15	11.0	—	11.0	8.25	—	11.0	—	
			I _{OUT} < 1 μA									
Input Low Voltage		V _{IL}	V _{OUT} = 0.5V, 4.5V	5	—	1.5	—	2.25	1.5	—	1.5	
			V _{OUT} = 1.0V, 9.0V	10	—	3.0	—	4.50	3.0	—	3.0	
			V _{OUT} = 1.5V, 13.5V	15	—	4.0	—	6.75	4.0	—	4.0	
			I _{OUT} < 1 μA									
Input Current	"H" Level	I _{IH}	V _{IH} = 18V	18	—	0.1	—	10 ⁻⁵	0.1	—	1.0	μA
	"L" Level	I _{IL}	V _{IL} = 0V	18	—	- 0.1	—	- 10 ⁻⁵	- 0.1	—	- 1.0	
Quiescent Supply Current		I _{DD}	V _{IN} = V _{SS} , V _{DD} *	5 10 15	— — —	0.25 0.50 1.00	— — —	0.001 0.001 0.002	0.25 0.50 1.00	— — —	7.5 15.0 30.0	

* All valid input combination

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

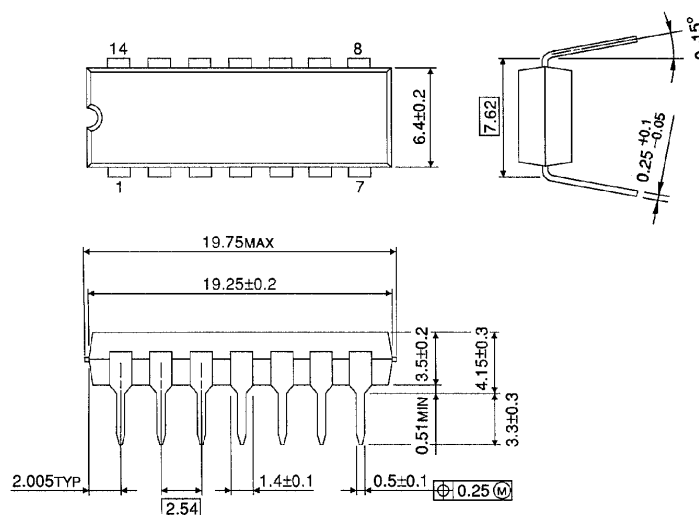
CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time	tTLH		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time	tTHL		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time	tPLH		5	—	65	200	
			10	—	30	100	
			15	—	25	80	
Propagation Delay Time	tPHL		5	—	65	200	
			10	—	30	100	
			15	—	25	80	
Input Capacitance	CIN			—	5	7.5	pF

CIRCUIT A D WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54)

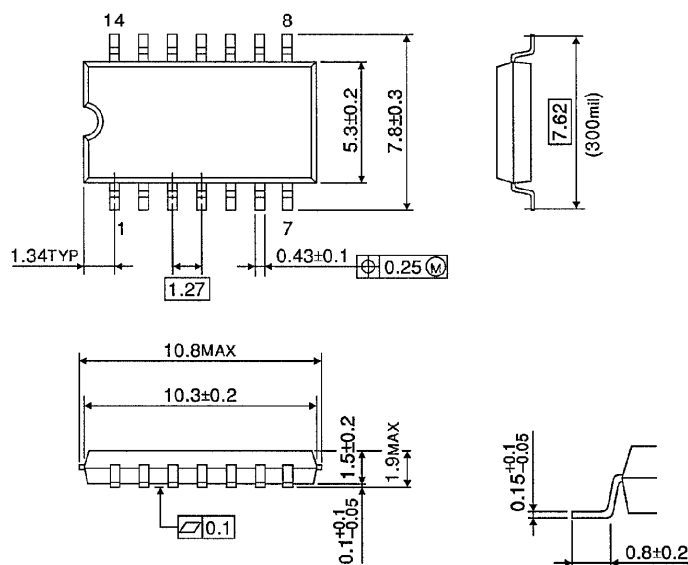
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm

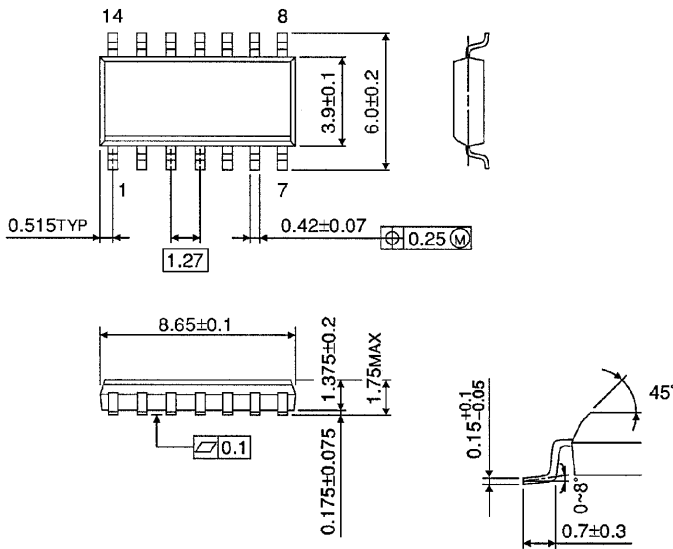


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

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000707EBA

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