

Product Summary

V_{BR} (min)	I_{PP} (max)	C_T (typ)
6V	4.7A	0.55pF

Description

The DT1446-04V is a high performance device suitable for protecting four high speed I/Os and one V_{CC} . These devices are assembled in SOT563 package. They have high ESD surge capability and low capacitance.

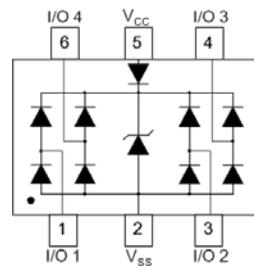
Applications

- Typically Used for High Speed Ports such as USB 2.0, IEEE1394, HDMI, Laptop and Personal Computers, Flat Panel Displays, Video Graphics Displays, SIM Ports



Top View

Bottom View



Device Schematic

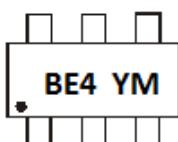
Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DT1446-04V-7	Standard	BE4	7	8	3,000/Tape & Reel

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



BE4 = Product Type Marking Code

YM = Date Code Marking

Y = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Date Code Key

Year	2013	2014	2015	2016	2017	2018
Code	A	B	C	D	E	F

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current ,per IEC 61000-4-5	$I_{PP_I/O}$	4.7	A	I/O to V_{SS} , 8/20 μs
Operating Voltage (DC)	V_{DC}	6	V	V_{CC} to V_{SS}
ESD Protection – Contact Discharge	$V_{ESD_I/O}$	± 16	kV	I/O to V_{SS} , per IEC 61000-4-2
	$V_{ESD_V_{CC}}$	± 30	kV	V_{CC} to V_{SS} , per IEC 61000-4-2
ESD Protection – Air Discharge, per IEC 61000-4-2	$V_{ESD_I/O}$	± 19	kV	I/O to V_{SS} , per IEC 61000-4-2
	$V_{ESD_V_{CC}}$	± 30	kV	V_{CC} to V_{SS} , per IEC 61000-4-2

Thermal Characteristics

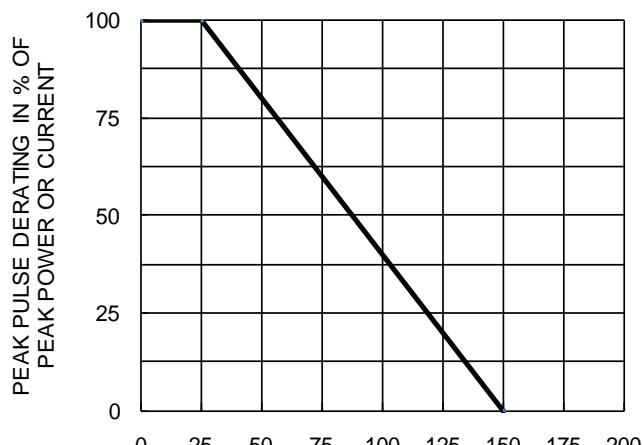
Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	380	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	327	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

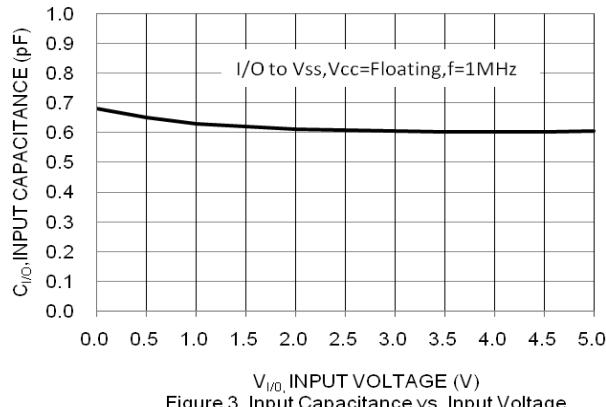
Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	—	—	5.5	V	V_{CC} to V_{SS}
Reverse Current (Note 6)	$I_R(V_{CC} \text{ to } V_{SS})$	—	—	5.0	μA	$V_R = 5\text{V}$, V_{CC} to V_{SS}
Reverse Current (Note 6)	$I_R(\text{I/O to } V_{SS})$	—	—	1.0	μA	$V_R = 5\text{V}$, any I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	6.0	—	9.0	V	$I_R = 1\text{mA}$, V_{CC} to V_{SS}
Forward Clamping Voltage	V_F	—	0.8	1.0	V	$I_F = 15\text{mA}$, V_{SS} to V_{CC}
Reverse Clamping Voltage (Note 7)	$V_{C_I/O}$	—	8.5	—	V	$I_{PP} = 4.7\text{A}$, I/O to V_{SS} , 8/20 μs
ESD Clamping Voltage	$V_{ESD_V_{CC}}$	—	10	—	V	TLP, 20A, $tp = 100\text{ ns}$, V_{CC} to V_{SS}
	$V_{ESD_I/O}$	—	12	—	V	TLP, 20A, $tp = 100\text{ ns}$, I/O to V_{SS}
Dynamic Resistance	$R_{DIF_V_{CC}}$	—	0.2	—	Ω	TLP, 20A, $tp = 100\text{ ns}$, V_{CC} to V_{SS}
	$R_{DIF_I/O}$	—	0.3	—	Ω	TLP, 20A, $tp = 100\text{ ns}$, I/O to V_{SS}
Channel Input Capacitance	$C_{I/O \text{ to } V_{SS}}$	—	0.55	0.65	pF	$V_R = 2.5\text{V}$, $V_{CC} = 5\text{V}$, $f = 1\text{MHz}$
Channel Input Capacitance	$C_{I/O \text{ to } V_{SS}}$	—	0.65	—	pF	$V_R = 2.5\text{V}$, $V_{CC} = \text{floating}$, $f = 1\text{MHz}$
Variation of Channel Input Capacitance	$C_{I/OMAX}-C_{I/OMIN}$	—	0.03	—	pF	$V_{CC} = 5\text{V}$, $V_{SS} = 0\text{V}$, $I/O = 2.5\text{V}$, $f = 1\text{MHz}$, $T = 25^\circ\text{C}$, $C_{I/OMAX}-C_{I/OMIN}$
Variation of Channel Input Capacitance	$C_{I/OMAX}-C_{I/OMIN}$	—	0.05	—	pF	$V_{CC} = \text{floating}$, $V_{SS} = 0\text{V}$, $I/O = 2.5\text{V}$, $f = 1\text{MHz}$, $T = +25^\circ\text{C}$, $C_{I/OMAX}-C_{I/OMIN}$

Notes:

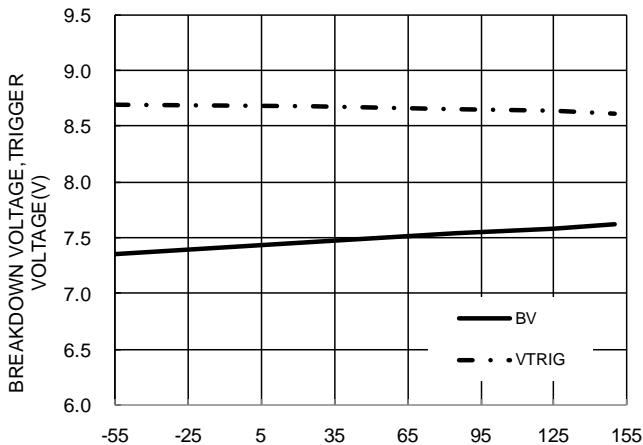
5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes, Inc. suggested pad layout AP02001, which can be found on our website at <http://www.diodes.com>.
6. Short duration pulse test used to minimize self-heating effect.
7. Clamping voltage value is based on an 8x20 μs peak pulse current (I_{PP}) waveform.



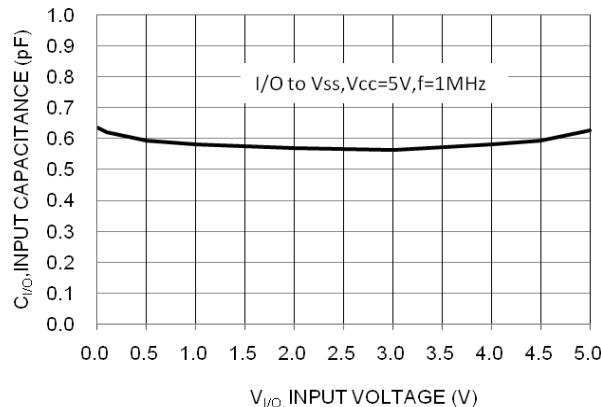
T_A, AMBIENT TEMPERATURE (°C)
Figure 1. Pulse Derating Curve



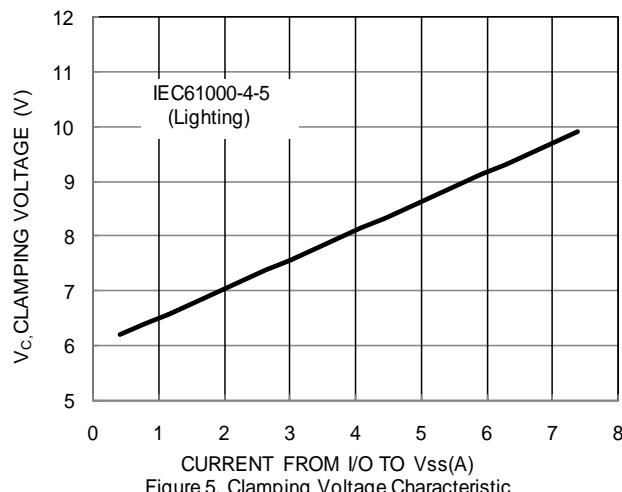
I/O to Vss, Vcc=Floating, f=1MHz
Figure 3. Input Capacitance vs. Input Voltage



T_A, AMBIENT TEMPERATURE (°C)
Figure 2. BV, Trigger Voltage vs. Ambient Temperature



I/O to Vss, Vcc=5V, f=1MHz
Figure 4. Input Capacitance vs. Input Voltage



IEC61000-4-5 (Lighting)
Figure 5. Clamping Voltage Characteristic

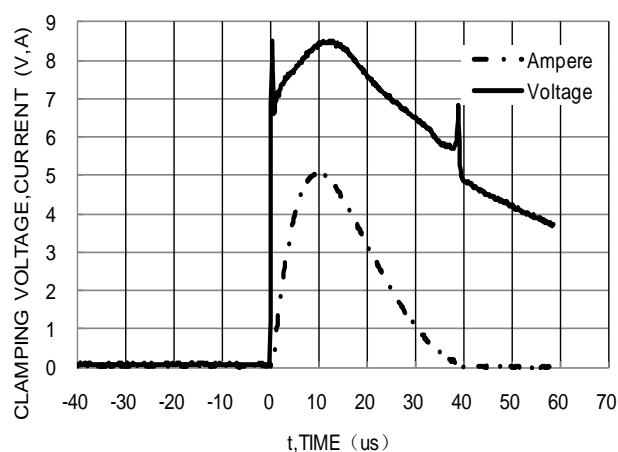


Figure 6. Waveform of Clamping Voltage, Current vs. Time (8/20us, I/O to Vss)

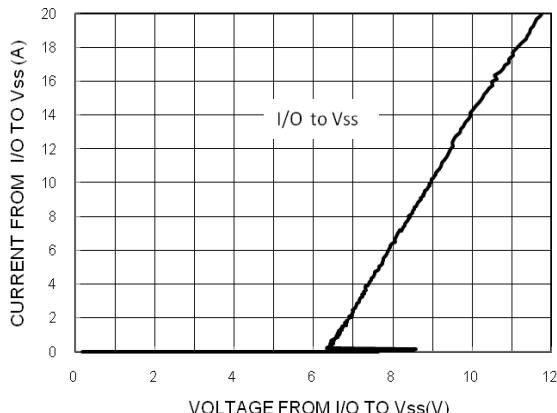


Figure 7. Transmission Line Pulsing (TLP) Measurement
Current vs. Voltage

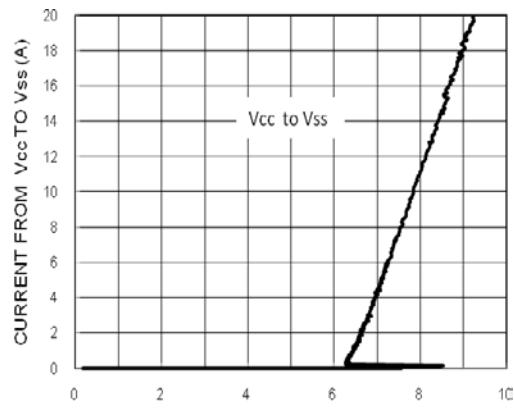
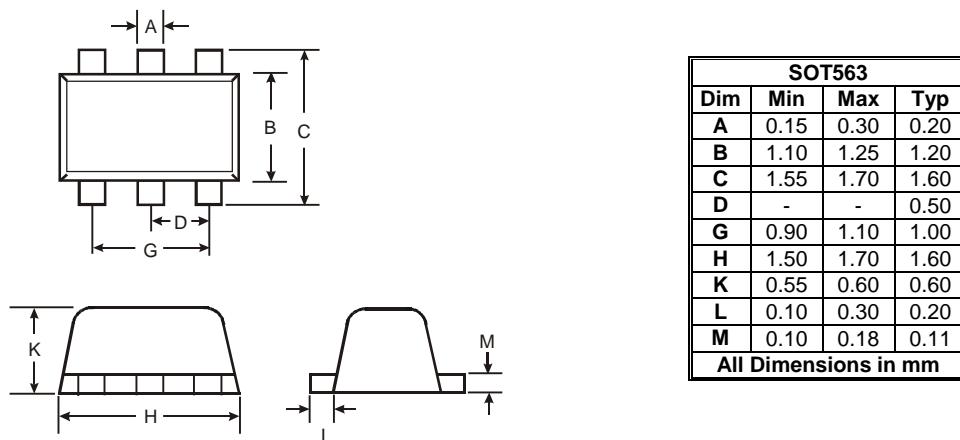


Figure 8. Transmission Line Pulsing (TLP) Measurement
Current vs. Voltage

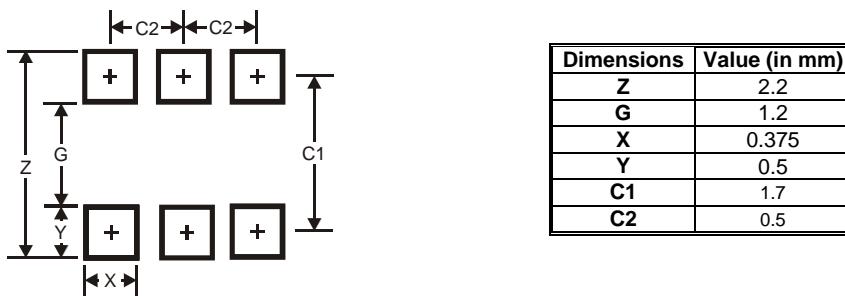
Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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