Enpirion® Power Datasheet ER3110DI Wide PVIN 1A Synchronous Buck Regulator

The ER3110DI is a 1A synchronous buck regulator with an input range of 3V to 36V. It provides an easy to use, high efficiency low BOM count solution for a variety of applications.

The ER3110DI integrates both high-side and low-side NMOS FETs and features a PFM mode for improved efficiency at light loads. This feature can be disabled if a forced PWM mode is desired. The part switches at a default frequency of 500kHz but may also be programmed using an external resistor from 300kHz to 2MHz. The ER3110DI has the ability to utilize internal or external compensation. By integrating both NMOS devices and providing internal configuration options, minimal external components are required, reducing BOM count and complexity of design.

With the wide V_{PVIN} range and reduced BOM, the part provides an easy to implement design solution for a variety of applications while giving superior performance. It will provide a very robust design for high voltage industrial applications as well as an efficient solution for battery powered applications.

The part is available in a small Pb-free 4mmx3mm DFN plastic package with a full-range industrial temperature of -40°C to +125°C.

Features

- Wide input voltage range 3V to 36V
- Synchronous operation for high efficiency
- No compensation required
- Integrated high-side and low-side NMOS devices
- Selectable PFM or forced PWM mode at light loads
- Internal fixed (500kHz) or adjustable switching frequency 300kHz to 2MHz
- Continuous output current up to 1A
- Internal or external soft-start
- Minimal external components required
- Power-good and enable functions available

Applications

- FPGA Applications
- Industrial control
- Medical devices
- Portable instrumentation
- Distributed power supplies
- Cloud infrastructure

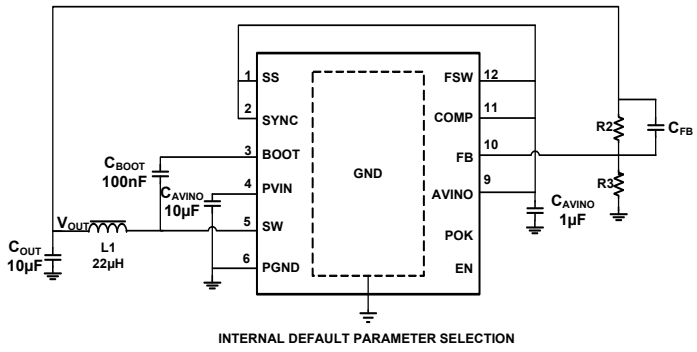


FIGURE 1. TYPICAL APPLICATION

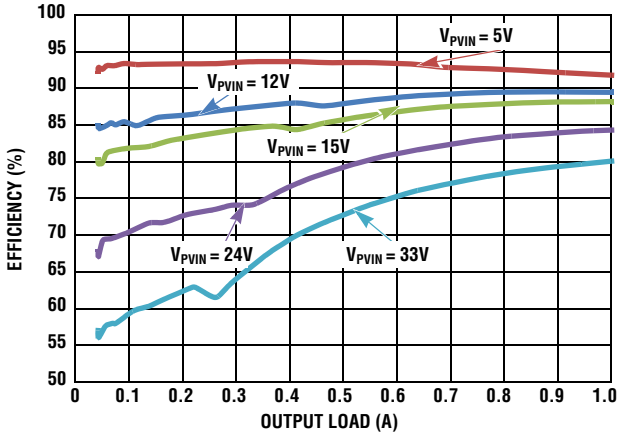


FIGURE 2. EFFICIENCY vs LOAD, PFM, V_{OUT} = 3.3V

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Ordering Information

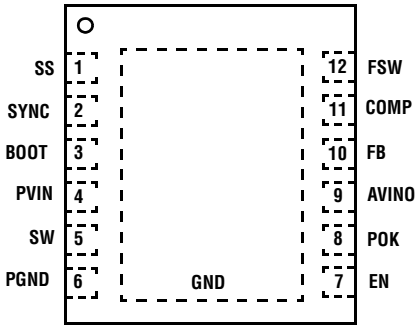
PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ER3110DI	3110	-40 to +125	12 Ld DFN	L12.4x3

NOTES:

1. Add “T” suffix for Tape and Reel. Please refer to Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html
2. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS3333 compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

ER3110DI
(12 LD 4X3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	SS	The SS pin controls the soft-start ramp time of the output. A single capacitor from the SS pin to ground determines the output ramp rate. See “Soft-Start” on page 14 for soft-start details. If the SS pin is tied to AVINO, an internal soft-start of 2ms will be used.
2	SYNC	Synchronization and light load operational mode selection input. Connect to logic high or AVINO for PWM mode. Connect to logic low or ground for PFM mode. Logic ground enables the IC to automatically choose PFM or PWM operation. Connect to an external clock source for synchronization with positive edge trigger. Sync source must be higher than the programmed IC frequency. There is an internal 5MΩ pull-down resistor to prevent an undefined logic state if SYNC is left floating.
3	BOOT	Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn on the internal N-Channel MOSFET. Connect an external 100nF capacitor from this pin to SW.
4	PVIN	The input supply for the power stage of the regulator and the source for the internal linear bias regulator. Place a minimum of 4.7µF ceramic capacitance from PVIN to GND and close to the IC for decoupling.
5	SW	Switch node output. It connects the switching FETs with the external output inductor.
6	PGND	Power ground connection. Connect directly to the system GND plane.
7	EN	Regulator enable input. The regulator and bias LDO are held off when the pin is pulled to ground. When the voltage on this pin rises above 1V, the chip is enabled. Connect this pin to PVIN for automatic start-up. Do not connect EN pin to AVINO since the LDO is controlled by EN voltage.
8	POK	Open drain power-good output that is pulled to ground when the output voltage is below regulation limits or during the soft-start interval. There is an internal 5MΩ internal pull-up resistor.
9	AVINO	Output of the internal 5V linear bias regulator. Decouple to PGND with a 1µF ceramic capacitor at the pin.
10	FB	Feedback pin for the regulator. FB is the inverting input to the voltage loop error amplifier. COMP is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the PWM regulator’s power-good and UVLO circuits use FB to monitor the regulator output voltage.
11	COMP	COMP is the output of the error amplifier. When it is tied to AVINO, internal compensation is used. When only an RC network is connected from COMP to GND, external compensation is used. See “Loop Compensation Design” on page 18 for more details.
12	FSW	Frequency selection pin. Tie to AVINO for 500kHz switching frequency. Connect a resistor to GND for adjustable frequency from 300kHz to 2MHz.
EPAD	GND	Signal ground connections. Connect to application board GND plane with at least 5 vias. All voltage levels are measured with respect to this pin. The EPAD MUST not float.

Typical Application Schematics

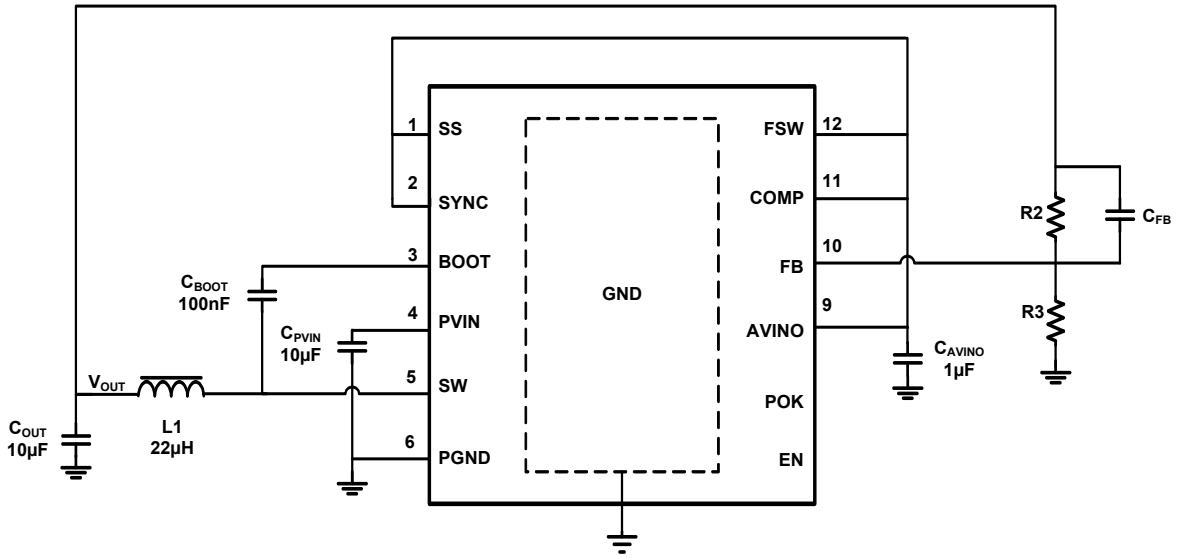


FIGURE 3. INTERNAL DEFAULT PARAMETER SELECTION

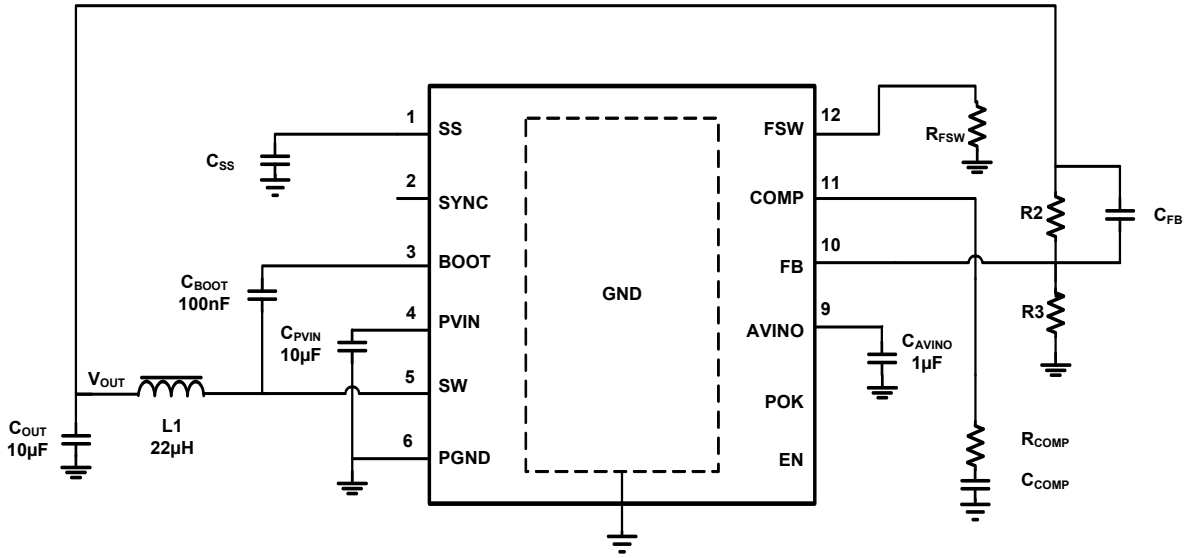


FIGURE 4. USER PROGRAMMABLE PARAMETER SELECTION

TABLE 1. EXTERNAL COMPONENT SELECTION

V_{OUT} (V)	L_1 (µH)	C_{OUT} (µF)	R_2 (kΩ)	R_3 (kΩ)	C_{FB} (pF)	R_{FSW} (kΩ)	R_{COMP} (kΩ)	C_{COMP} (pF)
12	22	2 x 22	90.9	4.75	22	115	150	470
5	22	47 + 22	90.9	12.4	27	DNP (Note 3)	100	470
3.3	22	47 + 22	90.9	20	27	DNP (Note 3)	100	470
2.5	22	47 + 22	90.9	28.7	27	DNP (Note 3)	100	470
1.8	12	47 + 22	90.9	45.5	27	DNP (Note 3)	70	470

NOTE:

3. Connect FSW to V_{AVINO}

Absolute Maximum Ratings

PVIN to GND . . . . . -0.3V to +42V
SW to GND . . . . . -0.3V to PVIN+0.3V (DC)
SW to GND . . . . . -2V to 43V (20ns)
EN to GND . . . . . -0.3V to +42V
BOOT to SW . . . . . -0.3V to +5.5V
COMP, FSW, POK, SYNC, SS, AVINO to GND . -0.3V to +5.9V
FB to GND . . . . . -0.3V to +2.95V
ESD Rating
Human Body Model (Tested per JESD22-A114) 2kV
Charged Device Model (Tested per JESD22-C101E) . . . 1.5kV
Latch Up (Tested per JESD-78A; Class 2, Level A) . . 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 4, 5)	42	4.5

Maximum Junction Temperature (Plastic Package) . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +125°C

Recommended Operating Conditions

Temperature . . . . . -40°C to +125°C
Supply Voltage . . . . . 3V to 36V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A = -40°C to +125°C, V_{PVIN} = 3V to 36V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the junction temperature range, -40°C to +125°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SUPPLY VOLTAGE						
V_{PVIN} Voltage Range	V_{PVIN}		**3**		**36**	V
V_{PVIN} Quiescent Supply Current	I_Q	V_{FB} = 0.7V, SYNC = 0V, F_{SW} = V_{AVINO}		80		µA
V_{PVIN} Shutdown Supply Current	I_{SD}	EN = 0V, V_{PVIN} = 36V (Note 6)		2	4	µA
V_{AVINO} Voltage	V_{AVINO}	V_{PVIN} = 6V, I_{OUT} = 0 to 10mA	4.5	5.1	5.7	V
POWER-ON RESET						
V_{AVINO} POR Threshold		Rising edge		2.75	2.95	V
		Falling edge	2.35	2.6		V
OSCILLATOR						
Nominal Switching Frequency	F_{SW}	F_{SW} = V_{AVINO}	430	500	570	kHz
		Resistor from F_{SW} to GND = 340kΩ	**240**	300	**360**	kHz
		Resistor from F_{SW} to GND = 32.4kΩ		2000		kHz
Minimum Off-Time	t_{OFF}	V_{PVIN} = 3V		150		ns
Minimum On-Time	t_{ON}	(Note 9)		90		ns
F_{SW} Voltage	V_{FSW}	F_{SW} = 100kΩ	**0.39**	0.4	**0.41**	V
Synchronization Frequency	SYNC		**300**		**2000**	kHz
SYNC Pulse Width			100			ns
ERROR AMPLIFIER						
Error Amplifier Transconductance Gain	gm	External compensation	**165**	230	**295**	µA/V
		Internal compensation		50		µA/V
FB Leakage Current		V_{FB} = 0.6V		1	150	nA
Current Sense Amplifier Gain	R_T		0.46	0.5	0.54	V/A
FB Voltage		T_A = -40°C to +85°C	0.590	0.599	**0.606**	V
		T_A = -40°C to +125°C	0.590	0.599	0.607	V

Electrical Specifications T_A = -40°C to +125°C, V_{PVIN} = 3V to 36V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the junction temperature range, -40°C to +125°C (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER-GOOD						
Lower POK Threshold - VFB Rising				90	**94**	%
Lower POK Threshold - VFB Falling			**82.5**	86		%
Upper POK Threshold - VFB Rising				116.5	**120**	%
Upper POK Threshold - VFB Falling			**107**	112		%
POK Propagation Delay		Percentage of the soft-start time		10		%
POK Low Voltage		I_{SINK} = 3mA, EN = V_{AVINO}, V_{FB} = 0V		0.05	0.3	V
TRACKING AND SOFT-START						
Soft-Start Charging Current	I_{SS}		4.2	5.5	6.5	µA
Internal Soft-Start Ramp Time		EN/SS = V_{AVINO}	1.5	2.4	3.4	ms
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising threshold		150		°C
	T_{HYS}	Hysteresis		20		°C
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	IPLIMIT	(Note 7)	1.3	1.5	1.7	A
PFM Peak Current Limit	I_{PK_PFM}		0.34	0.4	0.5	A
Zero Cross Threshold				15		mA
Negative Current Limit	INLIMIT	(Note 7)	-0.67	-0.6	-0.53	A
POWER MOSFET						
High-side	R_{HDS}	I_{SW} = 100mA, V_{AVINO} = 5V		250	350	mΩ
Low-side	R_{LDS}	I_{SW} = 100mA, V_{AVINO} = 5V		90	130	mΩ
SW Leakage Current		EN = SW = 0V			**300**	nA
SW Rise Time	t_{RISE}	V_{PVIN} = 36V		10		ns
EN/SYNC						
Input Threshold		Falling edge, logic low	**0.4**	1		V
		Rising edge, logic high		1.2	**1.4**	V
EN Logic Input Leakage Current		EN = 0V/36V	**-0.5**		**0.5**	µA
SYNC Logic Input Leakage Current		SYNC = 0V		10	**100**	nA
		SYNC = 5V		1.0	1.55	µA

NOTES:

6. Test Condition: V_{PVIN} = 36V, FB forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
7. Established by both current sense amplifier gain test and current sense amplifier output test @ I_L = 0A.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Minimum On-Time required to maintain loop stability.

Efficiency Curves

F_{SW} = 500kHz, T_A = +25°C

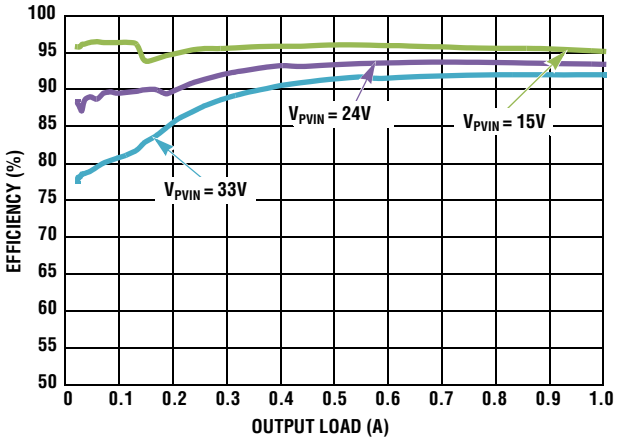


FIGURE 5. EFFICIENCY vs LOAD, PFM, V_{OUT} = 12V

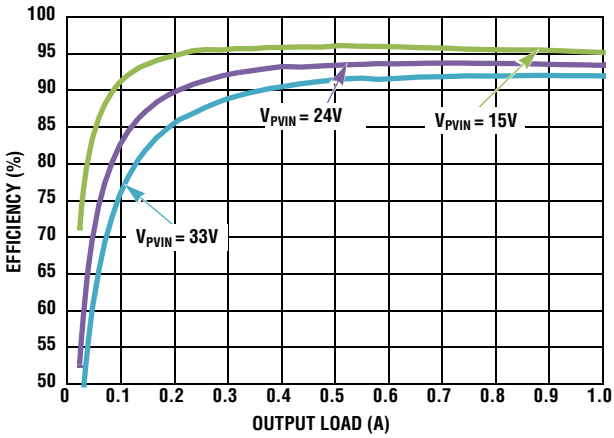


FIGURE 6. EFFICIENCY vs LOAD, PWM, V_{OUT} = 12V

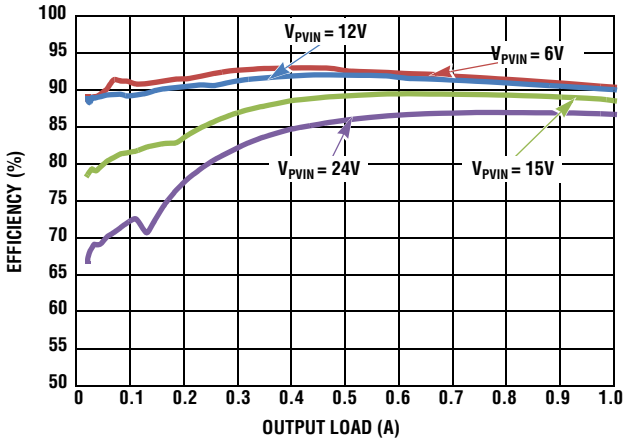


FIGURE 7. EFFICIENCY vs LOAD, PFM, V_{OUT} = 5V, L1 = 30µH

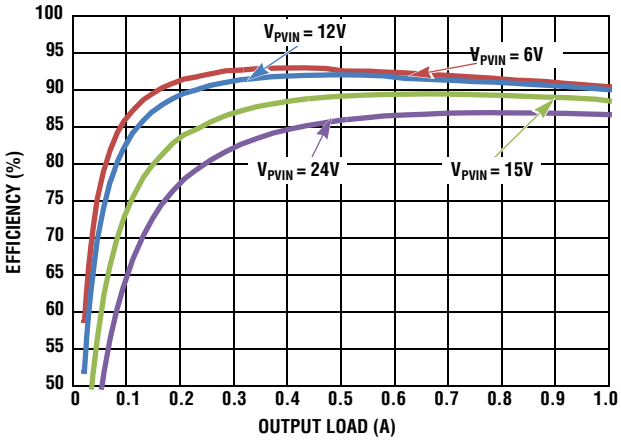


FIGURE 8. EFFICIENCY vs LOAD, PWM, V_{OUT} = 5V, L1 = 30µH

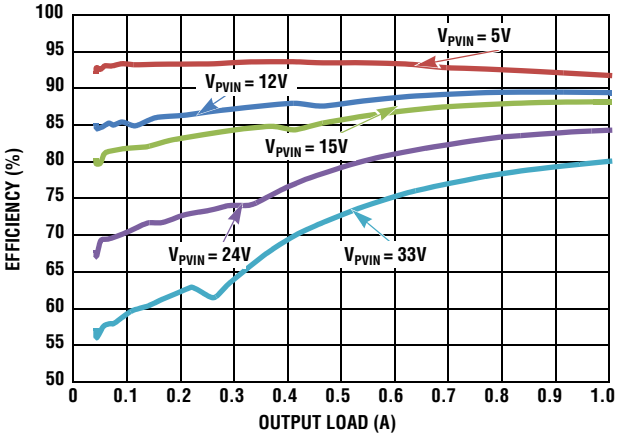


FIGURE 9. EFFICIENCY vs LOAD, PFM, V_{OUT} = 3.3V

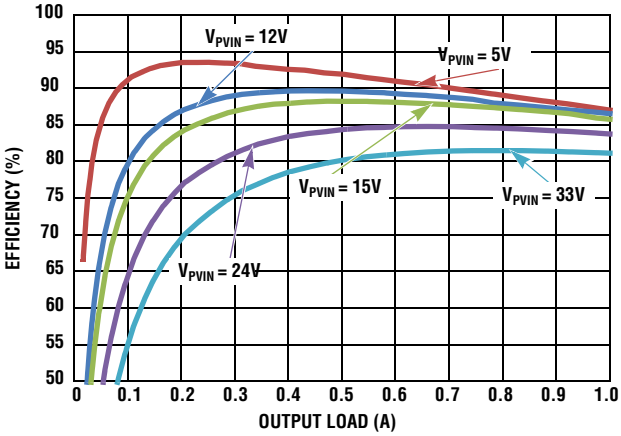


FIGURE 10. EFFICIENCY vs LOAD, PWM, V_{OUT} = 3.3V

Efficiency Curves F_{SW} = 500kHz, T_A = +25°C **(Continued)**

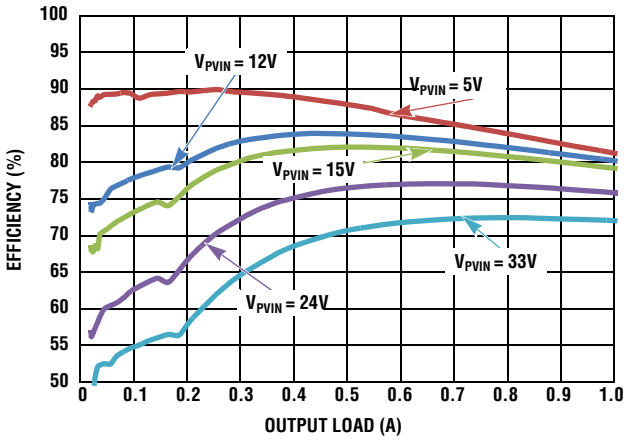


FIGURE 11. EFFICIENCY vs LOAD, PFM, V_{OUT} = 1.8V

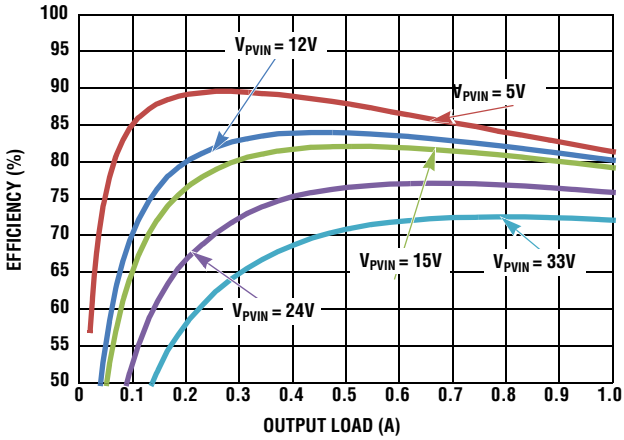


FIGURE 12. EFFICIENCY vs LOAD, PWM, V_{OUT} = 1.8V

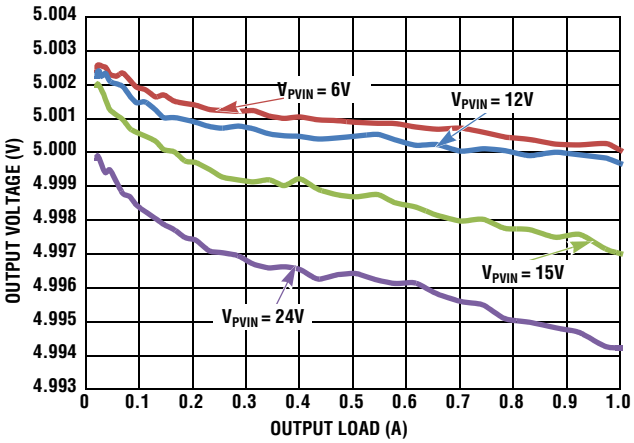


FIGURE 13. EFFICIENCY vs LOAD, PWM, V_{OUT} = 5V, L1 = 30µH

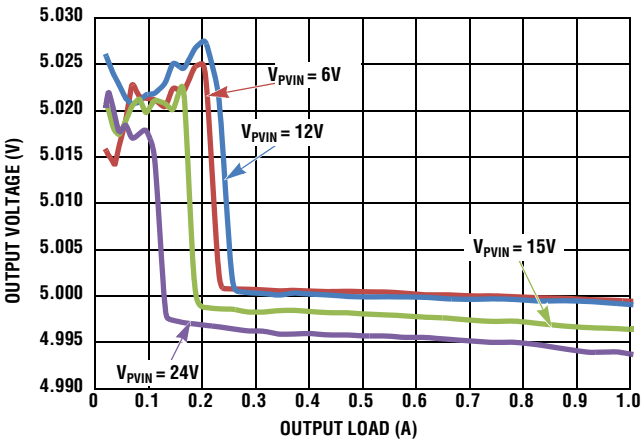


FIGURE 14. V_{OUT} REGULATION vs LOAD, PFM, V_{OUT} = 5V, L1 = 30µH

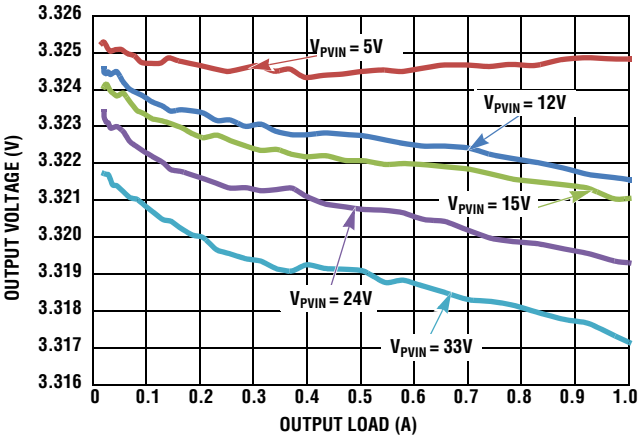


FIGURE 15. V_{OUT} REGULATION vs LOAD, PWM, V_{OUT} = 3.3V

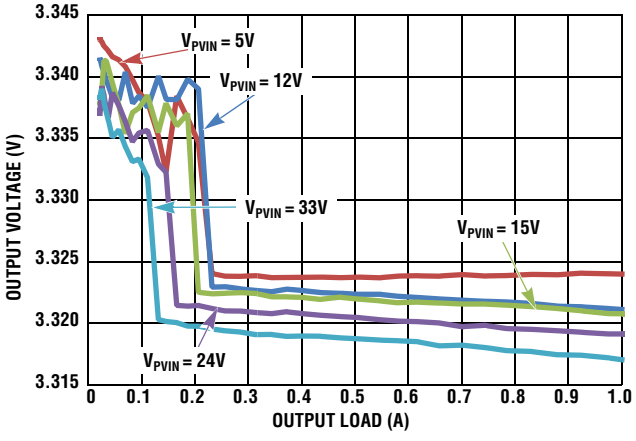


FIGURE 16. V_{OUT} REGULATION vs LOAD, PFM, V_{OUT} = 3.3V

Efficiency Curves F_{SW} = 500kHz, T_A = +25°C **(Continued)**

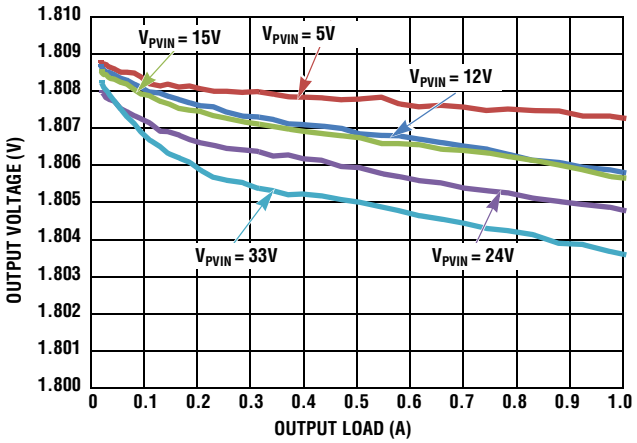


FIGURE 17. V_{OUT} REGULATION vs LOAD, PWM, V_{OUT} = 1.8V

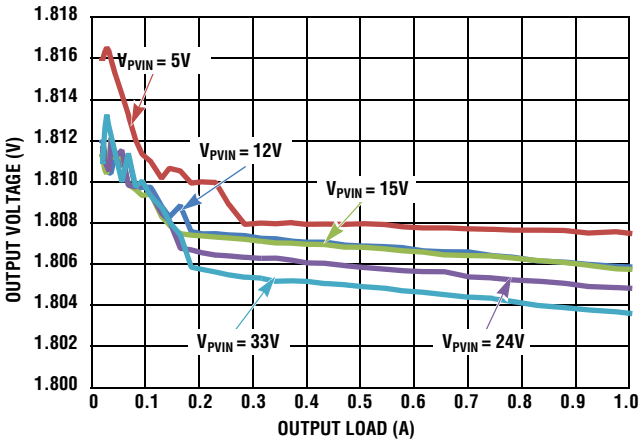


FIGURE 18. V_{OUT} REGULATION vs LOAD, PFM, V_{OUT} = 1.8V

Measurements F_{SW} = 500kHz, V_{PVIN} = 24V, V_{OUT} = 3.3V, T_A = +25°C

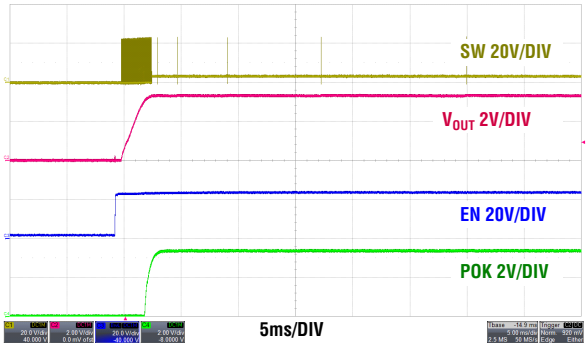


FIGURE 19. START-UP AT NO LOAD, PFM

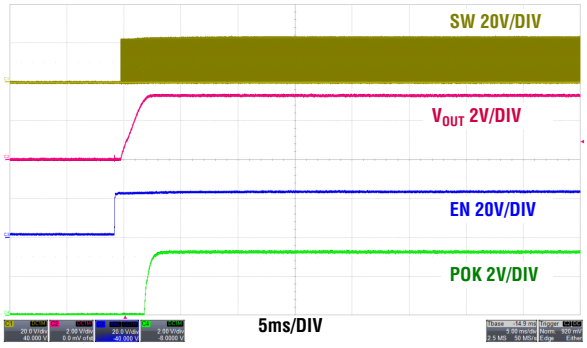


FIGURE 20. START-UP AT NO LOAD, PWM

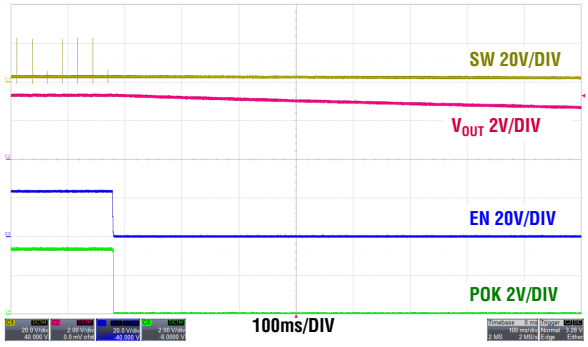


FIGURE 21. SHUTDOWN AT NO LOAD, PFM

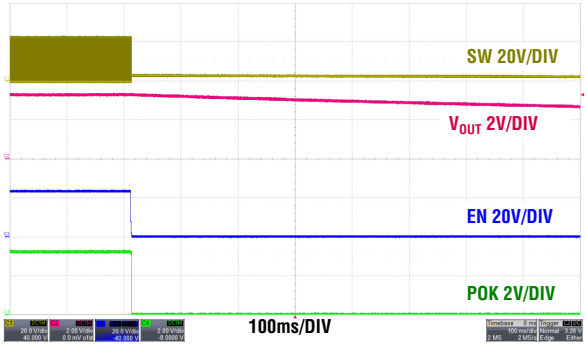


FIGURE 22. SHUTDOWN AT NO LOAD, PWM

Measurements

F_{SW} = 500kHz, V_{PVIN} = 24V, V_{OUT} = 3.3V, T_A = +25°C **(Continued)**

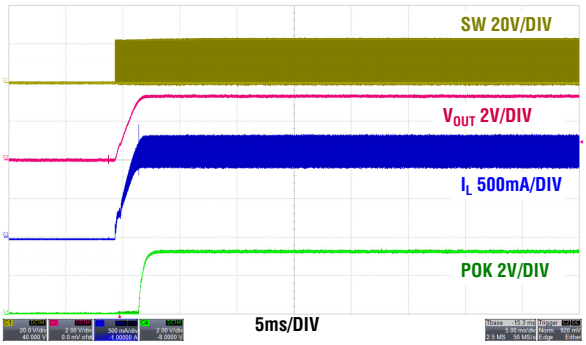


FIGURE 23. START-UP AT 1A, PWM

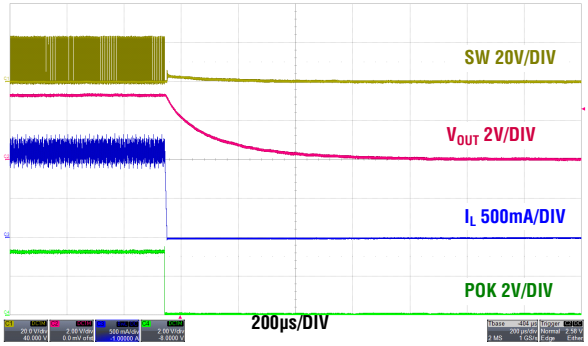


FIGURE 24. SHUTDOWN AT 1A, PWM

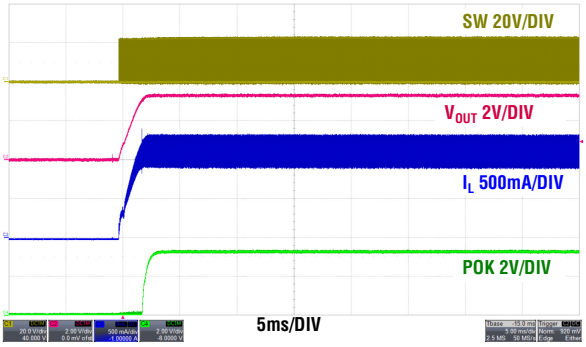


FIGURE 25. START-UP AT 1A, PFM

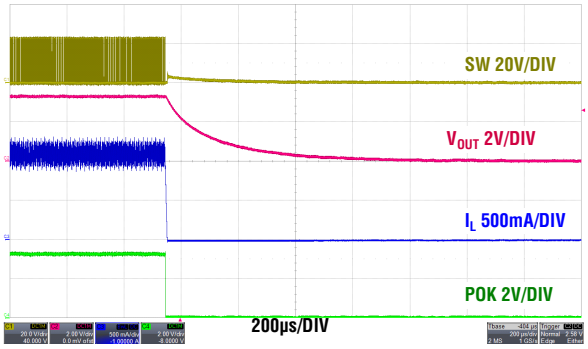


FIGURE 26. SHUTDOWN AT 1A, PFM

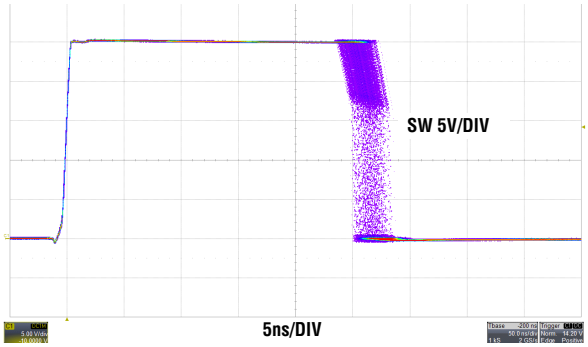


FIGURE 27. JITTER AT NO LOAD, PWM

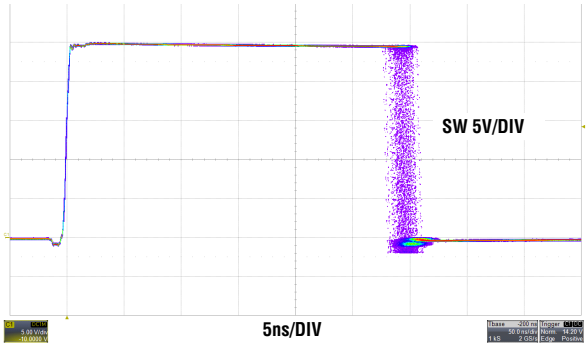


FIGURE 28. JITTER AT 1A LOAD, PWM

Measurements

F_{SW} = 500kHz, V_{PVIN} = 24V, V_{OUT} = 3.3V, T_A = +25°C **(Continued)**

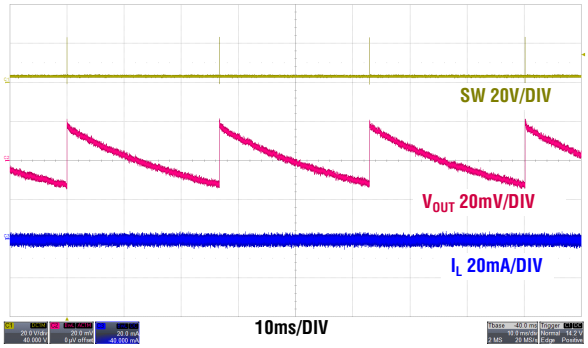


FIGURE 29. STEADY STATE AT NO LOAD, PFM

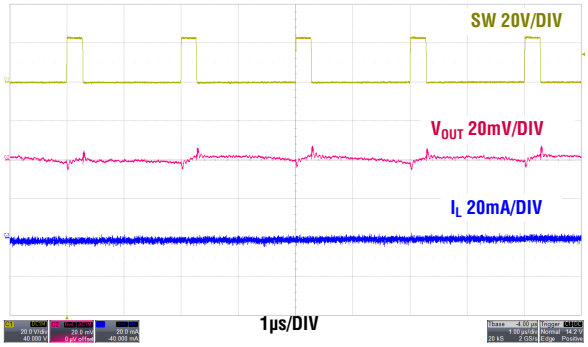


FIGURE 30. STEADY STATE AT NO LOAD, PWM

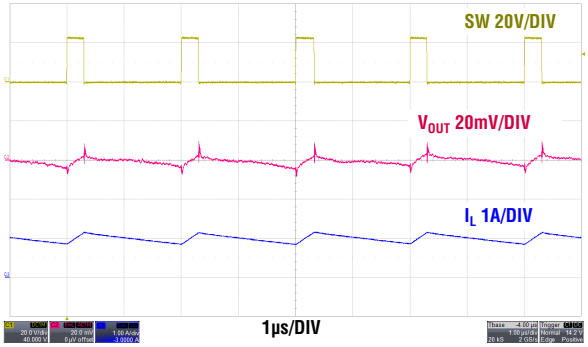


FIGURE 31. STEADY STATE AT 1A, PWM

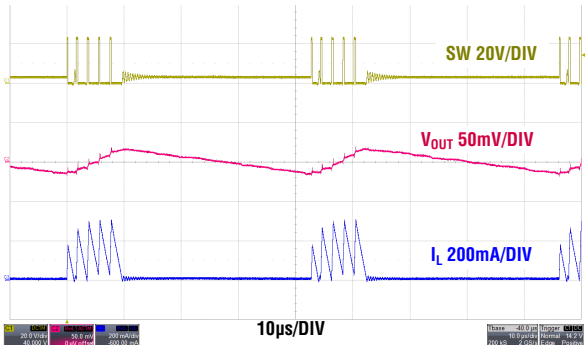


FIGURE 32. LIGHT LOAD OPERATION AT 20mA, PFM

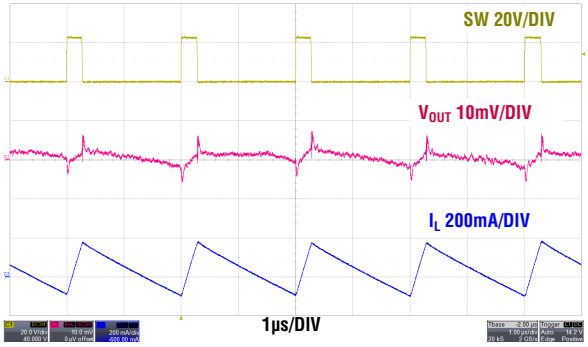


FIGURE 33. LIGHT LOAD OPERATION AT 20mA, PWM

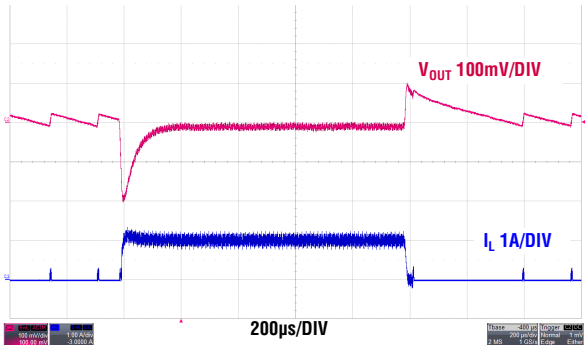


FIGURE 34. LOAD TRANSIENT, PFM

Measurements

F_{SW} = 500kHz, V_{PVIN} = 24V, V_{OUT} = 3.3V, T_A = +25°C **(Continued)**

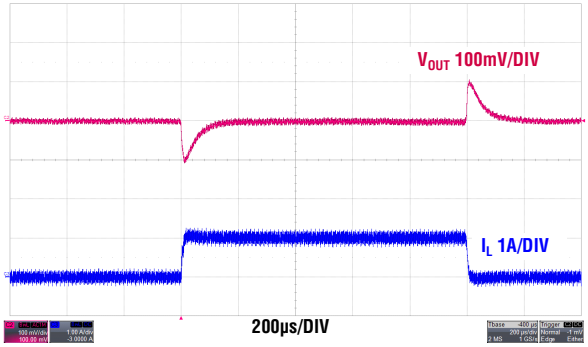


FIGURE 35. LOAD TRANSIENT, PWM

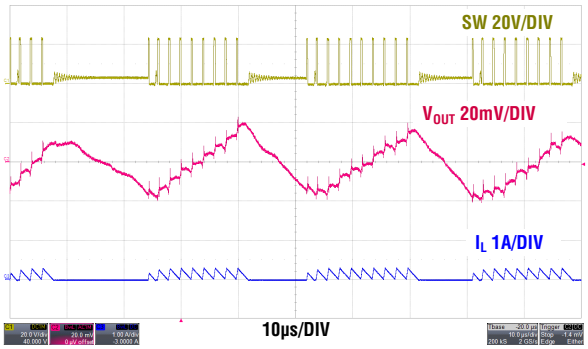


FIGURE 36. PFM TO PWM TRANSITION

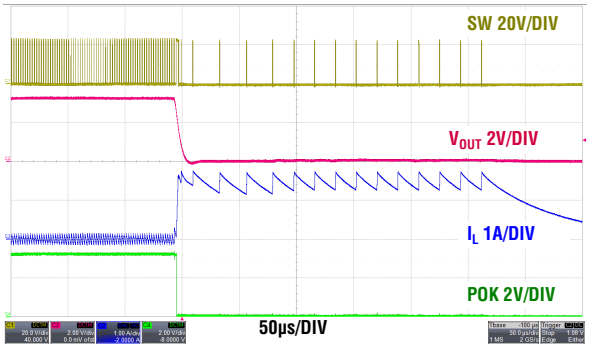


FIGURE 37. OVERCURRENT PROTECTION, PWM

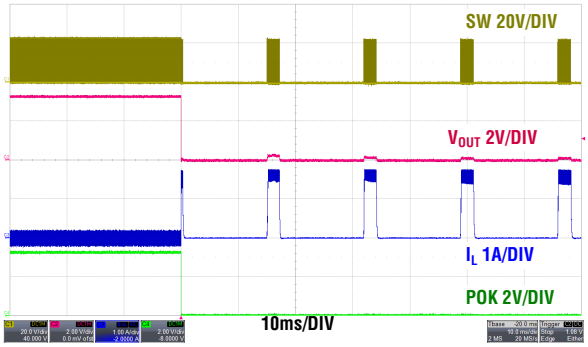


FIGURE 38. OVERCURRENT PROTECTION HICCUP, PWM

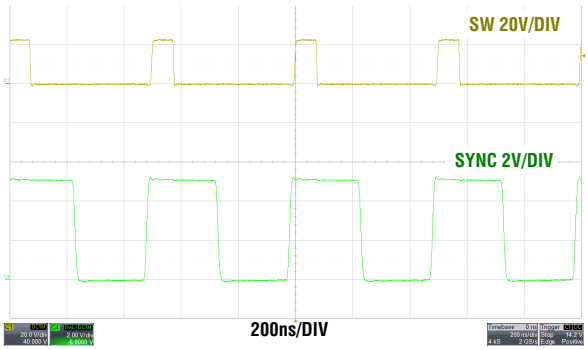


FIGURE 39. SYNC AT 1A LOAD, PWM

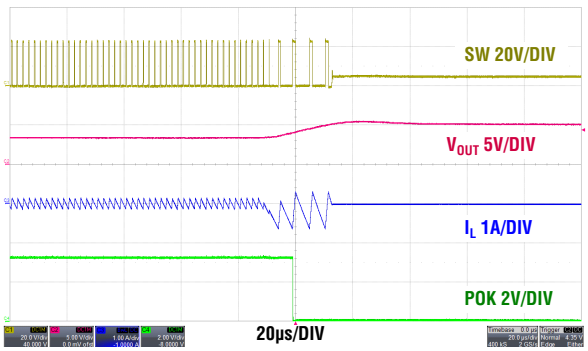


FIGURE 40. NEGATIVE CURRENT LIMIT, PWM

Measurements

F_{SW} = 500kHz, V_{PVIN} = 24V, V_{OUT} = 3.3V, T_A = +25°C **(Continued)**

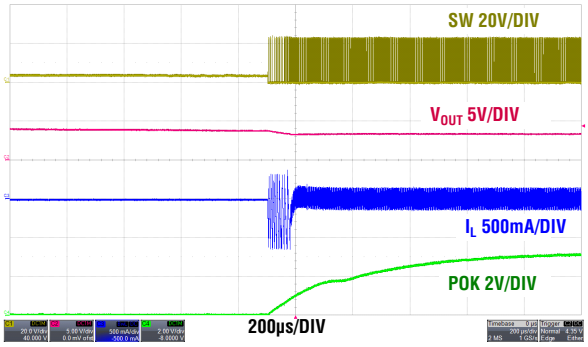


FIGURE 41. NEGATIVE CURRENT LIMIT RECOVERY, PWM

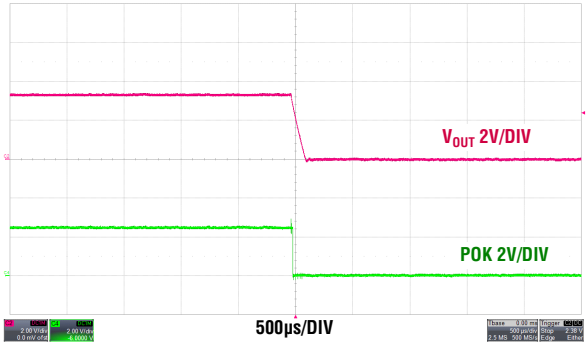
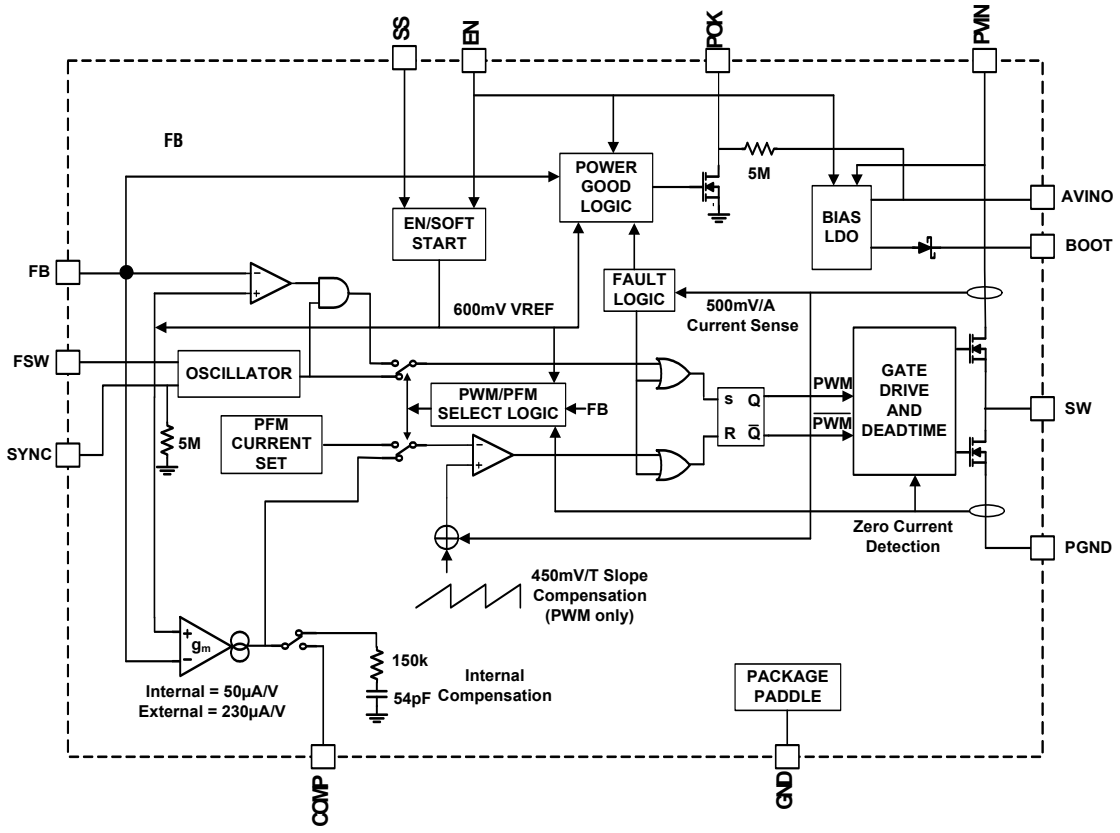


FIGURE 42. OVER-TEMPERATURE PROTECTION, PWM

Functional Block Diagram



Detailed Description

The ER3110DI combines a synchronous buck PWM controller with integrated power switches. The buck controller drives internal high-side and low-side N-channel MOSFETs to deliver load current up to 1A. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +3V to +36V. An internal LDO provides bias to the low voltage portions of the IC.

Peak current mode control is utilized to simplify feedback loop compensation and reject input voltage variation. User selectable internal feedback loop compensation further simplifies design. The ER3110DI switches at a default 500kHz.

The buck regulator is equipped with an internal current sensing circuit and the peak current limit threshold is typically set at 1.5A.

Power-On Reset

The ER3110DI automatically initializes upon receipt of the input power supply and continually monitors the EN pin state. If EN is held below its logic rising threshold the IC is held in shutdown and consumes typically 2µA from the V_{PVIN} supply. If EN exceeds its logic rising threshold, the regulator will enable the bias LDO and begin to monitor the AVINO pin voltage. When the AVINO pin voltage clears its rising POR threshold, the controller will initialize the switching regulator circuits. If AVINO never clears the rising POR threshold, the controller will not allow the switching regulator to operate. If AVINO falls below its falling POR threshold while the switching regulator is operating, the switching regulator will be shut down until AVINO returns.

Soft-Start

To avoid large in-rush current, V_{OUT} is slowly increased at startup to its final regulated value. Soft-start time is determined by the SS pin connection. If SS is pulled to AVINO, an internal 2ms timer is selected for soft-start. For other soft-start times, simply connect a capacitor from SS to GND. In this case, a 5.5µA current pulls up the SS voltage and the FB pin will follow this ramp until it reaches the 600mV reference level. Soft-start time for this case is described by Equation 1:

$$Time(ms) = C(nF) * 0.109 \quad \text{(EQ. 1)}$$

Power-Good

POK is the open-drain output of a window comparator that continuously monitors the buck regulator output voltage via the FB pin. POK is actively held low when EN is low and during the buck regulator soft-start period. After the soft-start period completes, POK becomes high impedance provided the FB pin is within the range specified in the "Electrical Specifications" on page 6. Should FB exit the specified window, POK will be pulled low until FB returns. Over-temperature faults also force POK low until the fault condition is cleared by an attempt to soft-start. There is an internal 5MΩ internal pull-up resistor.

PWM Control Scheme

The ER3110DI employs peak current-mode pulse-width modulation (PWM) control for fast transient response and pulse-by-pulse current limiting, as shown in the "Functional Block Diagram" on page 13. The current loop consists of the current sensing circuit, slope compensation ramp, PWM comparator, oscillator and latch. Current sense trans-resistance is typically 500mV/A and slope compensation rate, Se, is typically 450mV/T where T is the switching cycle period. The control reference for the current loop comes from the error amplifier's output (V_{COMP}).

A PWM cycle begins when a clock pulse sets the PWM latch and the upper FET is turned on. Current begins to ramp up in the upper FET and inductor. This current is sensed (V_{CSA}), converted to a voltage and summed with the slope compensation signal. This combined signal is compared to V_{COMP} and when the signal is equal to V_{COMP}, the latch is reset. Upon latch reset the upper FET is turned off and the lower FET turned on allowing current to ramp down in the inductor. The lower FET will remain on until the clock initiates another PWM cycle. Figure 44 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the current sense and slope compensation signal.

Output voltage is regulated as the error amplifier varies VCOMP and thus output inductor current. The error amplifier is a trans-conductance type and its output (COMP) is terminated with a series RC network to GND. This termination is internal (150k/54pF) if the COMP pin is tied to AVINO. Additionally, the trans-conductance for COMP = AVINO is 50µA/V vs 230µA/V for external RC connection. Its non-inverting input is internally connected to a 600mV reference voltage and its inverting input is connected to the output voltage via the FB pin and its associated divider network.

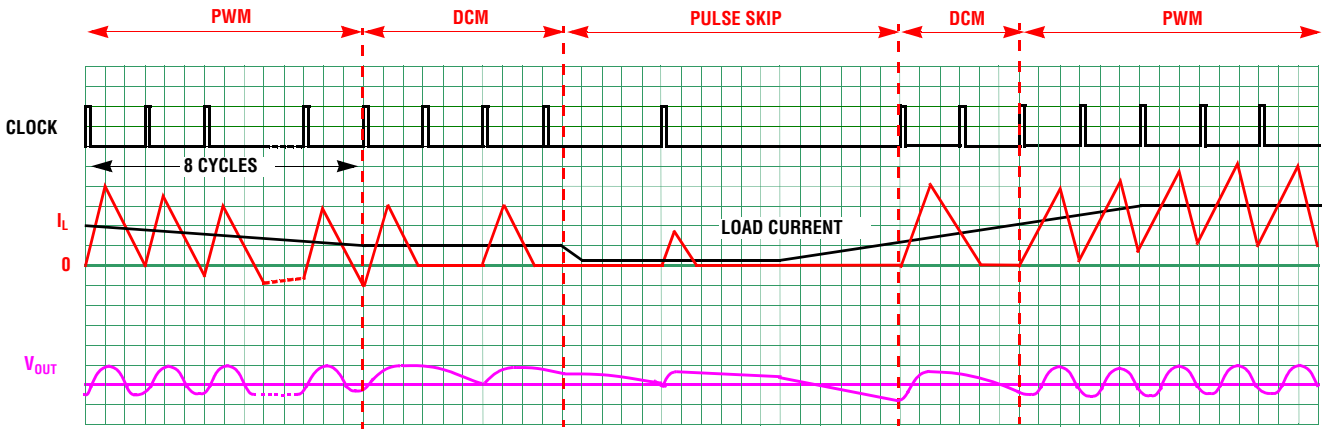


FIGURE 43. DCM MODE OPERATION WAVEFORMS

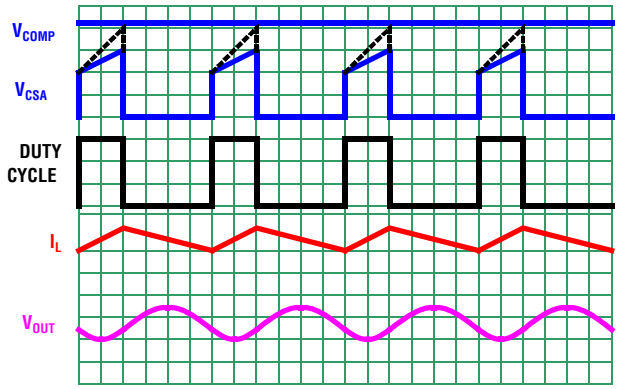


FIGURE 44. PWM OPERATION WAVEFORMS

Light Load Operation

At light loads, converter efficiency may be improved by enabling variable frequency operation (PFM). Connecting the SYNC pin to GND will allow the controller to choose such operation automatically when the load current is low. Figure 43 shows the DCM operation. The IC enters the DCM mode of operation when 8 consecutive cycles of inductor current crossing zero are detected. This corresponds to a load current equal to 1/2 the peak-to-peak inductor ripple current and set by Equation 2:

$$I_{OUT} = \frac{V_{OUT}(1 - D)}{2LF_{SW}} \quad \text{(EQ. 2)}$$

where D = duty cycle, F_{SW} = switching frequency, L = inductor value, I_{OUT} = output loading current, V_{OUT} = output voltage.

While operating in PFM mode, the regulator controls the output voltage with a simple comparator and pulsed FET current. A comparator signals the point at which FB is equal to the 600mV reference at which time the regulator begins providing pulses of current until FB is moved above the 600mV reference by 1%. The current pulses are approximately 300mA and are issued at a frequency equal to the converters programmed PWM operating frequency.

Due to the pulsed current nature of PFM mode, the converter can supply limited current to the load. Should load current rise beyond the limit, V_{OUT} will begin to decline. A second comparator signals an FB voltage 1% lower than the 600mV reference and forces the converter to return to PWM operation.

Output Voltage Selection

The regulator output voltage is easily programmed using an external resistor divider to scale V_{OUT} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; refer to Figure 45.

The output voltage programming resistor, R_3, depends on the value chosen for the feedback resistor, R_2, and the desired output voltage, V_{OUT}, of the regulator. Equation 3 describes the relationship between V_{OUT} and resistor values.

$$R_3 = \frac{R_2 x 0.6V}{V_{OUT} - 0.6V} \quad \text{(EQ. 3)}$$

If the desired output voltage is 0.6V, then R_3 is left unpopulated and R_2 is 0?.

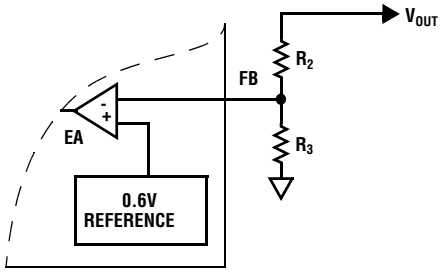


FIGURE 45. EXTERNAL RESISTOR DIVIDER

Protection Features

The ER3110DI is protected from overcurrent, negative overcurrent and over-temperature. The protection circuits operate automatically.

Overcurrent Protection

During PWM on-time, current through the upper FET is monitored and compared to a nominal 1.5A peak overcurrent limit. In the event that current reaches the limit, the upper FET will be turned off until the next switching cycle. In this way, FET peak current is always well limited.

If the overcurrent condition persists for 17 sequential clock cycles, the regulator will begin its hiccup sequence. In this case, both FETS will be turned off and POK will be pulled low. This condition will be maintained for 8 soft-start periods after which the regulator will attempt a normal soft-start.

Should the output fault persist, the regulator will repeat the hiccup sequence indefinitely. There is no danger even if the output is shorted during soft-start.

If V_{OUT} is shorted very quickly, FB may collapse below $5/8^{ths}$ of its target value before 17 cycles of overcurrent are detected. The ER3110DI recognizes this condition and will begin to lower its switching frequency proportional to the FB pin voltage. This insures that under no circumstance (even with V_{OUT} near 0V) will the inductor current run away.

Negative Current Limit

Should an external source somehow drive current into V_{OUT}, the controller will attempt to regulate V_{OUT} by reversing its inductor current to absorb the externally sourced current. In the event that the external source is low impedance, current may be reversed to unacceptable levels and the controller will initiate its negative current limit protection. Similar to normal overcurrent, the negative current protection is realized by monitoring the current through the lower FET. When the valley point of the inductor current reaches negative current limit, the lower FET is turned off and the upper FET is forced on until current reaches the **POSITIVE** current limit or an internal clock signal is issued. At this point, the lower FET is allowed to operate. Should the current again be pulled to the negative limit on the next cycle, the upper FET will again be forced on and current will be forced to $1/6^{th}$ of the positive current limit. At this point the controller will turn off both FET's and wait for COMP to indicate return to normal operation. During this time, the controller will apply a 100Ω load from SW to PGND and attempt to discharge the output. Negative current limit is a pulse-by-pulse style operation and recovery is automatic.

Over-Temperature Protection

Over-temperature protection limits maximum junction temperature in the ER3110DI. When junction temperature (T_J) exceeds +150°C, both FETs are turned off and the controller waits for temperature to decrease by approximately 20°C. During this time POK is pulled low. When temperature is within an acceptable range, the controller will initiate a normal soft-start sequence. For continuous operation, the +125°C junction temperature rating should not be exceeded.

Boot Undervoltage Protection

If the Boot capacitor voltage falls below 1.8V, the Boot undervoltage protection circuit will turn on the lower FET for 400ns to recharge the capacitor. This operation may arise during long periods of no switching such as PFM no load situations. In PWM operation near dropout (V_{PVIN} near V_{OUT}), the regulator may hold the upper FET on for multiple clock cycles. To prevent the boot capacitor from discharging, the lower FET is forced on for approximately 200ns every 10 clock cycles.

Application Guidelines

Simplifying the Design

While the ER3110DI offers user programmed options for most parameters, the easiest implementation with fewest components involves selecting internal settings for SS, COMP and FSW. Table 1 on page 4 provides component value selections for a variety of output voltages and will allow the designer to implement solutions with a minimum of effort.

Operating Frequency

The ER3110DI operates at a default switching frequency of 500kHz if F_{SW} is tied to V_{AVINO}. Tie a resistor from F_{SW} to GND to program the switching frequency from 300kHz to 2MHz, as shown in Equation 4.

$$R_{FSW}[k\Omega] = 108.75k\Omega * (t - 0.2\mu s) / 1\mu s \quad \text{(EQ. 4)}$$

Where:

t is the switching period in µs.

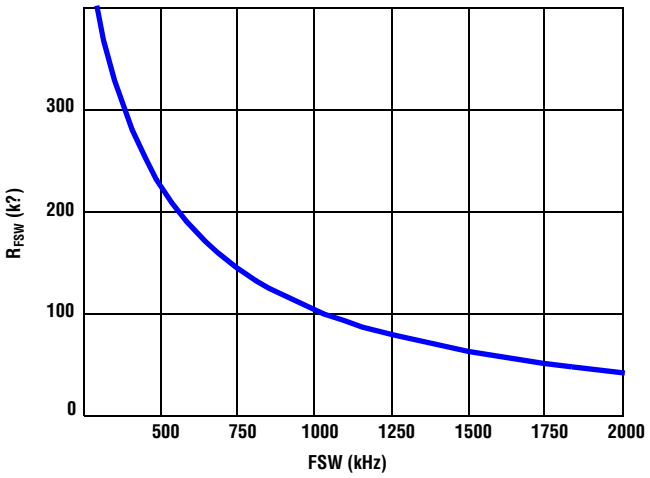


FIGURE 46. R_{FSW} SELECTION vs FSW

Synchronization Control

The frequency of operation can be synchronized up to 2MHz by an external signal applied to the SYNC pin. The rising edge on the SYNC triggers the rising edge of SW. To properly sync, the external source must be at least 10% greater than the programmed free running IC frequency.

Output Inductor Selection

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% of total load current. The inductor value can then be calculated using Equation 5:

$$L = \frac{V_{PVIN} - V_{OUT}}{FSW \times DI} \times \frac{V_{OUT}}{V_{PVIN}} \quad \text{(EQ. 5)}$$

Increasing the value of inductance reduces the ripple current and thus, the ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be

such that it will not saturate in overcurrent conditions. For typical ER3110DI applications, inductor values generally lies in the 10µH to 47µH range. In general, higher V_{OUT} will mean higher inductance.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current. The current mode control loop allows the use of low ESR ceramic capacitors and thus supports very small circuit implementations on the PC board. Electrolytic and polymer capacitors may also be used.

While ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. Nonetheless, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * F_{SW} * C_{OUT}} \quad \text{(EQ. 6)}$$

where DI is the inductor's peak-to-peak ripple current, F_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 7)}$$

Loop Compensation Design

When COMP is not connected to AVINO, the COMP pin is active for external loop compensation. The ER3110DI uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 47 shows the small signal model of the synchronous buck regulator.

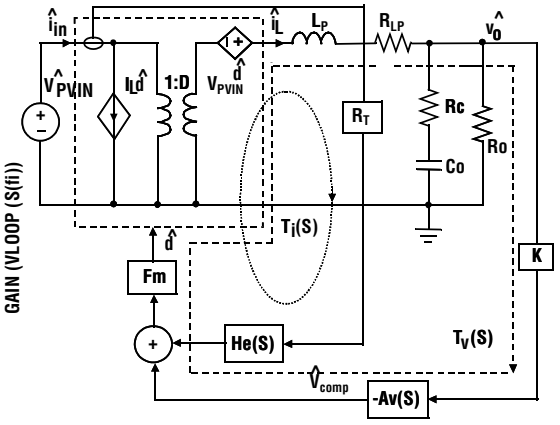


FIGURE 47. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

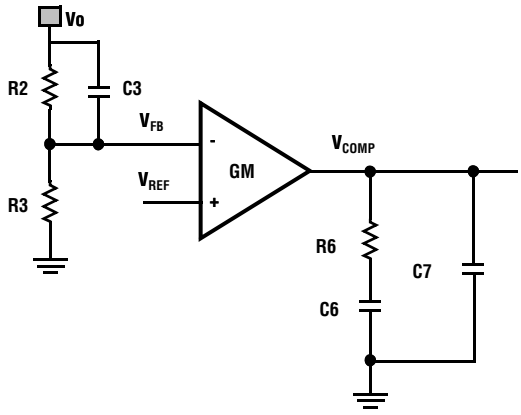


FIGURE 48. TYPE II COMPENSATOR

Figure 48 shows the type II compensator and its transfer function is expressed as shown in Equation 8:

$$A_v(S) = \frac{\hat{v}_{COMP}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \cdot \frac{\left(1 + \frac{S}{\omega_{tz1}}\right)\left(1 + \frac{S}{\omega_{tz2}}\right)}{S\left(1 + \frac{S}{\omega_{tp1}}\right)\left(1 + \frac{S}{\omega_{tp2}}\right)} \quad \text{(EQ. 8)}$$

where,

$$\omega_{tz1} = \frac{1}{R_6 C_6},\ \omega_{tz2} = \frac{1}{R_2 C_3},\ \omega_{tp1} = \frac{C_6 + C_7}{R_6 C_6 C_7},\ \omega_{tp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

High DC gain

Choose loop bandwidth f_c less than 100kHz

Gain margin: >10dB

Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 9.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 22.75 \times 10^3 \cdot f_c V_o C_o \quad \text{(EQ. 9)}$$

Where GM is the trans-conductance, g_m, of the voltage error amplifier in each phase. Compensator capacitor C_6 is then given by Equation 10.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_{SW} R_6}\right) \quad \text{(EQ. 10)}$$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 10. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

Put compensator zero 2 to 5 times f_c

$$C_3 = \frac{1}{\pi f_c R_2} \quad \text{(EQ. 11)}$$

Example: V_{PVIN} = 12V, V_O = 5V, I_O = 1A, F_{SW} = 500kHz, R_2 = 90.9kΩ, C_o = 22µF/5m?, L = 39µH, f_c = 50kHz, then compensator resistance R_6:

$$R_6 = 22.75\times10^3 \cdot 50kHz \cdot 5V \cdot 22\mu F = 125.12k\Omega \quad \text{(EQ. 12)}$$

It is acceptable to use 124kΩ as the closest standard value for R_6.

$$C_6 = \frac{5V \cdot 22\mu F}{1A \cdot 124k\Omega} = 0.88nF \quad \text{(EQ. 13)}$$

$$C_7 = \max\left(\frac{5m\Omega \cdot 22\mu F}{124k\Omega}, \frac{1}{\pi \cdot 500kHz \cdot 124k\Omega}\right) = (0.88pF, 5.1pF) \quad \text{(EQ. 14)}$$

It is also acceptable to use the closest standard values for C_6 and C_7. There is approximately 3pF parasitic capacitance from V_{COMP} to GND; Therefore, C_7 is optional. Use C_6 = 1500pF and C_7 = OPEN.

$$C_3 = \frac{1}{\pi \cdot 50kHz \cdot 90.9k\Omega} = 70pF \quad \text{(EQ. 15)}$$

Use C_3 = 68pF. Note that C_3 may increase the loop bandwidth from previous estimated value. Figure 49 shows the simulated voltage loop gain. It is shown that it has a 75kHz loop bandwidth with a 61° phase margin and 6dB gain margin. It may be more desirable to achieve an increased gain margin. This can be accomplished by lowering R_6 by 20% to 30%. In practice, ceramic capacitors have significant derating on voltage and temperature, depending on the type. Please refer to the ceramic capacitor datasheet for more details.

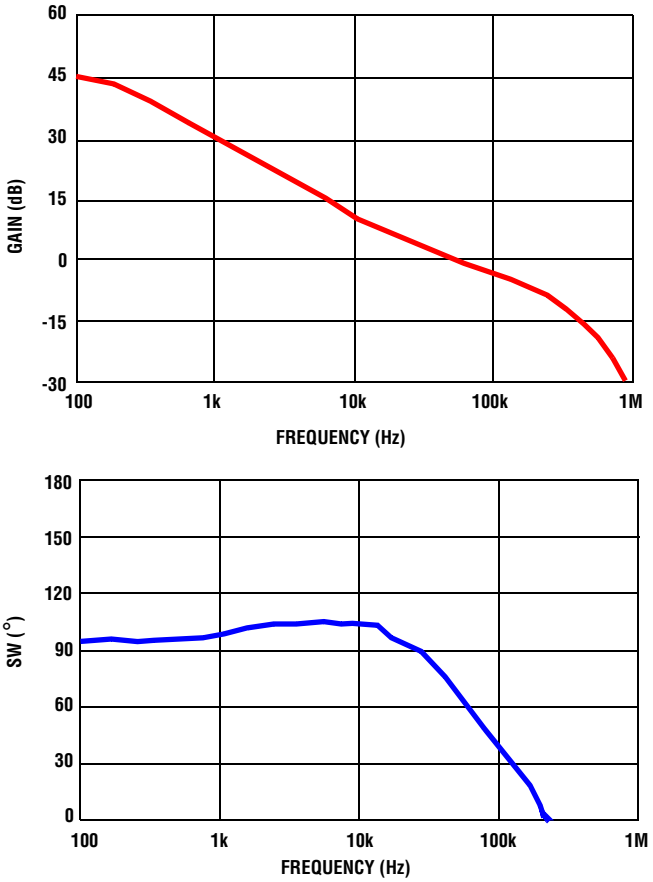


FIGURE 49. SIMULATED LOOP GAIN

Layout Considerations

Proper layout of the power converter will minimize EMI and noise and insure first pass success of the design. PCB layouts are provided in multiple formats on the Altera Enpirion web site. In addition, Figure 50 will make clear the important points in PCB layout. In reality, PCB layout of the ER3110DI is quite simple.

A multi-layer printed circuit board with GND plane is recommended. Figure 50 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent multiple physical capacitors. The most critical connections are to tie the PGND pin to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane insures a low impedance path for all return current, as well as an excellent thermal path to dissipate heat. With this connection made, place the high frequency MLCC input capacitor near the PVIN pin and use vias directly at the capacitor pad to tie the capacitor to the system GND plane.

The boot capacitor is easily placed on the PCB side opposite the controller IC and 2 vias directly connect the capacitor to BOOT and SW.

Place a 1µF MLCC near the AVINO pin and directly connect its return with a via to the system GND plane.

Place the feedback divider close to the FB pin and do not route any feedback components near SW or BOOT. If external components are used for SS, COMP or FSW the same advice applies.

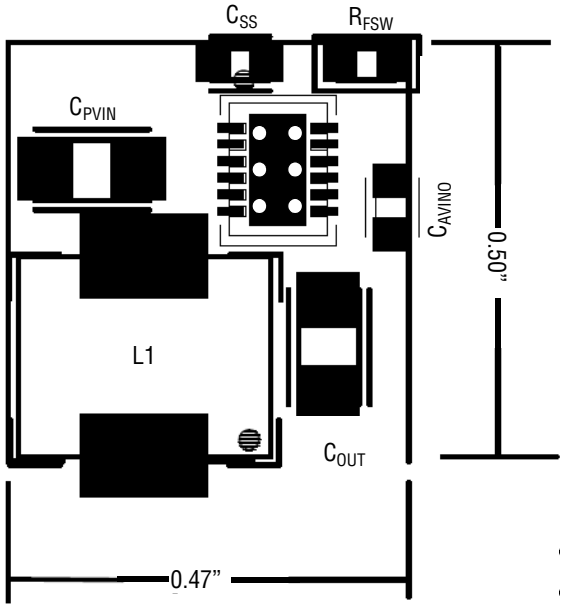


FIGURE 50. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Revision History

The table lists the revision history for this document.

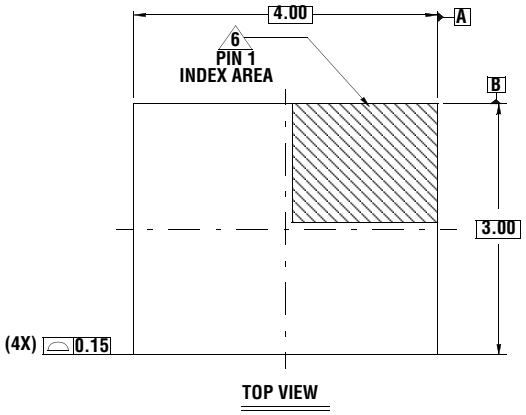
DATE	REVISION	CHANGE
May, 2014	1.0	Initial Release.

Package Outline Drawing

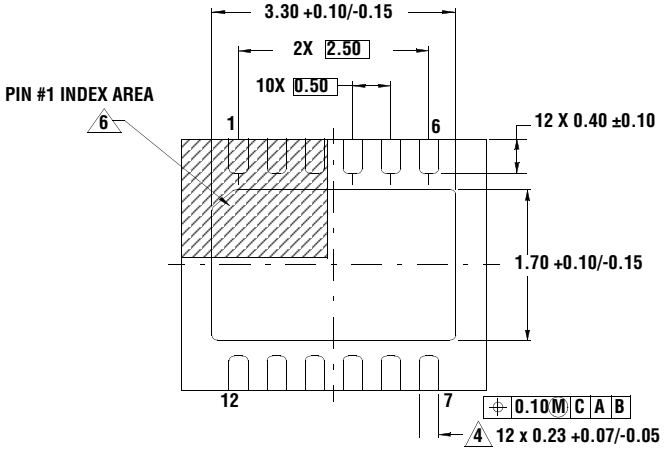
L12.4x3

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

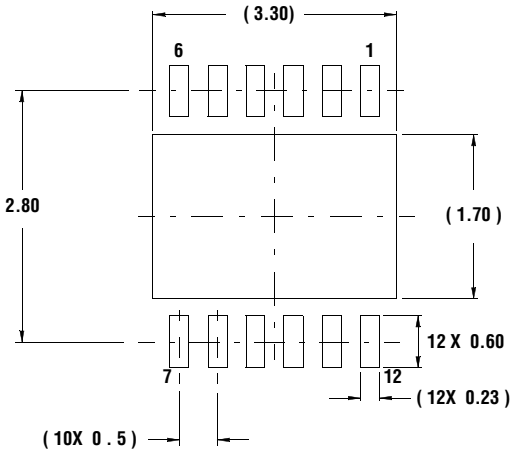
Rev 2, 7/10



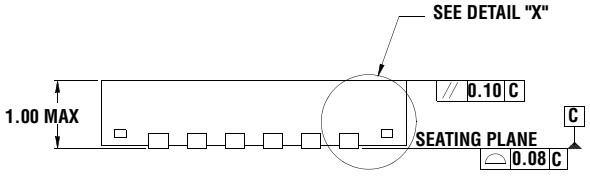
TOP VIEW



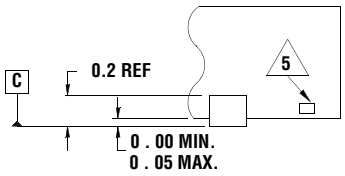
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229 V4030D-4 issue E.