M74LS161AP

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

DESCRIPTION

The M74LS161AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with direct reset input.

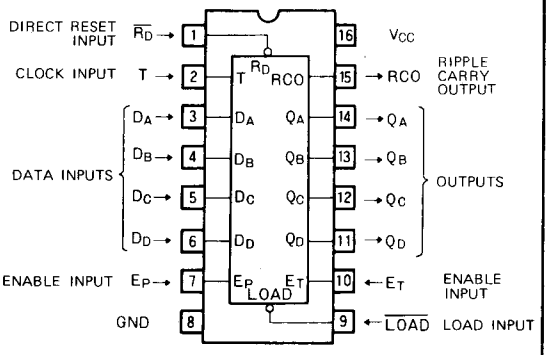
FEATURES

- Direct reset and synchronous preset inputs
- Enable input and carry output for cascaded operation
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20 ~ 75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPITON

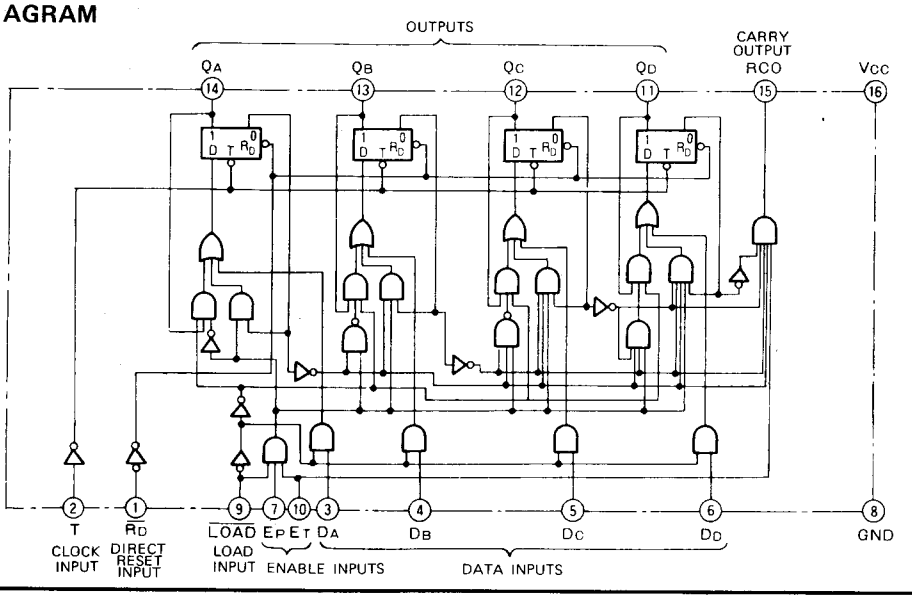
When a counting pulse is applied to the T input, the 4-bit binary representation of the count is output at Q_A, Q_B, Q_C and Q_D in synchronization with the count pulse. Counting is done on the transition of the T input signal from low to high.

Presetting is accomplished in synchronization with the counting pulse. When preset data is applied to the D_A, D_B, D_C and D_D inputs, the load input $\overline{LOAD}$ is made low, and T is changed from low to high, this data will appear in the Q_A, Q_B, Q_C and Q_D outputs, respectively regardless of the status of the enable inputs E_P and E_T, thereby presetting counter.

Resetting is performed asynchronously by setting the direct reset input $\overline{R_D}$ to low at which time the Q_A, Q_B, Q_C and Q_D outputs go to low-level regardless of the states of the other inputs.

The ripple carry output RCO is high only when all Q outputs and E_T are high. The two enable inputs E_P and E_T and the RCO carry output can be used to form an n-bit synchronous counter by means of cascade connection of several ICs (refer to the application example for the M74LS160AP).

BLOCK DIAGRAM



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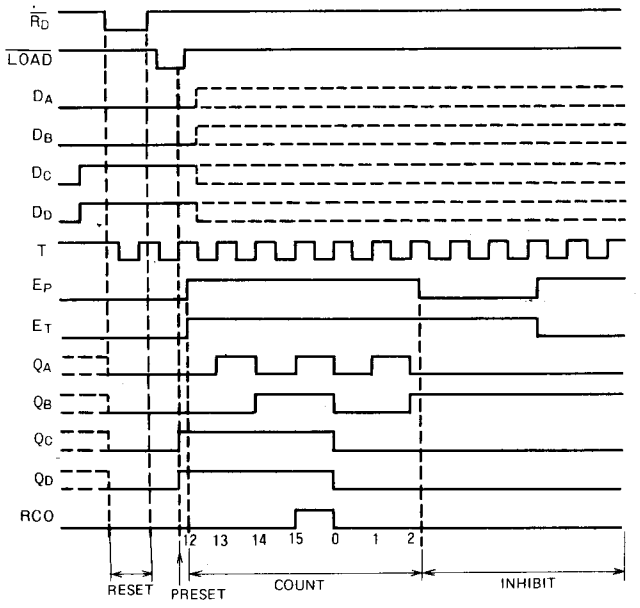
FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{LOAD}$	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1: ↑ : Indicates a transition from low to high (positive edge triggering).
* : RCO is normally low but is high when all Q outputs and E_T are high simultaneously, i.e., $RCO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$
X : irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

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ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	D_A, D_B, D_C, D_D, E_P	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		$\overline{LOAD}$, T, E_T					40	
		$\overline{R_D}$					20	
		D_A, D_B, D_C, D_D, E_P	V_{CC} = 5.25V, V_I = 10V				0.1	mA
		$\overline{LOAD}$, T, E_T					0.2	
		$\overline{R_D}$					0.1	
I_{IL}	Low-level input current	D_A, D_B, D_C, D_D, E_P	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
		$\overline{LOAD}$, T, E_T					−0.8	
		$\overline{R_D}$					−0.4	
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V (Note 3)			18	31	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V (Note 4)			19	32	mA

* : Typical values are for V_{CC}=5V and T_a=25°C

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T and $\overline{R_D}$ at 4.5V and the $\overline{LOAD}$ input at 0V, changing the T input from 0V to 4.5V.

4: Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T, $\overline{R_D}$ and $\overline{LOAD}$ at 0V, changing the T input from 0V to 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	C_L = 15pF (Note 5)	25	55		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			20	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Lwo-to-high-level, high-to-low-level output propagation time (when $\overline{LOAD}$ is high), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time (when $\overline{LOAD}$ is low), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_T to output RCO			8	14	ns
t_{PHL}				8	14	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ outputs Q_A, Q_B, Q_C, Q_D			15	28	ns

TIMING REQUIREMENTS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{W(TH)}$	Clock input T high pulse width		25	7		ns
$t_{W(TL)}$	Clock input T low pulse width		25	6		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		20	6		ns
t_r	Clock pulse rise-time			400	100	ns
$t_{SU(D)}$	Setup time D_A ~ D_D to T		20	3		ns
$t_{SU(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T (Note 8)		20	6		ns
$t_{SU(E)}$	Setup time E_P, E_T to T		20	8		ns
$t_{h(D)}$	Hold time D_A ~ D_D to T		3	0		ns
$t_{h(\overline{LOAD})}$	Hold time $\overline{LOAD}$ to T (Note 8)		3	−3		ns
$t_{h(E)}$	Hold time E_P, E_T to T		3	−3		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to T		15	6		ns

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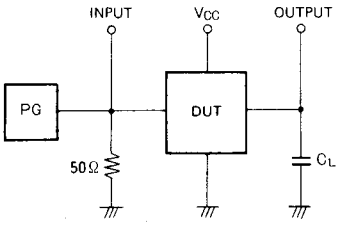
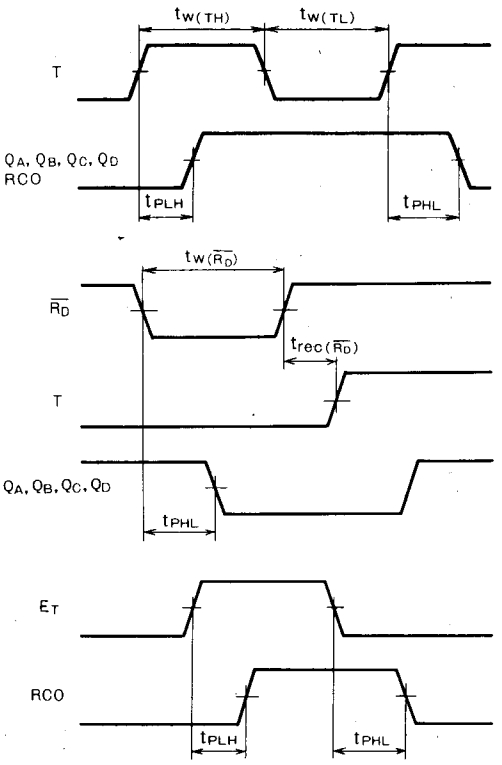
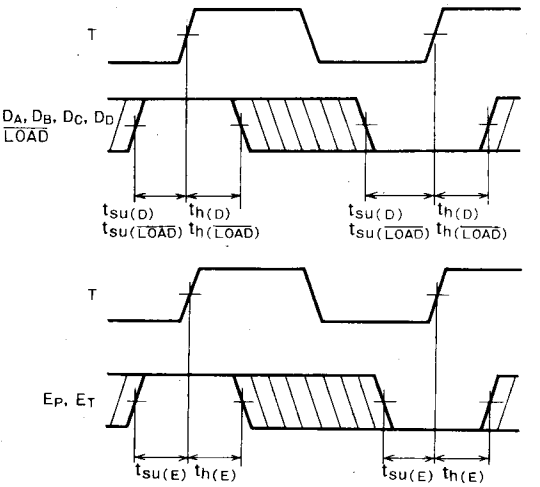
Note 5: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

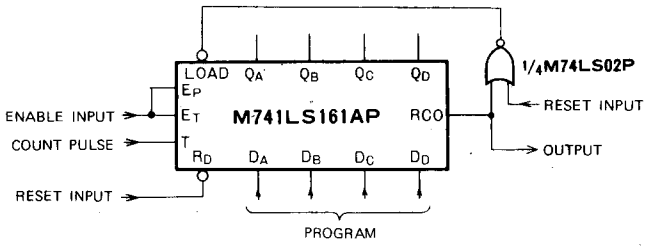




Note 6. The shaded area indicates the period within which switching may take place.

APPLICATION EXAMPLE

Programmable divider



Note 7: Reset is performed by applying countpulse with reset input high. $\overline{R_D}$ pin cannot be used since Q_A~Q_D should be set low.

DA	DB	DC	DD	Divide rate
L	L	L	L	1/16
H	L	L	L	1/15
L	H	L	L	1/14
H	H	L	L	1/13
L	L	H	L	1/12
H	L	H	L	1/11
L	H	H	L	1/10
H	H	H	L	1/9
L	L	L	H	1/8
H	L	L	H	1/7
L	H	L	H	1/6
H	H	L	H	1/5
L	L	H	H	1/4
H	L	H	H	1/3
L	H	H	H	1/2

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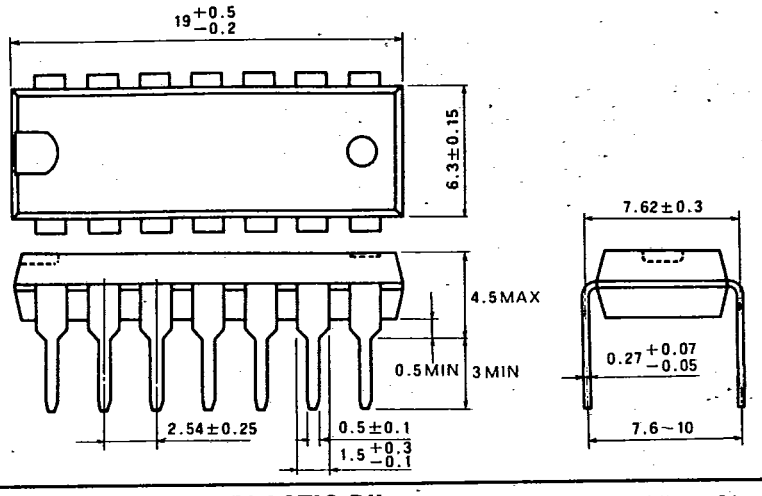
T-90-20

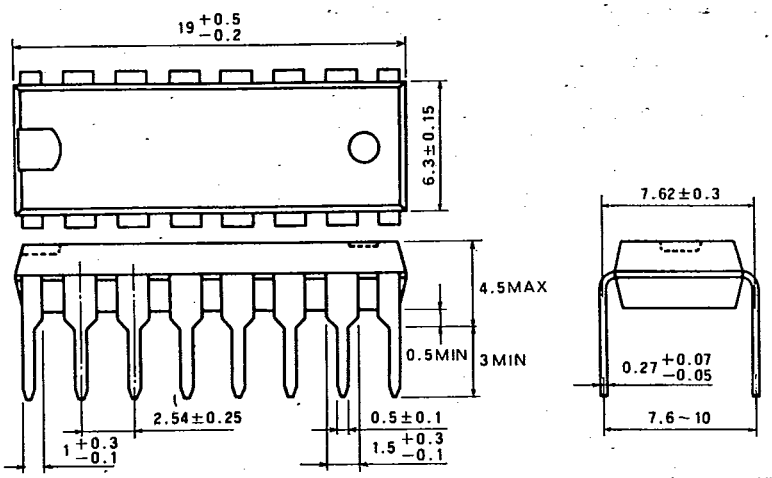
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm