ADVANCED
LINEAR
DEVICES, INC.

PRECISION LOW POWER CMOS OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD1732A/ALD1732 is a precision low-cost low-power monolithic CMOS operational amplifier intended for a broad range of precision applications requiring exremely low input signal power. Input signal power is the product of input offset voltage and input bias current, which represents the minimum required power draw from the signal source in order to drive the input of the operational amplifier. Input signal power is also a figure of merit in source loading and its associated error, and is a measure of the basic signal resolution possible through the operational amplifier for a given signal source. For certain types of signal sources, signal loading directly translates into a significant distortion or "interface noise equivalent" term.

Manufactured with Advanced Linear Devices' enhanced EPAD® silicon gate CMOS process, the ALD1732A/ALD1732 is designed to set a new standard in low input signal power requirements. The typical input loading at its input is 0.03 mV offset voltage and 0.01 pA input bias current at 25C, resulting in 0.0003 fW input signal power draw. This input characteristic virtually eliminates any loading effects on most types of signal sources, offering unparalled accuracy and signal integrity and fidelity. The ALD1732A/ALD1732 is ideally suited for capacitive and high sensitivity, high impedance signal sources. It is readily suited for +5V single supply (or ±2V to ±5V) systems, with low operating power dissipation, a traditional strength of CMOS technology. It is offered with industry standard μA741 and ICL7611 pin configurations.

The ALD1732A/ALD1732 can operate with rail to rail large signal input and output voltages with relatively high slew rate. The input voltage can be equal to or exceed the positive and negative supply voltages while the output voltage can swing close to these supply voltage rails. This feature significantly reduces the supply overhead voltage required to operate the operational amplifier and allows numerous analog serial stages to operate in a low power supply environment. In addition, the device can accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. This device also features rail-to-rail input and output voltage ranges, tolerance to over-voltage input spikes of 300mV beyond supply rails, high open loop voltage gain, useful bandwidth of 1.5MHz, slew rate of 2.1V/μs, and low supply current of 0.8mA. Finally, the output stage can typically drive up to 400pF capacitive loads in the unity gain mode and up to 4000pF capacitive loads at a gain of 5.

These features make the ALD1732A/ALD1732 a versatile, high precision operational amplifier that is user friendly and easy to use with virtually no source loading and zero input-loading induced source errors. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1732ASAL	ALD1732APAL	
ALD1732SAL	ALD1732PAL	
ALD1732ASA	ALD1732APA	ALD1732ADA
ALD1732SA	ALD1732PA	ALD1732DA

* Contact factory for leaded (non-RoHS) or high temperature versions.

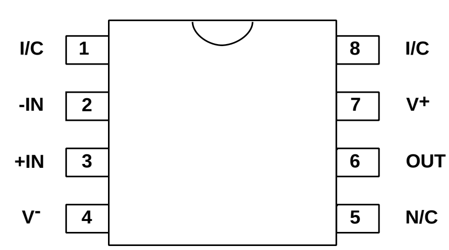
FEATURES & BENEFITS

- Extremely low input offset voltages and extremely low input bias currents
- Extremely low input signal power
- Robust high-temperature operation
- Industry standard pinout
- Rail-to-rail input/output
- Input bias current of 0.01pA at input offset voltage of 30μV
- No external components
- No internal chopper clocking noise
- No chopper dynamic power dissipation
- Simple and cost effective
- Small package size
- Drive up to 4000pF load capacitance
- Low power dissipation
- Suitable for rugged, temperature-extreme environments

APPLICATIONS

- Precision cable driver
- Sensor interface circuits
- Unity gain buffer amplifier
- Precision analog cable driver
- Transducer biasing circuits
- Capacitive and charge integration circuits
- Biochemical probe interface
- Signal conditioning
- Portable instruments
- High source impedance electrode amplifiers
- Precision Sample and Hold amplifiers
- Precision current to voltage converter
- Error correction circuits
- Sensor compensation circuits
- Precision gain amplifiers
- System output level shifter

PIN CONFIGURATION



TOP VIEW
SAL, PAL, SA, PA, DA PACKAGES

* I/C pins are internally connected. Do not connect externally.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+		10.6V
Differential input voltage range		-0.3V to V^+ +0.3V
Power dissipation		600mW
Operating temperature range	SAL, PAL, SA, PA packages	0°C to +70°C
	DA package	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature, 10 seconds		+260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	ALD1732A Min	ALD1732A Typ	ALD1732A Max	ALD1732 Min	ALD1732 Typ	ALD1732 Max	Unit	Test Conditions
Supply Voltage	V_S V^+	±2.0 4.0		±5.0 10.0	±2.0 4.0		±5.0 10.0	V V	Dual Supply Single Supply
Input Offset Voltage	V_{OS}		30	150		80	400	µV	R_S ≤ 100KΩ
Input Offset Current	I_{OS}		0.01	10 280		0.01	10 280	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Bias Current	I_B		0.01	10 280		0.01	10 280	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Voltage Range	V_{IR}	-0.3 -2.8		+5.3 +2.8	-0.3 -2.8		+5.3 +2.8	V V	V^+ = +5V V_S = ±2.5V
Input Resistance	R_{IN}		10^{14}			10^{14}		Ω	
Input Offset Voltage Drift	TCV_{OS}		5			5		µV/°C	R_S ≤ 100KΩ
Power Supply Rejection Ratio	PSRR		85			85		dB	R_S ≤ 100KΩ
Common Mode Rejection Ratio	CMRR		97			97		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V		250 500			250 500		V/mV V/mV	R_L = 10KΩ R_L = 1MΩ
Output Voltage Range	V_O low V_O high	 4.99	0.002 4.999	0.01	 4.99	0.002 4.999	0.01	V V	R_L = 1MΩ, V^+ = +5 0°C ≤ T_A ≤ +70°C
	V_O low V_O high	 2.35	-2.44 2.44	-2.35	 2.35	-2.44 2.44	-2.35	V V	R_L =10KΩ 0°C ≤ T_A ≤ +70°C
Output Short Circuit Current	I_{SC}		8			8		mA	
Supply Current	I_S		0.8	1.25		0.8	1.25	mA	V_{IN} = 0V, No Load
Power Dissipation	P_D		4.0	6.25		4.0	6.25	mW	V_S = ±2.5V
Input Capacitance	C_{IN}		1			1		pF	
Maximum Load Capacitance	C_L		400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Input Noise Voltage	en		26			26		nV/√Hz	f = 1KHz
Input Current Noise	in		0.6			0.6		fA/√Hz	f = 10Hz
Bandwidth	B_W	1.0	1.5		1.0	1.5		MHz	
Slew Rate	S_R	1.4	2.1		1.4	2.1		V/µs	A_V = +1, R_L = 10KΩ

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

T_A = 25°C V_S = ±2.5V unless otherwise specified (cont'd)

Parameter	Symbol	ALD1732A Min	ALD1732A Typ	ALD1732A Max	ALD1732 Min	ALD1732 Typ	ALD1732 Max	Unit	Test Conditions
Rise time	t_r		0.2			0.2		µs	R_L = 10KΩ
Overshoot Factor			10			10		%	R_L = 10KΩ, C_L = 100pF
Settling Time	t_S		8.0 3.0			8.0 3.0		µs µs	0.01% 0.1%, A_V = -1, R_L= 1MΩ, C_L = 25pF

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	ALD1732A Min	ALD1732A Typ	ALD1732A Max	ALD1732 Min	ALD1732 Typ	ALD1732 Max	Unit	Test Conditions
Power Supply Rejection Ratio	PSRR		85			85		dB	R_S ≤ 100KΩ
Common Mode Rejection Ratio	CMRR		97			97		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V		250			250		V/mV	R_L = 10KΩ
Output Voltage Range	V_O low V_O high	 4.80	-4.90 4.93	-4.80	 4.80	-4.90 4.93	-4.80	V	R_L = 10KΩ
Bandwidth	B_W		1.7			1.7		MHz	
Slew Rate	S_R		2.8			2.8		V/µs	A_V = +1, C_L = 50pF

V_S = ±2.5V -55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Symbol	ALD1732A Min	ALD1732A Typ	ALD1732A Max	ALD1732 Min	ALD1732 Typ	ALD1732 Max	Unit	Test Conditions
Input Offset Voltage	V_{OS}		0.5	2.0		0.7	3.5	mV	R_S ≤ 100KΩ
Input Offset Current	I_{OS}			2.0			2.0	nA	
Input Bias Current	I_B			2.0			2.0	nA	
Power Supply Rejection Ratio	PSRR		85			85		dB	R_S ≤ 100KΩ
Common Mode Rejection Ratio	CMRR		97			97		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V		25			25		V/mV	R_L = 10KΩ
Output Voltage Range	V_O low V_O high	 2.30	-2.40 2.40	-2.30	 2.30	-2.40 2.40	-2.30	V V	R_L = 10KΩ

Design & Operating Notes:

1. The ALD1732A/ALD1732 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1732A/ALD1732 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD1732A/ALD1732 will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD1732A/ALD1732 has shown itself to be more resistant to parasitic oscillations.

2. The ALD1732A/ALD1732 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail common mode input voltage ranges. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. Since offset voltage trimming on the ALD1732A/ALD1732 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions below this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer and should make provisions in the design to allow for input offset voltage variations.

3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{14}\Omega$ would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

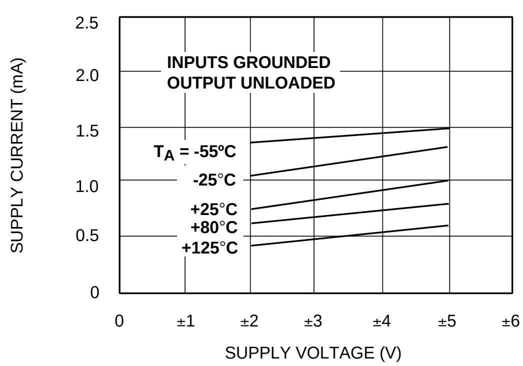
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

5. The ALD1732A/ALD1732 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

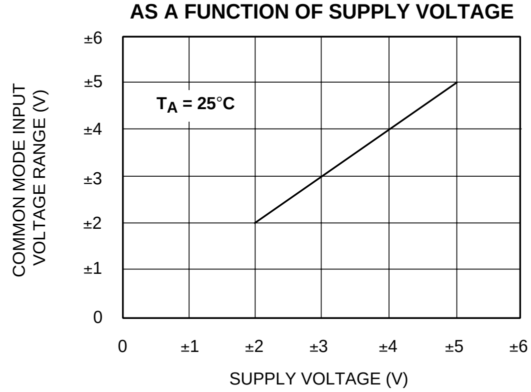
6. The ALD1732A/ALD1732 has an internal design architecture that provides robust high temperature operation. Contact factory for custom screening versions.

TYPICAL PERFORMANCE CHARACTERISTICS

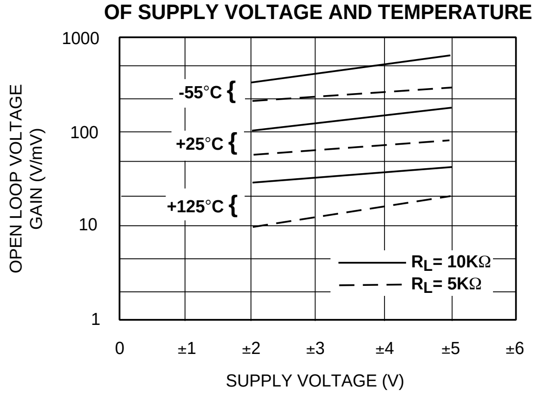
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



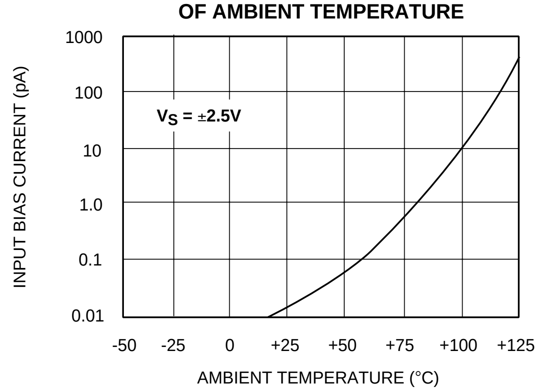
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE

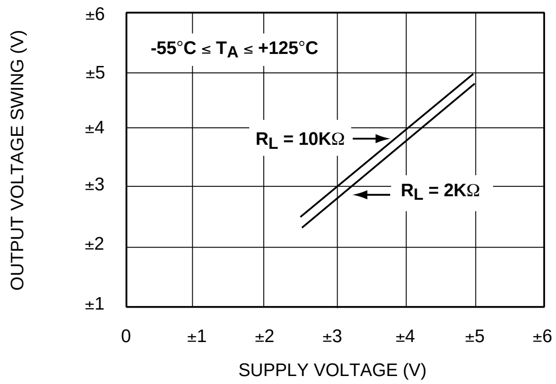


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

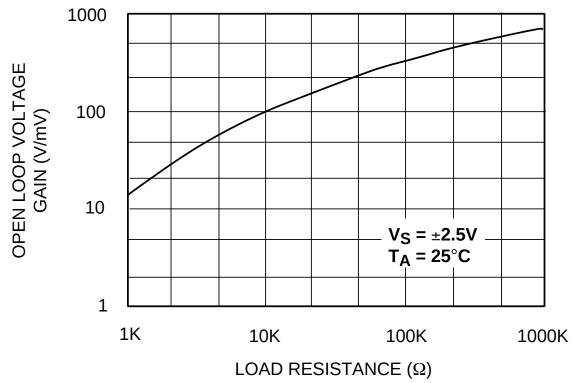


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

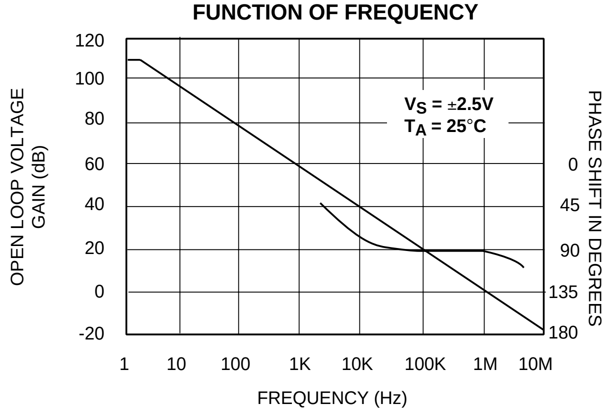
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



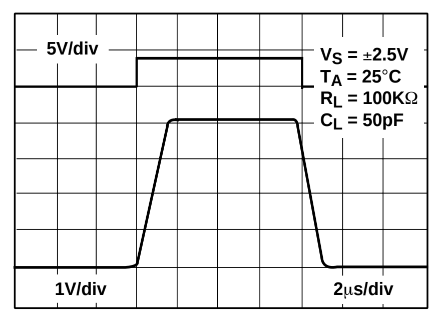
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



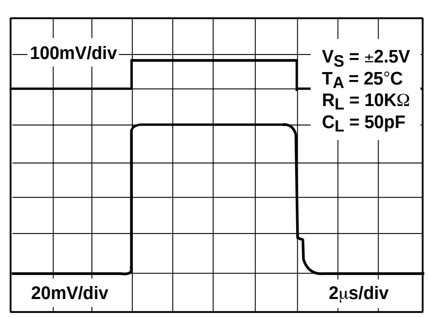
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



LARGE-SIGNAL TRANSIENT RESPONSE

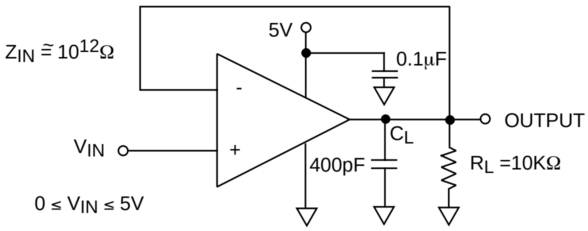


SMALL-SIGNAL TRANSIENT RESPONSE



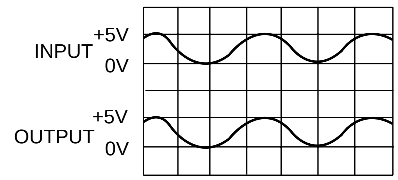
TYPICAL APPLICATIONS

RAIL TO RAIL VOLTAGE FOLLOWER/BUFFER



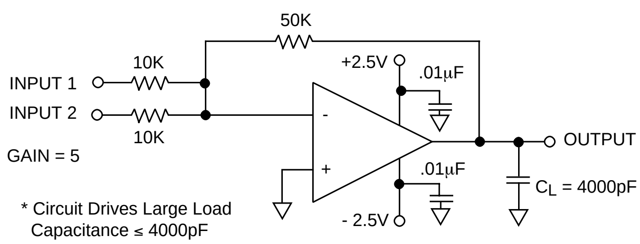
* See rail to rail waveform

RAIL-TO-RAIL WAVEFORM



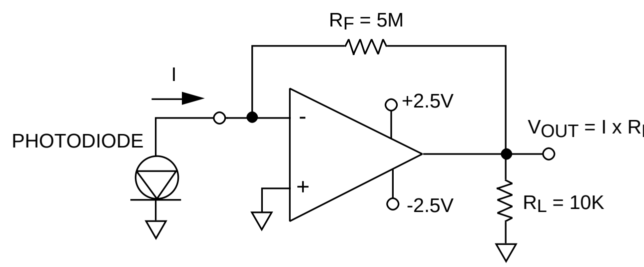
Performance waveforms.
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-rail voltage follower.

LOW OFFSET SUMMING AMPLIFIER

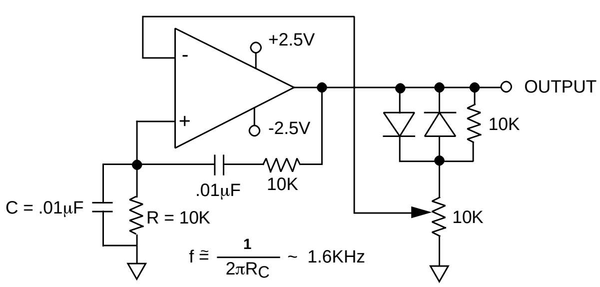


* Circuit Drives Large Load
Capacitance ≤ 4000pF

PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER

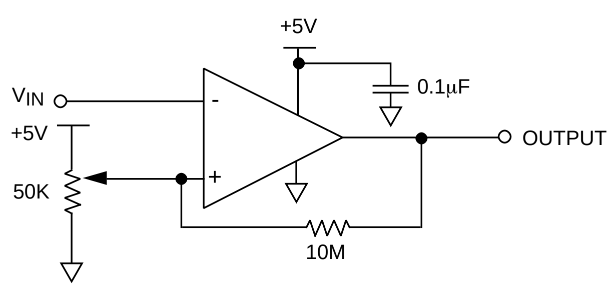


WIEN BRIDGE OSCILLATOR (RAIL-TO -RAIL) SINE WAVE GENERATOR



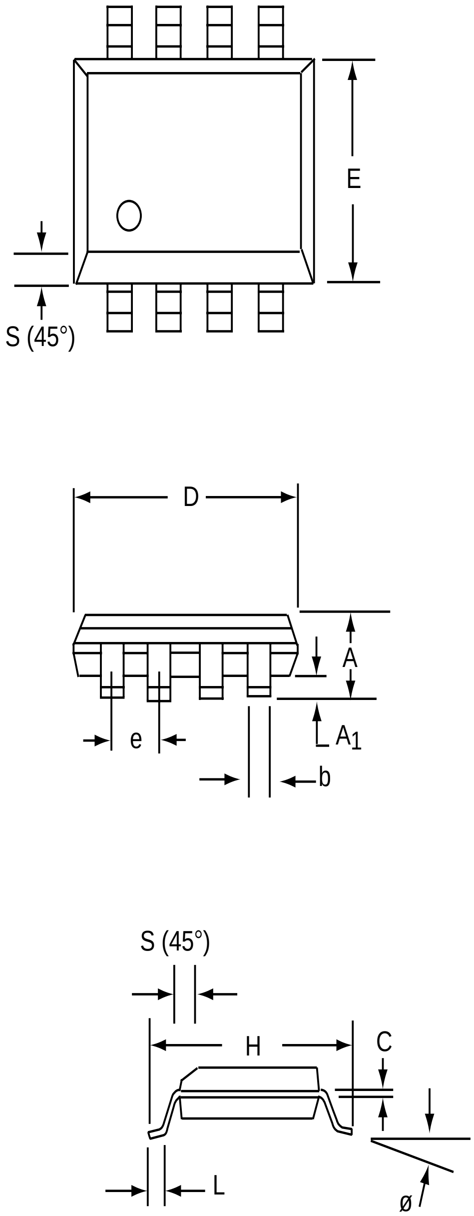
* See rail to rail waveform

RAIL-TO-RAIL VOLTAGE COMPARATOR



SOIC-8 PACKAGE DRAWING

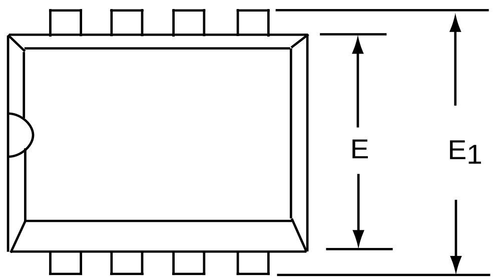
8 Pin Plastic SOIC Package

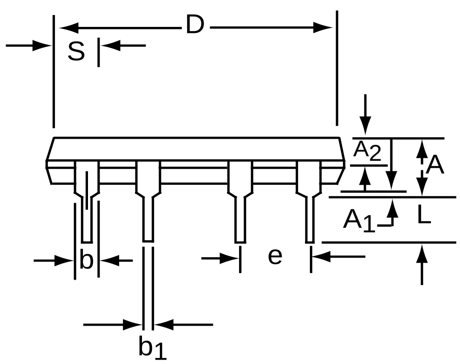


Dim	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

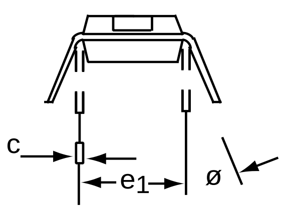
PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



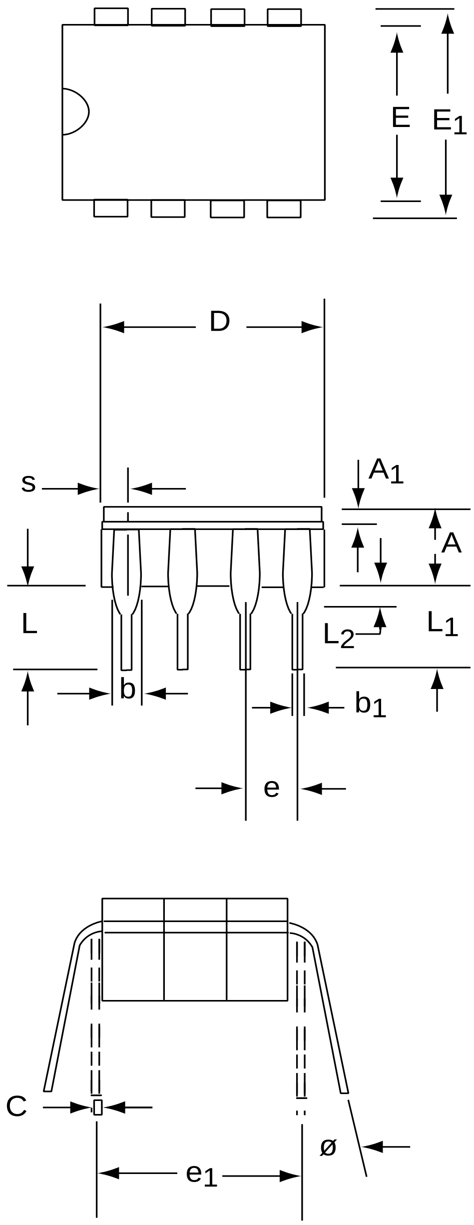


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°



CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°