

## 74ACTQ02

### Quad 2-Input NOR Gate

#### General Description

The ACTQ02 contains four, 2-input NOR gates.

The ACTQ utilize Fairchild's Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior AC/DC performance.

#### Features

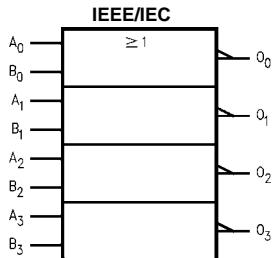
- $I_{CC}$  reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Outputs source/sink 24 mA
- ACTQ02 has TTL-compatible inputs

#### Ordering Code:

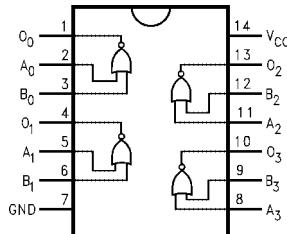
| Order Number | Package Number | Package Description   |
|--------------|----------------|---|
| 74ACTQ02SC   | M14A           | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body |
| 74ACTQ02SJ   | M14D           | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide                     |
| 74ACTQ02PC   | N14A           | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide            |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

| Pin Names  | Description |
|------------|-------------|
| $A_n, B_n$ | Inputs      |
| $O_n$      | Outputs     |

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**Absolute Maximum Ratings**(Note 1)

|  |                          |         |
|--|--------------------------|---------|
| Supply Voltage ( $V_{CC}$ )  | −0.5V to +7.0V           |         |
| DC Input Diode Current ( $I_{IK}$ )                                    |                          |         |
| $V_I = -0.5V$  | −20 mA                   |         |
| $V_I = V_{CC} + 0.5V$  | +20 mA                   |         |
| DC Input Voltage ( $V_I$ )   | −0.5V to $V_{CC} + 0.5V$ |         |
| DC Output Diode Current ( $I_{OK}$ )                                   |                          |         |
| $V_O = -0.5V$  | −20 mA                   |         |
| $V_O = V_{CC} + 0.5V$  | +20 mA                   |         |
| DC Output Voltage ( $V_O$ )  | −0.5V to $V_{CC} + 0.5V$ |         |
| DC Output Source or Sink Current ( $I_O$ )                             |                          | ±50 mA  |
| DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) |                          | ±50 mA  |
| Storage Temperature ( $T_{STG}$ )                                      | −65°C to +150°C          |         |
| DC Latch-Up Source or Sink Current                                     |                          | ±300 mA |
| Junction Temperature ( $T_J$ )   |                          | 140°C   |
| PDIP   |                          |         |

**Recommended Operating Conditions**

|   |                |
|---|----------------|
| Supply Voltage ( $V_{CC}$ )                     | 4.5V to 5.5V   |
| Input Voltage ( $V_I$ )                         | 0V to $V_{CC}$ |
| Output Voltage ( $V_O$ )                        | 0V to $V_{CC}$ |
| Operating Temperature ( $T_A$ )                 | −40°C to +85°C |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) | 125 mV/ns      |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

| Symbol    | Parameter                                | $V_{CC}$<br>(V)          | $T_A = +25^\circ C$            |                            | Units   | Conditions                            |
|-----------|--|--------------------------|--------------------------------|----------------------------|---|---------------------------------------|
|           |  |                          | Typ                            | Guaranteed Limits          |   |                                       |
| $V_{IH}$  | Minimum HIGH Level Input Voltage         | 4.5<br>5.5               | 1.5<br>1.5                     | 2.0<br>2.0                 | 2.0<br>2.0  | V $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| $V_{IL}$  | Maximum LOW Level Input Voltage          | 4.5<br>5.5               | 1.5<br>1.5                     | 0.8<br>0.8                 | 0.8<br>0.8  | V $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| $V_{OH}$  | Minimum HIGH Level Output Voltage        | 4.5<br>5.5<br>4.5<br>5.5 | 4.49<br>5.49<br>3.86<br>4.86   | 4.4<br>5.4<br>3.76<br>4.76 | V $I_{OUT} = -50 \mu A$<br>$V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OH} = -24 mA$<br>$I_{OH} = -24 mA$ (Note 2) |                                       |
| $V_{OL}$  | Maximum LOW Level Output Voltage         | 4.5<br>5.5<br>4.5<br>5.5 | 0.001<br>0.001<br>0.36<br>0.36 | 0.1<br>0.1<br>0.44<br>0.44 | V $I_{OUT} = 50 \mu A$<br>$V_{IN} = V_{IL}$ or $V_{IH}$<br>$I_{OL} = 24 mA$<br>$I_{OL} = 24 mA$ (Note 2)    |                                       |
| $I_{IN}$  | Maximum Input Leakage Current            | 5.5                      |                                | ±0.1                       | ±1.0  | µA $V_I = V_{CC}$ , GND               |
| $I_{CCT}$ | Maximum $I_{CC}$ /Input                  | 5.5                      | 1.6                            |                            | 1.5   | mA $V_I = V_{CC} - 2.1V$              |
| $I_{OLD}$ | Minimum Dynamic                          | 5.5                      |                                |                            | 75  | mA $V_{OLD} = 1.65V$ Max              |
| $I_{OHD}$ | Output Current (Note 3)                  | 5.5                      |                                |                            | −75   | mA $V_{OHD} = 3.85V$ Min              |
| $I_{CC}$  | Maximum Quiescent Supply Current         | 5.5                      |                                | 2.0                        | 20.0  | µA $V_{IN} = V_{CC}$ or GND           |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$    | 5.0                      | 1.1                            | 1.5                        |   | V Figure 1, Figure 2 (Note 4)(Note 5) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$    | 5.0                      | −0.6                           | −1.2                       |   | V Figure 1, Figure 2 (Note 4)(Note 5) |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 5.0                      | 1.9                            | 2.2                        |   | V (Note 4)(Note 6)                    |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage  | 5.0                      | 1.2                            | 0.8                        |   | V (Note 4)(Note 6)                    |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** Plastic DIP package

**Note 5:** Max number of outputs defined as (n). Data inputs are 0V to 3V. One output @ GND.

**Note 6:** Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ), f = 1 MHz.

## AC Electrical Characteristics

| Symbol   | Parameter                         | V <sub>CC</sub><br>(V)<br>(Note 7) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     |     | T <sub>A</sub> = -40°C to +85°C<br>C <sub>L</sub> = 50 pF |     |    | Units |
|--|-----------------------------------|------------------------------------|--|-----|-----|---|-----|----|-------|
|  |                                   |                                    | Min  | Typ | Max | Min   | Max |    |       |
| t <sub>PLH</sub>   | Propagation Delay Data to Output  | 5.0                                | 2.0  | 5.0 | 7.5 | 2.0   | 8.0 | ns |       |
| t <sub>PHL</sub>   | Propagation Delay Data to Output  | 5.0                                | 2.0  | 5.0 | 7.5 | 2.0   | 8.0 | ns |       |
| t <sub>O<sub>SHL</sub></sub> ,<br>t <sub>O<sub>SLH</sub></sub> | Output to Output<br>Skew (Note 8) | 5.0                                |  | 0.5 | 1.0 |   | 1.0 | ns |       |

**Note 7:** Voltage Range 5.0 is 5.0V  $\pm$  0.5V

**Note 8:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>O<sub>SHL</sub></sub>) or LOW-to-HIGH (t<sub>O<sub>SLH</sub></sub>). Parameter guaranteed by design.

## Capacitance

| Symbol          | Parameter                     | Typ | Units | Conditions             |
|-----------------|-------------------------------|-----|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance             | 4.5 | pF    | V <sub>CC</sub> = OPEN |
| C <sub>PD</sub> | Power Dissipation Capacitance | 75  | pF    | V <sub>CC</sub> = 5.0V |

## FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

### Equipment:

Hewlett Packard Model 8180A Word Generator  
PC-163A Test Fixture  
Tektronics Model 7854 Oscilloscope

### Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

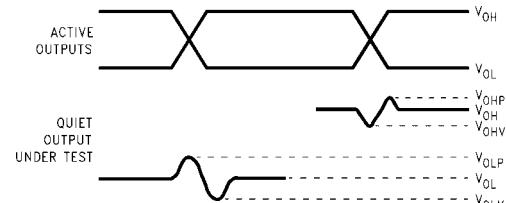


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note 9:  $V_{OHP}$  and  $V_{OLP}$  are measured with respect to ground reference.

Note 10: Input pulses have the following characteristics:  $f = 1$  MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, skew < 150 ps.

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

$V_{OLP}/V_{OLV}$  and  $V_{OHP}/V_{OHV}$ :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure  $V_{OLP}$  and  $V_{OLV}$  on the quiet output during the worst case transition for active and enable.  $V_{OHP}$  and  $V_{OHV}$  on the quiet output during the worst case transition for active and enable.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

$V_{ILD}$  and  $V_{IHD}$ :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{IL}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input LOW voltage level at which oscillation occurs is defined as  $V_{ILD}$ .
- Next decrease the input HIGH voltage level,  $V_{IH}$ , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds  $V_{IL}$  limits, or on output HIGH levels that exceed  $V_{IH}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{IHD}$ .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

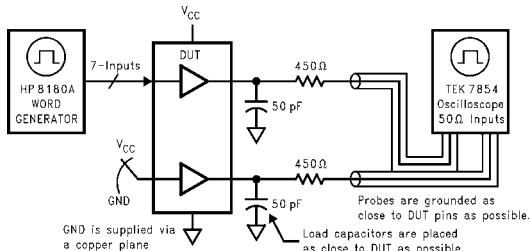
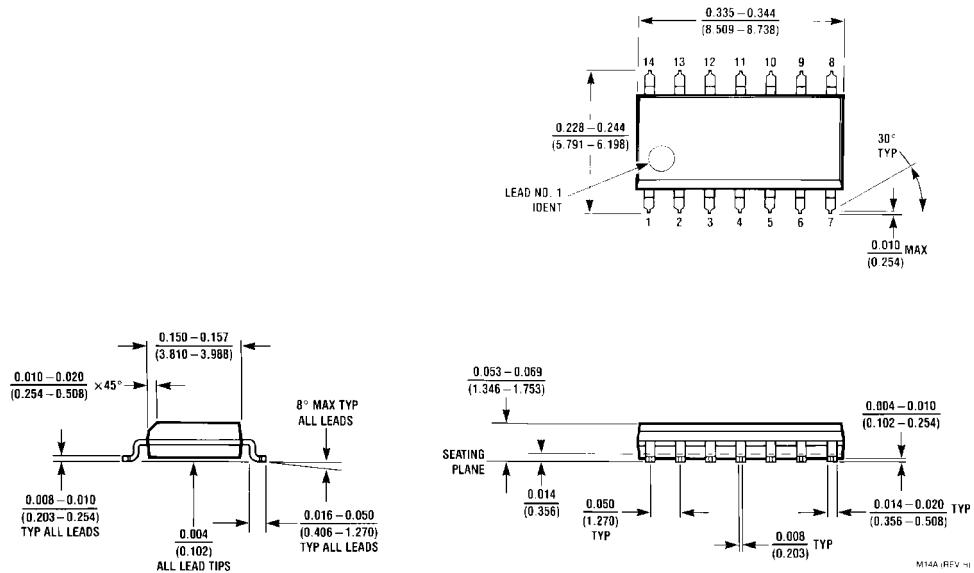
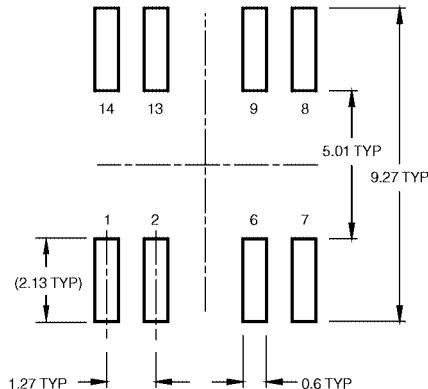
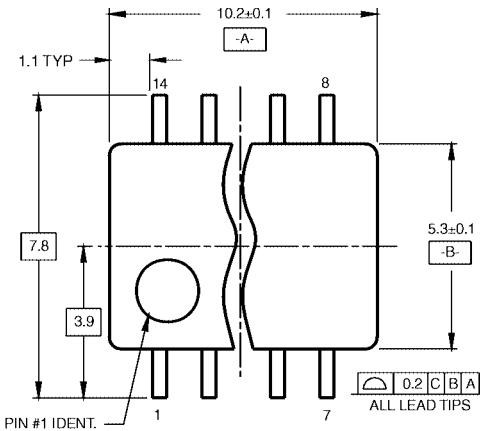
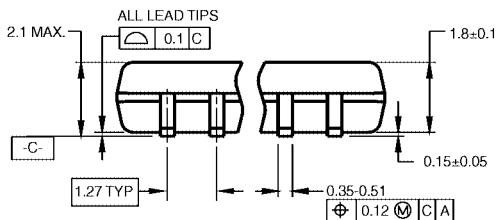


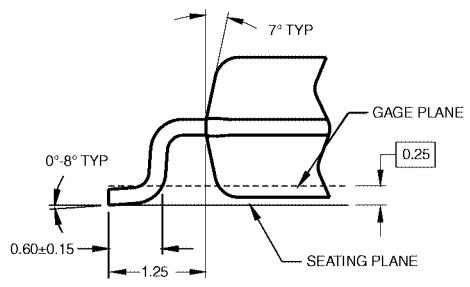
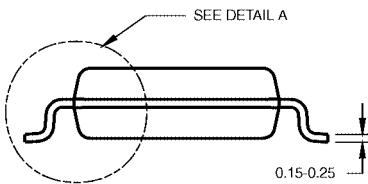
FIGURE 2. Simultaneous Switching Test Circuit

**Physical Dimensions** inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body  
Package Number M14A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS



## NOTES:

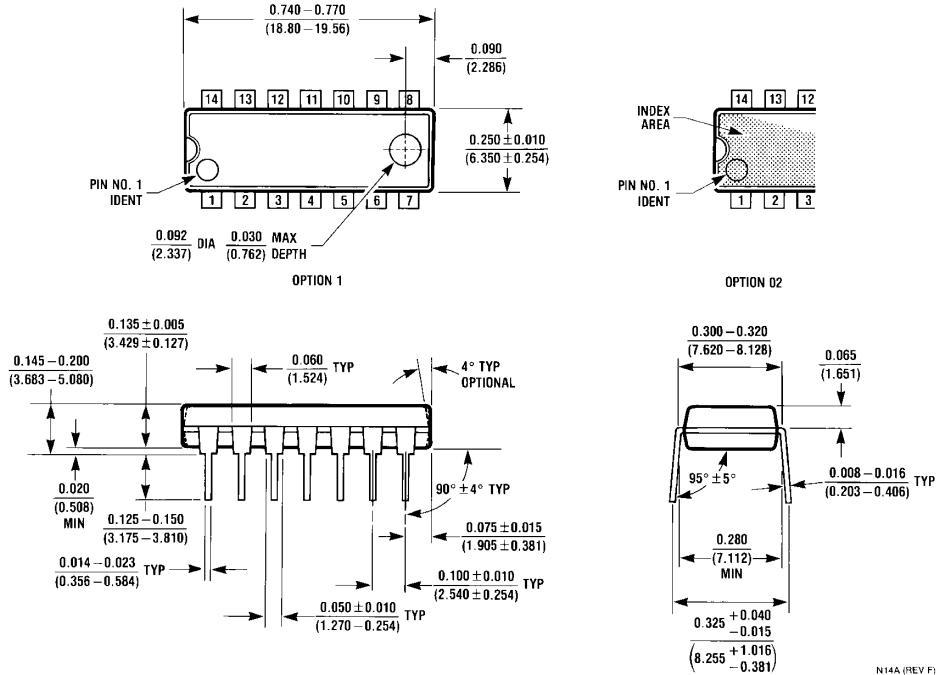
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**  
**Package Number M14D**

### Physical Dimensions

inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N14A

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