NEC

MOS FIELD EFFECT POWER TRANSISTOR
2SK2131

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2131 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance.
  - $R_{DS(on)} \leqq 0.12\ \Omega$ (V_{GS} = −10 V, I_D = 8 A)
  - $R_{DS(on)} \leqq 0.20\ \Omega$ (V_{GS} = −4 V, I_D = 8 A)
- Low C_{iss} C_{iss} = 1 600 pF TYP.
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	150	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±15	A
Drain Current (pulse)	$I_{D(pulse)}$*	±60	A
Total Power Dissipation (T_c = 25 °C)	P_{T1}	35	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

PACKAGE DIMENSIONS
in millimeters

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ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.09	0.12	Ω	V_{GS} = 10 V, I_D = 8 A
Drain to Source On-state Resistance	$R_{DS(on)}$		0.12	0.20	Ω	V_{GS} = 4.0 V, I_D = 8 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	10			S	V_{DS} = 10 V, I_D = 8 A
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 150 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Input Capacitance	C_{iss}		1600		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		360		pF	
Reverse Transfer Capacitance	C_{rss}		160		pF	
Turn-On Delay Time	$t_{d(on)}$		20		ns	$V_{GS(on)}$ = 10 V V_{DD} = 100 V I_D = 8 A, R_G = 10 Ω R_L = 12.5 Ω
Rise Time	t_r		50		ns	
Turn-Off Delay Time	$t_{d(off)}$		200		ns	
Fall Time	t_f		110		ns	
Total Gate Charge	Q_G		60		nC	V_{GS} = 10 V I_D = 15 A V_{DD} = 120 V
Gate to Source Charge	Q_{GS}		4		nC	
Gate to Drain Charge	Q_{GD}		20		nC	
Diode Forward Voltage	V_{SD}		1.0		V	I_F = 15 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		170		ns	I_F = 15 A di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		500		nC	

Test Circuit 1 : Switching Time

Test Circuit 2 : Gate Charge

TYPICAL CHARACTERISTICS (T_a = 25 °C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

FORWARD BIAS SAFE OPERATING AREA

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

TRANSFER CHARACTERISTICS

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURENT

GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

SWITCHING CHARACTERISTICS

DYNAMIC INPUT CHARACTERISTICS

REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT

Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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