

TPS65320EVM

The Texas Instruments TPS65320EVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS65320-Q1 device, a switch-mode DC-DC step-down converter with an integrated low-dropout voltage regulator (LDO). This document describes how to setup and configure the EVM for operation. The document also includes the board layout, schematic, and bill of materials (BOM) for the EVM.

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1 Introduction

The TPS65320EVM is a fully assembled PCB design for evaluation the TPS65320-Q1 device (revision C, TPS65320BQPWPRQ1) which contains a DC-DC step-down converter and a low-dropout voltage regulator.

NOTE: This document is the user's guide for revision C of the TPS65320EVM. The user's guides for revision B (TPS65320QPWPRQ1) and revision C (TPS65320BQPWPRQ1) has some minor differences. For access to the revision B user's guide, review the following forum to find the user's guide for revision B or request the PDF:
<https://e2e.ti.com/support/applications/automotive>.

This section provides a more detailed description of the Schematic, BOM, and Layout.

[illegible]

Figure 1. TPS65320EVM Schematic

Table 1. TPS65320EVM Bill of Materials

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Table 1. TPS65320EVM Bill of Materials (continued)

Designator	Quantity	Description	Footprint	PartNumber	Manufacturer
C6, C7	2	Capacitor, ceramic, 47 μ F, 25 V, $\pm$ 20%, X7S, 6x5x5mm	CKG57N	CKG57NX7S1E476M500JH	TDK
C8	1	Capacitor, ceramic, 10 μ F, 16 V, $\pm$ 10%, X5R, 0805	0805_HV	EMK212BJ106KG-T	Taiyo Yuden
C10	1	Capacitor, ceramic, 4700 pF, 50 V, $\pm$ 5%, X7R, 0603	0603	C0603C472J5RACTU	Kemet
C11	1	Capacitor, ceramic, 100 pF, 50 V, $\pm$ 5%, C0G/NP0, 0603	0603	C0603C101J5GAC	Kemet
C12	1	Capacitor, ceramic, 2200 pF, 100 V, $\pm$ 5%, X7R, 0603	0603	06031C222JAT2A	AVX
C13	1	Capacitor, ceramic, 10 pF, 50 V, $\pm$ 5%, C0G/NP0, 0603	0603	C0603C100J5GACTU	Kemet
D1, D2	2	Diode, Schottky, 40 V, 4 A, SMC	SMC	SL44-E3/57T	Vishay-Semiconductor
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	Fiducial10-20	N/A	N/A
H9, H10, H11, H12	4	Bump, Hemisphere, 0.44 $\times$ 0.20, clear	Bump_SJ5003Transparent	SJ-5303 (CLEAR)	3M
J1, J2	2	Header, 2.54 mm, 3 $\times$ 1, gold, TH	Sullins_Gxx03SAAN	GBC03SAAN	Sullins Connector Solutions
J3, J6	2	Header, 2.54 mm, 2 $\times$ 1, gold, TH	WURTH_61300211121	61300211121	Würth Elektronik eiSos
J4	1	Header, 100 mil, 4 $\times$ 2, gold, SMT	Molex_0015910080	0015910080	Molex
L1	1	Inductor, Shielded, Ferrite, 10 μ H, 5.8 A, 0.019 Ω , SMD	B82477P4	B82477P4103M000	TDK
R1, R4	2	Resistor, 49.9 Ω , 1%, 0.1 W, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R2	1	Resistor, 316 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603316KFKEA	Vishay-Dale
R3, R6	2	Resistor, 100 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R5	1	Resistor, 523 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603523KFKEA	Vishay-Dale
R7	1	Resistor, 20 k Ω , 1%, 0.1 W, 0603	0603	CRCW060320K0FKEA	Vishay-Dale
R8	1	Resistor, 3.9 k Ω , 1%, 0.1 W, 0603	0603	CRCW06033K90FKEA	Vishay-Dale
R9	1	Resistor, 1.2 M Ω , 1%, 0.1 W, 0603	0603	CRCW06031M20FKEA	Vishay-Dale
R10	1	Resistor, 300 k Ω , 1%, 0.1 W, 0603	0603	CRCW0603300KFKEA	Vishay-Dale
R11	1	Resistor, 49.9 k Ω , 1%, 0.1 W, 0603	0603	CRCW060349K9FKEA	Vishay-Dale
SH-BUCK, SH-J6, SH-J8, SH-LDO, SH-VIN	5	Shunt, 2 mm, gold plated, black	2SN-BK-G	2SN-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	16	Test point, miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1	40-V step-down converter with Eco-mode™ and LDO regulator, PWP0014E	PWP0014E_N	TPS65320BQPWPRQ1	Texas Instruments

2.3 Layout and Component Placement

Figure 2 shows the top and Figure 3 shows the bottom component placement for the EVM. Two additional solder pads are added to Buck_Out, between C6 and C7. Those pads allow the user to change the output capacitor configuration from the original setup with two ceramic capacitors (C6 and C7) to two electrolytic capacitors (C5 and solder pads). Also C14 is used if additional capacitance is needed at VIN_LDO.

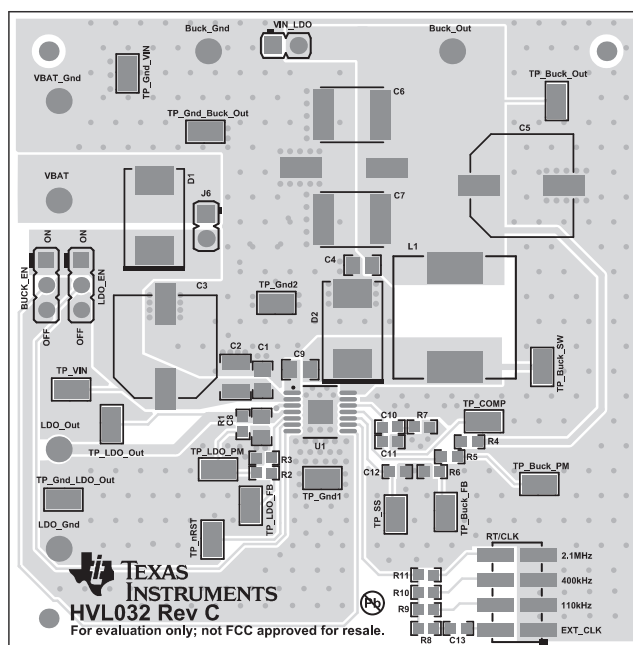


Figure 2. Component Placement, Top Overview

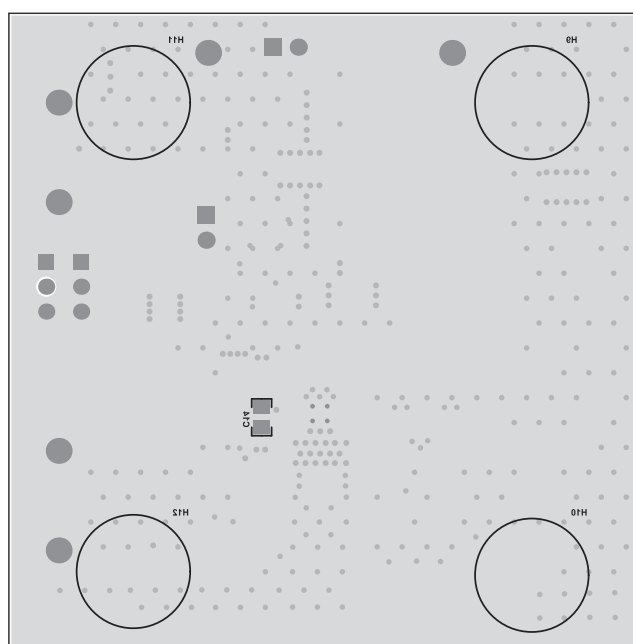


Figure 3. Component Placement, Bottom Overview

Figure 4 and Figure 5 show the top and bottom layout of the EVM. Although the TPS65320-Q1 device is a highly efficient converter a good connection between the heat sink and ground plane is important. Therefore ensuring that the thermal pad has a good connection to the copper landing is important. To improve the thermal performance of the board the thermal pad in this case is connected to ground with multiple vias to the bottom ground plane.

NOTE: The feedback trace from Buck_out to the feedback of the device is shielded with a ground plane which minimizes noise on the feedback node.

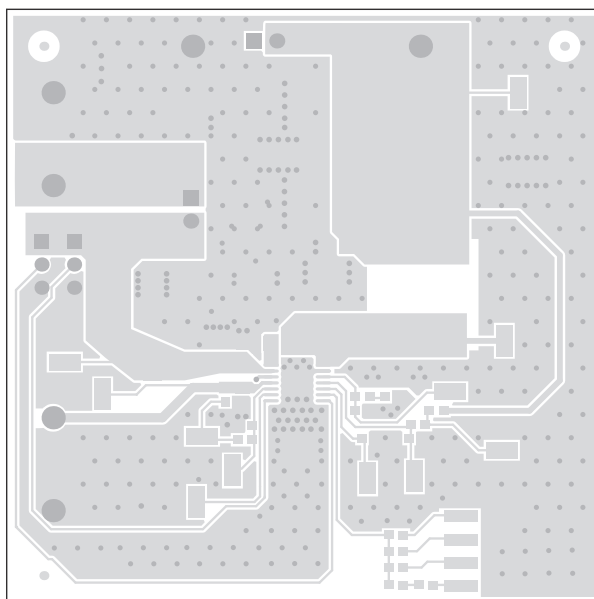


Figure 4. Top Layout

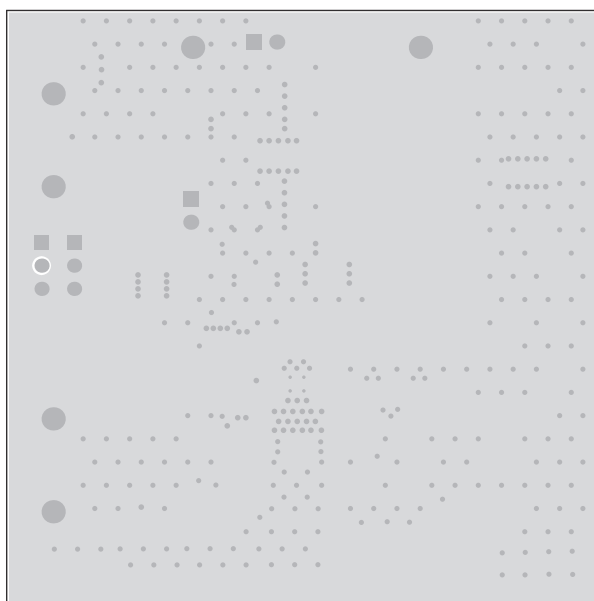


Figure 5. Bottom Layout

3 Setup and Operation

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. An example of the EVM operation is also included.

3.1 Input and Output Connectors

The EVM has three pairs of connectors: 1 input and 2 outputs. [Table 2](#) lists the connectors along with a function description. The description also includes the electrical specifications.

Table 2. Terminal Description

Terminal	Direction	Description
VBAT and VBAT_GND	Input	This terminal is the supply voltage for the device, the device and the design is capable of handling a input voltage between 4 to 40 V.
BUCK_Out and BUCK_Out_GND	Output	Buck is the output voltage of the buck regulator and are designed to deliver 5 V and capable to deliver a maximum output current of 3.2 A. This output is also the supply for the LDO.
LDO_Out and LDO_Out_GND	Output	LDO is the output voltage of the LDO and are able to deliver 0.28 A. In this design the output voltage set to 3.3 V.

3.2 Jumper Settings and Configuration

J8 = RT/CLK—This jumper is used to select the switching frequency for the switch-mode regulator. The jumper places a pulldown resistor to set the frequency to approximately 110 kHz, 400 kHz, or 2.1 MHz. If applying an external clock, use the pin closest to the label EXT_CLK.

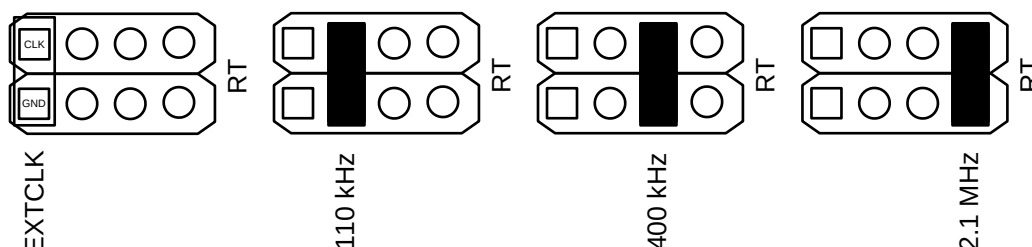


Figure 6. RT Jumper Settings

BUCK_EN and LDO_EN —These jumpers are used to enable or disable the buck converter and the LDO. Setting either jumper high enables respective rail; a low setting or a floating disables respective rail. Manual installation of the jumper may cause ringing, potentially asserting nRST low.

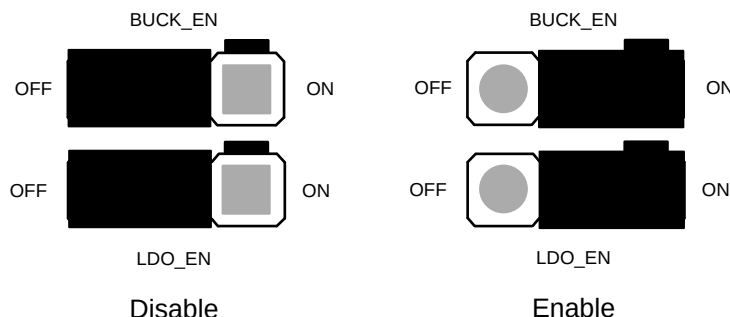


Figure 7. Enable Jumper Setting

VIN_LDO —This jumper should always be installed to supply the LDO for Buck_Out. The jumper can also be used for current measurements from Buck_Out to VIN_LDO.

J6 — This jumper can be used to short the protection diode D1 and avoid the diode voltage drop at the input of the device.

3.3 Test Point Description

The test points and descriptions are as follows:

TP_Vin and TP_Vin_Gnd — Used to measure the voltage on the Vin pin of the device .

TP_Buck_Out and TP_Gnd_Buck_Out — Used to measure the output voltage of the buck regulator .

TP_LDO_Out and TP_Gnd_LDO_Out — Used to measure the output voltage of the LDO.

TP_Buck_SW — Used to measure the switching of the buck converter.

TP_Buck_PM — Allows easy access for gain and phase analysis of the buck regulator .

TP_Buck_FB — Used to measure the feedback of the buck.

TP_LDO_PM — Allows easy access for gain and phase analysis of the LDO.

TP_LDO_FB — Used to measure the feedback of the LDO.

TP_COMP — Compensation network for the feedback of the buck regulator.

TP_SS — Used to measure the voltage drop over the soft start capacitor of the buck regulator.

TP_nRST — Used to measure when the LDO begins to regulate.

TP_Gnd1 and 2 — Additional ground points close to the device

3.4 Basic Operation

The input voltage range for the converter is 4 to 40 V.

For proper operation of the TPS65320EVM, configure BUCK_EN, LDO_EN, and RT properly, using the jumper terminals as follows:

- BUCK_EN — enabled
- LDO_EN — enabled
- RT — 400 kHz

In this configuration, both regulators turn on when power is applied. Disable the regulators using the enable jumpers.

With the BUCK disabled, the LDO supply comes from VIN. Consider the power dissipation at high VIN. TP_VIN_LDO is at GND level in this condition.

To change the switching frequency, power down the device before moving the jumper. If an external clock is applied, remove any jumper installed on RT; however, if the external clock is missing without a jumper installed, the buck does not regulate.

Table 3. Regulator Configuration

Regulator	Output Voltage	Maximum Output Current
BUCK	5 V	3.2 A
LDO	3.3 V	0.28 A

The output capacitors of the BUCK regulator are 25-V types, supporting up to 18 V of the output voltage, V_O . In case of higher output voltage, TI recommends replacing these with capacitors having higher voltage ratings.

Low switching frequencies, high load transients, or limited allowed deviation of V_O , may require larger capacitance values. If needed, use the footprints of the unassembled electrolytic capacitor C5. Low-ESR capacitors also further reduce the coupled noise from the buck to the LDO.

On the EVM, a soft-start capacitor (C12) of 2.2 nF is installed, setting the time to approximately 700 μ s. For other soft-start-times, the capacitor may be replaced.

Revision History

Changes from Original (February 2013) to A Revision	Page
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- | | |
|--|-------------------|
| <ul style="list-style-type: none">Changed TPS65320QPWPRQ1 to TPS65320BQPWPRQ1 and updated the schematic, PCB and BOM for revision C of the board | 1 |
|--|-------------------|

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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