

STF24NM60N, STI24NM60N, STP24NM60N, STW24NM60N

N-channel 600 V, 0.168 Ω typ., 17 A MDmesh™ II Power MOSFETs
in TO-220FP, I²PAK, TO-220 and TO-247 packages

Datasheet — production data

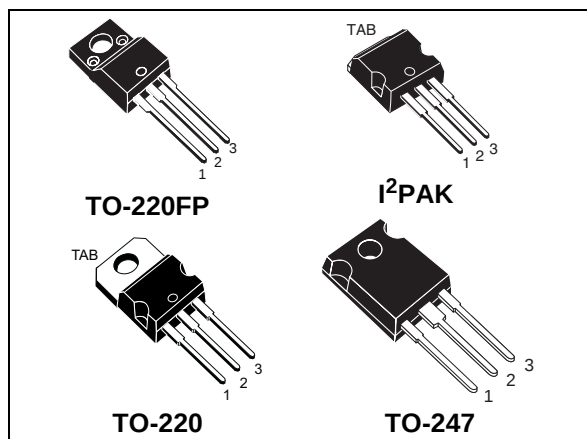
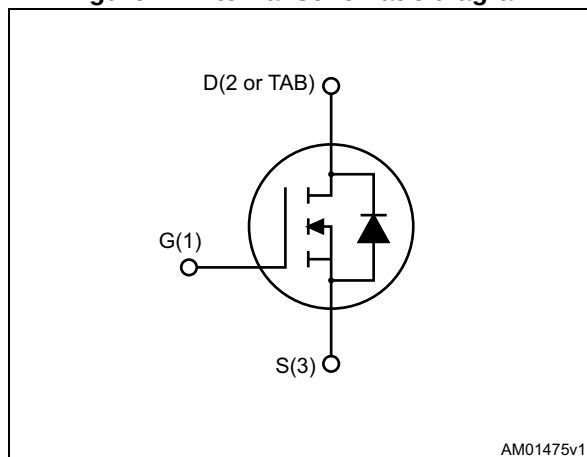


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS} @T _{jmax}	R _{DS(on)} max.	I _D
STF24NM60N	650 V	0.19 Ω	17 A
STI24NM60N			
STP24NM60N			
STW24NM60N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STF24NM60N	24NM60N	TO-220FP	Tube
STI24NM60N		I ² PAK	
STP24NM60N		TO-220	
STW24NM60N		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I ² PAK TO-220 TO-247	TO-220FP	
V _{GS}	Gate- source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	17	17 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	11	11 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	68	68 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	125	30	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500	V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. I_{SD} ≤ 17 A, di/dt ≤ 400 A/μs, peak V_{DS} ≤ V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220FP	I ² PAK	TO-220	TO-247	
R _{thj-case}	Thermal resistance junction-case max.	4.17	1			°C/W
R _{thj-amb}	Thermal resistance junction-ambient max.	62.5			50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not- repetitive (pulse width limited by T _J max)	6	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	300	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1 \text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600 \text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25 \text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$		0.168	0.19	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	1330	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Reverse transfer capacitance		-	3.2	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0$	-	182	-	pF
R_g	Gate input resistance	$f = 1 \text{ MHz}$ open drain	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 17 \text{ A}, V_{GS} = 10 \text{ V}$ (see Figure 19)	-	44	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	24	-	nC

1. $C_{o(eff)}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 18)	-	11.5	-	ns
$t_{r(v)}$	Voltage rise time		-	16.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	73	-	ns
$t_{f(i)}$	Fall time		-	37	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 20)	-	340		ns
Q_{rr}	Reverse recovery charge		-	4.6		μC
I_{RRM}	Reverse recovery current		-	27		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20)	-	404		ns
Q_{rr}	Reverse recovery charge		-	5.7		μC
I_{RRM}	Reverse recovery current		-	28		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

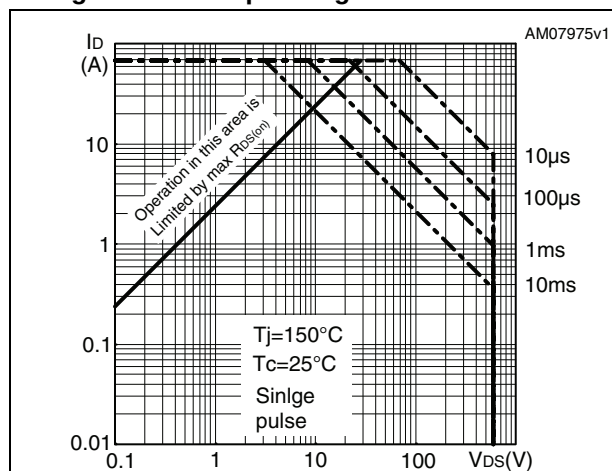


Figure 3. Thermal impedance for TO-220FP

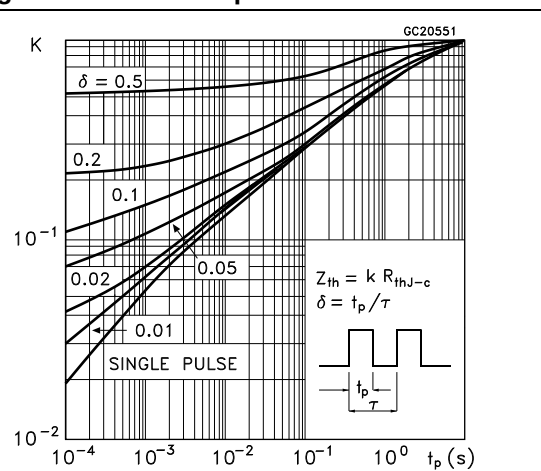
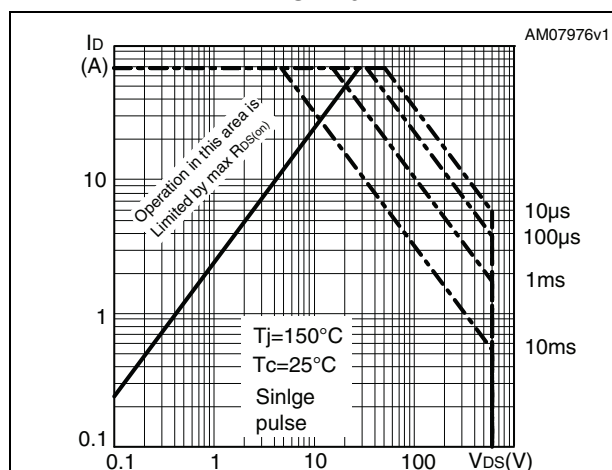
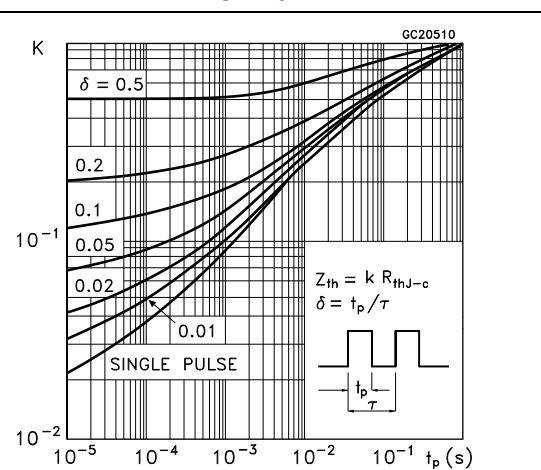
Figure 4. Safe operating area for I²PAK and TO-220Figure 5. Thermal impedance for I²PAK and TO-220

Figure 6. Safe operating area for TO-247

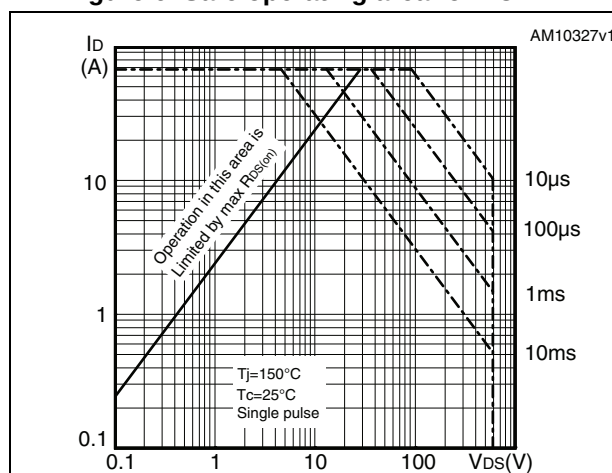


Figure 7. Thermal impedance for TO-247

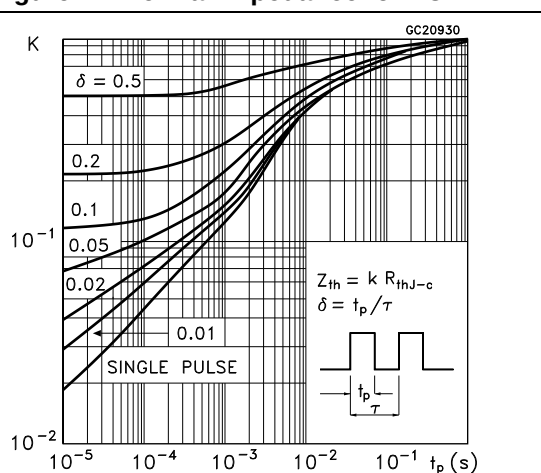


Figure 8. Output characteristics

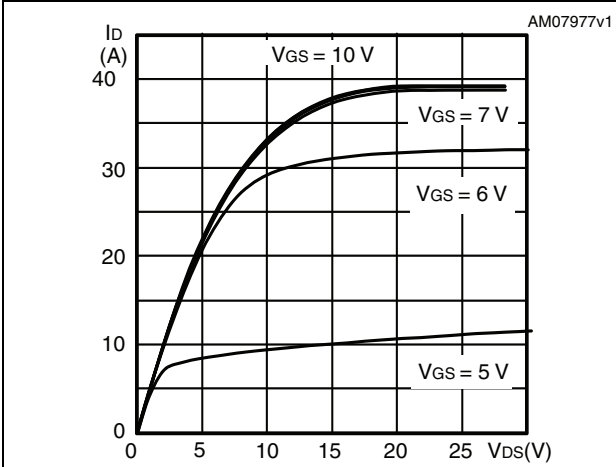


Figure 9. Transfer characteristics

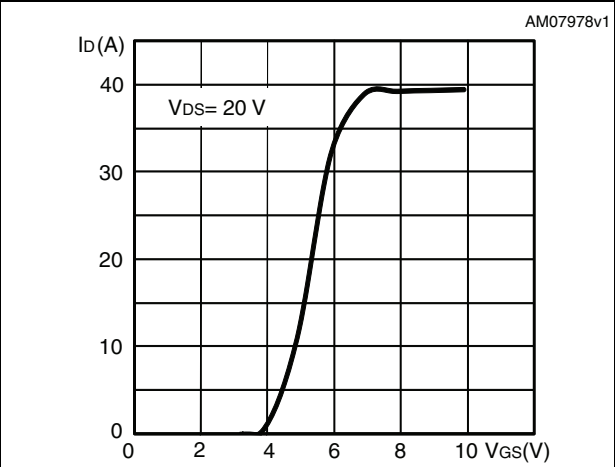


Figure 10. Gate charge vs gate-source voltage

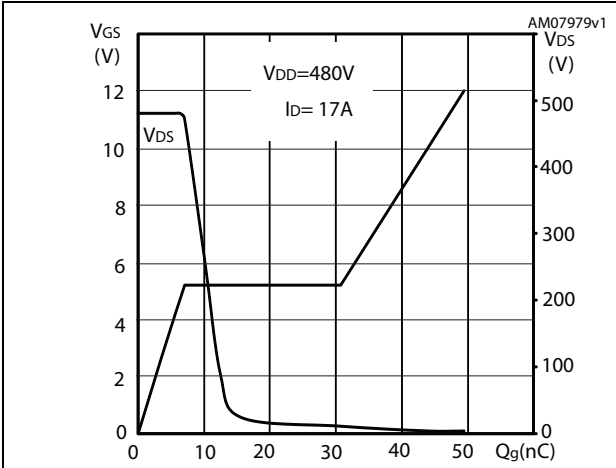


Figure 11. Static drain-source on-resistance

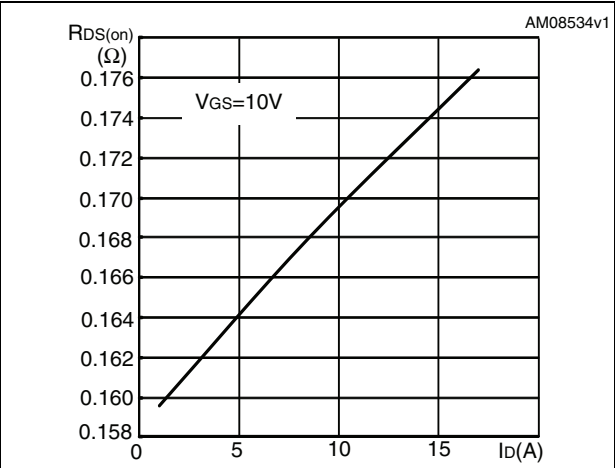


Figure 12. Capacitance variations

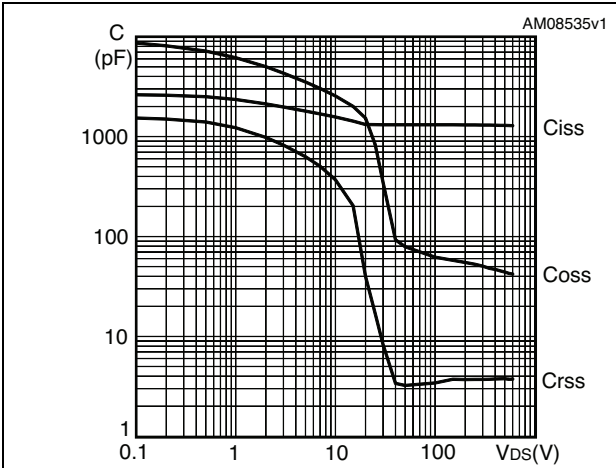


Figure 13. Output capacitance stored energy

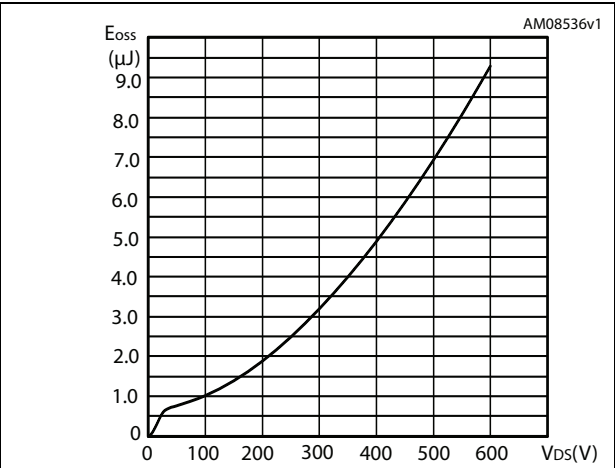


Figure 14. Normalized gate threshold voltage vs temperature

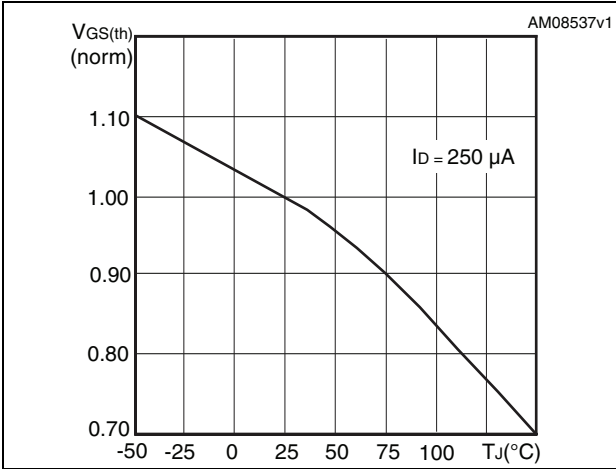


Figure 15. Normalized on-resistance vs temperature

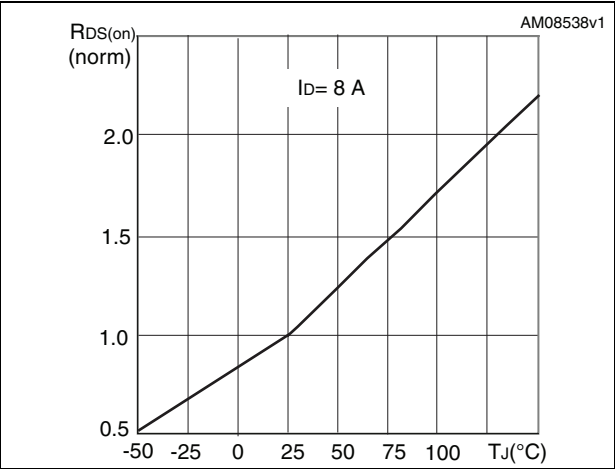


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature

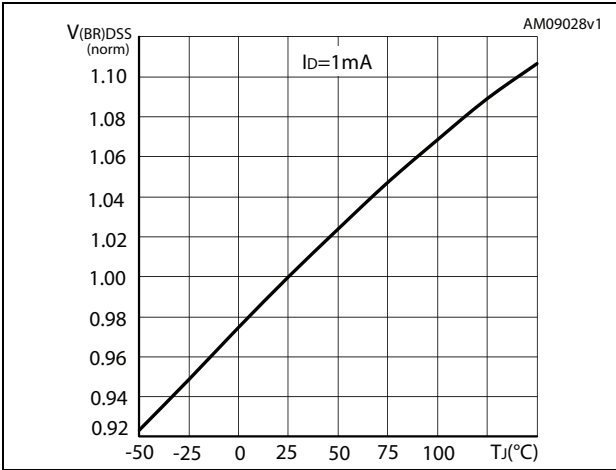
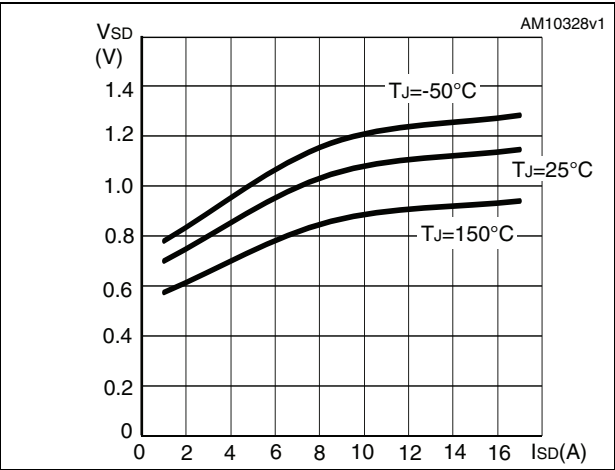


Figure 17. Source-drain diode forward characteristics



3 Test circuits

Figure 18. Switching times test circuit for resistive load

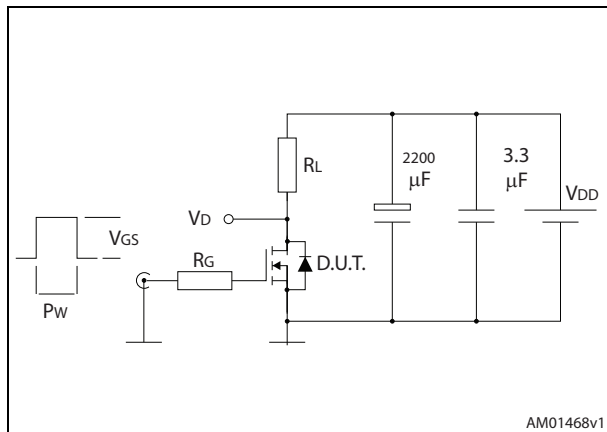


Figure 19. Gate charge test circuit

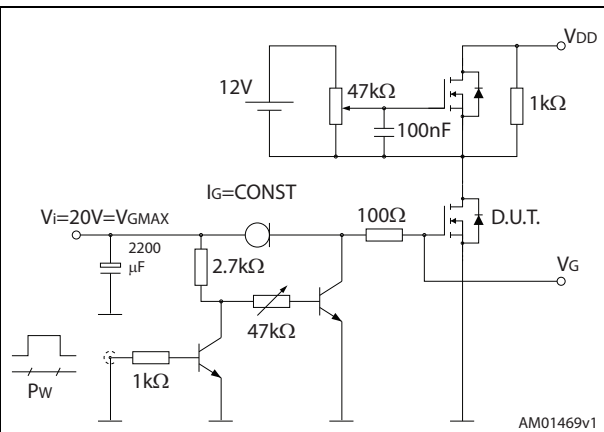


Figure 20. Test circuit for inductive load switching and diode recovery times

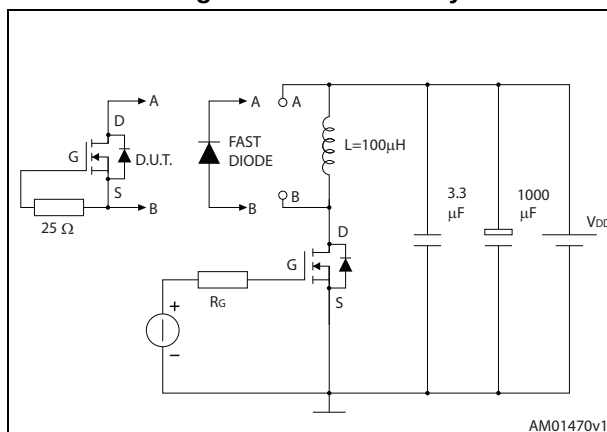


Figure 21. Unclamped inductive load test circuit

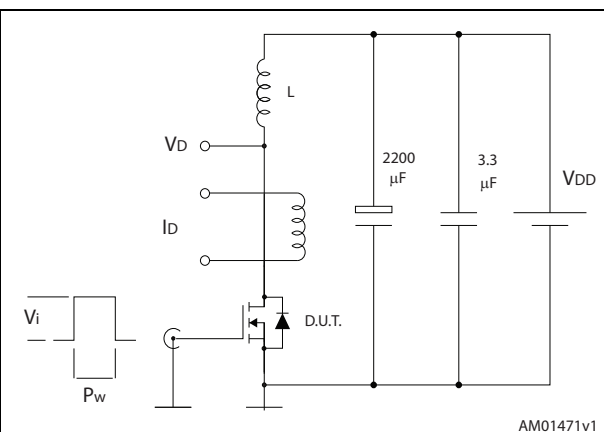


Figure 22. Unclamped inductive waveform

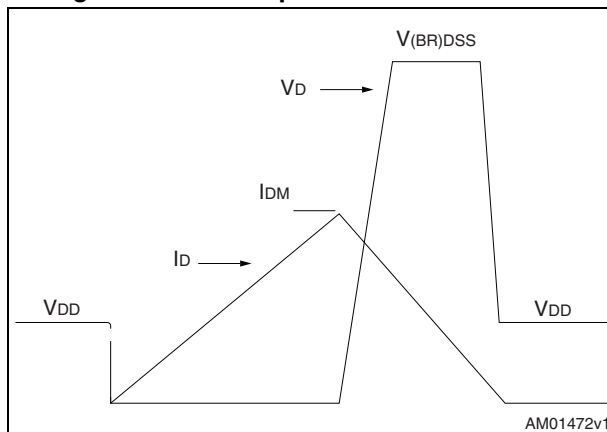
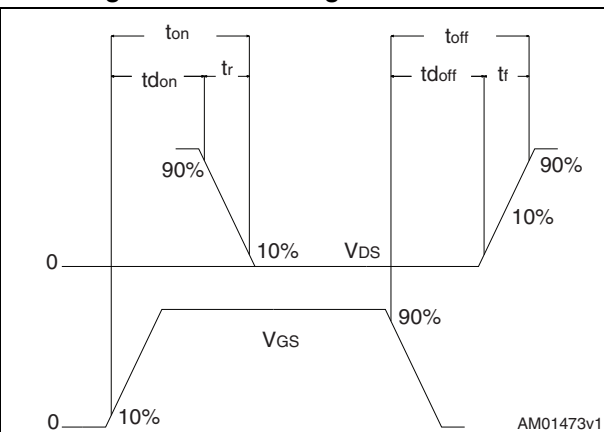


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

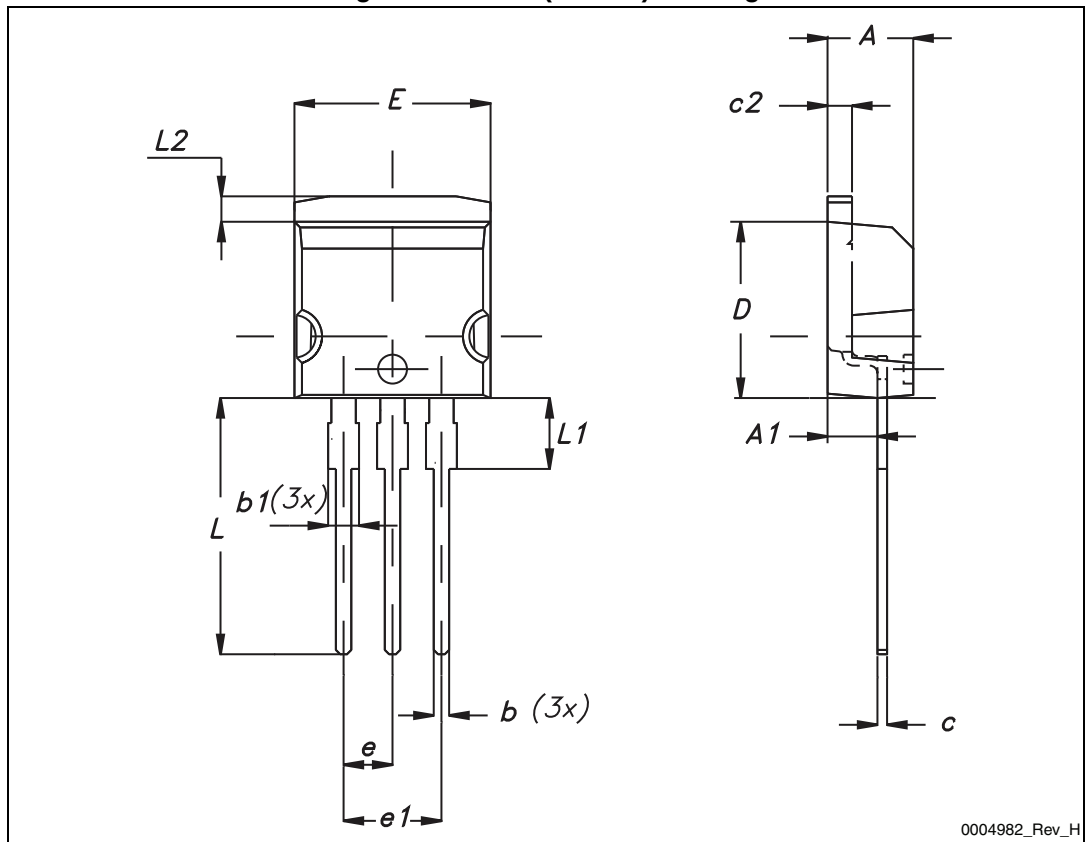
4.2 I²PAK, STI24NM60NFigure 25. I²PAK (TO-262) drawing

Table 10. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

4.3 TO-220, STP24NM60N

Figure 26. TO-220 type A drawing

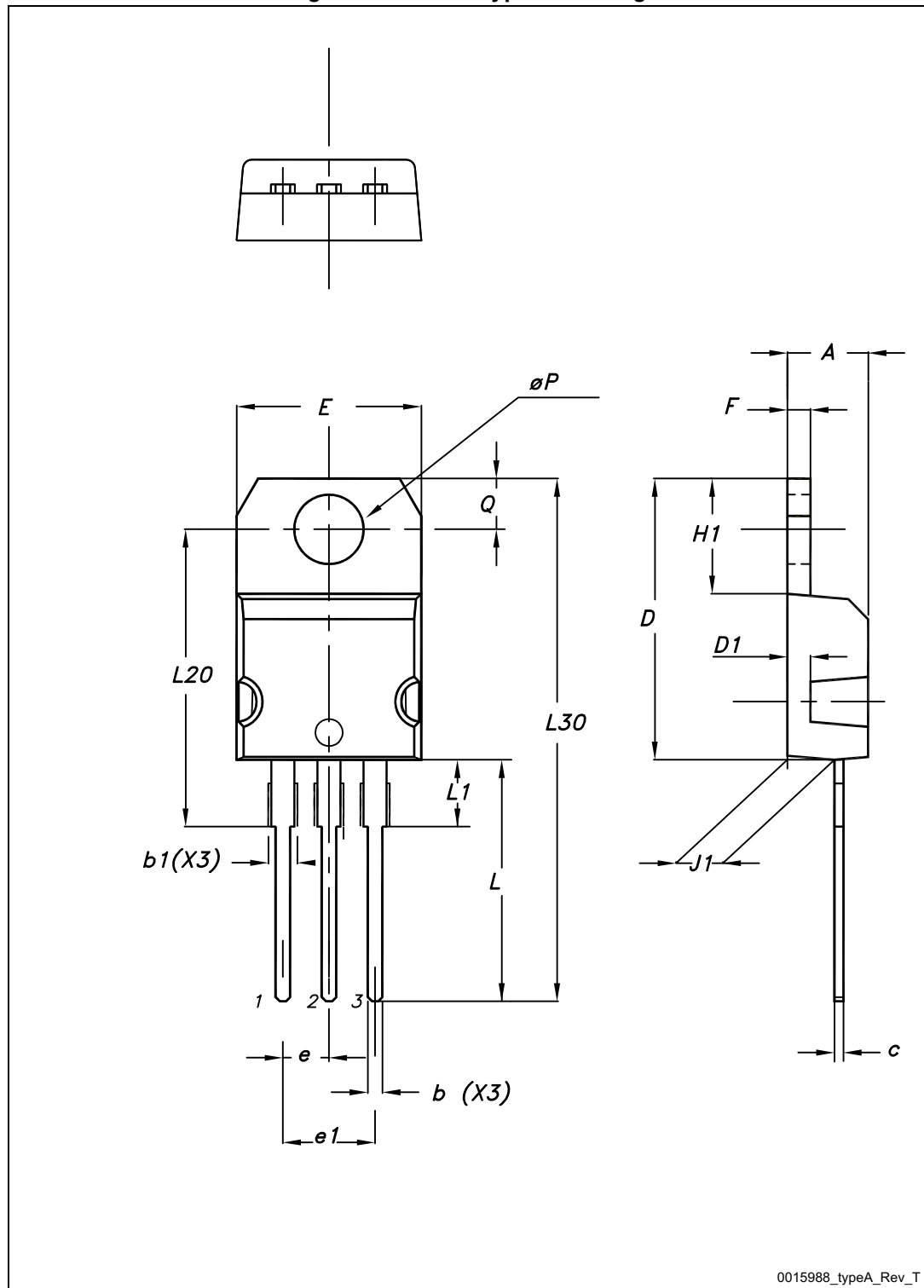


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

4.4 TO-247, STW24NM60N

Figure 27. TO-247 drawing

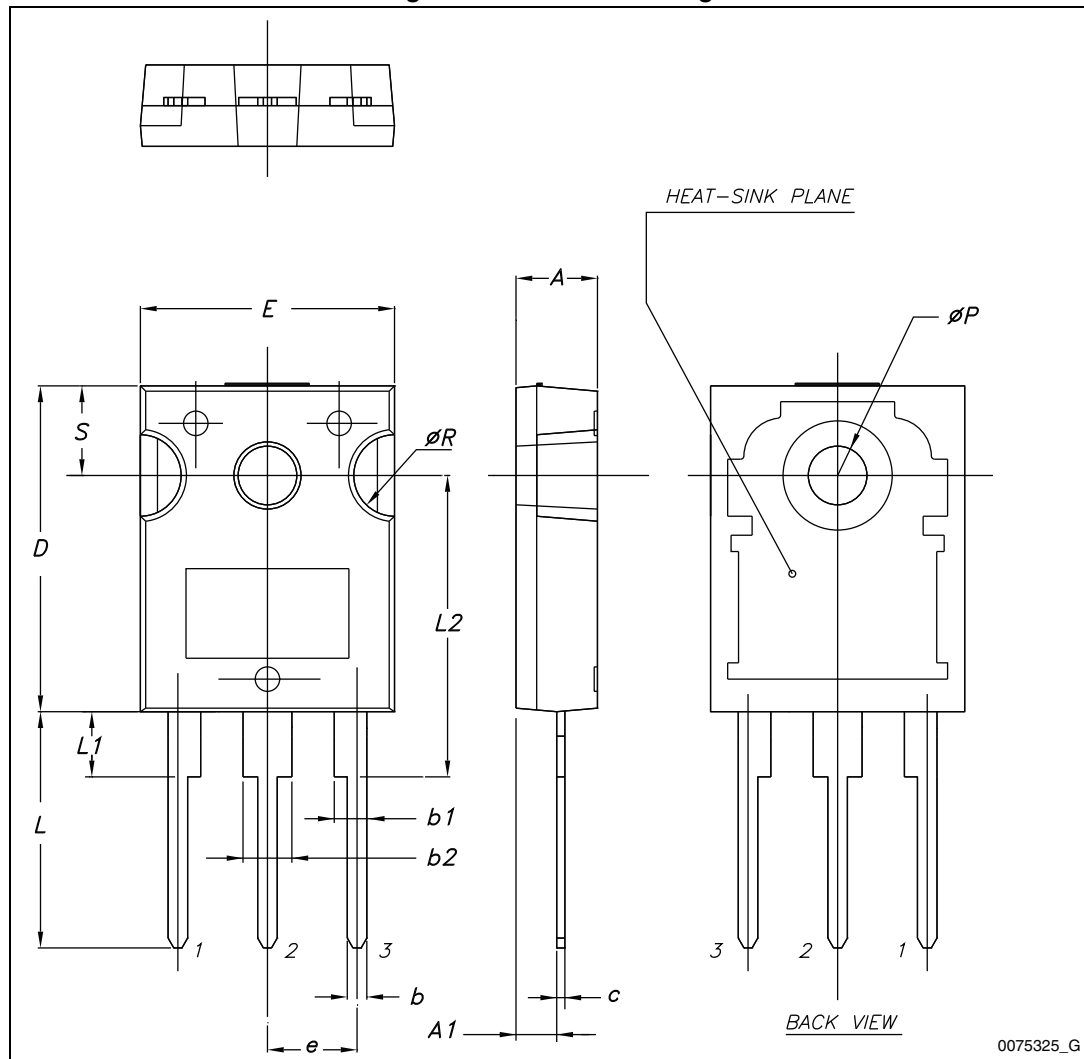


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 13. Document revision history

Date	Revision	Changes
05-Jan-2011	1	First release.
01-Jul-2011	2	Corrected $R_{thj-amb}$ value (see Table 3: Thermal data) Added new package and mechanical data: TO-247.
22-Aug-2011	3	Inserted device in I ² PAK: updated Table 1: Device summary , Table 2: Absolute maximum ratings , Table 3: Thermal data inserted new mechanical data in Section 4: Package mechanical data
24-Jul-2014	4	– Modified: the entire typical values in Table 6 – Modified: Figure 12 – Updated: Section 4: Package mechanical data – Minor text changes

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