Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

CY54/74FCT138T

1-of-8 Decoder

SCCS013 - May 1994 - Revised February 2000

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.0 ns max. (Com'l), FCT-A speed at 5.8 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **ESD > 2000V**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Extended commercial range of –40˚C to +85˚C**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
- **Source current 32 mA (Com'l), 12 mA (Mil)**
- **Dual 1-of-8 decoder with enables**

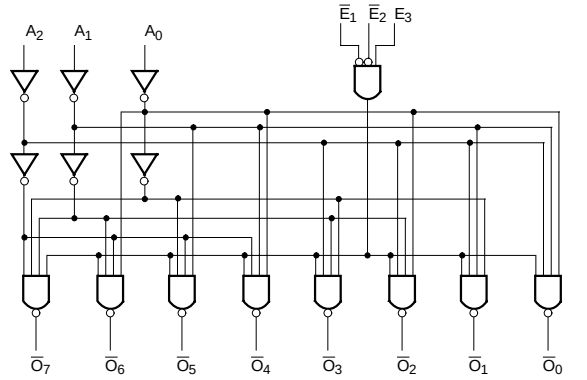
Functional Description

The FCT138T is a 1-of-8 decoder. The FCT138T accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The FCT138T features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3).

All inputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four FCT138T devices and one inverter.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

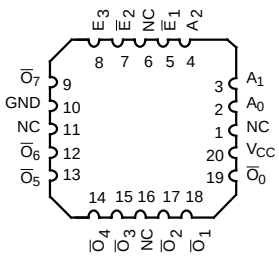
Logic Block Diagram



FCT138T–1

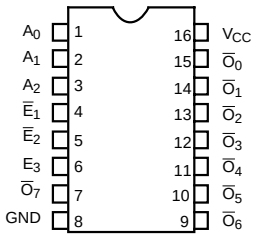
Pin Configurations

LCC
Top View



FCT138T–2

DIP/SOIC/QSOP
Top View



FCT138T–3

Pin Description

Name	Description
A	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
O	Outputs

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Function Table[1]

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage.....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin).....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	All	–40°C to +85°C	5V ± 5%
Military[4]	All	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–32 mA	Com'l	2.0			V
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–15 mA	Com'l	2.4	3.3		V
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, Toggle $\overline{E}_1$, $\overline{E}_2$, or E_3, One Output Toggling, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, Toggle $\overline{E}_1$, $\overline{E}_2$, or E_3, One Output Toggling, V_{IN}=3.4V or V_{IN}=GND	1.0	2.4	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT138T Commercial Min.[11]	FCT138T Commercial Max.	FCT138AT Commercial Min.[11]	FCT138AT Commercial Max.	Unit	Fig. No.[12]
t_{PLH} t_{PHL}	Propagation Delay A to $\overline{O}$	1.5	9.0	1.5	5.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}$	1.5	9.0	1.5	5.9	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}$	1.5	9.0	1.5	5.9	ns	1, 5

Parameter	Description	FCT138CT Military Min.[11]	FCT138CT Military Max.	FCT138CT Commercial Min.[11]	FCT138CT Commercial Max.	Unit	Fig. No.[12]
t_{PLH} t_{PHL}	Propagation Delay A to $\overline{O}$	1.5	6.0	1.5	5.0	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}$	1.5	6.1	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}$	1.5	6.1	1.5	5.0	ns	1, 5

Ordering Information

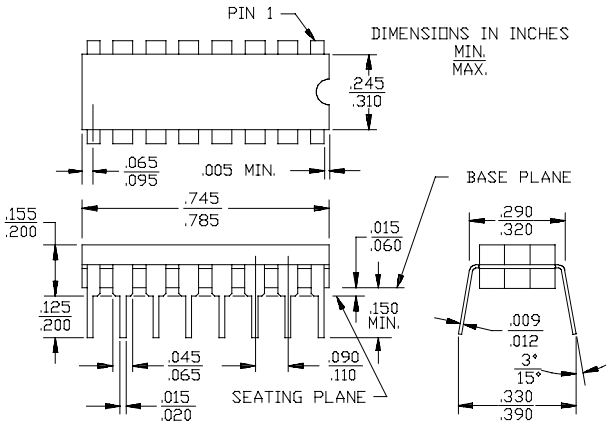
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.0	CY74FCT138CTQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT138CTSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY74FCT138ATQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT138ATSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT138CTLMB	L61	20-Pin Square Leadless Chip Carrier	Military
9.0	CY74FCT138TQCT	S1	16-Lead (150-Mil) QSOP	Commercial

Notes:
11. Minimum limits are specified but not tested on Propagation Delays.
12. See “Parameter Measurement Information” in the General Information Section.

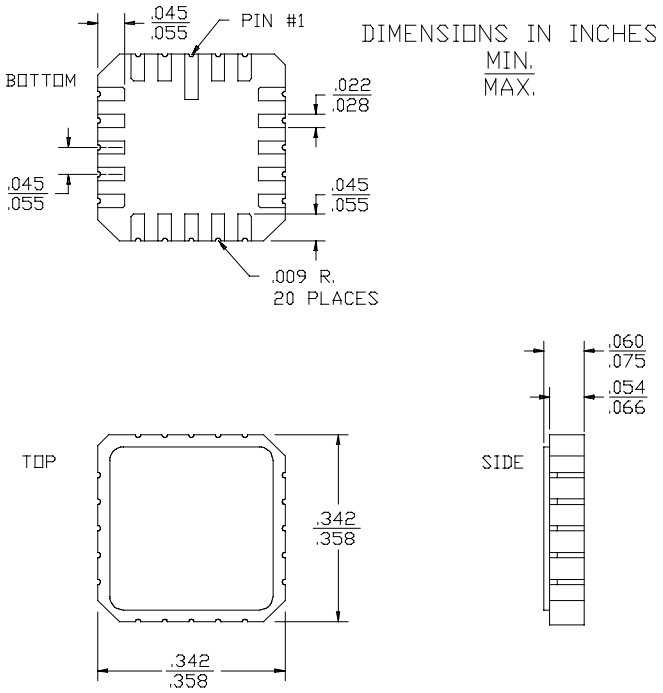
Document #: 38-00297-B

Package Diagrams

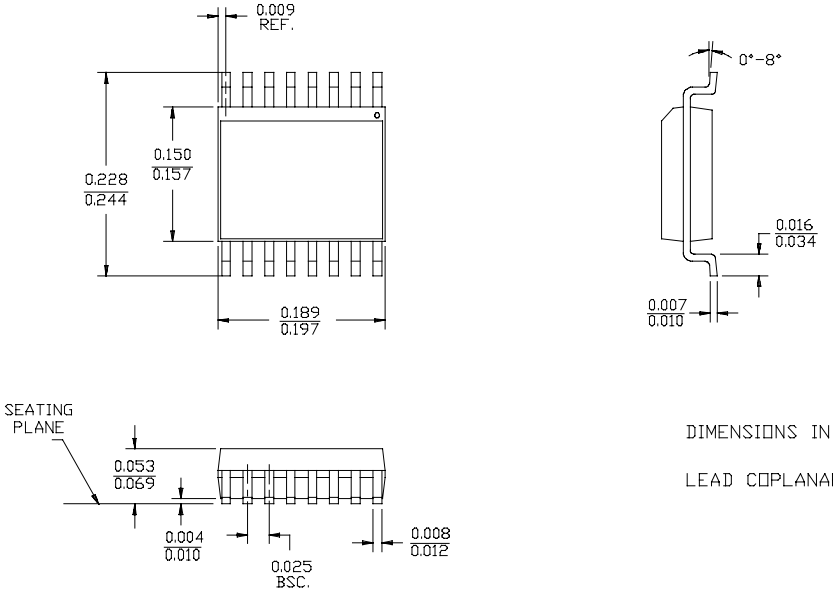
16-Lead (300-Mil) CerDIP D2
MIL-STD-1835 D-2 Config.A



20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A

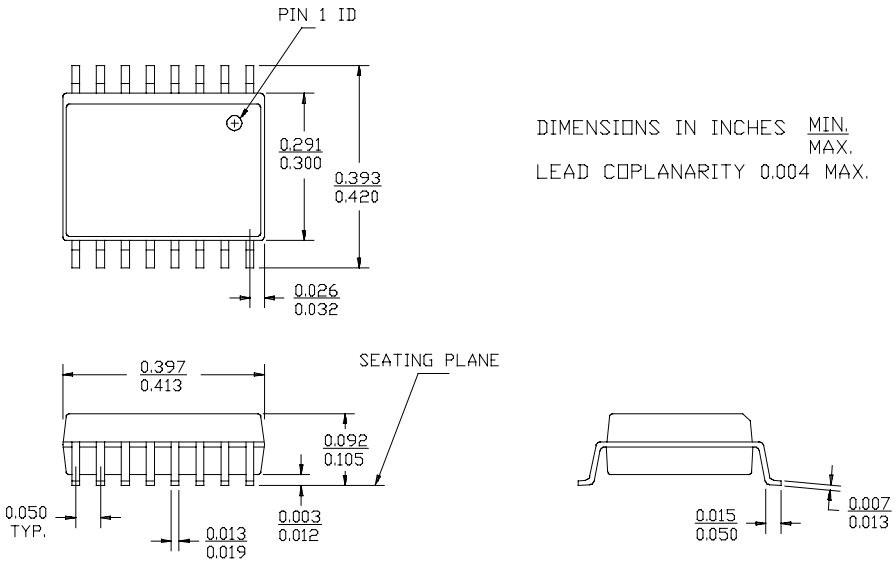


16-Lead Quarter Size Outline Q1



Package Diagrams (continued)

16-Lead Molded SOIC S1



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