

AN1458 (AN6572), AN1458S, AN6571

Dual Operational Amplifiers

■ Outline

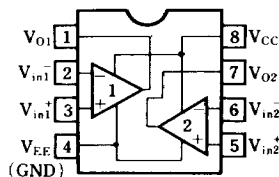
The AN1458 (AN6572), the AN1458S, and the AN6571 are dual operational amplifiers with phase compensation circuits built-in and also an output short-circuit protection built-in, so that they are highly stable and can be used widely in various electronic circuits.

■ Features

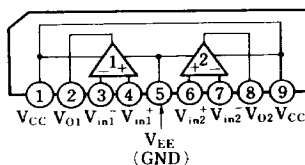
- Built-in phase compensation circuit
- Wide range of common-mode input voltage, no latch-up
- Built-in short-circuit protection
- Low input offset voltage : $V_{I(offset)} = 0.5\text{mV typ.}$
- Low input offset current : $I_{io} = 10\text{nA typ.}$

■ Block Diagrams

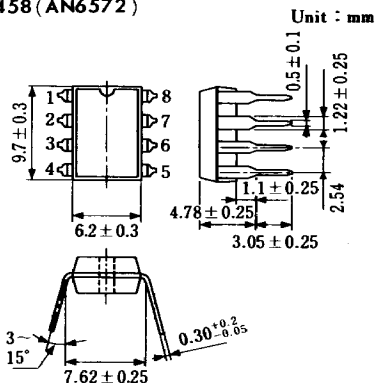
AN1458 (AN6572), AN1458S



AN6571

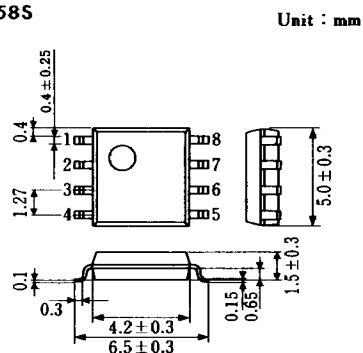


AN1458 (AN6572)



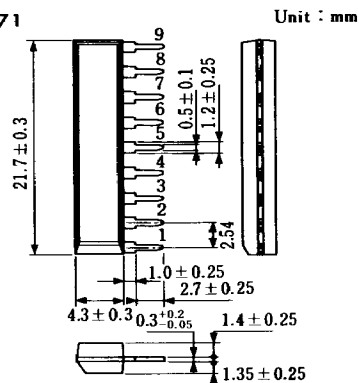
8-Lead DIL Plastic Package

AN1458S



8-Lead PANAFLAT Package (SO-8D)

AN6571



9-Lead SIL Plastic Package (Slim)

■ Pin

<AN1458 (AN6572), AN1458S>

Pin No.	Pin Name
1	Ch. 1 Output
2	Ch. 1 Invert Input
3	Ch. 1 Non Invert Input
4	V_{EE} (GND)
5	Ch. 2 Non Invert Input
6	Ch. 2 Invert Input
7	Ch. 2 Output
8	V_{CC}

<AN6571>

Pin No.	Pin Name
1	V_{CC}
2	Ch. 1 Output
3	Ch. 1 Invert Input
4	Ch. 1 Non Invert Input
5	V_{EE} (GND)
6	Ch. 2 Non Invert Input
7	Ch. 2 Invert Input
8	Ch. 2 Output
9	V_{CC}

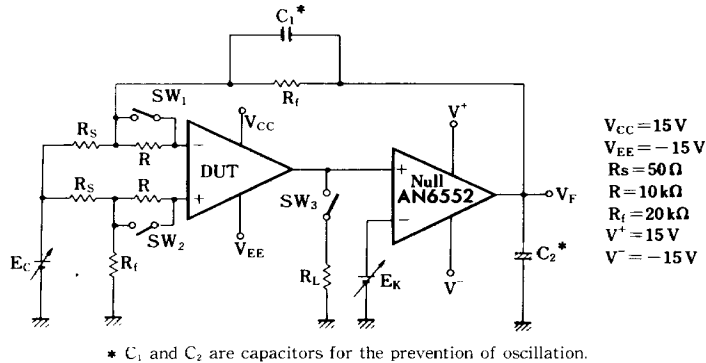
■ Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item		Symbol	Rating	Unit
Voltage	Supply Voltage	V_{CC}	± 18	V
	Differential Input Voltage	V_{ID}	± 30	V
	Common-Mode Input Voltage	V_{ICM}	± 15	V
Power Dissipation	AN1458 (AN6572), AN6571	P_D	500	mW
	AN1458S		360	
Operating Ambient Temperature		T_{opr}	$-20 \sim +75$	$^\circ\text{C}$
Storage Temperature	AN1458 (AN6572), AN6571	T_{stg}	$-55 \sim +150$	$^\circ\text{C}$
	AN1458S		$-55 \sim +125$	

■ Electrical Characteristics ($V_{CC} = 15\text{V}$, $V_{EE} = -15\text{V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Input Offset Voltage	$V_{I(\text{offset})}$	1	$R_S \leq 10\text{k}\Omega$		0.5	4	mV
Input Offset Current	I_{IO}	1			10	100	nA
Input Bias Current	I_{BIAS}	1			50	250	nA
Voltage Gain	G_V	1	$R_L \geq 2\text{k}\Omega$, $V_o = \pm 10\text{V}$	86	106		dB
Maximum Output Voltage	$V_{O(\text{max.})}$	2	$R_L \geq 10\text{k}\Omega$	± 12	± 14		V
		2	$R_L \geq 2\text{k}\Omega$	± 10	± 13		V
Common-Mode Input Voltage Width	V_{CM}	3		± 12	± 13		V
Common-Mode Rejection Ratio	CMR	1	$R_S \leq 10\text{k}\Omega$	70	90		dB
Supply Voltage Rejection Ratio	SVR	1	$R_S \leq 2\text{k}\Omega$		3	150	$\mu\text{V/V}$
Supply Current	I_{CC}	4	$R_L = \infty$			5.6	mA
Power Consumption	P_C	4	$R_L = \infty$			170	mW
Output Short-Circuit Current	$I_{O(\text{short})}$	2			± 20		mA
Slew Rate	SR	5			0.7		V/ μs

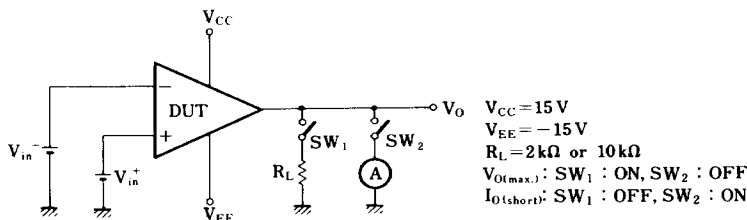
Test Circuit 1 ($V_{I(offset)}$, I_{IO} , I_{Bias} , G_V , CMR , SVR)



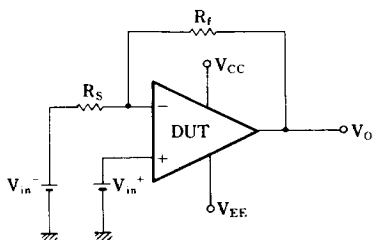
Item	Measurement Conditions
Input Offset Voltage	V_{F1} is measured with the SW_1 , SW_2 and SW_3 set to OFF and $E_C=E_K=OV$. Can be given by $V_{I(offset)} = \frac{V_{F1}}{400} (V)$
Input Offset Current	V_{F2} is measured with the SW_1 and SW_2 set to ON, the SW_3 set to OFF and $E_C=E_K=OV$. Can be given by $I_{IO} = \frac{ V_{F2}-V_{F1} }{4 \times 10^6} (A)$
Input Bias Current	V_{F3} is measured with the SW_3 set to OFF, $E_C=E_K=OV$, the SW_1 set to ON and the SW_2 set to OFF. V_{F4} is measured with the SW_1 and SW_2 reversed. Can be given by $I_{Bias} = \frac{ V_{F3}-V_{F4} }{8 \times 10^6} (A)$
Voltage Gain	V_{F5} is measured with the SW_1 , SW_2 and SW_3 set to ON, $E_C=OV$ and $E_K=10V$. V_{F5} is measured with $E_K=-10V$. Can be given by $G_V = 20 \log \left(\frac{8000}{ V_{F5}-V_{F5}' } \right)$
Common-Mode Rejection Ratio	V_{F6} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K=OV$ and $E_C=5V$. V_{F6}' is measured with $E_C=-5V$. Can be given by $CMR = 20 \log \left(\frac{4000}{ V_{F6}-V_{F6}' } \right)$
Supply Voltage Rejection Ratio I	V_{F7} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K=E_C=OV$ and $V_{CC}=10V$. Can be given by $SVR(+) = \frac{ V_{F7}-V_{F2} }{2 \times 10^3}$
Supply Voltage Rejection Ratio II	V_{F8} is measured with both the SW_1 and SW_2 set to ON, the SW_3 set to OFF, $E_K=E_C=OV$ and $V_{EE}=-10V$. Can be given by $SVR(-) = \frac{ V_{F8}-V_{F2} }{2 \times 10^3}$

Note) When not specified in the above table, $V_{CC}=15V$ and $V_{EE}=-15V$.

Test Circuit 2 ($V_{O(max)}$, $I_{O(short)}$)



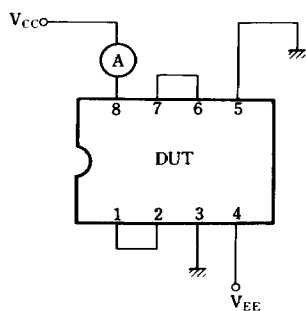
Test Circuit 3 (V_{CM})



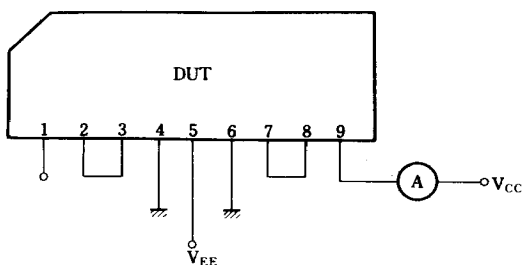
$V_{CC} = 15\text{ V}$
 $V_{EE} = -15\text{ V}$
 $R_S = 200\ \Omega$
 $R_f = 2\text{ k}\Omega$

Note¹⁾ Apply a voltage of $|v_{in+}| > 12\text{ V}$ and check $V_O = V_{in+} + \frac{R_f}{R_S}(V_{in+} - V_{in-})$

Test Circuit 4 (I_{CC} , P_C)

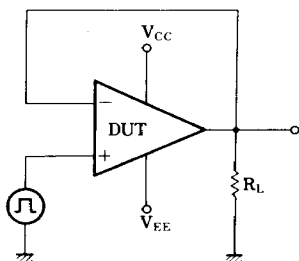


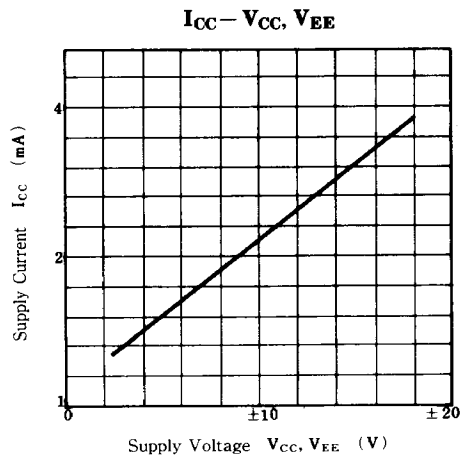
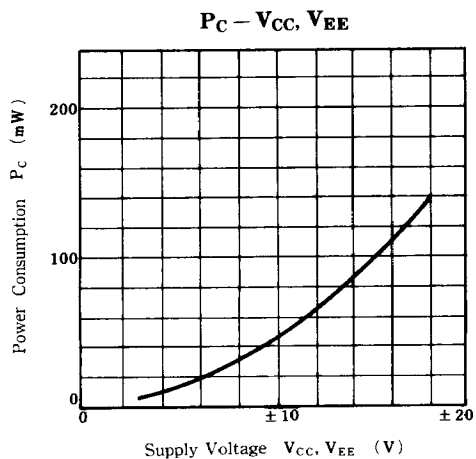
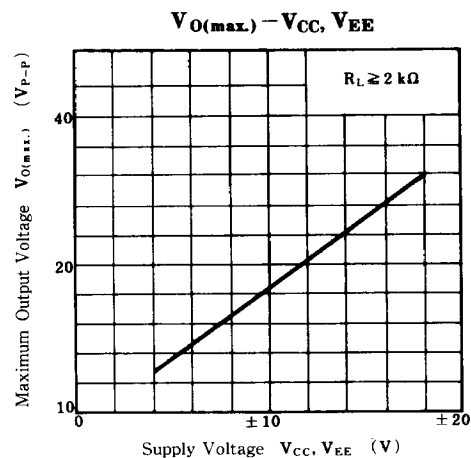
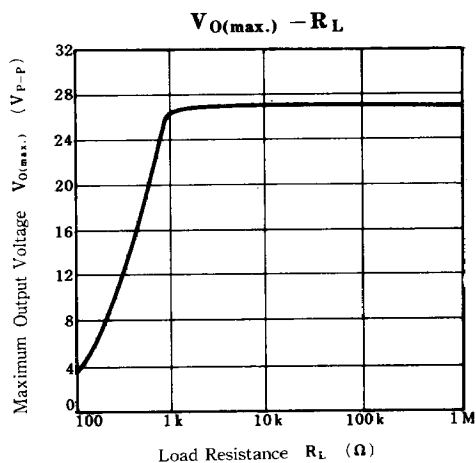
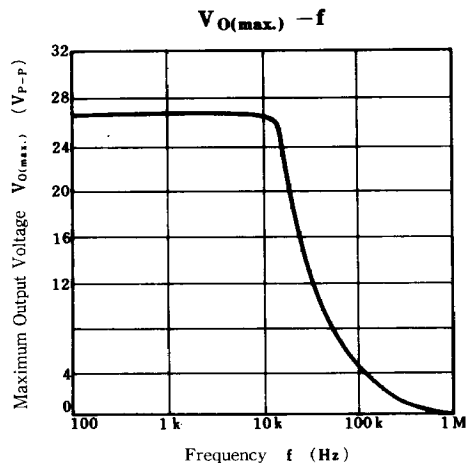
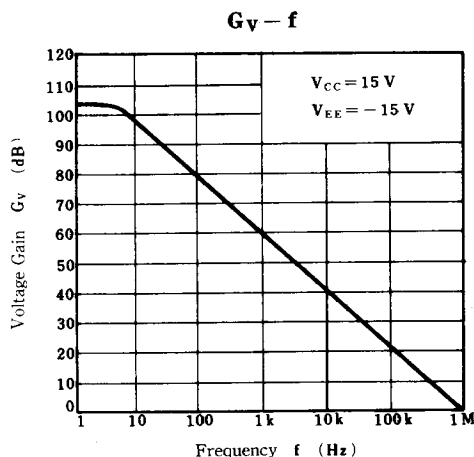
(AN1458 (AN6572)
AN1458S)

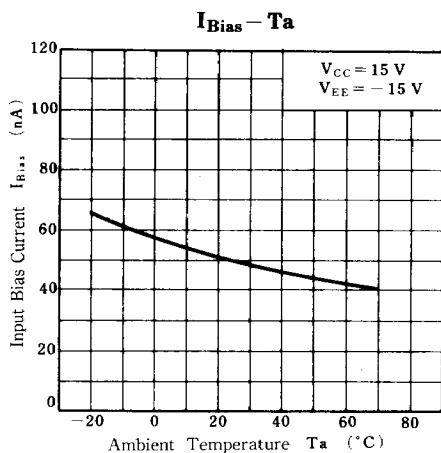
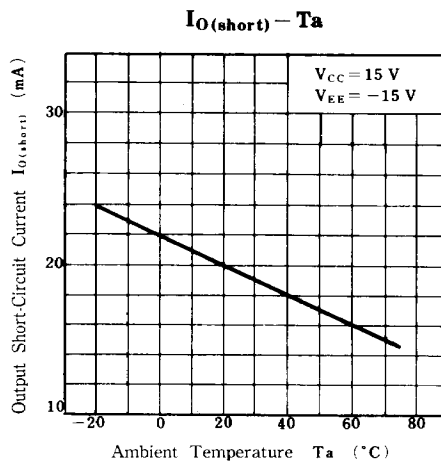
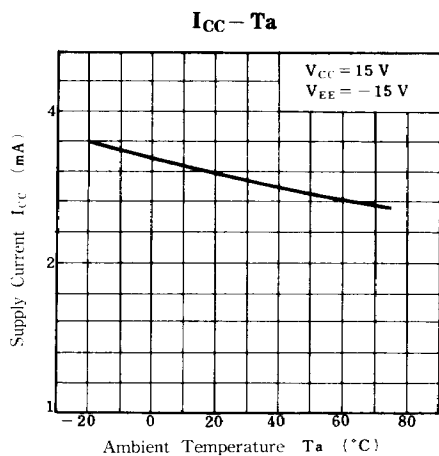


(AN6571)

Test Circuit 5 (SR)







■ Application Circuit

Differential Amplifier Circuit

