

DATA SHEET

74ALVC16836A

20-bit registered driver with
inverted register enable (3-State)

Product specification
Replaces datasheet 74ALVC16836 of 2000 Jan 04
IC24 Data Handbook

2000 Mar 14

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FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines @ 85°C
- Input diodes to accommodate strong drivers

DESCRIPTION

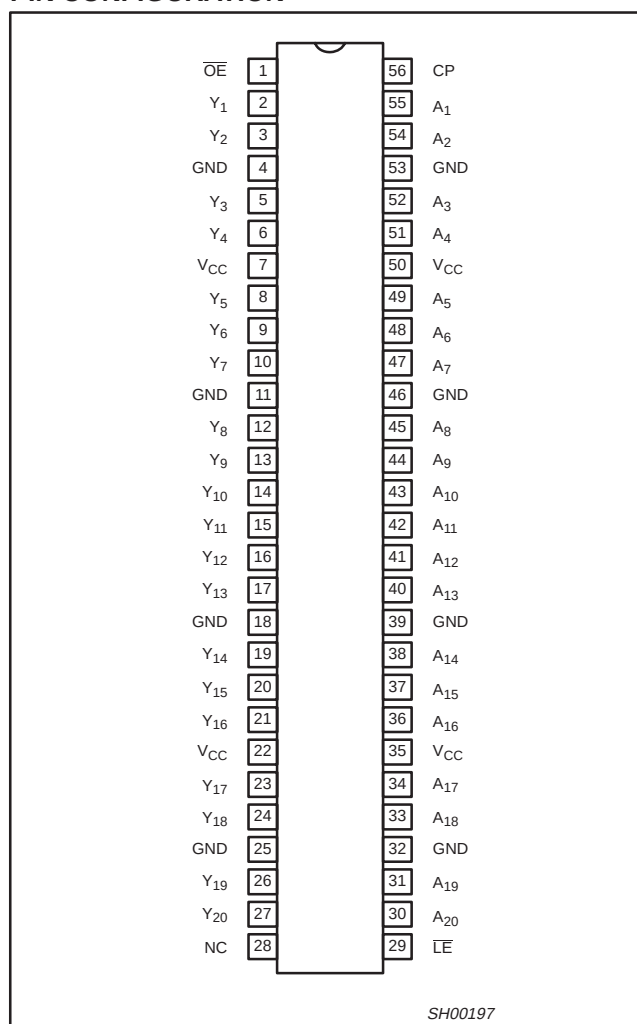
The 74ALVC16836A is a 20-bit universal bus driver. Data flow is controlled by active low output enable ($\overline{OE}$), active low latch enable ($\overline{LE}$) and clock inputs (CP).

When $\overline{LE}$ is LOW, the A to Y data flow is transparent. When $\overline{LE}$ is HIGH and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

When $\overline{OE}$ is LOW the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip-flop.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn; LE to Yn; CP to Yn	$V_{CC} = 3.3$ V, $C_L = 50$ pF		2.3 2.6 2.5	ns
f_{max}	Maximum clock frequency	$V_{CC} = 3.3$ V, $C_L = 50$ pF		350	MHz
C_i	Input capacitance			4.0	pF
$C_{I/O}$	Input/Output capacitance			8.0	pF
C_{PD}	Power dissipation capacitance per buffer	$V_i = \text{GND to } V_{CC}^1$	transparent mode Output enabled Output disabled	13 3	pF
			Clocked mode Output enabled Output disabled	22 15	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

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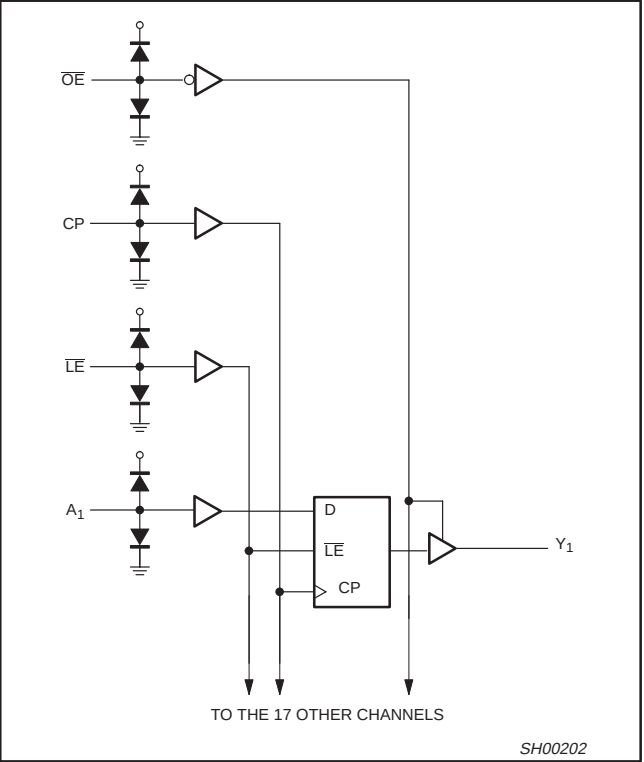
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	−40°C to +85°C	74ALVC16836A DGG	SOT364-1

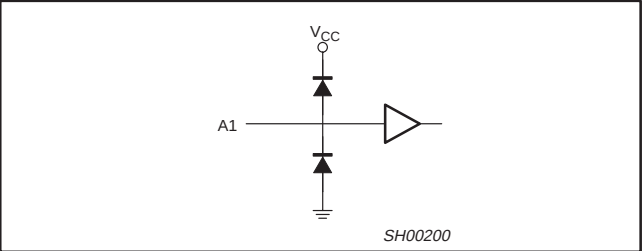
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
28	NC	No connection
2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	Y ₁ to Y ₁₈	Data outputs
4, 11, 18, 25, 32, 39, 46, 53, 56	GND	Ground (0 V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
1	$\overline{OE}$	Output enable input (active LOW)
29	$\overline{LE}$	Latch enable input (active LOW)
56	CP	Clock input
55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	A ₁ to A ₁₈	Data inputs

LOGIC SYMBOL



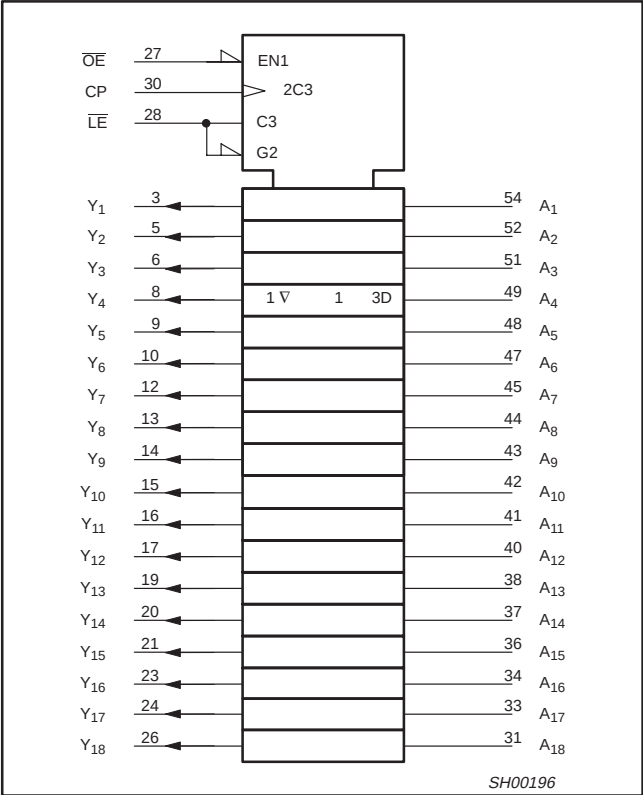
TYPICAL INPUT (DATA OR CONTROL)



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LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS
OE	LE	CP	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y ₀ ¹
L	H	L	X	Y ₀ ²

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH level transition

- NOTES:
- Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
 - Output level before the indicated steady-state input conditions were established.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5 V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3 V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 2.3$ to 3.0 V $V_{CC} = 3.0$ to 3.6 V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For control pins ¹	-0.5 to +4.6	V
		For data inputs ¹	-0.5 to $V_{CC} + 0.5$	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW

NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = −40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 2.3 to 2.7 V	1.7	1.2		V
		V _{CC} = 2.7 to 3.6 V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 2.3 to 2.7 V		1.2	0.7	V
		V _{CC} = 2.7 to 3.6 V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.3 to 3.6 V; V _I = V _{IH} or V _{IL} ; I _O = −100 μA	V _{CC} − 0.2	V _{CC}		V
		V _{CC} = 2.3 V; V _I = V _{IH} or V _{IL} ; I _O = −6 mA	V _{CC} − 0.3	V _{CC} − 0.08		
		V _{CC} = 2.3 V; V _I = V _{IH} or V _{IL} ; I _O = −12 mA	V _{CC} − 0.6	V _{CC} − 0.26		
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL} ; I _O = −12 mA	V _{CC} − 0.5	V _{CC} − 0.14		
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = −12 mA	V _{CC} − 0.6	V _{CC} − 0.09		
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = −24 mA	V _{CC} − 1.0	V _{CC} − 0.28		
V _{OL}	LOW level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100 μA		GND	0.20	V
		V _{CC} = 2.3 V; V _I = V _{IH} or V _{IL} ; I _O = 6 mA		0.07	0.40	V
		V _{CC} = 2.3 V; V _I = V _{IH} or V _{IL} ; I _O = 12 mA		0.15	0.70	V
		V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL} ; I _O = 12 mA		0.14	0.40	
		V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = 24 mA		0.27	0.55	
I _I	Input leakage current	V _{CC} = 2.3 to 3.6 V; V _I = V _{CC} or GND		0.1	5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 2.3 to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	μA
I _{CC}	Quiescent supply current	V _{CC} = 2.3 to 3.6 V; V _I = V _{CC} or GND; I _O = 0		0.2	40	μA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} − 0.6 V; I _O = 0		150	750	μA

NOTES:

1. All typical values are at $T_{amb} = 25^\circ\text{C}$.

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AC CHARACTERISTICS FOR $V_{CC} = 2.3 \text{ V TO } 2.7 \text{ V RANGE}$

GND = 0 V; $t_r = t_f \leq 2.0 \text{ ns}$; $C_L = 30 \text{ pF}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V _{CC} = 2.3 to 2.7 V			
			MIN	TYP ¹	MAX	
t _{PHL} /t _{PLH}	Propagation delay An to Yn	1, 7	1.0	2.4	4.2	ns
	Propagation delay LE to Yn	2, 7	1.3	2.8	4.5	
	Propagation delay CP to Yn	4, 7	1.4	2.8	5.0	
t _{PZH} /t _{PZL}	3-State output enable time OE to Yn	6, 7	1.4	2.2	4.0	ns
t _{PHZ} /t _{PLZ}	3-State output disable time OE to Yn	6, 7	1.4	2.0	4.5	ns
t _W	CP pulse width HIGH or LOW	4, 7	2.0	–	–	ns
	LE pulse width HIGH	2, 7	2.0	–	–	
t _{SU}	Set-up time An to CP	5, 7	1.0	–	–	ns
	Set-up time An to LE	3, 7	1.5	–	–	
t _H	Hold time An to CP	5, 7	0.6	0.2	–	ns
	Hold time An to LE	3, 7	1.4	0.4	–	
f _{max}	Maximum clock pulse frequency	4, 7	150	300	–	MHz

NOTE:

1. All typical values are at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25^\circ\text{C}$.

AC CHARACTERISTICS FOR $V_{CC} = 3.0 \text{ V TO } 3.6 \text{ V RANGE AND } V_{CC} = 2.7 \text{ V}$

GND = 0 V; $t_r = t_f \leq 2.5 \text{ ns}$; $C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			V _{CC} = 3.3 ± 0.3 V			V _{CC} = 2.7 V			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	
t _{PHL} /t _{PLH}	Propagation delay An to Yn	1, 7	1.0	2.3	3.6	1.3	2.7	4.0	ns
	Propagation delay $\overline{LE}$ to Yn	2, 7	1.3	2.6	4.2	1.3	2.8	4.5	
	Propagation delay CP to Yn	4, 7	1.3	2.5	4.2	1.3	2.7	4.5	
t _{PZH} /t _{PZL}	3-State output enable time OE to Yn	6, 7	1.1	2.3	4.4	1.4	3.0	4.5	ns
t _{PHZ} /t _{PLZ}	3-State output disable time OE to Yn	6, 7	1.3	2.8	4.3	1.4	3.1	4.3	ns
t _W	CP pulse width HIGH or LOW	4, 7	2.0	–	–	2.0	–	–	ns
	$\overline{LE}$ pulse width HIGH	2, 7	2.0	–	–	2.0	–	–	
t _{SU}	Set-up time An to CP	5, 7	1.0	–	–	1.0	–	–	ns
	Set-up time An to $\overline{LE}$	3, 7	1.5	–	–	1.5	–	–	
t _h	Hold time An to CP	5, 7	0.9	0.3	–	0.6	0.3	–	ns
	Hold time An to $\overline{LE}$	3, 7	1.4	0.3	–	1.7	0.4	–	
f _{max}	Maximum clock pulse frequency	4, 7	150	300	–	200	350	–	MHz

NOTES:

1. All typical values are measured $T_{amb} = 25^\circ\text{C}$.2. Typical value is measured at $V_{CC} = 3.3 \text{ V}$

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AC WAVEFORMS FOR $V_{CC} = 3.0\text{ V TO } 3.6\text{ V}$ AND $V_{CC} = 2.7\text{ V RANGE}$

$$V_M = 1.5 V_{CC}$$

$$V_X = V_{OL} + 0.3\text{ V}$$

$$V_Y = V_{OH} - 0.3\text{ V}$$

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$$V_I = 2.7\text{ V}$$

AC WAVEFORMS FOR $V_{CC} = 2.3\text{ V TO } 2.7\text{ V}$ AND $V_{CC} < 2.3\text{ V RANGE}$

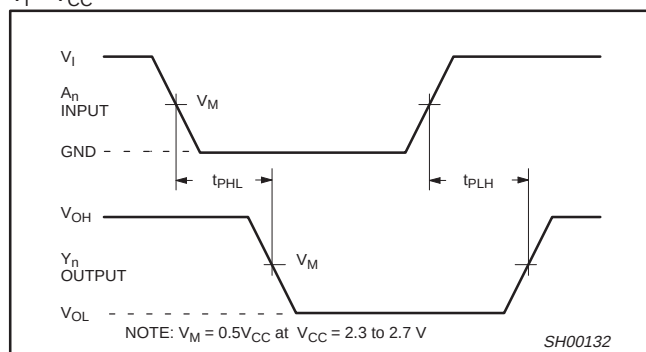
$$V_M = 0.5\text{ V}$$

$$V_X = V_{OL} + 0.15\text{ V}$$

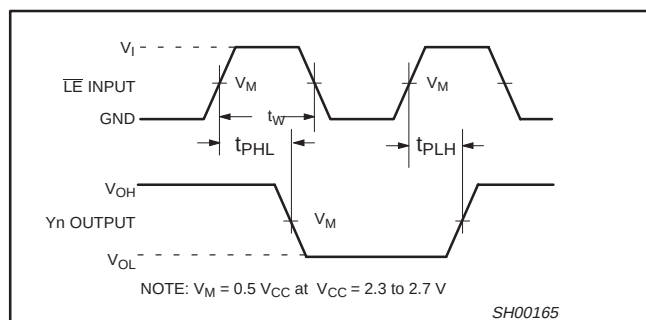
$$V_Y = V_{OH} - 0.15\text{ V}$$

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

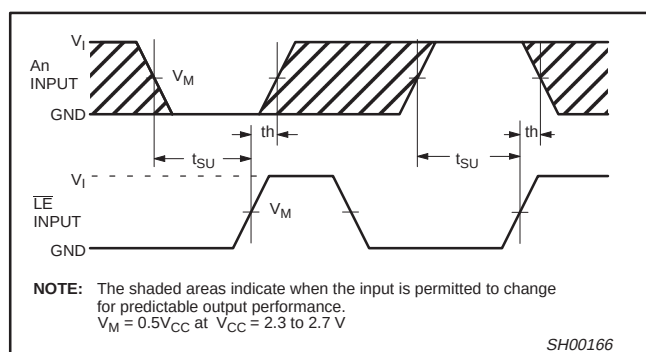
$$V_I = V_{CC}$$



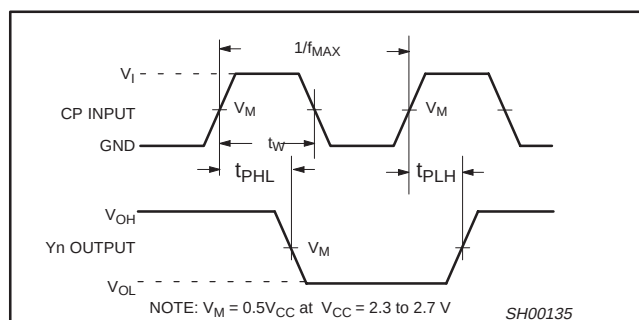
Waveform 1. Input (An) to output (Yn) propagation delay



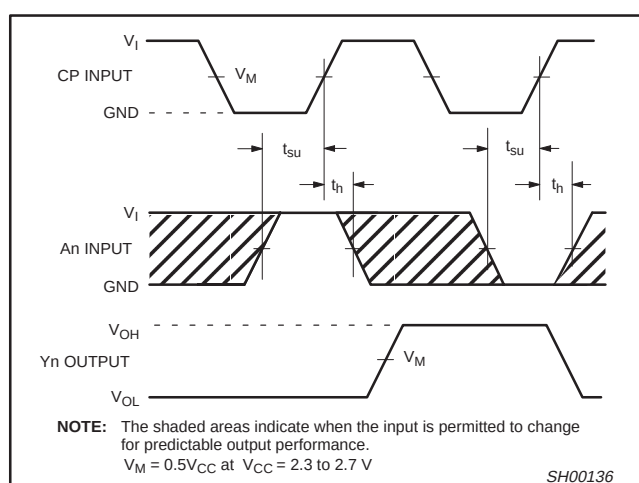
Waveform 2. Latch enable input ($\overline{LE}$) pulse width, the latch enable input to output (Yn) propagation delays.



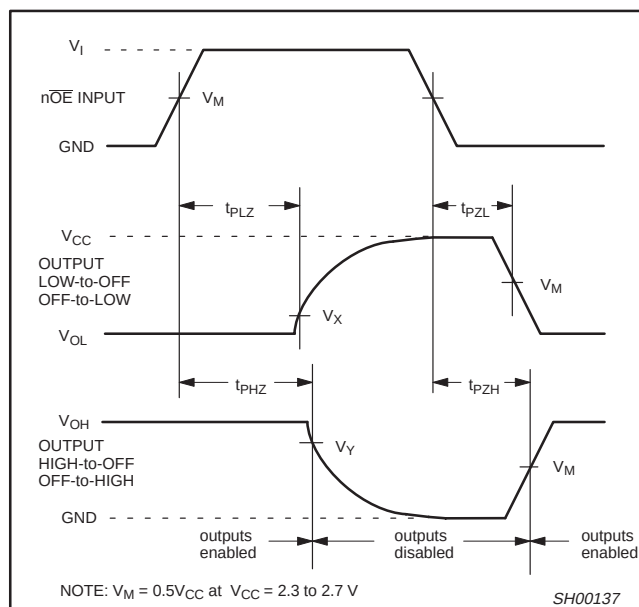
Waveform 3. Data set-up and hold times for the An input to the $\overline{LE}$ input



Waveform 4. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.



Waveform 5. Data set-up and hold times for the An input to the clock CP input

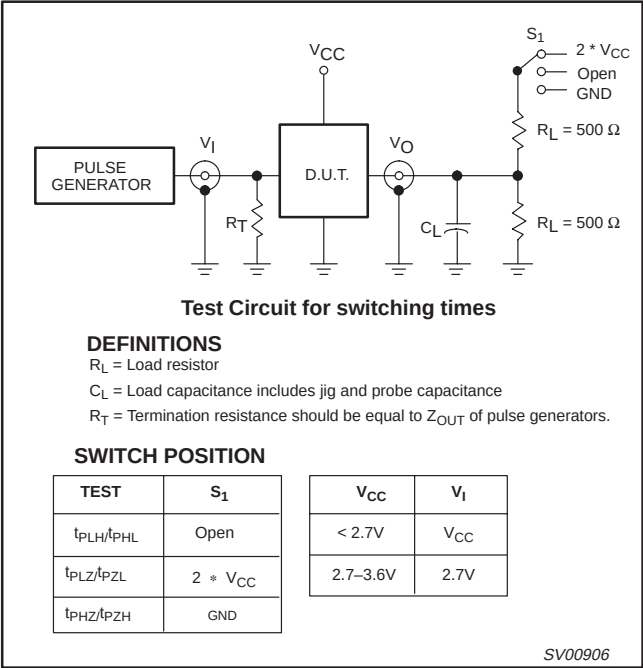


Waveform 6. 3-State enable and disable times

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TEST CIRCUIT



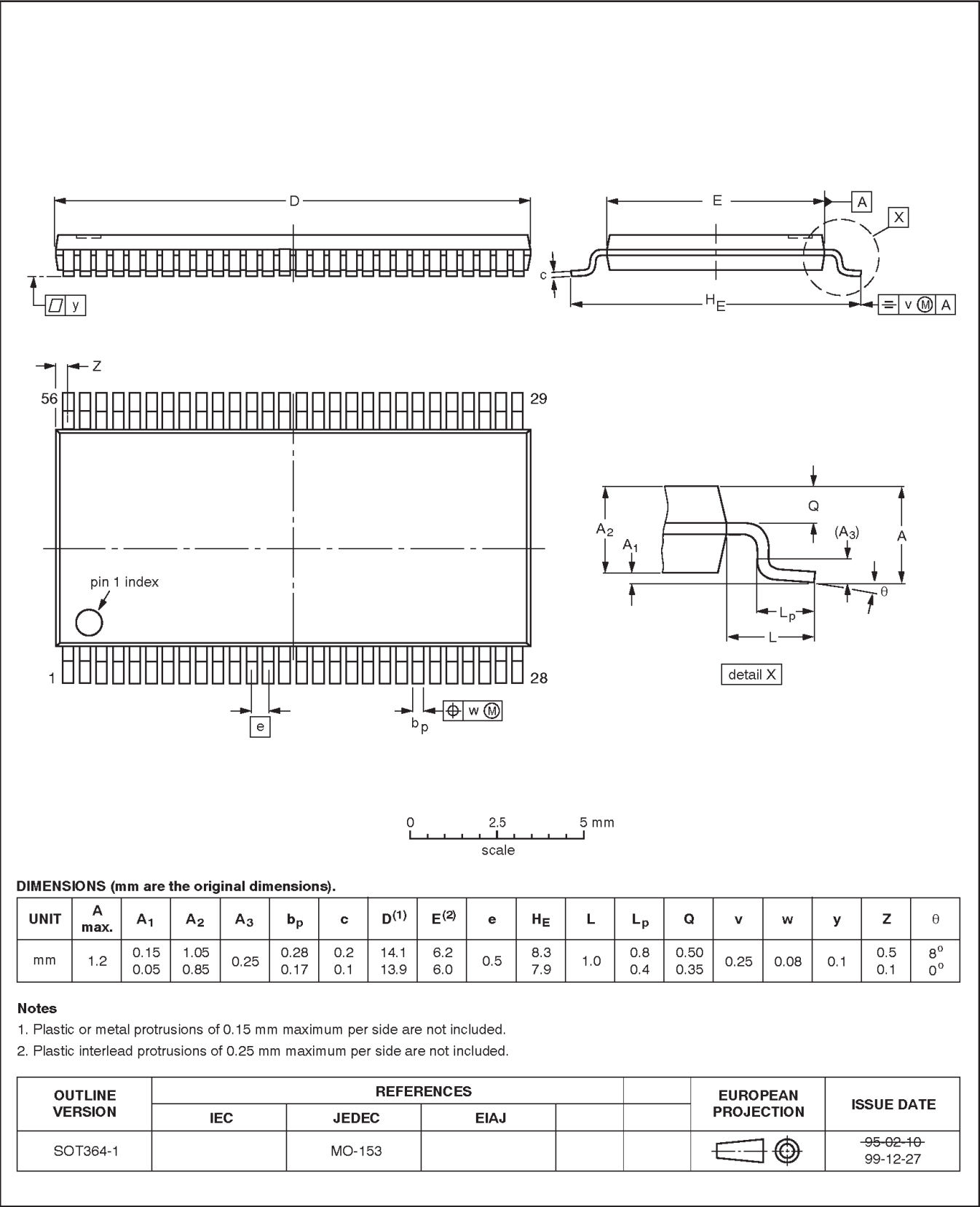
Waveform 7. Load circuitry for switching times

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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