1 pC Charge Injection, 100 pA Leakage, CMOS, ±5 V/+5 V/+3 V Dual SPDT Switch

ADG636

FEATURES

1 pC charge injection
±2.7 V to ±5.5 V dual supply
+2.7 V to +5.5 V single supply
Automotive temperature range: −40°C to +125°C
100 pA (maximum at 25°C) leakage currents
85 Ω typical on resistance
Rail-to-rail operation
Fast switching times
Typical power consumption (<0.1 µW)
TTL-/CMOS-compatible inputs
14-lead TSSOP package

APPLICATIONS

Automatic test equipment
Data acquisition systems
Battery-powered instruments
Communication systems
Sample-and-hold systems
Remote-powered equipment
Audio and video signal routing
Relay replacement
Avionics

FUNCTIONAL BLOCK DIAGRAM

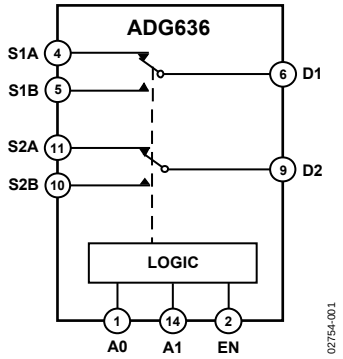

Figure 1.

GENERAL DESCRIPTION

The ADG636 is a monolithic device, comprising two independently selectable CMOS single pole, double throw (SPDT) switches. When on, each switch conducts equally well in both directions.

The ADG636 operates from a dual ±2.7 V to ±5.5 V supply, or from a single supply of +2.7 V to +5.5 V.

This switch offers ultralow charge injection of ±1.5 pC over the entire signal range and leakage current of 10 pA typical at 25°C. In addition, it offers on resistance of 85 Ω typical, which is matched to within 2 Ω between channels. The ADG636 also has low power dissipation yet is capable of high switching speeds.

The ADG636 exhibits break-before-make switching action and is available in a 14-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Ultralow charge injection. Q_{INJ}: ±1.5 pC typical over the full signal range.
2. Leakage current <0.25 nA maximum at 85°C.
3. Dual ±2.7 V to ±5 V or single +2.7 V to +5.5 V supply.
4. Automotive temperature range: −40°C to +125°C.
5. Small 14-lead TSSOP package.

Rev. B

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ADG636* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADG636: 1 pC Charge Injection, 100 pA Leakage, CMOS ±5 V/+5 V/+3 V Dual SPDT Switch Data Sheet

REFERENCE MATERIALS

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

Technical Articles

- CMOS Switches Offer High Performance in Low Power, Wideband Applications
- Data-acquisition system uses fault protection
- Enhanced Multiplexing for MEMS Optical Cross Connects
- Temperature monitor measures three thermal zones

DESIGN RESOURCES

- ADG636 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG636 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

9/09—Rev. A to Rev. B

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8/08—Rev. 0 to Rev. A

Updated Format ..... Universal
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Added Table 5; Renumbered Sequentially 10
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1/02—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V. All specifications −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
					V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance, R_{ON}	85			Ω typ	V_S = ±3 V, I_{DS} = −1 mA, Figure 14
	115	140	160	Ω max	V_S = ±3 V, I_{DS} = −1 mA, Figure 14
On-Resistance Match Between Channels, ΔR_{ON}	2			Ω typ	V_S = ±3 V, I_{DS} = −1 mA
	4	5.5	6.5	Ω max	V_S = ±3 V, I_{DS} = −1 mA
On-Resistance Flatness, $R_{FLAT(ON)}$	25			Ω typ	V_S = ±3 V, I_{DS} = −1 mA
	40	55	60	Ω max	V_S = ±3 V, I_{DS} = −1 mA
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, Figure 15
	±0.1	±0.25	±2	nA max	V_S = ±4.5 V, V_D = ∓4.5 V, Figure 15
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, Figure 15
	±0.1	±0.25	±2	nA max	V_S = ±4.5 V, V_D = ∓4.5 V, Figure 15
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = ±4.5 V, Figure 16
	±0.1	±0.25	±6	nA max	V_S = V_D = ±4.5 V, Figure 16
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time	70			ns typ	V_{S1A} = +3 V, V_{S1B} = −3 V, R_L = 300 Ω, C_L = 35 pF, Figure 17
	100	120	150	ns max	V_{S1A} = +3 V, V_{S1B} = −3 V, R_L = 300 Ω, C_L = 35 pF, Figure 17
t_{ON} Enable	100			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
	135	170	190	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
t_{OFF} Enable	55			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
	80	90	100	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 18
			10	ns min	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 18
Charge Injection	−1.2			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Figure 20
Off Isolation	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Figure 21
Channel-to-Channel Crosstalk	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Figure 23
Bandwidth −3 dB	610			MHz typ	R_L = 50 Ω, C_L = 5 pF, Figure 22

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_S (Off)	5			pF typ	f = 1 MHz
C_D (Off)	8			pF typ	f = 1 MHz
C_D (On), C_S (On)	8			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or 5.5 V
			1.0	μA max	Digital inputs = 0 V or 5.5 V
I_{SS}	0.001			μA typ	Digital inputs = 0 V or 5.5 V
			1.0	μA max	Digital inputs = 0 V or 5.5 V

[1] Guaranteed by design; not subject to production test.

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
					V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance, R_{ON}	210			Ω typ	V_S = 3.5 V, I_{DS} = −1 mA, Figure 14
	290	350	380	Ω max	V_S = 3.5 V, I_{DS} = −1 mA, Figure 14
On Resistance Match Between Channels, ΔR_{ON}	3			Ω typ	V_S = 3.5 V, I_{DS} = −1 mA
		12	13	Ω max	V_S = 3.5 V, I_{DS} = −1 mA
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, Figure 15
	±0.1	±0.25	±2	nA max	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, Figure 15
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, Figure 15
	±0.1	±0.25	±2	nA max	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V, Figure 15
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = 4.5 V/1 V, Figure 16
	±0.1	±0.25	±6	nA max	V_S = V_D = 4.5 V/1 V, Figure 16
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.4	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time	90			ns typ	V_{S1A} = 3 V, V_{S1B} = 0 V, R_L = 300 Ω, C_L = 35 pF, Figure 17
	150	185	210	ns max	V_{S1A} = 3 V, V_{S1B} = 0 V, R_L = 300 Ω, C_L = 35 pF, Figure 17
t_{ON} Enable	135			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
	180	235	275	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
t_{OFF} Enable	70			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
	105	120	135	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 19
Break-Before-Make Time Delay, t_{BBM}	30			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 18
			10	ns min	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V, Figure 18
Charge Injection	0.3			pC typ	V_S = 0 V, RS = 0 Ω, C_L = 1 nF, Figure 20
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Figure 21
Channel-to-Channel Crosstalk	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Figure 23
Bandwidth −3 dB	530			MHz typ	R_L = 50 Ω, C_L = 5 pF, Figure 22
C_S (Off)	5			pF typ	f = 1 MHz
C_D (Off)	8			pF typ	f = 1 MHz
C_D (On), C_S (On)	8			pF typ	f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or 5.5 V
			1.0	µA max	Digital inputs = 0 V or 5.5 V

[1] Guaranteed by design; not subject to production test.

V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
					V_{DD} = 2.7 V, V_{SS} = 0 V
On Resistance, R_{ON}	380	420	460	Ω typ	V_S = 1.5 V, I_{DS} = −1 mA, Figure 14
On Resistance Match Between Channels, ΔR_{ON}			5	Ω typ	V_S = 1.5 V, I_{DS} = −1 mA
LEAKAGE CURRENTS					V_{DD} = 3.3 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V, Figure 15
	±0.1	±0.25	±2	nA max	V_S = 1 V/3 V, V_D = 3 V/1 V, Figure 15
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V, Figure 15
	±0.1	±0.25	±2	nA max	V_S = 1 V/3 V, V_D = 3 V/1 V, Figure 15
Channel On Leakage, I_D (On), I_S (On)	±0.01			nA typ	V_S = V_D = 1 V/3 V, Figure 16
	±0.1	±0.25	±6	nA max	V_S = V_D = 1 V/3 V, Figure 16
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time	170			ns typ	V_{S1A} = 2 V, V_{S1B} = 0 V, R_L = 300 Ω, C_L = 35 pF, Figure 17
	320	390	450	ns max	V_{S1A} = 2 V, V_{S1B} = 0 V, R_L = 300 Ω, C_L = 35 pF, Figure 17
t_{ON} Enable	250			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 2 V, Figure 19
	360	460	530	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 2 V, Figure 19
t_{OFF} Enable	110			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 2 V, Figure 19
	175	205	230	ns max	R_L = 300 Ω, C_L = 35 pF, V_S = 2 V, Figure 19
Break-Before-Make Time Delay, t_{BBM}	80			ns typ	R_L = 300 Ω, C_L = 35 pF, V_{S1} = 2 V, Figure 18
			10	ns min	R_L = 300 Ω, C_L = 35 pF, V_{S1} = 2 V, Figure 18
Charge Injection	0.6			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, Figure 20
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Figure 21
Channel-to-Channel Crosstalk	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz, Figure 23
Bandwidth −3 dB	530			MHz typ	R_L = 50 Ω, C_L = 5 pF, Figure 22
C_S (Off)	5			pF typ	f = 1 MHz
C_D (Off)	8			pF typ	f = 1 MHz
C_D (On), C_S (On)	8			pF typ	f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 3.3 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or 3.3 V
			1.0	μA max	Digital inputs = 0 V or 3.3 V

[1] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +6.5 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	20 mA
Continuous Current, S or D	10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	150°C/W
θ_{JC} Thermal Impedance	27°C/W
Lead Soldering	
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	220°C
Pb-Free Soldering	
Reflow, Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	20 sec to 40 sec

[1] Overvoltages at EN, A0, A1, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

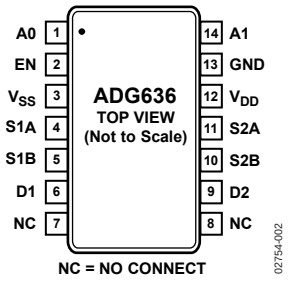

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin number	Mnemonic	Description
1	A0	Digital Input (LSB).
2	EN	Active High Digital Input.
3	V_{SS}	Negative Power Supply. For single-supply operation, connect this pin to GND.
4	S1A	Source Terminal. Can be an input or output.
5	S1B	Source Terminal. Can be an input or output.
6	D1	Drain Terminal. Can be an input or output.
7	NC	Not Electrically Connected.
8	NC	Not Electrically Connected.
9	D2	Drain Terminal. Can be an input or output.
10	S2B	Source Terminal. Can be an input or output.
11	S2A	Source Terminal. Can be an input or output.
12	V_{DD}	Positive Power Supply.
13	GND	Ground (0 V) Power Supply.
14	A1	Digital Input (MSB).

Table 6. Truth Table

A1	A0	EN	On Switch
X[1]	X[1]	0	None
0	0	1	S1A, S2A
0	1	1	S1B, S2A
1	0	1	S1A, S2B
1	1	1	S1B, S2B

[1] X = logic state doesn't matter; it can be either 0 or 1.

TYPICAL PERFORMANCE CHARACTERISTICS

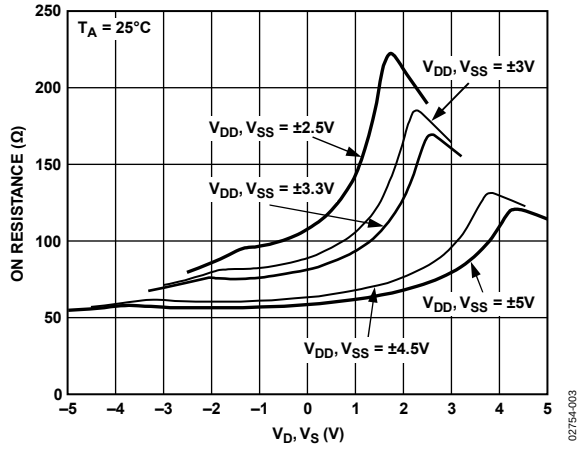

Figure 3. On Resistance vs. V_D (V_S), Dual Supply

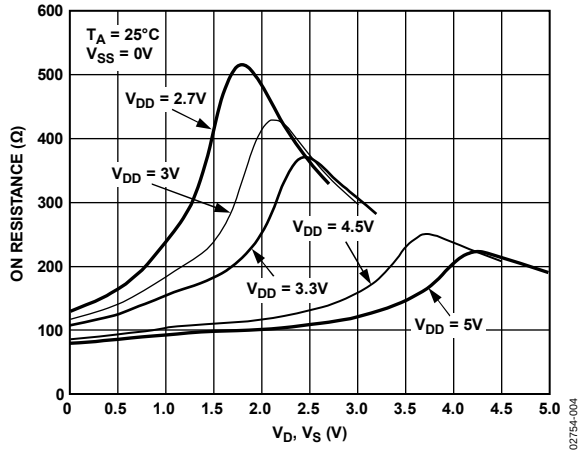

Figure 4. On Resistance vs. V_D (V_S), Single Supply

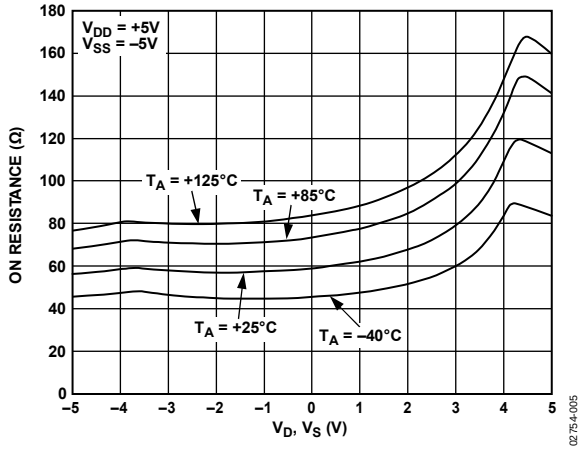

Figure 5. On Resistance vs. V_D (V_S) for Different Temperatures, Dual Supply

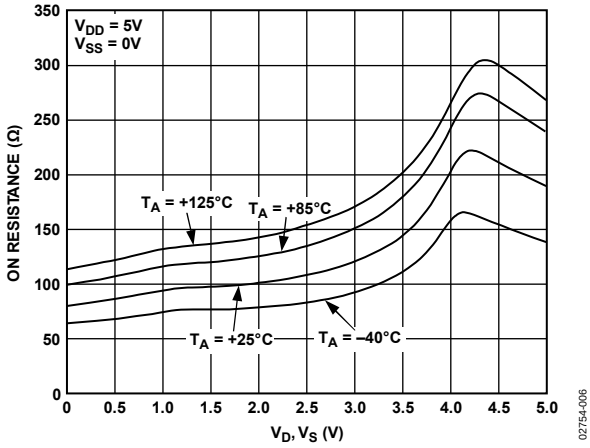

Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, Single Supply

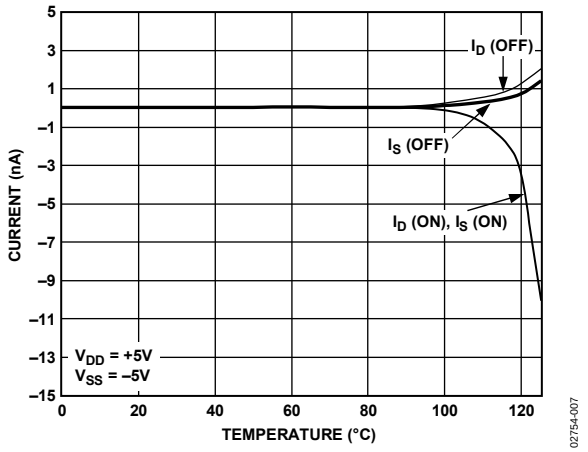

Figure 7. Leakage Currents vs. Temperatures, Dual Supply

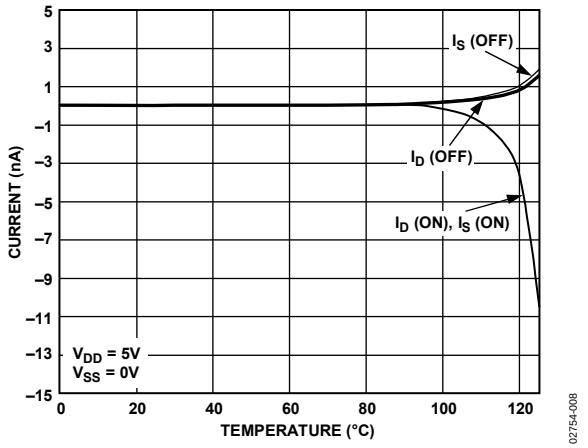

Figure 8. Leakage Currents vs. Temperature, Single Supply

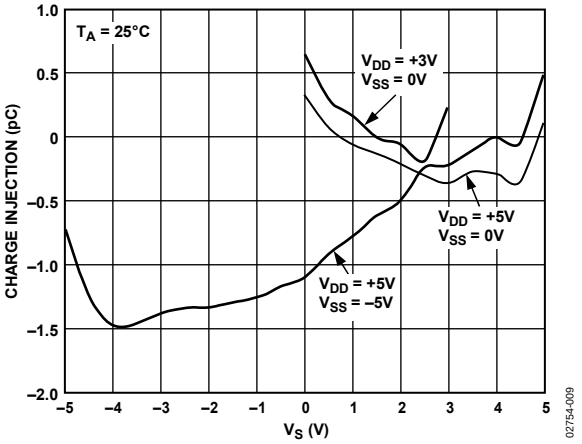

Figure 9. Charge Injection vs. Source Voltage

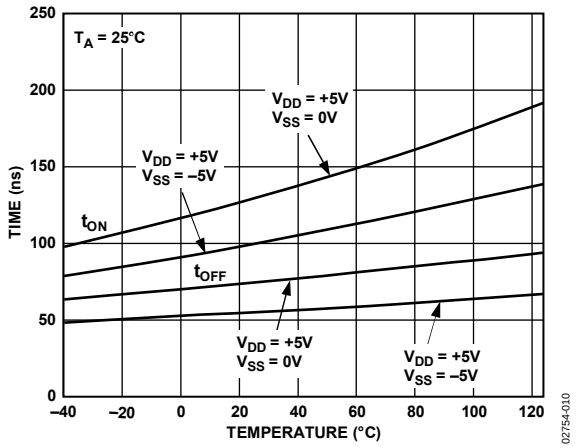

Figure 10. t_{ON}/t_{OFF} Enable Timing vs. Temperature

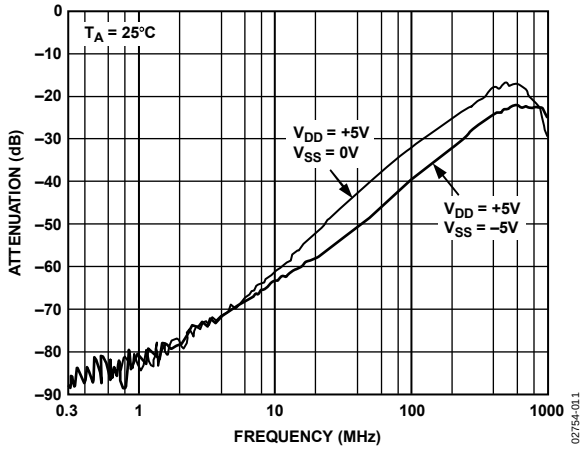

Figure 11. Off Isolation vs. Frequency

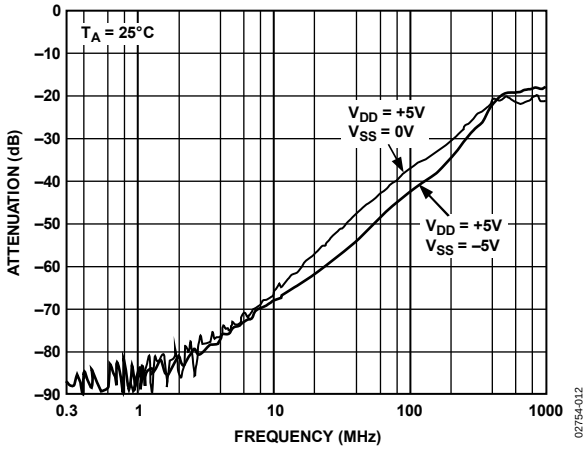

Figure 12. Crosstalk vs. Frequency

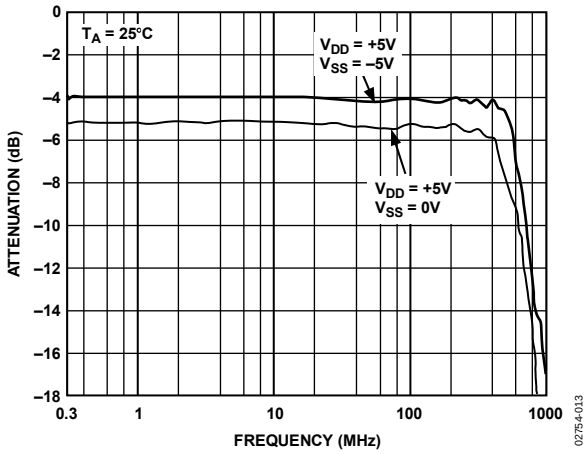

Figure 13. On Response vs. Frequency

TEST CIRCUITS

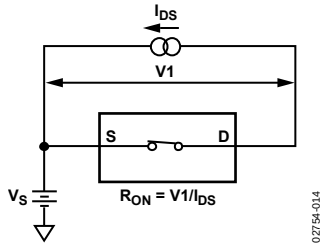

Figure 14. On Resistance

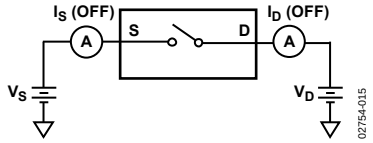

Figure 15. Off Leakage

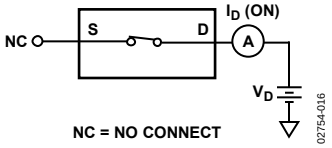

Figure 16. On Leakage

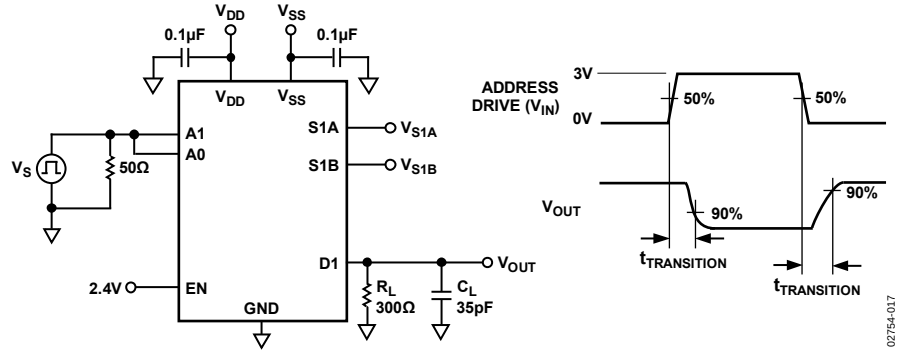

Figure 17. Transition Time, $t_{TRANSITION}$

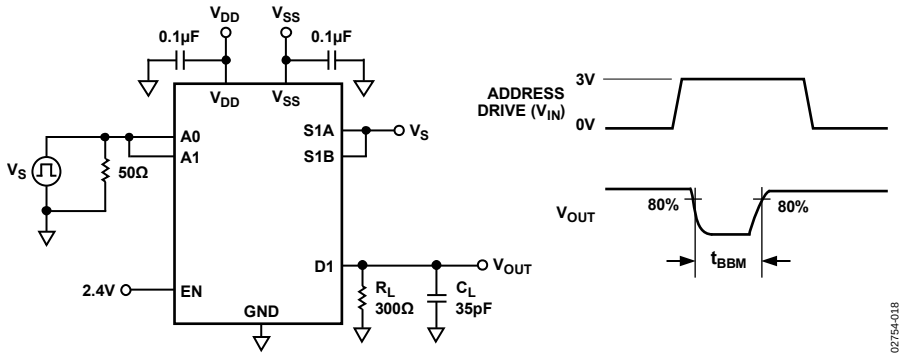

Figure 18. Break-Before-Make Delay, t_{BBM}

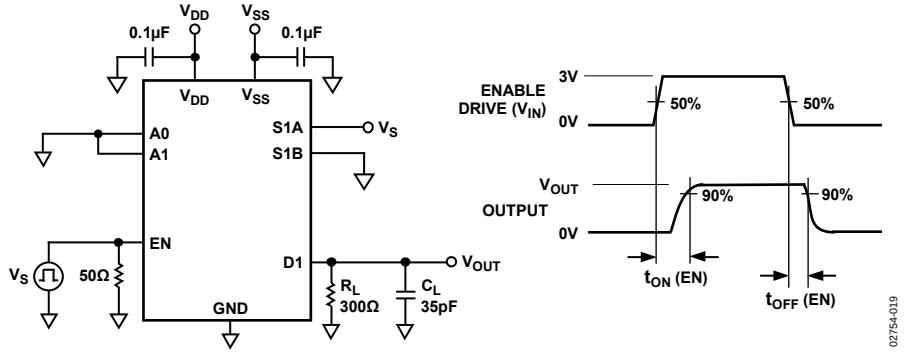

Figure 19. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

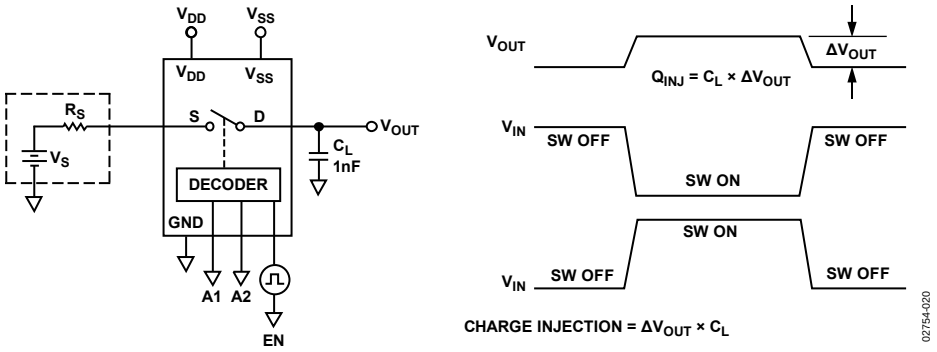

Figure 20. Charge Injection

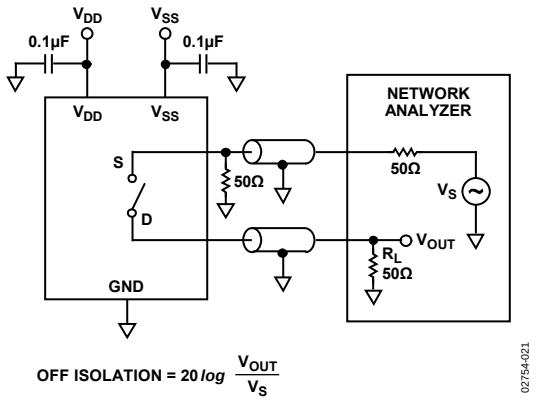

Figure 21. Off Isolation

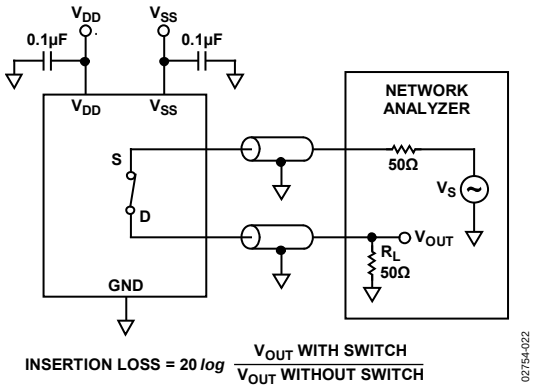

Figure 22. Bandwidth

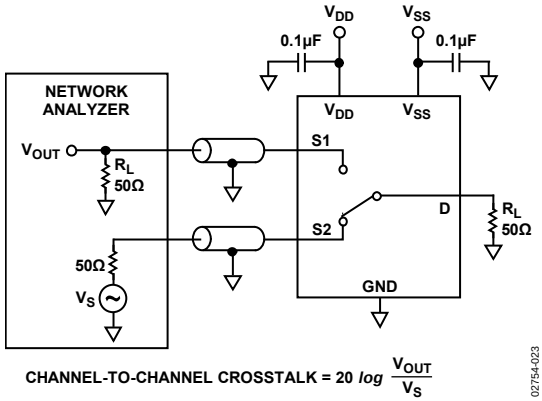

Figure 23. Channel-to-Channel Crosstalk

TERMINOLOGY

V_{DD}
Most positive supply potential.

V_{SS}
Most negative power supply in a dual-supply application. In single-supply applications, this should be tied to ground at the device.

GND
Ground (0 V) reference.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

S
Source terminal. May be an input or output.

D
Drain terminal. May be an input or output.

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
On resistance match between any two channels (that is, R_{ON} max − R_{ON} min).

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum values of on resistance as measured over the specified analog signal range.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D (On), I_S (On)
Channel leakage current with the switch on.

V_D, V_S
Analog voltage on Terminal D and Terminal S.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

$I_{INL(IINH)}$
Input current of the digital input.

C_S (Off)
Channel input capacitance for the off condition.

C_D (Off)
Channel output capacitance for the off condition.

C_D (On), C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and the switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and the switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital input and the switch on condition when switching from one address state to another.

t_{BBM}
Off time or on time measured between the 80% points of both switches when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Bandwidth
The frequency response of the on switch.

Insertion Loss
Loss due to the on resistance of the switch.

OUTLINE DIMENSIONS

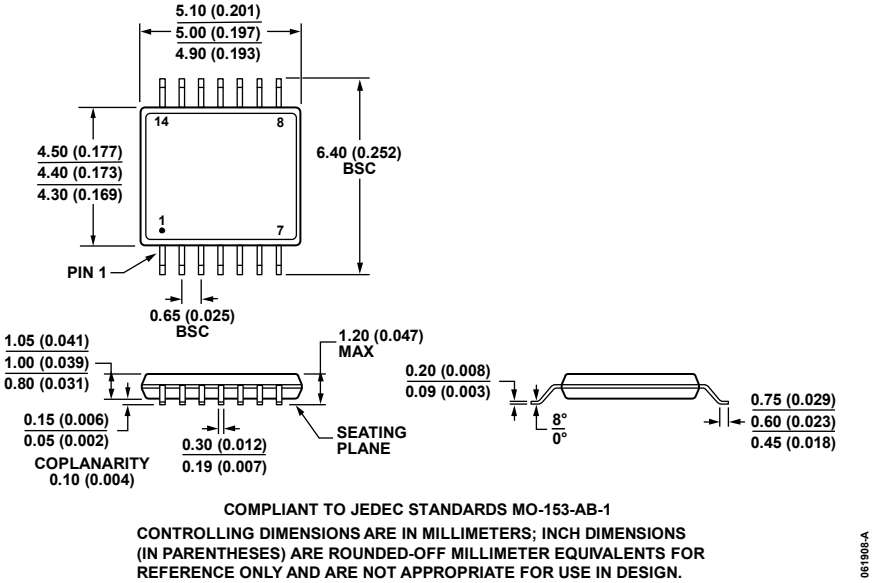

Figure 24. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG636YRU	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG636YRU-REEL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG636YRUZ[1]	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG636YRUZ-REEL[1]	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG636YRUZ-REEL7[1]	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14

[1] Z = RoHS Compliant Part.

D02754-0-9/09(B)