CY25562

Spread Spectrum Clock Generator

Features

- 50 to 200 MHz operating frequency range
- Wide range of spread selections: 9
- Accepts clock and crystal inputs
- Low power dissipation
  - 70 mW Typ (Fin = 65 MHz)
- Frequency spread disable function
- Center spread modulation
- Low cycle-to-cycle jitter
- 8-pin SOIC package

Functional Description

CY25562 is a spread spectrum clock generator (SSCG) IC used to reduce electromagnetic interference (EMI) found in today's high speed digital electronic systems.

CY25562 uses a Cypress proprietary phase locked loop (PLL) and spread spectrum clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By doing this, the measured EMI at the fundamental and harmonic frequencies of clock (SSCLK) is reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading system performance.

CY25562 is a simple and versatile device. The frequency and spread percentage range is selected by programming S0 and S1 digital inputs. These inputs use three logic states including high (H), low (L), and middle (M) logic levels to select one of the nine available spread percentage ranges. Refer to Figure 2 on page 4 for programming details.

CY25562 is intended for applications with a reference frequency in the range of 50 to 200 MHz.

A wide range of digitally selectable spread percentages is made possible by using the tri-level (high, low, and middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

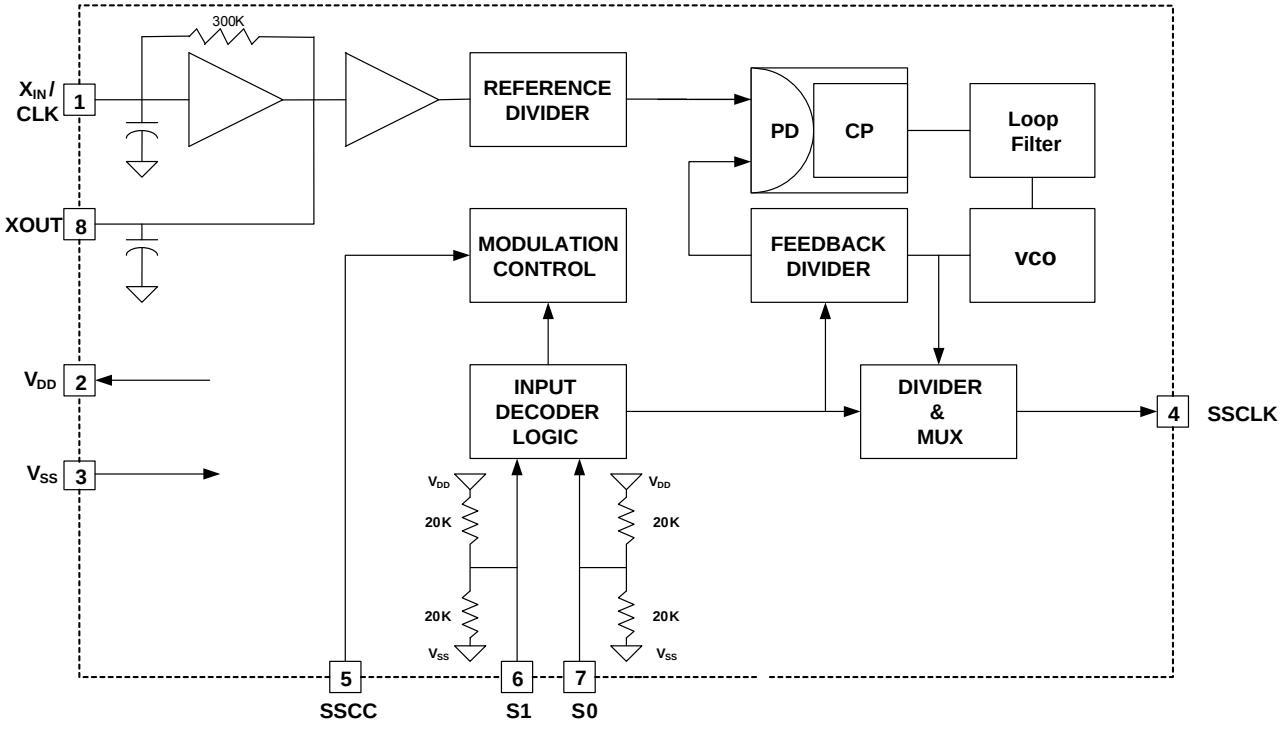
Spread spectrum clock control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

CY25562 is available in an eight-pin SOIC package with a 0 to 70 °C operating temperature range.

Refer to CY25561 for applications with lower drive requirements and CY25560 with lower drive and frequency requirements.

For a complete list of related documentation, click here.

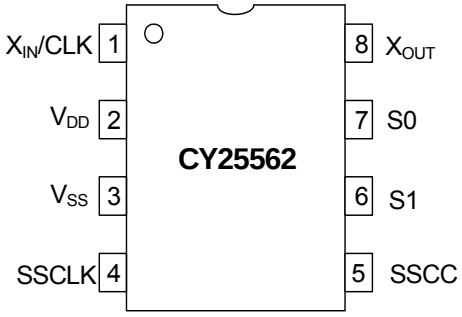
Logic Block Diagram



Contents

Pinout

Figure 1. 8-pin SOIC Pinout



Pin Description

Pin #	Pin Name	Type	Pin Description
1	X_{IN}/CLK	I	Clock or crystal connection input. Refer to Figure 2 on page 4 for input frequency range selection.
2	V_{DD}	P	Positive power supply
3	V_{SS}	P	Power supply ground
4	SSCLK	O	SSCG modulated clock output
5	SSCC	I	Spread spectrum clock control (enable/disable) function. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally.
6	S1	I	Tri-level logic input control pin used to select frequency and bandwidth. Frequency/bandwidth selection and tri-level logic programming. See Figure 3 on page 4. Pin 6 has internal resistor divider network to V_{DD} and V_{SS}. Refer to Logic Block Diagram on page 1.
7	S0	I	Tri-level logic input control pin used to select frequency and bandwidth. Frequency/bandwidth selection and tri-level logic programming. See Figure 3 on page 4. Pin 7 has internal resistor divider network to V_{DD} and V_{SS}. Refer to Logic Block Diagram on page 1.
8	X_{OUT}	O	Oscillator output pin connected to crystal. Leave this pin unconnected If an external clock drives X_{IN}/CLK.

Functional Overview

Frequency and Spread Percentage Selection

Figure 2. Frequency and Spread Percentage Selection (Center Spread)

50–100 MHz (Low Range)

Input Frequency (MHz)	S1=M S0=M (%)	S1=M S0=0 (%)	S1=1 S0=0 (%)	S1=0 S0=0 (%)	S1=0 S0=M (%)
50 - 60	4.3	3.9	3.3	2.9	2.7
60 - 70	4.0	3.6	3.1	2.6	2.5
70 - 80	3.8	3.4	2.9	2.5	2.4
80 - 100	3.5	3.1	2.7	2.2	2.1

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

100–200 MHz (High Range)

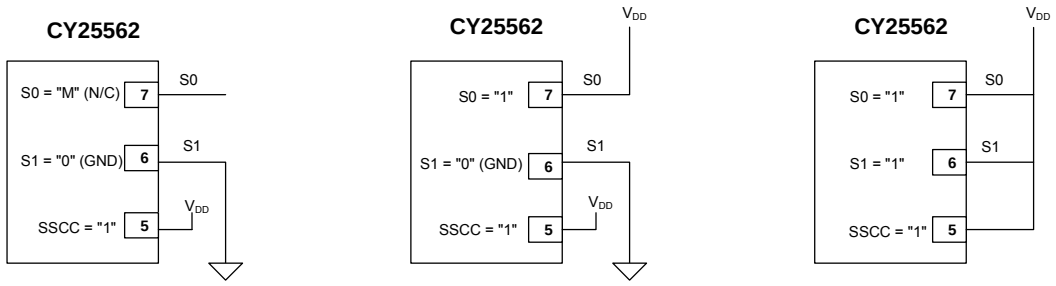
Input Frequency (MHz)	S1=1 S0=M (%)	S1=0 S0=1 (%)	S1=1 S0=1 (%)	S1=M S0=1 (%)
100 – 120	3.0	2.4	1.6	1.3
120 -130	2.7	2.1	1.4	1.1
130 - 140	2.6	2.0	1.3	1.1
140 - 150	2.6	2.0	1.3	1.1
150 - 160	2.5	1.8	1.2	1.0
160 - 170	2.4	1.8	1.2	1.0
170 - 180	2.4	1.8	1.2	1.0
180 - 190	2.3	1.7	1.1	0.9
190 - 200	2.3	1.6	1.1	0.9

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

Trilevel Logic

With binary logic, four states can be programmed with two control lines, whereas tri-level logic can program nine logic states using two control lines. Trilevel logic in CY25562 is implemented by defining a third logic state in addition to the standard logic “1” and “0.” Pins six and seven of CY25562 recognize a logic state by the voltage applied to the respective pin. These states are defined as “0” (low), “M” (middle), and “1” (one). Each of these states have a defined voltage range that is interpreted by CY25562 as “0”, “M,” or “1” logic state. Refer to Electrical Characteristics on page 7 for voltage ranges for each logic state. CY25562 has two equal value resistors connected internally to pin 6 and pin 7, which produce the default “M” state. Pins 6 or 7 can be tied directly to ground or V_{DD} to program a logic “0” or “1” state, respectively. See the following examples:

Figure 3. Trilevel Logic Example



SSCG Theory of Operation

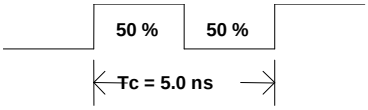
CY25562 is a PLL-type clock generator using a proprietary Cypress design to modulate the reference clock. By precisely controlling the bandwidth of the output clock, CY25562 becomes a low-EMI clock generator. The theory and detailed operation of CY25562 is discussed in the following sections.

EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 percent. Because of this 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, that is; third, fifth, seventh, etc. The amount of energy contained in the fundamental and odd harmonics can be reduced by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor; all the energy at that frequency is concentrated in a very narrow bandwidth, and consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test satisfies agency requirements for EMI. Conventional methods of reducing EMI use shielding, filtering, multi-layer PCBs, etc. CY25562 reduces the peak energy in the clock by increasing the clock bandwidth, thus lowering the Q.

SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle-to-cycle. CY25562 takes a narrow band digital reference clock in the range of 50 to 200 MHz and produces a clock that sweeps between a controlled start (F1) and stop (F2) frequency at a precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 200 MHz clock with a 50 percent duty cycle, as shown in this figure.



Clock frequency = fc = 200 MHz
Clock period = Tc = 1/200 MHz

If this clock is applied to the X_{IN}/CLK pin of CY25562, the output clock at pin 4 (SSCLK) sweeps back and forth between two frequencies. These two frequencies, F1 and F2, calculate total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition, sweep, from F1 to F2, the amount of time and sweep waveform become a very important factor in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. Figure 4 shows the modulation profile of a 200 MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. Figure 4 also shows a scan of the same SSCG clock using a spectrum analyzer. The spectrum analyzer scan shows a 10 dB reduction in the peak RF energy when using CY25562 SSCG clock.

Modulation Rate

Spread spectrum clock generators use frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the modulation rate, Tmod. Modulation rates of SSCG clocks are generally referred to in terms of frequency or Fmod = 1/Tmod.

The input clock frequency, Fin, and the internal divider count, Cdiv, determine the modulation rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. CY25562 has a fixed divider count of 2332.

Figure 4. SSCG Clock, Part Number, Fin = 200 MHz

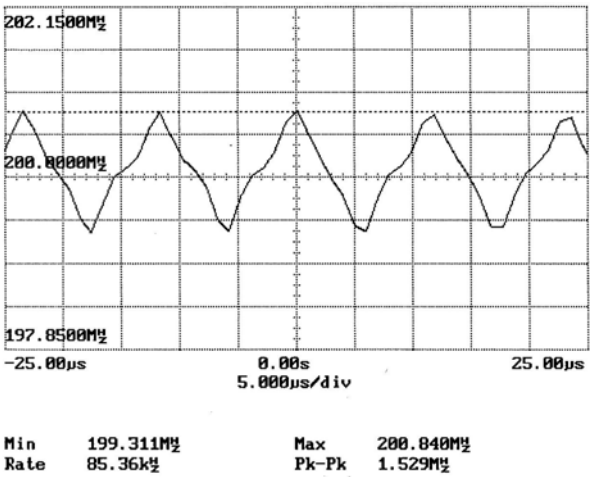
Device	**Cdiv**	
CY25562	2332	(All Ranges)

Example:

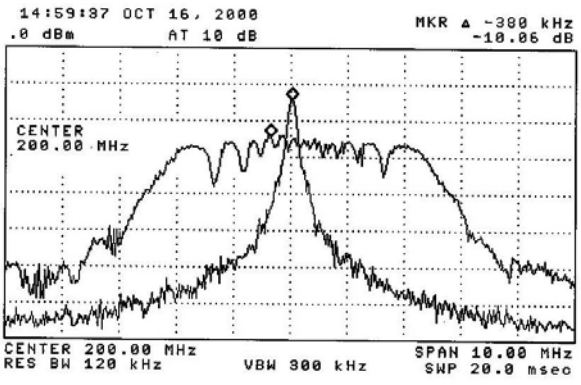
Device = CY25562
Fin = 200 MHz
Range = S1 = 1, S0 = 1

Then;

Modulation Rate = Fmod = 200 MHz/2332 = 85.7 kHz.



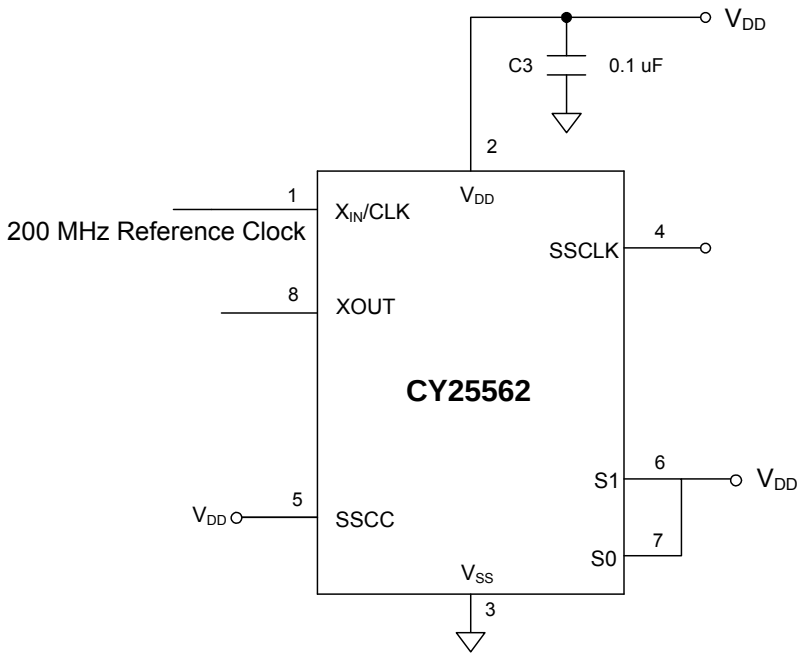
Modulation Profile



Spectrum Analyzer

CY25562 Application Schematic

Figure 5. Application Schematic



The schematic in Figure 5 demonstrates how CY25562 is configured in a typical application. This application is using a 200 MHz reference clock connected to pin 1. Because an external reference clock is used, pin 8 (Xout) is left unconnected.

This configuration depicts the profile and spectrum scans shown in Figure 4 on page 5. Note that S0 = S1 = 1, for a spread of approximately 1.1 percent.

Absolute Maximum Ratings

Exceeding maximum ratings [1, 2] may shorten the useful life of the device. User guidelines are not tested.

Supply voltage (V_{DD}) .....–0.5 V to +6.0 V

DC input voltage .....–0.5 V to V_{DD} + 0.5 V

Junction temperature ..... –40 °C to +140 °C

Operating temperature ..... 0 °C to 70 °C

Storage temperature ..... –65 °C to +150 °C

Static discharge voltage (ESD) ..... 2,000 V Min

Electrical Characteristics

V_{DD} = 3.3 V, T_A = 25 °C, and C_L (Pin 4) = 15 pF unless otherwise noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply range	±10%	2.97	3.3	3.63	V
V_{INH}	Input high voltage	S0 and S1 only	0.85 × V_{DD}	V_{DD}	V_{DD}	V
V_{INM}	Input middle voltage	S0 and S1 only	0.40 × V_{DD}	0.50 × V_{DD}	0.60 × V_{DD}	V
V_{INL}	Input low voltage	S0 and S1 only	0.0	0.0	0.15 × V_{DD}	V
V_{OH1}	Output high voltage	I_{OH} = 6 mA	2.4	–	–	V
V_{OH2}	Output high voltage	I_{OH} = 20 mA	2.0	–	–	V
V_{OL1}	Output low voltage	I_{OH} = 6 mA	–	–	0.4	V
V_{OL2}	Output low voltage	I_{OH} = 20 mA	–	–	1.2	V
C_{in1}	Input capacitance	X_{IN}/CLK (pin 1)	3	4	5	pF
C_{in2}	Input capacitance	Xout (pin 8)	6	8	10	pF
C_{in2}	Input capacitance	S0, S1, SSCC (pins 7, 6, 5)	3	4	5	pF
I_{DD1}	Power supply current	Fin = 65 MHz, CL = 15 pF	–	23	30	mA
I_{DD2}	Power supply current	Fin = 200 MHz, CL =15 pF	–	53	66	mA
I_{DD3}	Power supply current	Fin = 200 MHz, no load	–	48	60	mA

Thermal Resistance

Parameter [3]	Description	Test Conditions	8-pin SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	131	°C/W
θ_{JC}	Thermal resistance (junction to case)		41	°C/W

Notes
1. Operation at any absolute maximum rating is not implied.
2. Single power supply: The voltage on any input or I/O pin cannot exceed the power pine during power-up.
3. These parameters are guaranteed by design and are not tested.

X_{IN}/CLK DC Specification

Parameter	Description	Conditions	Min	Max	Units
$V_{IH(X)}$	Input high voltage, X_{IN} Clock Input	F ≤ 100 MHz	80	–	% of V_{DD}
		F ≤ 133 MHz	86	–	% of V_{DD}
		F ≤ 200 MHz	92	–	% of V_{DD}
$V_{IL(X)}$	Input low voltage, X_{IN} Clock Input	–	–	15	% of V_{DD}

Electrical Timing Characteristics

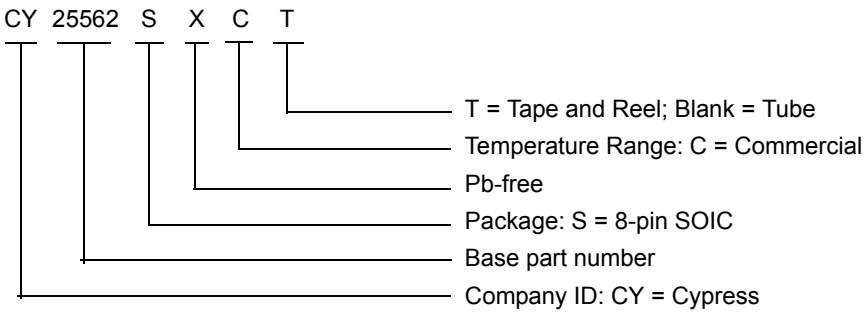
V_{DD} = 3.3 V, T_A = 25 °C, and C_L = 15 pF unless otherwise noted. Rise/Fall at 0.4 to 2.4 V, Duty at 1.5 V

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CLKFR}	Input clock frequency range	Pk–Pk = 3.3 V	50	–	200	MHz
t_{RISE}	Clock rise time (pin 4)	SSCLK, CL = 15 pF, 200 MHz	0.8	0.9	1.0	ns
t_{FALL}	Clock fall time (pin 4)	SSCLK, CL = 15 pF, 200 MHz	0.8	0.9	1.0	ns
t_{RISE}	Clock rise time (pin 4)	SSCLK, CL = 33 pF, 200 MHz	1.1	1.45	1.8	ns
t_{FALL}	Clock fall time (pin 4)	SSCLK, CL = 33 pF, 200 MHz	1.1	1.5	1.9	ns
D_{TYin}	Input clock duty cycle	X_{IN}/CLK (pin 1)	30	50	70	%
D_{TYout}	Output clock duty cycle	SSCLK1 (pin 4)	45	50	55	%
FM1	Frequency modulation	Fin = 70 MHz	29.5	30.0	30.5	kHz
FM2	Frequency modulation	Fin = 200 MHz	85.0	85.4	86	kHz
C_{CJ1}	Cycle-to-Cycle jitter	Fin = 50 MHz, mod ON	–	150	175	ps
C_{CJ2}	Cycle-to-Cycle jitter	Fin = 120 MHz, mod ON	–	175	200	ps
C_{CJ3}	Cycle-to-Cycle jitter	Fin = 200 MHz, mod ON	–	250	300	ps

Ordering Information

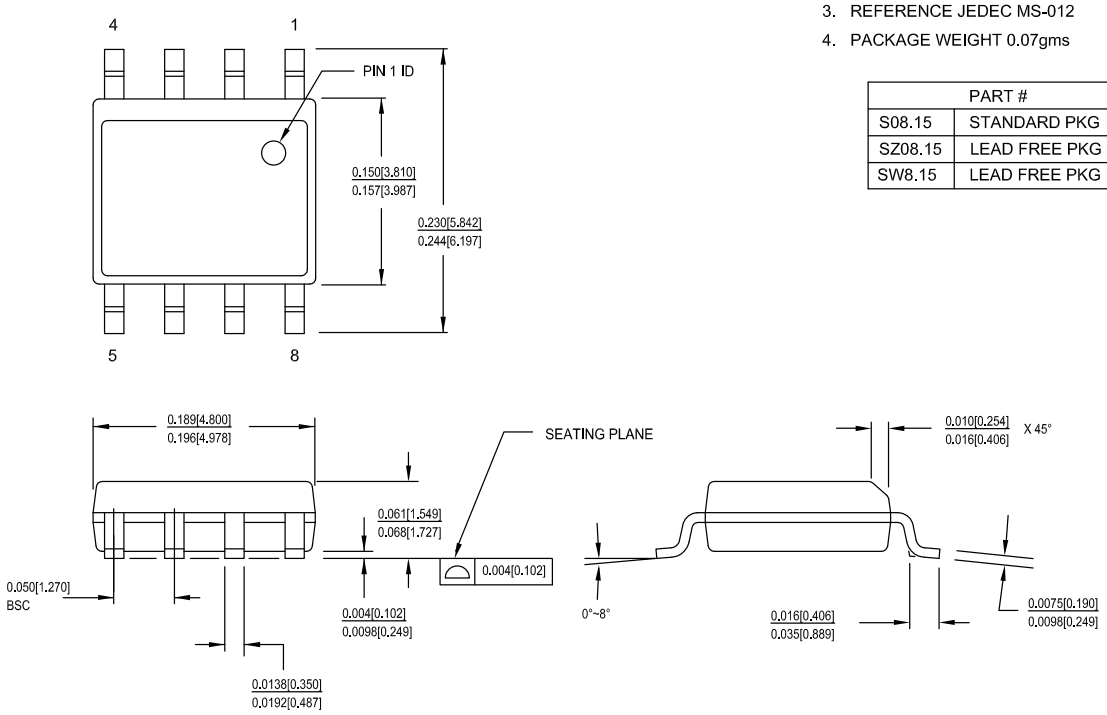
Part Number	Package Type	Product Flow
CY25562SXC	8-pin SOIC, Pb-free	Commercial, 0 °C to 70 °C
CY25562SXCT	8-pin SOIC – tape and reel, Pb-free	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 6. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066



Acronyms

Acronym	Description
EMI	Electromagnetic Interference
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SOIC	Small-Outline Integrated Circuit
SSC	Spread Spectrum Clock
SSCG	Spread Spectrum Clock Generator

Document Conventions

Units of Measure

Symbol	Unit of Measure
%	percent
°C	degree Celsius
dB	decibel
mA	milliampere
MHz	megahertz
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt
Ω	ohm
W	watt

Document History Page

Document Title: CY25562, Spread Spectrum Clock Generator Document Number: 38-07392				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	115526	07/08/02	OXC	New data sheet.
*A	119444	10/17/02	RGL	Updated Absolute Maximum Ratings: Corrected the values to match the device.
*B	122703	12/28/02	RBI	Updated Absolute Maximum Ratings: Added power up requirements to maximum ratings information.
*C	2567245	09/16/08	PYG / KVM / AESA	Replaced CY25562SC w/ CY25562SXC, CY255652SCT w/ CY25562SXCT. Package changed from S8 to SZ8. Updated to new template.
*D	3187957	03/04/2011	CXQ	Updated Package Drawing and Dimensions.
*E	3537234	02/28/2012	PURU	Removed Benefits. Removed Applications. Added Ordering Code Definitions under Ordering Information. Added Acronyms and Units of Measure.
*F	4586478	12/03/2014	AJU	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Drawing and Dimensions: Updated package diagram 51-85066 to current revision.
*G	4709860	04/01/2015	TAVA	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*H	5278942	05/20/2016	PSR	Added Thermal Resistance. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *G to *H. Updated to new template.
*I	5779322	06/20/2017	PSR	Added XIN/CLK DC Specification.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Clock Tree Services

cypress.com/cts