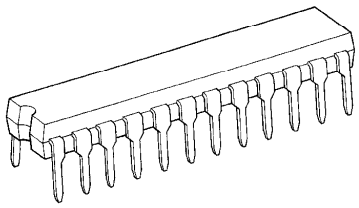
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9198P, TC9198F

PROGRAMMABLE COUNTER

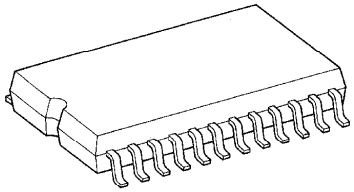
TC9198P, TC9198F are high speed programmable counters developed for dividing PLL circuits and other various circuits.

TC9198P



DIP24-P-300-2.54

TC9198F



SOP24-P-450-1.27A

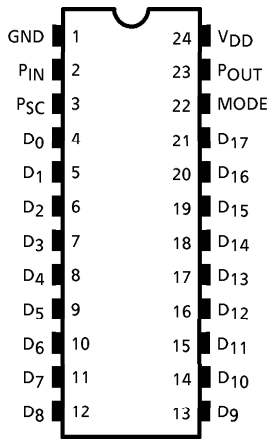
Weight
DIP24-P-300-2.54 : 1.2g (Typ.)
SOP24-P-450-1.27A : 0.48g (Typ.)

FEATURES

- Setting of number of divisions can be made directly from the input terminals.
- The counter allows changing-over of swallow system / simple division.
- At simple division, changing-over of BCD code / BINARY code can be performed.
- The number of division is 262, 143 in maximum in swallow mode, and can be 5 to 65,535 at BINARY in simple division mode and can be 5 to 15,999 at BCD code.
- Owing to CMOS construction, the operating power voltage range is wide, and the power consumption is low.
- The package is DIP-24PIN for TC9198P and SOP-24PIN for TC9198F.

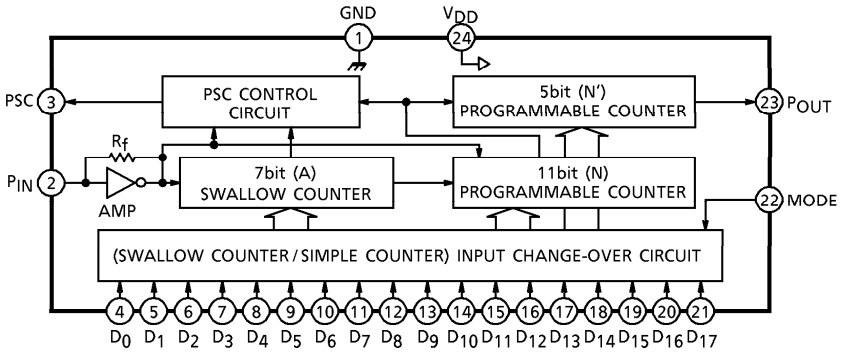
PIN CONNECTION

(TOP VIEW)



980910EBA2

BLOCK DIAGRAM



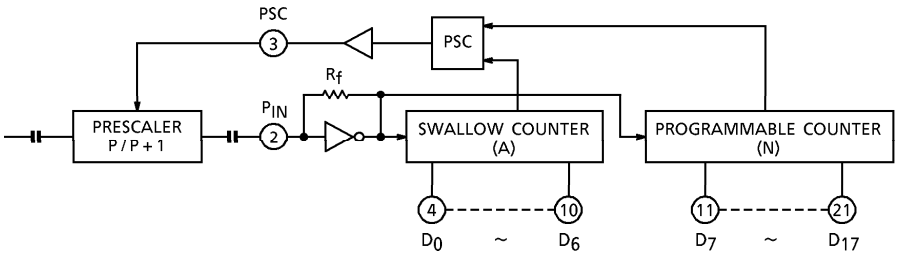
PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	NOTE
1	GND	Ground Terminal	—	—
24	V_{DD}	Power Supply Terminal		
2	P_{IN}	Programmable Counter Input	Programmable counter input terminal. Prescaler output is input by the capacitor coupling.	Amp. Circuit built in
3	PSC	Prescaler Control Output	No. of division control signal output prescaler. It becomes P in "H" level, and P + 1 in "L" level.	—
22	MODE	Counter Operation Change-over Input	Change-over input for swallow counter operation and simple counter operation. It becomes swallow counter at "L" level, or open and simple counter operation at "H" level.	Pull down resistance built in
4	D_0	Number of Division Setting Input	Input terminal for setting number of division of programmable counter. (1) MODE (22PIN) = at "L" level ● D_0~D_6→Swallow counter : A ● D_7~D_{17}→Programmable counter : N (2) MODE = at "H" and D_{17} = at "L" level ● Simple counter operation in setting BINARY code. ● D_0~D_{15}→Programmable counter : N ● D_{16}→NC (3) MODE = at "H" and D_{17} = at "H" level ● Simple counter operation in setting BCD code. ● D_0~D_3→N = 1~9 setting ● D_4~D_7→N = 10~90 setting ● D_8~D_{11}→N = 100~900 setting ● D_{12}~D_{15}→N = 1000~15000 setting ● D_{16}→NC	
5	D_1			
6	D_2			
7	D_3			
8	D_4			
9	D_5			
10	D_6			
11	D_7			
12	D_8			
13	D_9			
14	D_{10}			
15	D_{11}			
16	D_{12}			
17	D_{13}			
18	D_{14}			
19	D_{15}			
20	D_{16}			
21	D_{17}			
23	P_{OUT}	Programmable Counter Output Terminal	1 / N of P_{IN} input frequency is output pulse width corresponds to 4 cycles of input frequency.	—

DESCRIPTION ON FUNCTION AND OPERATION

1. Programmable counter

When the MODE INPUT (Pin 22) is set to "L" level (or opened), the programmable counter becomes swallow system.
The system consists of a 7bit swallow counter, 11bit programmable counter and a prescaler logic which change-over the number of divisions of the 2-module prescaler connected to the outside.



- Total number of divisions can be determined by the following formula

$$\text{Number of divisions} = (P+1)\cdot A + P\cdot(N-A)$$
$$= N\cdot P + A \qquad \text{Where, } N > A$$

- The prescaler used requires to be the number of divisions of P + 1 when the PSC terminal is in "L" level and of P when it is in "H" level.
- The input for setting the number of divisions of the programmable counter consists of 18bits, but it should be cared that it changes by the number of divisions P of the prescaler used. ($P \leqq 128$)

(1) When prescaler is P = 128

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}	2^{17}

(*) The BINARY code D of the number of division is $16{,}384 \leqq D \leqq 262{,}143$, as a rule.

(2) When prescaler is P = 64

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}
2^0	2^1	2^2	2^3	2^4	2^5	"0"	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}

(*) The BINARY code D of the number of divisions is $4{,}096 \leqq D \leqq 131{,}071$, as a rule.
(*) D_6 (Pin 10) is used as GND or in open.

(3) When prescaler is P = 32

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}
2^0	2^1	2^2	2^3	2^4	"0"		2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}

(*) The BINARY code D of the number of divisions is $1,024 \leqq D \leqq 65,535$, as a rule.
(*) D_5 (Pin 9) and D_6 (Pin 10) are used as GND or in open.

(4) When prescaler is P = 16

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}
2^0	2^1	2^2	2^3	"0"			2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}

(*) The BINARY code D of the number of divisions is $256 \leqq D \leqq 32,767$, as a rule.
(*) $D_4 \sim D_6$ (Pin 8~Pin 9) are used as GND or in open.

2. Simple program counter

When the MODE INPUT (Pin 22) is set to "H" level, the simple counter system is established. When D_{17} (Pin 21) is made to "H" level, the system operates in BCD mode, and to "L" level, in BINARY mode.

(1) Operation in BINARY MODE : D_{17} (Pin 21) = D_{16} (Pin 20) = "L" level or in open

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}

※ The BINARY code D of number of divisions becomes $5 \leqq D \leqq 65,535$

(2) Operation in BCD MODE : D_{17} (Pin 21) = "H", D_{16} (Pin 20) = "L" level or open

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
1	2	4	8	1	2	4	8	1	2	4	8	1	2	4	8
×1				×10				×100				×1000			

(*) $D_0 \sim D_3$, $D_4 \sim D_7$, $D_8 \sim D_{11}$ set number of divisions by BCD code.
It should be cared that it does not operate when it is set N = 10 or more.
(*) In $D_{12} \sim D_{15}$, the number of division can be set by the BINARY code.
$D_{12} \sim D_{15}$ = 0101 (A) → N = 10,000
$D_{12} \sim D_{15}$ = 1101 (B) → N = 11,000
$D_{12} \sim D_{15}$ = 0011 (C) → N = 12,000
$D_{12} \sim D_{15}$ = 1011 (D) → N = 13,000
$D_{12} \sim D_{15}$ = 0111 (E) → N = 14,000
$D_{12} \sim D_{15}$ = 1111 (F) → N = 15,000
(*) The BCD code of the number of divisions becomes $5 \leqq D \leqq 15,999$

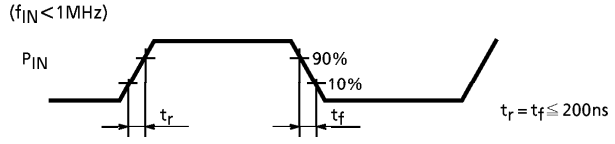
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	−0.3~7.0	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−65~150	°C

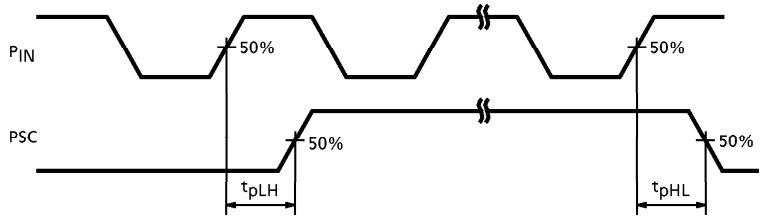
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = −40~85°C, V_{DD} = 5.0V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	—	f_{IN} = 15MHz, V_{IN} = 1.0V_{p-p}		4.0	5.0	6.0	V
Operating Supply Current		I_{DD}	—			—	5.0	10	mA
Maximum Operating Frequency		f_{opr} (1)	—	V_{IN} = 1.0V_{p-p}, BINARY mode		1.0	—	15	MHz
		f_{opr} (2)	—	V_{IN} = 1.0V_{p-p}, BCD mode		1.0	—	15	
Minimum Operating Frequency		f_{MIN}	—	V_{IN} = 1.0V_{p-p} (Note 1)		—	0.5	1.0	kHz
Operating Input Amplitude		V_{IN}	—	f_{IN} = 15MHz		1.0	~	V_{DD} − 0.1	V_{p-p}
Input Voltage	"H" Level	V_{IH}	—	D_0~D_{17} terminal MODE terminal		V_{DD} × 0.7	~	V_{DD}	V
	"L" Level	V_{IL}	—			0	~	V_{DD} × 0.3	
Pull-down Resistance		R_{DW}	—			32	47	62	kΩ
Output Current	"H" Level	I_{OH}	—	PSC, P_{OUT} terminal	V_{OH} = 4.0V	0.5	1.0	—	mA
	"L" Level	I_{OL}	—		V_{OL} = 1.0V	0.5	1.0	—	
Input Resistance		R_f	—	P_{IN} terminal		82	125	250	kΩ
Transfer Time	"H" Level	t_{pLH}	—	P_{IN}→PSC transfer time		—	100	200	ns
	"L" Level	t_{pHL}	—	C_L = 15pF (Note 2)		—	100	200	

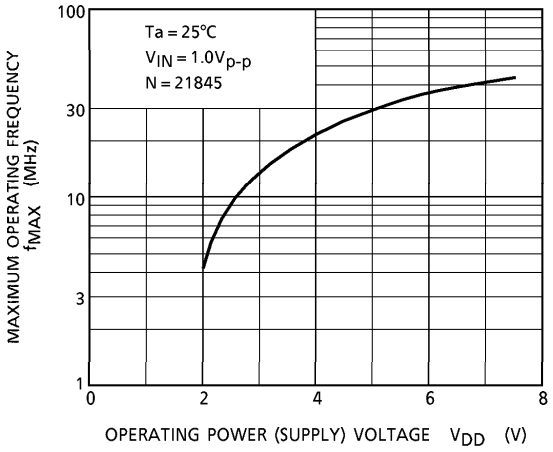
(Note 1) At the test of the minimum operating frequency, the input waveform is specified as follows.



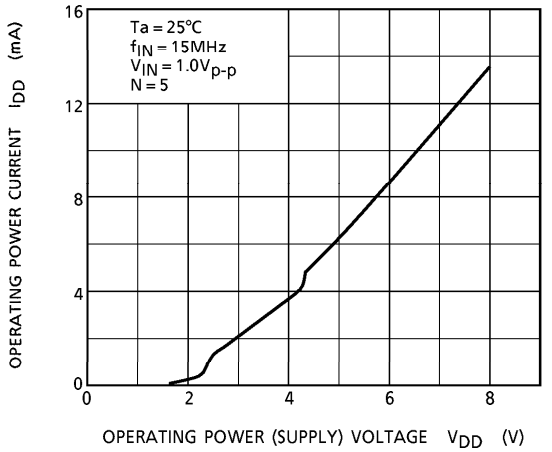
(Note 2) P_{IN}→P_{SC} transfer time



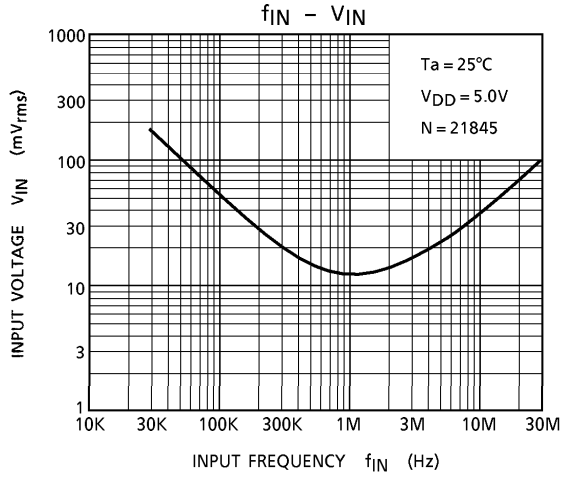
V_{DD} – f_{MAX}



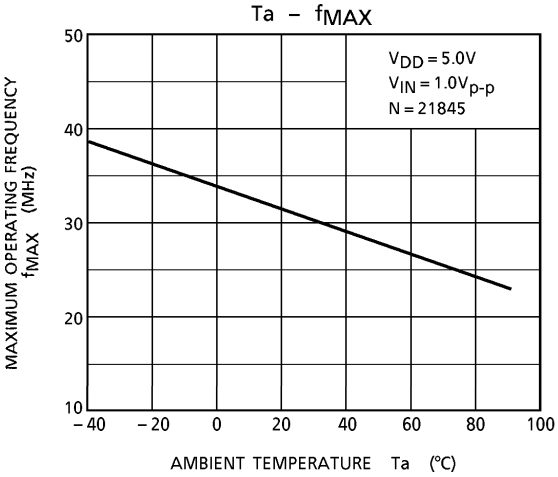
V_{DD} – I_{DD}



f_{IN} – V_{IN}

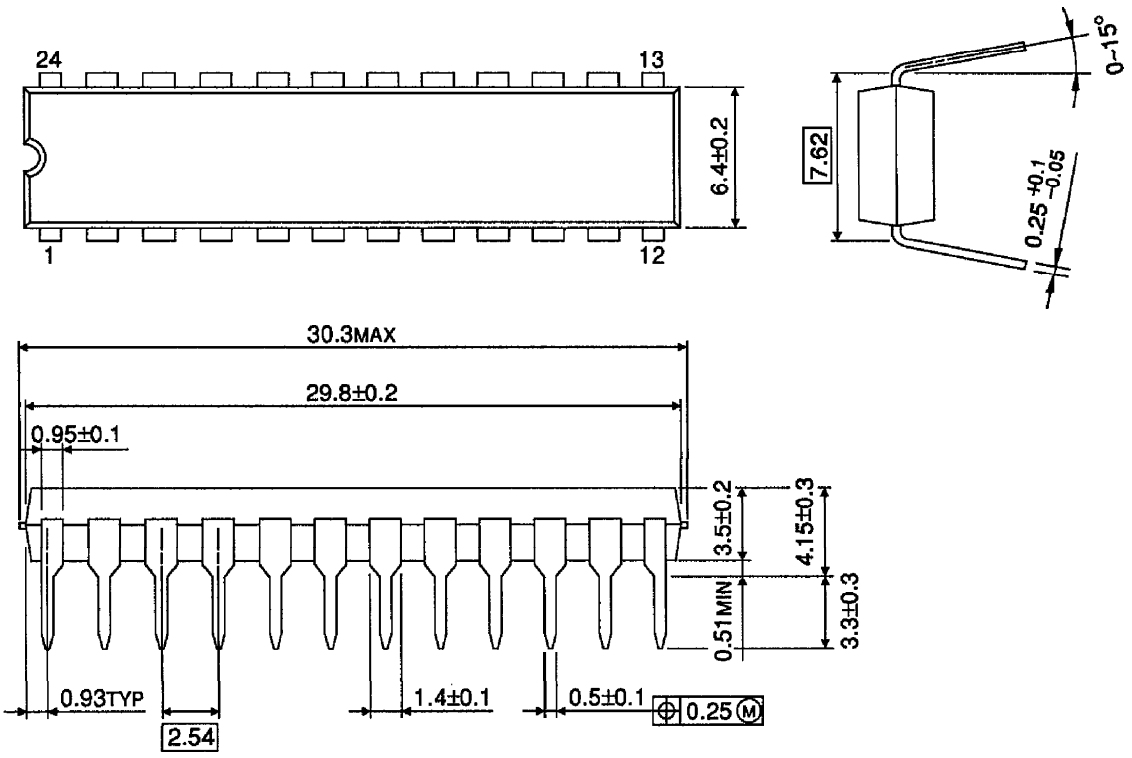


Ta – f_{MAX}



OUTLINE DRAWING

DIP24-P-300-2.54 Unit : mm

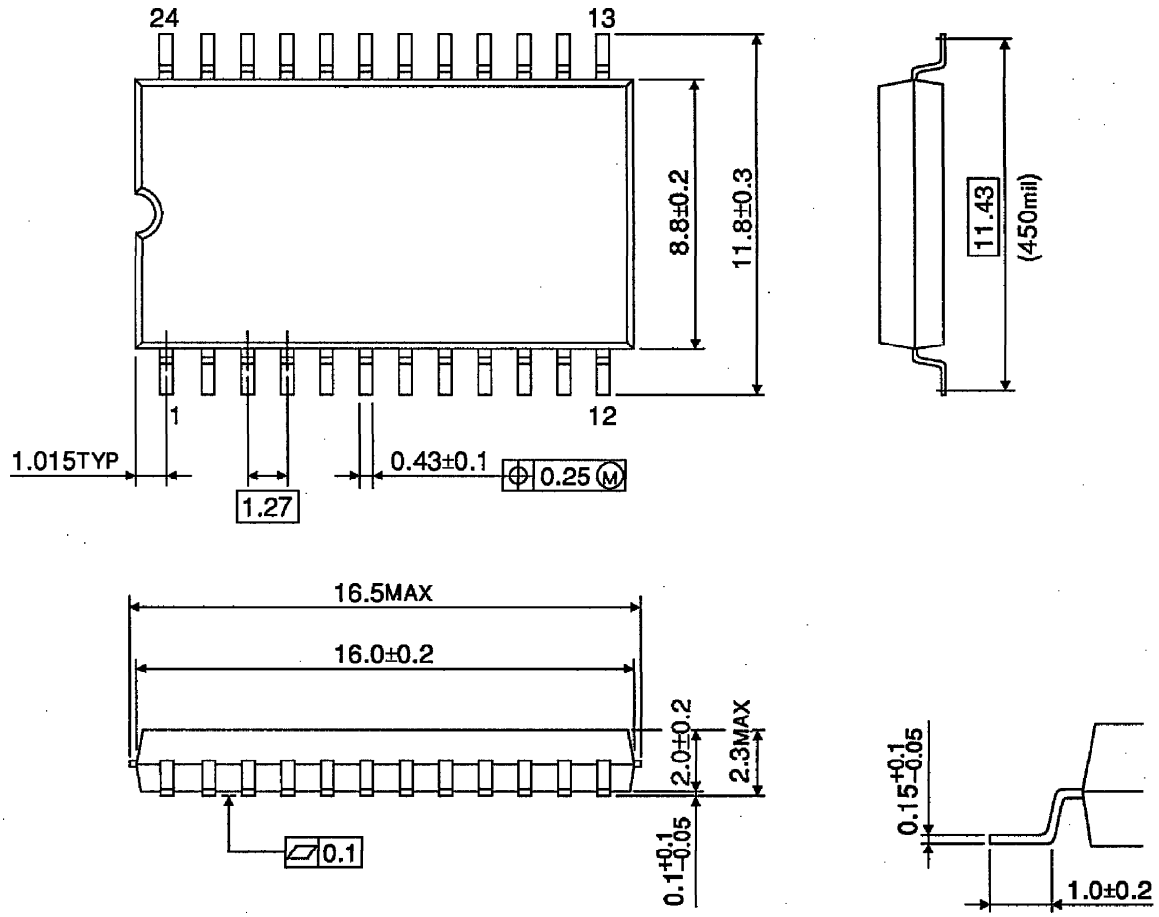


Weight : 1.2g (Typ.)

OUTLINE DRAWING

SOP24-P-450-1.27A

Unit : mm



Weight : 0.48g (Typ.)