TMS320F28388D, TMS320F28386D, TMS320F28386D-Q1
TMS320F28384D, TMS320F28384D-Q1, TMS320F28388S
TMS320F28386S, TMS320F28386S-Q1, TMS320F28384S, TMS320F28384S-Q1
SPRSP14E – MAY 2019 – REVISED JUNE 2023

TMS320F2838x Real-Time Microcontrollers With Connectivity Manager

1 Features

- Dual-core C28x architecture
  - Two TMS320C28x 32-bit CPUs
    - 200 MHz
    - IEEE 754 double-precision (64-bit) Floating-Point Unit (FPU)
    - Trigonometric Math Unit (TMU)
    - CRC engine and instructions (VCRC)
    - Fast Integer Division (FINTDIV)
  - 512KB (256KW) of flash on each CPU (ECC-protected)
  - 44KB (22KW) of local RAM on each CPU
  - 128KB (64KW) of global RAM shared between the two CPUs (parity-protected)
- Two Control Law Accelerators (CLAs)
  - 200 MHz
  - IEEE 754 single-precision floating-point
  - Executes code independently of C28x CPU
- System peripherals
  - Two External Memory Interfaces (EMIFs) with ASRAM and SDRAM support
  - Two 6-channel Direct Memory Access (DMA) controllers
  - Up to 169 General-Purpose Input/Output (GPIO) pins with input filtering
  - Expanded Peripheral Interrupt controller (ePIE)
  - Low-power mode (LPM) support
  - Dual-zone security for third-party development
  - Unique Identification (UID) number
  - Embedded Real-time Analysis and Diagnostic (ERAD)
  - Background CRC (BGCRC)
- Connectivity Manager (CM)
  - Arm® Cortex®-M4 processor
  - 125 MHz
  - 512KB of flash (ECC-protected)
  - 96KB of RAM (ECC-protected or parity-protected)
  - Advanced Encryption Standard (AES) accelerator
  - Generic CRC (GCRC)
  - 32-channel Micro Direct Memory Access (μDMA) controller
  - Universal Asynchronous Receiver/Transmitter (CM-UART)
  - Inter-integrated Circuit (CM-I2C)
  - Synchronous Serial Interface (SSI)
  - 10/100 Ethernet 1588 MII/RMII
- C28x communications peripherals
  - Fast Serial Interface (FSI) with two transmitters and eight receivers
  - Four high-speed (up to 50-MHz) SPI ports (pin-bootable)
  - Four Serial Communications Interfaces (SCI/UART) (pin-bootable)
  - Two I2C interfaces (pin-bootable)
  - Power-Management Bus (PMBus) interface
  - Two Multichannel Buffered Serial Ports (McBSPs)
- CM-C28x shared communications peripherals
  - EtherCAT® Slave Controller (ESC)
  - USB 2.0 (MAC + PHY)
  - Two Controller Area Network (CAN) modules (pin-bootable)
  - MCAN (CAN FD)
- Analog subsystem
  - Four Analog-to-Digital Converters (ADCs)
    - 16-bit mode
      - 1.1 MSPS each
      - 12 differential or 24 single-ended inputs
    - 12-bit mode
      - 3.5 MSPS each
      - 24 single-ended inputs
    - Single sample-and-hold (S/H) on each ADC
    - Hardware post-processing of conversions
  - Eight windowed comparators with 12-bit Digital-to-Analog Converter (DAC) references
  - Three 12-bit buffered DAC outputs
- Control peripherals
  - 32 Pulse Width Modulator (PWM) channels
    - High resolution on both A and B channels of 8 PWM modules (16 channels)
    - Dead-band support (on both standard and high resolution)
  - Seven Enhanced Capture (eCAP) modules
    - High-resolution Capture (HRCAP) available on two of the seven eCAP modules
  - Three Enhanced Quadrature Encoder Pulse (eQEP) modules
  - Eight Sigma-Delta Filter Module (SDFM) input channels, 2 independent filters per channel

- Configurable Logic Block (CLB)
  - Augments existing peripheral capability
  - Supports position manager solutions
- Clock and system control
  - Two internal zero-pin 10-MHz oscillators
  - On-chip crystal oscillator
  - Windowed watchdog timer module
  - Missing clock detection circuitry
  - Dual-clock Comparator (DCC)
- Hardware Built-in Self Test (HWBIST)
- 1.2-V core, 3.3-V I/O design
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 and IEC 61508 system design
  - Systematic capability up to ASIL D and SIL 3
  - Hardware capability up to ASIL B and SIL 2
- Safety-related certification
  - ISO 26262 certified up to ASIL B by TÜV SÜD
  - IEC 61508 certified up to SIL 2 by TÜV SÜD
- Package options:
  - Lead-free, green packaging
  - 337-ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT suffix]
  - 176-pin PowerPAD™ Thermally Enhanced Low-profile Quad Flatpack (HLQFP) [PTP suffix]
- Temperature options:
  - S: –40°C to 125°C junction
  - Q: –40°C to 125°C ambient (AEC Q100 qualification for automotive applications)

2 Applications

- Medium/short range radar
- HVAC large commercial motor control
- Automated sorting equipment
- CNC control
- Central inverter
- String inverter
- Inverter & motor control
- On-board (OBC) & wireless charger
- Linear motor segment controller
- Servo drive control module
- Industrial AC-DC
- Three phase UPS

3 Description

The TMS320F2838x (F2838x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- Industrial motor drives
- Motor control
- Solar inverters
- Digital power
- Electrical vehicles and transportation
- Sensing and signal processing

The real-time control subsystem is based on TI’s 32-bit C28x DSP core, which provides 200 MHz of signal-processing performance in each core for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the Trigonometric Math Unit (TMU) and VCRC (Cyclical Redundancy Check) extended instruction sets, speeding up common algorithms key to real-time control systems. Extended instruction sets enable IEEE double-precision 64-bit floating-point math. Finally, the Control Law Accelerator (CLA) enables an additional 200 MHz per core of independent processing ability.

This device also contains an independent Connectivity Manager (CM), based on the ARM Cortex-M4 processor, that runs at 125 MHz. With its own dedicated flash and SRAM, the CM allows fully independent control of the interfaces coming in and out of the F2838x, allowing maximum bandwidth for the C28x DSPs to focus on real-time control.

High-performance analog blocks are tightly integrated with the processing and control units to provide optimal real-time signal chain performance. Thirty-two frequency-independent PWMs enable control of multiple power stages, from a 3-phase inverter to advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add custom logic and potentially integrate FPGA-like functions into the C2000 real-time MCU.

For the first time on a C2000 real-time MCU, there is an EtherCAT Slave Controller, along with other industry-standard protocols like CAN FD and USB 2.0. The Fast Serial Interface (FSI) enables up to 200 Mbps of robust communications across an isolation boundary.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD28388D evaluation board and download C2000Ware.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TMS320F28388D	ZWT (nFBGA, 337)	16 mm × 16 mm
	PTP (HLQFP, 176)	24 mm × 24 mm
TMS320F28388S	ZWT (nFBGA, 337)	16 mm × 16 mm
	PTP (HLQFP, 176)	24 mm × 24 mm
TMS320F28386D	ZWT (nFBGA, 337)	16 mm × 16 mm
	PTP (HLQFP, 176)	24 mm × 24 mm
TMS320F28386S	ZWT (nFBGA, 337)	16 mm × 16 mm
	PTP (HLQFP, 176)	24 mm × 24 mm
TMS320F28384D	ZWT (nFBGA, 337)	16 mm × 16 mm
	PTP (HLQFP, 176)	24 mm × 24 mm
TMS320F28384S	ZWT (nFBGA, 337)	16 mm × 16 mm
	PTP (HLQFP, 176)	24 mm × 24 mm

(1) For more information on these devices, see Mechanical, Packaging, and Orderable Information.

3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

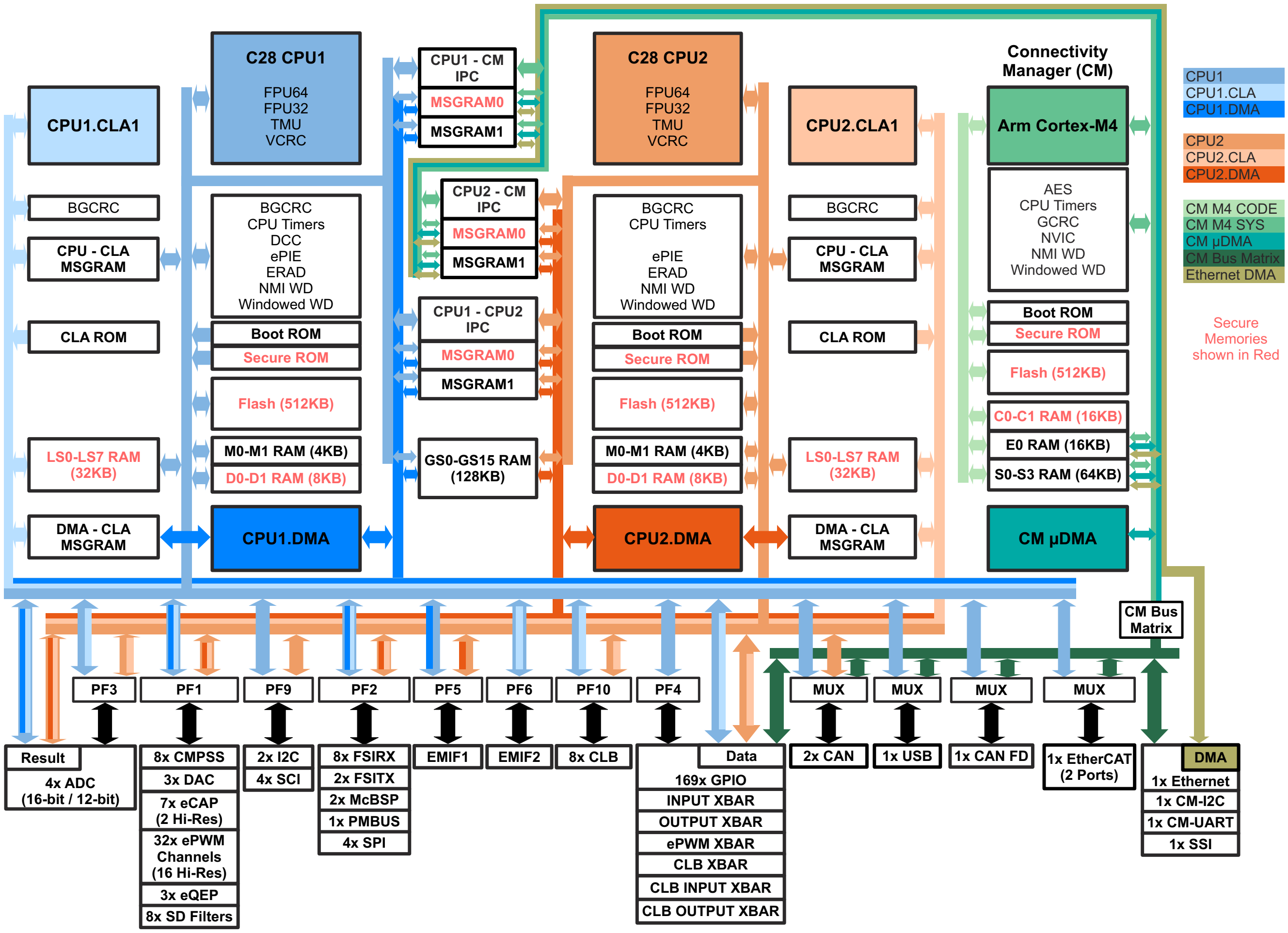

Figure 3-1. Functional Block Diagram

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4 Revision History

Changes from February 2, 2021 to June 28, 2023 Page

- **This Revision History lists the changes from SPRSP14D to SPRSP14E.** 1
- **Global:** Changed "CAN-FD" to "CAN FD"....1
- **Global:** Changed the Pin Type of ESC_TX0_ENA and ESC_TX1_ENA from "I/O" to "O"....1
- *Features* section: Added "Functional Safety-Compliant" feature and "Safety-related certification" feature. Added "Hardware Built-in Self Test (HWBIST)" feature. Deleted "MCAN (CAN FD)" feature from "Connectivity Manager (CM)" group. Added "MCAN (CAN FD)" to "CM-C28x shared communications peripherals" group...1
- *Description* section: Added reference paragraph to *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide*....2
- *Package Information* table: Changed table title from *Device Information* to *Package Information*. Updated table....2
- *Functional Block Diagram* figure: Changed blue MUX arrow of "1x CAN FD"....4
- *Device Comparison* table: Updated CAN with Flexible Data-Rate (CAN FD) by changing value to "1 **(can be assigned to CPU1 or CM)**". 8
- *Pin Attributes* table: Updated table. Changed Ball H4 on 337-ball ZWT package from "NC" to "NC1" and removed pin assignment 119 from 176-pin PTP package. Added "NC2" (Ball J18 on 337-ball ZWT package; pin 119 on 176-pin PTP package). Changed the description of TRSTn. Deleted duplicate sentence from the description of XRSn. Changed the VSS Description and pin number for the 176-pin package. 18
- *Analog Signals* table: Updated table....51
- *Digital Signals* table: Updated table....51
- *Power and Ground* table: Updated table. Changed the VSS Description and pin number for the 176-pin package.... 51
- *Test, JTAG, and Reset* table: Updated table. Changed "NC" to "NC1". Changed "337 BGA" ball number from "H4, J18" to "H4". Deleted "176 Pin" pin number 119. Added "NC2" (337 BGA ball number J18, 176 Pin number 119). Changed the description of TRSTn. Deleted duplicate sentence from the description of XRSn.... 51
- *Specifications* section: Moved "Stresses beyond those listed under *Absolute Maximum Ratings* ..." paragraph text to *Absolute Maximum Ratings* table as footnotes....90
- *Absolute Maximum Ratings* table: Added "Stresses beyond those listed under *Absolute Maximum Ratings* ..." footnote and "All voltage values are with respect to VSS, unless otherwise noted" footnote....90
- *Recommended Operating Conditions* table: Deleted $t_{VDDIO\text{-}RAMP}$.... 90
- *ESD Ratings – Commercial* table: Removed JEDEC specification JESD22-C101 from Charged-device model (CDM) description. Added CDM values for corner pins....90
- *Power Management Module (PMM)* section: Added section....100
- *Power Sequencing* section: Changed section.... 100
- *Reset Circuit* figure: Replaced 4-way tie dot.... 106
- *Reset Sources* section: Updated lead-in paragraph. Added Reset Signals table.... 106
- *Clocking System* figure: Added CLB....110
- *Internal Clock Frequencies* table: Changed MIN $f_{(INTCLK)}$ and MIN $f_{(AUXINTCLK)}$ from 10 MHz to 2 MHz. Added $f_{(CLBTILECLK)}$ and $f_{(CLBREGCLK)}$....114
- *XTAL Oscillator* section: Changed section title from *Crystal Oscillator* to *XTAL Oscillator*. Updated section. 115
- *Flash Parameters* table: Changed "N_{wec} Write/Erase Cycles" to "N_{wec} Write/Erase Cycles per sector". Added "N_{wec} Write/Erase Cycles for entire Flash (combined all sectors)" and its associated footnote. Added "$t_{retention}$ Data retention duration at T_J = 125°C" and its associated footnote.... 123
- *RAM Specifications* section: Added section.... 124
- *ROM Specifications* section: Added section....125
- *Connecting to the 14-Pin JTAG Header* figure: Added 2.2-kΩ pullup resistor on TMS....126
- *Connecting to the 20-Pin JTAG Header* figure: Added 2.2-kΩ pullup resistor on TMS....126
- *EMIF Asynchronous Memory Switching Characteristics* table: Updated MIN and MAX values of parameters 3, 10, 15, and 24 for EW = 1. Added "Maximum wait timeout condition" footnote.... 139
- *Single-Ended Input Model* section: Added "The user should analyze the ADC input setting assuming worst-case initial conditions on C_h ..." paragraph....160

5 Device Comparison

The Device Comparison table lists the features of each 2838x device.

Table 5-1. Device Comparison

<table>
<tr><th colspan="3">FEATURE(1)</th><th>28388D</th><th>28386D
28386D-Q1</th><th>28384D
28384D-Q1</th><th>28388S</th><th>28386S
28386S-Q1</th><th>28384S
28384S-Q1</th></tr>
<tr><td colspan="9">C28x Subsystem</td></tr>
<tr><td rowspan="5">C28x</td><td colspan="2">Number</td><td colspan="3">2</td><td colspan="3">1</td></tr>
<tr><td colspan="2">Frequency (MHz)</td><td colspan="6">200</td></tr>
<tr><td colspan="2">32-bit and 64-bit Floating-Point Unit (FPU)</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">VCRC</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">TMU – Type 0</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="2">CLA – Type 2</td><td colspan="2">Number</td><td colspan="3">2 (1 per CPU)</td><td colspan="3">1</td></tr>
<tr><td colspan="2">Frequency (MHz)</td><td colspan="6">200</td></tr>
<tr><td colspan="3">C28x Flash</td><td colspan="3">1MB (512KW)
[512KB (256KW) per CPU]</td><td colspan="3">512KB (256KW)</td></tr>
<tr><td rowspan="4">C28x RAM</td><td colspan="2">Dedicated RAM</td><td colspan="3">24KB (12KW)
[12KB (6KW) per CPU]</td><td colspan="3">12KB (6KW)</td></tr>
<tr><td colspan="2">Local Shared RAM</td><td colspan="3">64KB (32KW)
[32KB (16KW) per CPU]</td><td colspan="3">32KB (16KW)</td></tr>
<tr><td colspan="2">Global Shared RAM</td><td colspan="3">128KB (64KW)
(Shared between CPUs)</td><td colspan="3">128KB (64KW)</td></tr>
<tr><td colspan="2">Total RAM</td><td colspan="3">216KB (108KW)</td><td colspan="3">172KB (86KW)</td></tr>
<tr><td colspan="3">Background Cyclic Redundancy Check (BGCRC) module</td><td colspan="6">1</td></tr>
<tr><td colspan="3">Configurable Logic Block (CLB)</td><td colspan="2">8 tiles</td><td>No</td><td colspan="2">8 tiles</td><td>No</td></tr>
<tr><td colspan="3">32-bit CPU timers</td><td colspan="3">6 (3 per CPU)</td><td colspan="3">3</td></tr>
<tr><td colspan="3">6-Channel DMA – Type 0</td><td colspan="3">2 (1 per CPU)</td><td colspan="3">1</td></tr>
<tr><td colspan="3">Dual-zone Code Security Module (DCSM) for on-chip flash and RAM</td><td colspan="6">Yes</td></tr>
<tr><td colspan="3">Embedded Real-time Analysis and Diagnostic (ERAD)</td><td colspan="6">Yes</td></tr>
<tr><td rowspan="4">EMIF</td><td rowspan="2">EMIF1
(16-bit or 32-bit)</td><td>337-ball ZWT</td><td colspan="6">1</td></tr>
<tr><td>176-pin PTP</td><td colspan="6">1</td></tr>
<tr><td rowspan="2">EMIF2 (16-bit)</td><td>337-ball ZWT</td><td colspan="6">1</td></tr>
<tr><td>176-pin PTP</td><td colspan="6">–</td></tr>
<tr><td colspan="3">External interrupts</td><td colspan="6">5</td></tr>
<tr><td rowspan="4">GPIO</td><td rowspan="2">I/O pins (shared among CPU1, CPU2, and CM)</td><td>337-ball ZWT</td><td colspan="6">169</td></tr>
<tr><td>176-pin PTP</td><td colspan="6">97</td></tr>
<tr><td colspan="2">Input XBAR</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">Output XBAR</td><td colspan="6">Yes</td></tr>
</table>

Table 5-1. Device Comparison (continued)

FEATURE[(1)]			28388D	28386D 28386D-Q1	28384D 28384D-Q1	28388S	28386S 28386S-Q1	28384S 28384S-Q1
Message RAM	C28x CPU1, C28x CPU2, and Cortex-M4		24KB (4KB each direction between each of the three pairs)			8KB (4KB each direction between CPU1 and Cortex-M4)		
	C28x CPUs and CLAs		1KB (256 bytes each direction between each CPU and CLA pair)			512 bytes (256 bytes each direction between CPU and CLA)		
	DMAs and CLAs		1KB (256 bytes each direction between each DMA and CLA pair)			512 bytes (256 bytes each direction between DMA and CLA)		
Nonmaskable Interrupt Watchdog (NMIWD) timers			2 (1 per CPU)			1		
Watchdog (WD) timers			2 (1 per CPU)			1		
Connectivity Manager (CM) Subsystem								
Arm Cortex-M4			125 MHz					
Flash on Cortex-M4			512KB					
RAM on Cortex-M4			96KB					
Advanced Encryption Standard (AES) Accelerator			1					
CPU timers			3					
Generic Cyclic Redundancy Check (GCRC) module			1					
Memory Protection Unit (MPU) for Cortex-M4, µDMA, and Ethernet DMA			3					
CM Nonmaskable Interrupt (CMNMI) Module			1					
Trace Port Interface Unit (TPIU)			1					
µDMA			1					
Watchdog (WD) timer			1					
C28x Analog Peripherals								
Analog-to-Digital Converter (ADC) (configurable to 12-bit or 16-bit)			4					
ADC 16-bit mode	MSPS		1.1					
	Conversion Time (ns)[(2)]		915					
	Input channels (single-ended mode)	337-ball ZWT	24					
		176-pin PTP	20					
	Input channels (differential mode)	337-ball ZWT	12					
		176-pin PTP	9					
ADC 12-bit mode	MSPS		3.5					
	Conversion Time (ns)[(2)]		280					
	Input channels (single-ended)	337-ball ZWT	24					
		176-pin PTP	20					
Temperature sensor			1					

Table 5-1. Device Comparison (continued)

<table>
<tr><th colspan="2">FEATURE[(1)]</th><th>28388D</th><th>28386D
28386D-Q1</th><th>28384D
28384D-Q1</th><th>28388S</th><th>28386S
28386S-Q1</th><th>28384S
28384S-Q1</th></tr>
<tr><td colspan="2">Comparator subsystem (CMPSS)
(each CMPSS has two comparators and two internal DACs)</td><td colspan="6">8</td></tr>
<tr><td colspan="2">Buffered Digital-to-Analog Converter (DAC)</td><td colspan="6">3</td></tr>
<tr><td colspan="8">C28x Control Peripherals</td></tr>
<tr><td rowspan="2">eCAP/HRCAP – Type 2</td><td>Total inputs</td><td colspan="6">7</td></tr>
<tr><td>Channels with high-resolution capability</td><td colspan="6">2 (eCAP6 and eCAP7)</td></tr>
<tr><td rowspan="2">ePWM/HRPWM – Type 4</td><td>Total channels</td><td colspan="6">32</td></tr>
<tr><td>Channels with high-resolution capability</td><td colspan="6">16 (ePWM1–ePWM8)</td></tr>
<tr><td colspan="2">ePWM XBAR</td><td colspan="6">Yes</td></tr>
<tr><td colspan="2">eQEP modules – Type 2</td><td colspan="6">3</td></tr>
<tr><td colspan="2">SDFM channels – Type 2</td><td colspan="6">8</td></tr>
<tr><td colspan="8">C28x Communications Peripherals</td></tr>
<tr><td colspan="2">Fast Serial Interface (FSI) RX - Type 1</td><td colspan="6">8</td></tr>
<tr><td colspan="2">Fast Serial Interface (FSI) TX - Type 1</td><td colspan="6">2</td></tr>
<tr><td colspan="2">Inter-Integrated Circuit (I2C) – Type 0</td><td colspan="6">2</td></tr>
<tr><td colspan="2">Multichannel Buffered Serial Port (McBSP) – Type 1</td><td colspan="6">2</td></tr>
<tr><td colspan="2">Power Management Bus (PMBus) – Type 0</td><td colspan="6">1</td></tr>
<tr><td colspan="2">Serial Communications Interface (SCI) – Type 0
(UART-compatible)</td><td colspan="6">4</td></tr>
<tr><td colspan="2">Serial Peripheral Interface (SPI) – Type 2</td><td colspan="6">4</td></tr>
<tr><td colspan="8">Connectivity Manager (CM) Communications Peripherals</td></tr>
<tr><td colspan="2">Controller Area Network (CAN) 2.0B – Type 0[(3)]</td><td colspan="3">2
(can be assigned to
CPU1, CPU2, or CM)</td><td colspan="3">2
(can be assigned to CPU1 or CM)</td></tr>
<tr><td colspan="2">CAN with Flexible Data-Rate (CAN FD)</td><td colspan="6">1 (can be assigned to CPU1 or CM)</td></tr>
<tr><td colspan="2">Ethernet for Control Automation Technology (EtherCAT)</td><td>1
(can be assigned to CPU1 or CM)</td><td colspan="2">–</td><td>1
(can be assigned to CPU1 or CM)</td><td colspan="2">–</td></tr>
<tr><td colspan="2">Ethernet Media Access Controller (EMAC)</td><td colspan="6">1</td></tr>
<tr><td colspan="2">CM Inter-Integrated Circuit (CM-I2C)</td><td colspan="6">1</td></tr>
<tr><td colspan="2">Synchronous Serial Interface (SSI)</td><td colspan="6">1</td></tr>
<tr><td colspan="2">CM Universal Asynchronous Receiver-Transmitter (CM-UART)</td><td colspan="6">1</td></tr>
<tr><td colspan="2">Universal Serial Bus (USB) – Type 0</td><td colspan="6">1
(shared between CPU1 and CM)</td></tr>
</table>

Table 5-1. Device Comparison (continued)

FEATURE[(1)]			28388D	28386D 28386D-Q1	28384D 28384D-Q1	28388S	28386S 28386S-Q1	28384S 28384S-Q1
Temperature and Qualification								
Temperature Options	S: –40°C to 125°C Junction Temperature (T_J)	337-ball ZWT	28388D, 28386D, 28384D 28388S, 28386S, 28384S					
		176-pin PTP						
	Q: –40°C to 125°C[(4)] Ambient Temperature (T_A)	337-ball ZWT	–	28386D-Q1	28384D-Q1	–	–	–
		176-pin PTP	–	28386D-Q1	28384D-Q1	–	28386S-Q1	28384S-Q1

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the *C2000 Real-Time Control Peripherals Reference Guide*.
(2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
(3) The CAN module uses the IP known as *DCAN*. This document uses the names *CAN* and *DCAN* interchangeably to reference this peripheral.
(4) The letter Q refers to AEC Q100 qualification for automotive applications.

5.1 Related Products

TMS320F2837xD Real-Time Dual-Core Microcontrollers

The F2837xD series sets a new standard for performance with dual subsystems. Each subsystem consists of a C28x CPU and a parallel control law accelerator (CLA), each running at 200 MHz. Enhancing performance are TMU and VCU accelerators. New capabilities include multiple 16-bit/12-bit mode ADCs, DAC, Sigma-Delta filters, USB, configurable logic block (CLB), on-chip oscillators, and enhanced versions of all peripherals. The F2837xD is available with up to 1MB of Flash. It is available in a 176-pin QFP or 337-pin BGA package.

TMS320F2837xS Real-Time Microcontrollers

The F2837xS series is a pin-to-pin compatible version of F2837xD but with only one C28x-CPU-and-CLA subsystem enabled. It is also available in a 100-pin QFP to enable compatibility with the TMS320F2807x series.

6 Terminal Configuration and Functions

6.1 Pin Diagrams

Figure 6-1 shows the terminal assignments on the 337-ball ZWT New Fine Pitch Ball Grid Array (nFBGA). Figure 6-2 to Figure 6-5 show the terminal assignments on the 337-ball ZWT nFBGA in quadrants.

Figure 6-6 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
W	VSSA	ADCINB1 ,DACOUTC	ADCINB3 ,CMPIN3N	ADCINB5	VREFHIB	VREFLOD	VSS	VDDIO	GPIO128	GPIO116	GPIO29	FLT1	TDI	TMS	TDO	GPIO121	GPIO39	GPIO132	VSS
V	VREFHIA	ADCINB0 ,VDAC	ADCINB2 ,CMPIN3P	ADCINB4	VREFHID	VREFLOB	VSSA	GPIO124	GPIO127	GPIO131	GPIO28	GPIO115	FLT2	TRSTn	TCK	GPIO36	GPIO40	GPIO134	VDDIO
U	ADCINA0 ,DACOUTA	ADCINA2 ,CMPIN1P	ADCINA4 ,CMPIN2P	ADCIN15 ,CMPIN4N	ADCIND1 ,CMPIN7N	ADCIND3 ,CMPIN8N	ADCIND5	GPIO123	GPIO126	GPIO130	GPIO31	GPIO117	GPIO32	GPIO34	GPIO120	GPIO37	GPIO41	GPIO135	ERRORSTS
T	ADCINA1 ,DACOUTB	ADCINA3 ,CMPIN1N	ADCINA5 ,CMPIN2N	ADCIN14 ,CMPIN4P	ADCIND0 ,CMPIN7P	ADCIND2 ,CMPIN8P	ADCIND4	GPIO122	GPIO125	GPIO129	GPIO30	GPIO118	GPIO33	GPIO35	GPIO119	GPIO38	GPIO136	GPIO137	GPIO138
R	VREFHIC	VREFLOA	ADCINC2 ,CMPIN6P	ADCINC4 ,CMPIN5P	VSSA	VDDA	VSS	VSS	VDDIO	VDD	VDD3VFL	VDD3VFL	VDD	VSS	VSS	GPIO48	GPIO49	GPIO50	GPIO51
P	VSSA	VREFLOC	ADCINC3 ,CMPIN6N	ADCINC5 ,CMPIN5N	VSSA	VDDA	VSS	VSS	VDDIO	VDD	VSS	VSS	VDD	VSS	VSS	GPIO52	GPIO53	GPIO54	GPIO55
N	VSS	GPIO109	GPIO114	GPIO113	VSS	VSS								VDDIO	VDDIO	GPIO56	GPIO58	GPIO57	GPIO139
M	VDDIO	GPIO110	GPIO112	GPIO111	VDDIO	VDDIO		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO59	GPIO60	GPIO141	GPIO140
L	GPIO27	GPIO106	GPIO107	GPIO108	VSS	VSS		VSS	VSS	VSS	VSS	VSS		VDDIO	VDDIO	GPIO61	GPIO64	VSS	GPIO142
K	GPIO26	GPIO25	GPIO24	GPIO23	VDD	VDD		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO65	GPIO66	GPIO44	GPIO45
J	GPIO103	GPIO104	GPIO105	GPIO22	VSS	VSS		VSS	VSS	VSS	VSS	VSS		VDD	VDD	GPIO63	GPIO62	NC	X2
H	GPIO100	GPIO101	GPIO102	NC	VDDIO	VDDIO		VSS	VSS	VSS	VSS	VSS		VSS	VSS	VDDOSC	VDDOSC	VSSOSC	VSSOSC
G	GPIO99	GPIO8	GPIO9	VDDIO	VDDIO	VDDIO								VDD	VDD	VSS	VSS	GPIO133	X1
F	GPIO98	GPIO20	GPIO21	VDDIO	VSS	VSS	VDDIO	VSS	VDD	VDDIO	VDD	VSS	VDDIO	VSS	VSS	VDDIO	GPIO144	GPIO143	XRSn
E	GPIO16	GPIO17	GPIO18	GPIO19	VSS	VSS	VDDIO	VSS	VDD	VDDIO	VDD	VSS	VDDIO	VSS	VSS	VDDIO	GPIO145	GPIO47	GPIO46
D	GPIO13	GPIO14	GPIO15	GPIO168	GPIO166	GPIO89	GPIO5	GPIO1	GPIO162	GPIO159	GPIO87	GPIO156	GPIO152	GPIO148	GPIO80	GPIO75	GPIO147	GPIO146	GPIO42
C	GPIO11	GPIO12	GPIO96	GPIO167	GPIO165	GPIO88	GPIO4	GPIO0	GPIO161	GPIO158	GPIO86	GPIO155	GPIO151	GPIO83	GPIO79	GPIO76	GPIO74	GPIO68	GPIO43
B	VDDIO	GPIO10	GPIO95	GPIO93	GPIO91	GPIO7	GPIO3	GPIO164	GPIO160	GPIO157	GPIO85	GPIO154	GPIO150	GPIO82	GPIO78	GPIO72	GPIO71	GPIO69	GPIO67
A	VSS	GPIO97	GPIO94	GPIO92	GPIO90	GPIO6	GPIO2	GPIO163	VDDIO	VSS	GPIO84	GPIO153	GPIO149	GPIO81	GPIO77	GPIO73	GPIO70	VDDIO	VSS

Not to scale

A. Only the GPIO function is shown on GPIO terminals. See the Pin Attributes table for the complete, muxed signal name.

Figure 6-1. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View)

	1	2	3	4	5	6	7	8	9	10
W	VSSA	ADCINB1 ,DACOUTC	ADCINB3 ,CMPIN3N	ADCINB5	VREFHIB	VREFLOD	VSS	VDDIO	GPIO128	GPIO116
V	VREFHIA	ADCINB0 ,VDAC	ADCINB2 ,CMPIN3P	ADCINB4	VREFHID	VREFLOB	VSSA	GPIO124	GPIO127	GPIO131
U	ADCINA0 ,DACOUTA	ADCINA2 ,CMPIN1P	ADCINA4 ,CMPIN2P	ADCIN15 ,CMPIN4N	ADCIND1 ,CMPIN7N	ADCIND3 ,CMPIN8N	ADCIND5	GPIO123	GPIO126	GPIO130
T	ADCINA1 ,DACOUTB	ADCINA3 ,CMPIN1N	ADCINA5 ,CMPIN2N	ADCIN14 ,CMPIN4P	ADCIND0 ,CMPIN7P	ADCIND2 ,CMPIN8P	ADCIND4	GPIO122	GPIO125	GPIO129
R	VREFHIC	VREFLOA	ADCINC2 ,CMPIN6P	ADCINC4 ,CMPIN5P	VSSA	VDDA	VSS	VSS	VDDIO	VDD
P	VSSA	VREFLOC	ADCINC3 ,CMPIN6N	ADCINC5 ,CMPIN5N	VSSA	VDDA	VSS	VSS	VDDIO	VDD
N	VSS	GPIO109	GPIO114	GPIO113	VSS	VSS				
M	VDDIO	GPIO110	GPIO112	GPIO111	VDDIO	VDDIO		VSS	VSS	VSS
L	GPIO27	GPIO106	GPIO107	GPIO108	VSS	VSS		VSS	VSS	VSS
K	GPIO26	GPIO25	GPIO24	GPIO23	VDD	VDD		VSS	VSS	VSS

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See the Pin Attributes table for the complete, muxed signal name.

Figure 6-2. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 1]

	11	12	13	14	15	16	17	18	19
W	GPIO29	FLT1	TDI	TMS	TDO	GPIO121	GPIO39	GPIO132	VSS
V	GPIO28	GPIO115	FLT2	TRSTn	TCK	GPIO36	GPIO40	GPIO134	VDDIO
U	GPIO31	GPIO117	GPIO32	GPIO34	GPIO120	GPIO37	GPIO41	GPIO135	ERRORSTS
T	GPIO30	GPIO118	GPIO33	GPIO35	GPIO119	GPIO38	GPIO136	GPIO137	GPIO138
R	VDD3VFL	VDD3VFL	VDD	VSS	VSS	GPIO48	GPIO49	GPIO50	GPIO51
P	VSS	VSS	VDD	VSS	VSS	GPIO52	GPIO53	GPIO54	GPIO55
N				VDDIO	VDDIO	GPIO56	GPIO58	GPIO57	GPIO139
M	VSS	VSS		VSS	VSS	GPIO59	GPIO60	GPIO141	GPIO140
L	VSS	VSS		VDDIO	VDDIO	GPIO61	GPIO64	VSS	GPIO142
K	VSS	VSS		VSS	VSS	GPIO65	GPIO66	GPIO44	GPIO45

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See the Pin Attributes table for the complete, muxed signal name.

Figure 6-3. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 2]

	1	2	3	4	5	6	7	8	9	10
J	GPIO103	GPIO104	GPIO105	GPIO22	VSS	VSS		VSS	VSS	VSS
H	GPIO100	GPIO101	GPIO102	NC	VDDIO	VDDIO		VSS	VSS	VSS
G	GPIO99	GPIO8	GPIO9	VDDIO	VDDIO	VDDIO				
F	GPIO98	GPIO20	GPIO21	VDDIO	VSS	VSS	VDDIO	VSS	VDD	VDDIO
E	GPIO16	GPIO17	GPIO18	GPIO19	VSS	VSS	VDDIO	VSS	VDD	VDDIO
D	GPIO13	GPIO14	GPIO15	GPIO168	GPIO166	GPIO89	GPIO5	GPIO1	GPIO162	GPIO159
C	GPIO11	GPIO12	GPIO96	GPIO167	GPIO165	GPIO88	GPIO4	GPIO0	GPIO161	GPIO158
B	VDDIO	GPIO10	GPIO95	GPIO93	GPIO91	GPIO7	GPIO3	GPIO164	GPIO160	GPIO157
A	VSS	GPIO97	GPIO94	GPIO92	GPIO90	GPIO6	GPIO2	GPIO163	VDDIO	VSS

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See the Pin Attributes table for the complete, muxed signal name.

Figure 6-4. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 3]

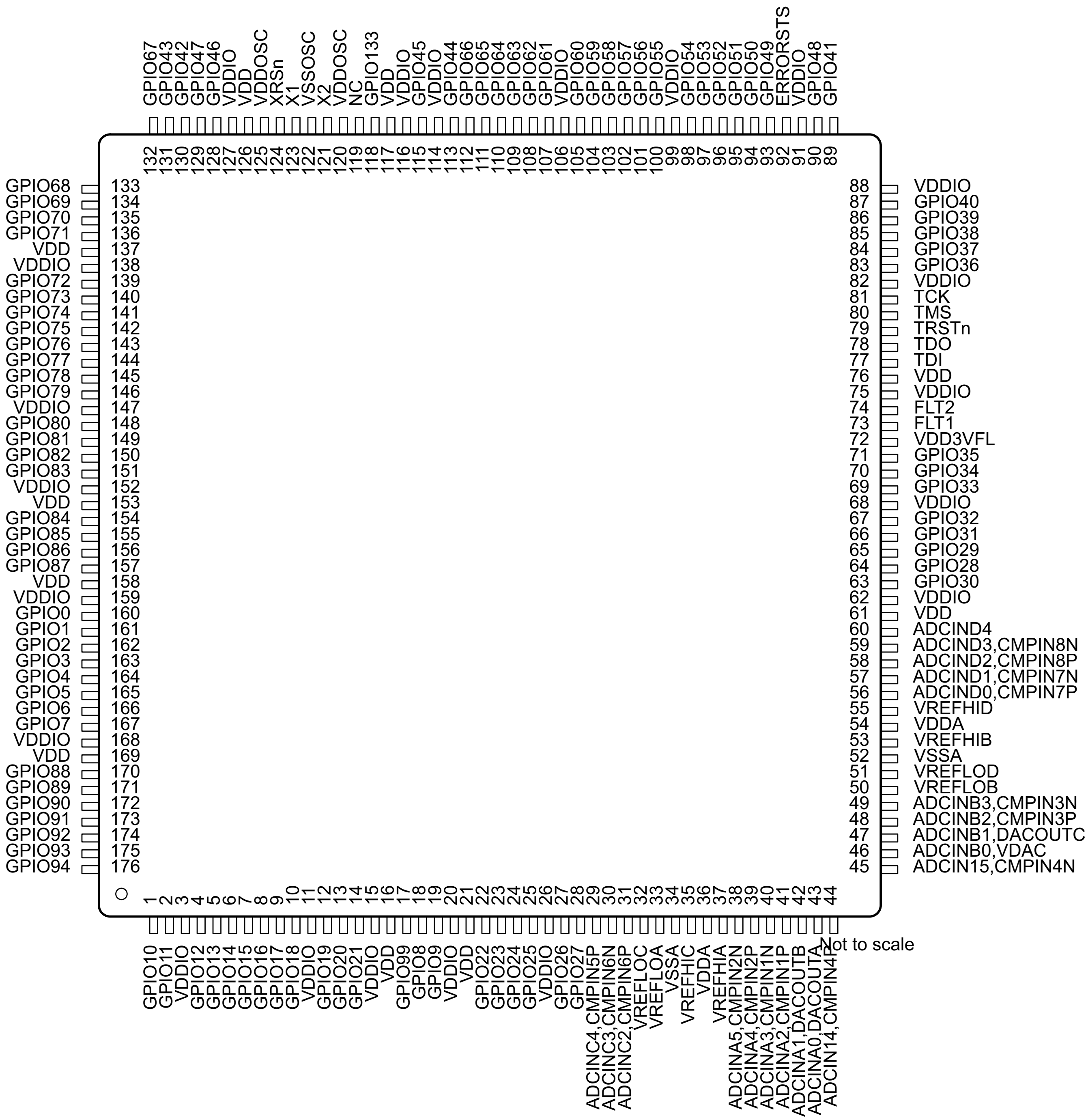
	11	12	13	14	15	16	17	18	19
J	VSS	VSS		VDD	VDD	GPIO63	GPIO62	NC	X2
H	VSS	VSS		VSS	VSS	VDDOSC	VDDOSC	VSSOSC	VSSOSC
G				VDD	VDD	VSS	VSS	GPIO133	X1
F	VDD	VSS	VDDIO	VSS	VSS	VDDIO	GPIO144	GPIO143	XRSn
E	VDD	VSS	VDDIO	VSS	VSS	VDDIO	GPIO145	GPIO47	GPIO46
D	GPIO87	GPIO156	GPIO152	GPIO148	GPIO80	GPIO75	GPIO147	GPIO146	GPIO42
C	GPIO86	GPIO155	GPIO151	GPIO83	GPIO79	GPIO76	GPIO74	GPIO68	GPIO43
B	GPIO85	GPIO154	GPIO150	GPIO82	GPIO78	GPIO72	GPIO71	GPIO69	GPIO67
A	GPIO84	GPIO153	GPIO149	GPIO81	GPIO77	GPIO73	GPIO70	VDDIO	VSS

Not to scale

1	2
3	4

A. Only the GPIO function is shown on GPIO terminals. See the Pin Attributes table for the complete, muxed signal name.

Figure 6-5. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant 4]



A. Only the GPIO function is shown on GPIO terminals. See the Pin Attributes table for the complete, muxed signal name.

Figure 6-6. 176-Pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack (Top View)

6.2 Pin Attributes

Table 6-1. Pin Attributes

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
ANALOG					
ADCIN14		T4	44	I	Input 14 to all ADCs. This pin can be used as a general purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference
CMPIN4P				I	Comparator 4 positive input
ADCIN15		U4	45	I	Input 15 to all ADCs. This pin can be used as a general purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference
CMPIN4N				I	Comparator 4 negative input
ADCINA0		U1	43	I	ADC-A Input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTA				O	Buffered DAC-A Output.
ADCINA1		T1	42	I	ADC-A Input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTB				O	Buffered DAC-B Output.
ADCINA2		U2	41	I	ADC-A Input 2
CMPIN1P				I	Comparator 1 positive input
ADCINA3		T2	40	I	ADC-A Input 3
CMPIN1N				I	Comparator 1 negative input
ADCINA4		U3	39	I	ADC-A Input 4
CMPIN2P				I	Comparator 2 positive input
ADCINA5		T3	38	I	ADC-A Input 5
CMPIN2N				I	Comparator 2 negative input
ADCINB0		V2	46	I	ADC-B Input 0. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-μF capacitor on this pin.
VDAC				I	Optional external reference voltage for on-chip DACs.
ADCINB1		W2	47	I	ADC-B Input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTC				O	Buffered DAC-C Output.
ADCINB2		V3	48	I	ADC-B Input 2
CMPIN3P				I	Comparator 3 positive input
ADCINB3		W3	49	I	ADC-B Input 3
CMPIN3N				I	Comparator 3 negative input
ADCINB4		V4		I	ADC-B Input 4
ADCINB5		W4		I	ADC-B Input 5
ADCINC2		R3	31	I	ADC-C Input 2
CMPIN6P				I	Comparator 6 positive input
ADCINC3		P3	30	I	ADC-C Input 3
CMPIN6N				I	Comparator 6 negative input

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
ADCINC4		R4	29	I	ADC-C Input 4
CMPIN5P				I	Comparator 5 positive input
ADCINC5		P4		I	ADC-C Input 5
CMPIN5N				I	Comparator 5 negative input
ADCIND0		T5	56	I	ADC-D Input 0
CMPIN7P				I	Comparator 7 positive input
ADCIND1		U5	57	I	ADC-D Input 1
CMPIN7N				I	Comparator 7 negative input
ADCIND2		T6	58	I	ADC-D Input 2
CMPIN8P				I	Comparator 8 positive input
ADCIND3		U6	59	I	ADC-D Input 3
CMPIN8N				I	Comparator 8 negative input
ADCIND4		T7	60	I	ADC-D Input 4
ADCIND5		U7		I	ADC-D Input 5
VREFHIA		V1	37	I	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. NOTE: Do not load this pin externally
VREFHIB		W5	53	I	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. NOTE: Do not load this pin externally
VREFHIC		R1	35	I	ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. NOTE: Do not load this pin externally
VREFHID		V5	55	I	ADC-D high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHID and VREFLOD pins. NOTE: Do not load this pin externally
VREFLOA		R2	33	I	ADC-A Low Reference
VREFLOB		V6	50	I	ADC-B Low Reference
VREFLOC		P2	32	I	ADC-C Low Reference
VREFLOD		W6	51	I	ADC-D Low Reference

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO					
GPIO0	0, 4, 8, 12	C8	160	I/O	General-Purpose Input Output 0
EPWM1A	1			O	ePWM-1 Output A (High-res available on ePWM1-8)
I2CA_SDA	6			I/OD	I2C-A Open-Drain Bidirectional Data
CM-I2CA_SDA	9			I/OD	CM-I2C-A Open-Drain Bidirectional Data
ESC_GPI0	10			I	EtherCAT General-Purpose Input 0
FSITXA_D0	13			O	FSITX-A Data Output 0
GPIO1	0, 4, 8, 12	D8	161	I/O	General-Purpose Input Output 1
EPWM1B	1			O	ePWM-1 Output B (High-res available on ePWM1-8)
MFSRB	3			I	McBSP-B Receive Frame Sync
I2CA_SCL	6			I/OD	I2C-A Open-Drain Bidirectional Clock
CM-I2CA_SCL	9			I/OD	CM-I2C-A Open-Drain Bidirectional Clock
ESC_GPI1	10			I	EtherCAT General-Purpose Input 1
FSITXA_D1	13			O	FSITX-A Data Output 1
GPIO2	0, 4, 8, 12	A7	162	I/O	General-Purpose Input Output 2
EPWM2A	1			O	ePWM-2 Output A (High-res available on ePWM1-8)
OUTPUTXBAR1	5			O	Output X-BAR Output 1
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
ESC_GPI2	10			I	EtherCAT General-Purpose Input 2
FSITXA_CLK	13			O	FSITX-A Output Clock
GPIO3	0, 4, 8, 12	B7	163	I/O	General-Purpose Input Output 3
EPWM2B	1			O	ePWM-2 Output B (High-res available on ePWM1-8)
OUTPUTXBAR2	2, 5			O	Output X-BAR Output 2
MCLKRB	3			I	McBSP-B Receive Clock
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
ESC_GPI3	10			I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13			I	FSIRX-A Data Input 0
GPIO4	0, 4, 8, 12	C7	164	I/O	General-Purpose Input Output 4
EPWM3A	1			O	ePWM-3 Output A (High-res available on ePWM1-8)
OUTPUTXBAR3	5			O	Output X-BAR Output 3
CANA_TX	6			O	CAN-A Transmit
MCAN_TX	9			O	CAN/CAN FD Transmit
ESC_GPI4	10			I	EtherCAT General-Purpose Input 4
FSIRXA_D1	13			I	FSIRX-A Data Input 1
GPIO5	0, 4, 8, 12	D7	165	I/O	General-Purpose Input Output 5
EPWM3B	1			O	ePWM-3 Output B (High-res available on ePWM1-8)
MFSRA	2			I	McBSP-A Receive Frame Sync
OUTPUTXBAR3	3			O	Output X-BAR Output 3
CANA_RX	6			I	CAN-A Receive
MCAN_RX	9			I	CAN/CAN FD Receive
ESC_GPI5	10			I	EtherCAT General-Purpose Input 5
FSIRXA_CLK	13			I	FSIRX-A Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO6	0, 4, 8, 12	A6	166	I/O	General-Purpose Input Output 6
EPWM4A	1			O	ePWM-4 Output A (High-res available on ePWM1-8)
OUTPUTXBAR4	2			O	Output X-BAR Output 4
EXTSYNCOUT	3			O	External ePWM Synchronization Pulse
EQEP3_A	5			I	eQEP-3 Input A
CANB_TX	6			O	CAN-B Transmit
ESC_GPI6	10			I	EtherCAT General-Purpose Input 6
FSITXB_D0	13			O	FSITX-B Data Output 0
GPIO7	0, 4, 8, 12	B6	167	I/O	General-Purpose Input Output 7
EPWM4B	1			O	ePWM-4 Output B (High-res available on ePWM1-8)
MCLKRA	2			I	McBSP-A Receive Clock
OUTPUTXBAR5	3			O	Output X-BAR Output 5
EQEP3_B	5			I	eQEP-3 Input B
CANB_RX	6			I	CAN-B Receive
ESC_GPI7	10			I	EtherCAT General-Purpose Input 7
FSITXB_D1	13			O	FSITX-B Data Output 1
GPIO8	0, 4, 8, 12	G2	18	I/O	General-Purpose Input Output 8
EPWM5A	1			O	ePWM-5 Output A (High-res available on ePWM1-8)
CANB_TX	2			O	CAN-B Transmit
ADCSOCAO	3			O	ADC Start of Conversion A Output for External ADC (from ePWM modules)
EQEP3_STROBE	5			I/O	eQEP-3 Strobe
SCIA_TX	6			O	SCI-A Transmit Data
MCAN_TX	9			O	CAN/CAN FD Transmit
ESC_GPO0	10			O	EtherCAT General-Purpose Output 0
FSITXB_CLK	13			O	FSITX-B Output Clock
FSITXA_D1	14			O	FSITX-A Data Output 1
FSIRXA_D0	15			I	FSIRX-A Data Input 0
GPIO9	0, 4, 8, 12	G3	19	I/O	General-Purpose Input Output 9
EPWM5B	1			O	ePWM-5 Output B (High-res available on ePWM1-8)
SCIB_TX	2			O	SCI-B Transmit Data
OUTPUTXBAR6	3			O	Output X-BAR Output 6
EQEP3_INDEX	5			I/O	eQEP-3 Index
SCIA_RX	6			I	SCI-A Receive Data
ESC_GPO1	10			O	EtherCAT General-Purpose Output 1
FSIRXB_D0	13			I	FSIRX-B Data Input 0
FSITXA_D0	14			O	FSITX-A Data Output 0
FSIRXA_CLK	15			I	FSIRX-A Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO10	0, 4, 8, 12	B2	1	I/O	General-Purpose Input Output 10
EPWM6A	1			O	ePWM-6 Output A (High-res available on ePWM1-8)
CANB_RX	2			I	CAN-B Receive
ADCSOCBO	3			O	ADC Start of Conversion B Output for External ADC (from ePWM modules)
EQEP1_A	5			I	eQEP-1 Input A
SCIB_TX	6			O	SCI-B Transmit Data
MCAN_RX	9			I	CAN/CAN FD Receive
ESC_GPO2	10			O	EtherCAT General-Purpose Output 2
FSIRXB_D1	13			I	FSIRX-B Data Input 1
FSITXA_CLK	14			O	FSITX-A Output Clock
FSIRXA_D1	15			I	FSIRX-A Data Input 1
GPIO11	0, 4, 8, 12	C1	2	I/O	General-Purpose Input Output 11
EPWM6B	1			O	ePWM-6 Output B (High-res available on ePWM1-8)
SCIB_RX	2, 6			I	SCI-B Receive Data
OUTPUTXBAR7	3			O	Output X-BAR Output 7
EQEP1_B	5			I	eQEP-1 Input B
ESC_GPO3	10			O	EtherCAT General-Purpose Output 3
FSIRXB_CLK	13			I	FSIRX-B Input Clock
FSIRXA_D1	14			I	FSIRX-A Data Input 1
GPIO12	0, 4, 8, 12	C2	4	I/O	General-Purpose Input Output 12
EPWM7A	1			O	ePWM-7 Output A (High-res available on ePWM1-8)
CANB_TX	2			O	CAN-B Transmit
MDXB	3			O	McBSP-B Transmit Serial Data
EQEP1_STROBE	5			I/O	eQEP-1 Strobe
SCIC_TX	6			O	SCI-C Transmit Data
ESC_GPO4	10			O	EtherCAT General-Purpose Output 4
FSIRXC_D0	13			I	FSIRX-C Data Input 0
FSIRXA_D0	14			I	FSIRX-A Data Input 0
GPIO13	0, 4, 8, 12	D1	5	I/O	General-Purpose Input Output 13
EPWM7B	1			O	ePWM-7 Output B (High-res available on ePWM1-8)
CANB_RX	2			I	CAN-B Receive
MDRB	3			I	McBSP-B Receive Serial Data
EQEP1_INDEX	5			I/O	eQEP-1 Index
SCIC_RX	6			I	SCI-C Receive Data
ESC_GPO5	10			O	EtherCAT General-Purpose Output 5
FSIRXC_D1	13			I	FSIRX-C Data Input 1
FSIRXA_CLK	14			I	FSIRX-A Input Clock
GPIO14	0, 4, 8, 12	D2	6	I/O	General-Purpose Input Output 14
EPWM8A	1			O	ePWM-8 Output A (High-res available on ePWM1-8)
SCIB_TX	2			O	SCI-B Transmit Data
MCLKXB	3			O	McBSP-B Transmit Clock
OUTPUTXBAR3	6			O	Output X-BAR Output 3
ESC_GPO6	10			O	EtherCAT General-Purpose Output 6
FSIRXC_CLK	13			I	FSIRX-C Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO15	0, 4, 8, 12	D3	7	I/O	General-Purpose Input Output 15
EPWM8B	1			O	ePWM-8 Output B (High-res available on ePWM1-8)
SCIB_RX	2			I	SCI-B Receive Data
MFSXB	3			O	McBSP-B Transmit Frame Sync
OUTPUTXBAR4	6			O	Output X-BAR Output 4
ESC_GPO7	10			O	EtherCAT General-Purpose Output 7
FSIRXD_D0	13			I	FSIRX-D Data Input 0
GPIO16	0, 4, 8, 12	E1	8	I/O	General-Purpose Input Output 16
SPIA_SIMO	1			I/O	SPI-A Slave In, Master Out (SIMO)
CANB_TX	2			O	CAN-B Transmit
OUTPUTXBAR7	3			O	Output X-BAR Output 7
EPWM9A	5			O	ePWM-9 Output A (High-res available on ePWM1-8)
SD1_D1	7			I	SDFM-1 Channel 1 Data Input
SSIA_TX	11			I/O	SSI-A Serial Data Transmit
FSIRXD_D1	13			I	FSIRX-D Data Input 1
GPIO17	0, 4, 8, 12	E2	9	I/O	General-Purpose Input Output 17
SPIA_SOMI	1			I/O	SPI-A Slave Out, Master In (SOMI)
CANB_RX	2			I	CAN-B Receive
OUTPUTXBAR8	3			O	Output X-BAR Output 8
EPWM9B	5			O	ePWM-9 Output B (High-res available on ePWM1-8)
SD1_C1	7			I	SDFM-1 Channel 1 Clock Input
SSIA_RX	11			I/O	SSI-A Serial Data Receive
FSIRXD_CLK	13			I	FSIRX-D Input Clock
GPIO18	0, 4, 8, 12	E3	10	I/O	General-Purpose Input Output 18
SPIA_CLK	1			I/O	SPI-A Clock
SCIB_TX	2			O	SCI-B Transmit Data
CANA_RX	3			I	CAN-A Receive
EPWM10A	5			O	ePWM-10 Output A (High-res available on ePWM1-8)
SD1_D2	7			I	SDFM-1 Channel 2 Data Input
MCAN_RX	9			I	CAN/CAN FD Receive
EMIF1_CS2n	10			O	External memory interface 1 chip select 2
SSIA_CLK	11			I/O	SSI-A Clock
FSIRXE_D0	13			I	FSIRX-E Data Input 0
GPIO19	0, 4, 8, 12	E4	12	I/O	General-Purpose Input Output 19
SPIA_STEn	1			I/O	SPI-A Slave Transmit Enable (STE)
SCIB_RX	2			I	SCI-B Receive Data
CANA_TX	3			O	CAN-A Transmit
EPWM10B	5			O	ePWM-10 Output B (High-res available on ePWM1-8)
SD1_C2	7			I	SDFM-1 Channel 2 Clock Input
MCAN_TX	9			O	CAN/CAN FD Transmit
EMIF1_CS3n	10			O	External memory interface 1 chip select 3
SSIA_FSS	11			I/O	SSI-A Frame Sync
FSIRXE_D1	13			I	FSIRX-E Data Input 1

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO20	0, 4, 8, 12	F2	13	I/O	General-Purpose Input Output 20
EQEP1_A	1			I	eQEP-1 Input A
MDXA	2			O	McBSP-A Transmit Serial Data
CANB_TX	3			O	CAN-B Transmit
EPWM11A	5			O	ePWM-11 Output A (High-res available on ePWM1-8)
SD1_D3	7			I	SDFM-1 Channel 3 Data Input
EMIF1_BA0	10			O	External memory interface 1 bank address 0
TRACE_DATA0	11			O	Trace Data 0
FSIRXE_CLK	13			I	FSIRX-E Input Clock
SPIC_SIMO	14			I/O	SPI-C Slave In, Master Out (SIMO)
GPIO21	0, 4, 8, 12	F3	14	I/O	General-Purpose Input Output 21
EQEP1_B	1			I	eQEP-1 Input B
MDRA	2			I	McBSP-A Receive Serial Data
CANB_RX	3			I	CAN-B Receive
EPWM11B	5			O	ePWM-11 Output B (High-res available on ePWM1-8)
SD1_C3	7			I	SDFM-1 Channel 3 Clock Input
EMIF1_BA1	10			O	External memory interface 1 bank address 1
TRACE_DATA1	11			O	Trace Data 1
FSIRXF_D0	13			I	FSIRX-F Data Input 0
SPIC_SOMI	14			I/O	SPI-C Slave Out, Master In (SOMI)
GPIO22	0, 4, 8, 12	J4	22	I/O	General-Purpose Input Output 22
EQEP1_STROBE	1			I/O	eQEP-1 Strobe
MCLKXA	2			O	McBSP-A Transmit Clock
SCIB_TX	3			O	SCI-B Transmit Data
EPWM12A	5			O	ePWM-12 Output A (High-res available on ePWM1-8)
SPIB_CLK	6			I/O	SPI-B Clock
SD1_D4	7			I	SDFM-1 Channel 4 Data Input
MCAN_TX	9			O	CAN/CAN FD Transmit
EMIF1_RAS	10			O	External memory interface 1 row address strobe
TRACE_DATA2	11			O	Trace Data 2
FSIRXF_D1	13			I	FSIRX-F Data Input 1
SPIC_CLK	14			I/O	SPI-C Clock
GPIO23	0, 4, 8, 12	K4	23	I/O	General-Purpose Input Output 23
EQEP1_INDEX	1			I/O	eQEP-1 Index
MFSXA	2			O	McBSP-A Transmit Frame Sync
SCIB_RX	3			I	SCI-B Receive Data
EPWM12B	5			O	ePWM-12 Output B (High-res available on ePWM1-8)
SPIB_STEn	6			I/O	SPI-B Slave Transmit Enable (STE)
SD1_C4	7			I	SDFM-1 Channel 4 Clock Input
MCAN_RX	9			I	CAN/CAN FD Receive
EMIF1_CAS	10			O	External memory interface 1 column address strobe
TRACE_DATA3	11			O	Trace Data 3
FSIRXF_CLK	13			I	FSIRX-F Input Clock
SPIC_STEn	14			I/O	SPI-C Slave Transmit Enable (STE)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO24	0, 4, 8, 12	K3	24	I/O	General-Purpose Input Output 24
OUTPUTXBAR1	1			O	Output X-BAR Output 1
EQEP2_A	2			I	eQEP-2 Input A
MDXB	3			O	McBSP-B Transmit Serial Data
SPIB_SIMO	6			I/O	SPI-B Slave In, Master Out (SIMO)
SD2_D1	7			I	SDFM-2 Channel 1 Data Input
PMBUSA_SCL	9			I/OD	PMBus-A Open-Drain Bidirectional Clock
EMIF1_DQM0	10			O	External memory interface 1 Input/output mask for byte 0
TRACE_CLK	11			O	Trace Clock
EPWM13A	13			O	ePWM-13 Output A (High-res available on ePWM1-8)
FSIRXG_D0	15			I	FSIRX-G Data Input 0
GPIO25	0, 4, 8, 12	K2	25	I/O	General-Purpose Input Output 25
OUTPUTXBAR2	1			O	Output X-BAR Output 2
EQEP2_B	2			I	eQEP-2 Input B
MDRB	3			I	McBSP-B Receive Serial Data
SPIB_SOMI	6			I/O	SPI-B Slave Out, Master In (SOMI)
SD2_C1	7			I	SDFM-2 Channel 1 Clock Input
PMBUSA_SDA	9			I/OD	PMBus-A Open-Drain Bidirectional Data
EMIF1_DQM1	10			O	External memory interface 1 Input/output mask for byte 1
TRACE_SWO	11			O	Trace Single Wire Out
EPWM13B	13			O	ePWM-13 Output B (High-res available on ePWM1-8)
FSITXA_D1	14			O	FSITX-A Data Output 1
FSIRXG_D1	15			I	FSIRX-G Data Input 1
GPIO26	0, 4, 8, 12	K1	27	I/O	General-Purpose Input Output 26
OUTPUTXBAR3	1, 5			O	Output X-BAR Output 3
EQEP2_INDEX	2			I/O	eQEP-2 Index
MCLKXB	3			O	McBSP-B Transmit Clock
SPIB_CLK	6			I/O	SPI-B Clock
SD2_D2	7			I	SDFM-2 Channel 2 Data Input
PMBUSA_ALERT	9			I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
EMIF1_DQM2	10			O	External memory interface 1 Input/output mask for byte 2
ESC_MDIO_CLK	11			O	EtherCAT MDIO Clock
EPWM14A	13			O	ePWM-14 Output A (High-res available on ePWM1-8)
FSITXA_D0	14			O	FSITX-A Data Output 0
FSIRXG_CLK	15			I	FSIRX-G Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO27	0, 4, 8, 12	L1	28	I/O	General-Purpose Input Output 27
OUTPUTXBAR4	1, 5			O	Output X-BAR Output 4
EQEP2_STROBE	2			I/O	eQEP-2 Strobe
MFSXB	3			O	McBSP-B Transmit Frame Sync
SPIB_STEn	6			I/O	SPI-B Slave Transmit Enable (STE)
SD2_C2	7			I	SDFM-2 Channel 2 Clock Input
PMBUSA_CTL	9			I	PMBus-A Control Signal
EMIF1_DQM3	10			O	External memory interface 1 Input/output mask for byte 3
ESC_MDIO_DATA	11			I/O	EtherCAT MDIO Data
EPWM14B	13			O	ePWM-14 Output B (High-res available on ePWM1-8)
FSITXA_CLK	14			O	FSITX-A Output Clock
FSIRXH_D0	15			I	FSIRX-H Data Input 0
GPIO28	0, 4, 8, 12	V11	64	I/O	General-Purpose Input Output 28
SCIA_RX	1			I	SCI-A Receive Data
EMIF1_CS4n	2			O	External memory interface 1 chip select 4
OUTPUTXBAR5	5			O	Output X-BAR Output 5
EQEP3_A	6			I	eQEP-3 Input A
SD2_D3	7			I	SDFM-2 Channel 3 Data Input
EMIF1_CS2n	9			O	External memory interface 1 chip select 2
EPWM15A	13			O	ePWM-15 Output A (High-res available on ePWM1-8)
FSIRXH_D1	15			I	FSIRX-H Data Input 1
GPIO29	0, 4, 8, 12	W11	65	I/O	General-Purpose Input Output 29
SCIA_TX	1			O	SCI-A Transmit Data
EMIF1_SDCKE	2			O	External memory interface 1 SDRAM clock enable
OUTPUTXBAR6	5			O	Output X-BAR Output 6
EQEP3_B	6			I	eQEP-3 Input B
SD2_C3	7			I	SDFM-2 Channel 3 Clock Input
EMIF1_CS3n	9			O	External memory interface 1 chip select 3
ESC_LATCH0	10			I	EtherCAT LatchSignal Input 0
ESC_I2C_SDA	11			I/OC	EtherCAT I2C Data
EPWM15B	13			O	ePWM-15 Output B (High-res available on ePWM1-8)
ESC_SYNC0	14			O	EtherCAT SyncSignal Output 0
FSIRXH_CLK	15			I	FSIRX-H Input Clock
GPIO30	0, 4, 8, 12	T11	63	I/O	General-Purpose Input Output 30
CANA_RX	1			I	CAN-A Receive
EMIF1_CLK	2			O	External memory interface 1 clock
MCAN_RX	3			I	CAN/CAN FD Receive
OUTPUTXBAR7	5			O	Output X-BAR Output 7
EQEP3_STROBE	6			I/O	eQEP-3 Strobe
SD2_D4	7			I	SDFM-2 Channel 4 Data Input
EMIF1_CS4n	9			O	External memory interface 1 chip select 4
ESC_LATCH1	10			I	EtherCAT LatchSignal Input 1
ESC_I2C_SCL	11			I/OC	EtherCAT I2C Clock
EPWM16A	13			O	ePWM-16 Output A (High-res available on ePWM1-8)
ESC_SYNC1	14			O	EtherCAT SyncSignal Output 1
SPID_SIMO	15			I/O	SPI-D Slave In, Master Out (SIMO)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO31	0, 4, 8, 12	U11	66	I/O	General-Purpose Input Output 31
CANA_TX	1			O	CAN-A Transmit
EMIF1_WEn	2			O	External memory interface 1 write enable
MCAN_TX	3			O	CAN/CAN FD Transmit
OUTPUTXBAR8	5			O	Output X-BAR Output 8
EQEP3_INDEX	6			I/O	eQEP-3 Index
SD2_C4	7			I	SDFM-2 Channel 4 Clock Input
EMIF1_RNW	9			O	External memory interface 1 read not write
I2CA_SDA	10			I/OD	I2C-A Open-Drain Bidirectional Data
CM-I2CA_SDA	11			I/OD	CM-I2C-A Open-Drain Bidirectional Data
EPWM16B	13			O	ePWM-16 Output B (High-res available on ePWM1-8)
SPID_SOMI	15			I/O	SPI-D Slave Out, Master In (SOMI)
GPIO32	0, 4, 8, 12	U13	67	I/O	General-Purpose Input Output 32
I2CA_SDA	1			I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_CS0n	2			O	External memory interface 1 chip select 0
SPIA_SIMO	3			I/O	SPI-A Slave In, Master Out (SIMO)
CLB_OUTPUTXBAR1	7			O	CLB Output X-BAR Output 1
EMIF1_OEn	9			O	External memory interface 1 output enable
I2CA_SCL	10			I/OD	I2C-A Open-Drain Bidirectional Clock
CM-I2CA_SCL	11			I/OD	CM-I2C-A Open-Drain Bidirectional Clock
SPID_CLK	15			I/O	SPI-D Clock
GPIO33	0, 4, 8, 12	T13	69	I/O	General-Purpose Input Output 33
I2CA_SCL	1			I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF1_RNW	2			O	External memory interface 1 read not write
SPIA_SOMI	3			I/O	SPI-A Slave Out, Master In (SOMI)
CLB_OUTPUTXBAR2	7			O	CLB Output X-BAR Output 2
EMIF1_BA0	9			O	External memory interface 1 bank address 0
SPID_STEn	15			I/O	SPI-D Slave Transmit Enable (STE)
GPIO34	0, 4, 8, 12	U14	70	I/O	General-Purpose Input Output 34
OUTPUTXBAR1	1			O	Output X-BAR Output 1
EMIF1_CS2n	2			O	External memory interface 1 chip select 2
SPIA_CLK	3			I/O	SPI-A Clock
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
CLB_OUTPUTXBAR3	7			O	CLB Output X-BAR Output 3
EMIF1_BA1	9			O	External memory interface 1 bank address 1
ESC_LATCH0	10			I	EtherCAT LatchSignal Input 0
ENET_MII_CRS	11			I	EMAC MII carrier sense
SCIA_TX	13			O	SCI-A Transmit Data
ESC_SYNC0	14			O	EtherCAT SyncSignal Output 0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO35	0, 4, 8, 12	T14	71	I/O	General-Purpose Input Output 35
SCIA_RX	1			I	SCI-A Receive Data
EMIF1_CS3n	2			O	External memory interface 1 chip select 3
SPIA_STEn	3			I/O	SPI-A Slave Transmit Enable (STE)
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
CLB_OUTPUTXBAR4	7			O	CLB Output X-BAR Output 4
EMIF1_A0	9			O	External memory interface 1 address line 0
ESC_LATCH1	10			I	EtherCAT LatchSignal Input 1
ENET_MII_COL	11			I	EMAC MII collision detect
ESC_SYNC1	14			O	EtherCAT SyncSignal Output 1
GPIO36	0, 4, 8, 12	V16	83	I/O	General-Purpose Input Output 36
SCIA_TX	1			O	SCI-A Transmit Data
EMIF1_WAIT	2			I	External memory interface 1 Asynchronous SRAM WAIT
CANA_RX	6			I	CAN-A Receive
CLB_OUTPUTXBAR5	7			O	CLB Output X-BAR Output 5
EMIF1_A1	9			O	External memory interface 1 address line 1
MCAN_RX	10			I	CAN/CAN FD Receive
SD1_D1	13			I	SDFM-1 Channel 1 Data Input
GPIO37	0, 4, 8, 12	U16	84	I/O	General-Purpose Input Output 37
OUTPUTXBAR2	1			O	Output X-BAR Output 2
EMIF1_OEn	2			O	External memory interface 1 output enable
CANA_TX	6			O	CAN-A Transmit
CLB_OUTPUTXBAR6	7			O	CLB Output X-BAR Output 6
EMIF1_A2	9			O	External memory interface 1 address line 2
MCAN_TX	10			O	CAN/CAN FD Transmit
SD1_D2	13			I	SDFM-1 Channel 2 Data Input
GPIO38	0, 4, 8, 12	T16	85	I/O	General-Purpose Input Output 38
EMIF1_A0	2			O	External memory interface 1 address line 0
SCIC_TX	5			O	SCI-C Transmit Data
CANB_TX	6			O	CAN-B Transmit
CLB_OUTPUTXBAR7	7			O	CLB Output X-BAR Output 7
EMIF1_A3	9			O	External memory interface 1 address line 3
ENET_MII_RX_DV	10			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
ENET_MII_CRS	11			I	EMAC MII carrier sense
SD1_D3	13			I	SDFM-1 Channel 3 Data Input
GPIO39	0, 4, 8, 12	W17	86	I/O	General-Purpose Input Output 39
EMIF1_A1	2			O	External memory interface 1 address line 1
SCIC_RX	5			I	SCI-C Receive Data
CANB_RX	6			I	CAN-B Receive
CLB_OUTPUTXBAR8	7			O	CLB Output X-BAR Output 8
EMIF1_A4	9			O	External memory interface 1 address line 4
ENET_MII_RX_ERR	10			I	EMAC MII / RMII receive error
ENET_MII_COL	11			I	EMAC MII collision detect
SD1_D4	13			I	SDFM-1 Channel 4 Data Input

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO40	0, 4, 8, 12	V17	87	I/O	General-Purpose Input Output 40
EMIF1_A2	2			O	External memory interface 1 address line 2
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
ENET_MII_CRS	11			I	EMAC MII carrier sense
ESC_I2C_SDA	14			I/OC	EtherCAT I2C Data
GPIO41	0, 4, 8, 12	U17	89	I/O	General-Purpose Input Output 41
EMIF1_A3	2			O	External memory interface 1 address line 3
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
ENET_REVMII_MDIO_RST	10			I	EMAC REVMII MDIO reset
ENET_MII_COL	11			I	EMAC MII collision detect
ESC_I2C_SCL	14			I/OC	EtherCAT I2C Clock
GPIO42	0, 4, 8, 12	D19	130	I/O	General-Purpose Input Output 42
I2CA_SDA	6			I/OD	I2C-A Open-Drain Bidirectional Data
ENET_MDIO_CLK	10			I/O	EMAC management data clock, Output in MII/RMII modes, Input in RevMII mode
UARTA_TX	11			I/O	UART-A Serial Data Transmit
SCIA_TX	15			O	SCI-A Transmit Data
USB0DM	ALT			O	USB-0 PHY differential data
GPIO43	0, 4, 8, 12	C19	131	I/O	General-Purpose Input Output 43
I2CA_SCL	6			I/OD	I2C-A Open-Drain Bidirectional Clock
ENET_MDIO_DATA	10			I/O	EMAC management data
UARTA_RX	11			I/O	UART-A Serial Data Receive
SCIA_RX	15			I	SCI-A Receive Data
USB0DP	ALT			O	USB-0 PHY differential data
GPIO44	0, 4, 8, 12	K18	113	I/O	General-Purpose Input Output 44
EMIF1_A4	2			O	External memory interface 1 address line 4
ENET_MII_TX_CLK	11			I	EMAC MII transmit clock
ESC_TX1_CLK	14			I	EtherCAT MII Transmit-1 Clock
GPIO45	0, 4, 8, 12	K19	115	I/O	General-Purpose Input Output 45
EMIF1_A5	2			O	External memory interface 1 address line 5
ENET_MII_TX_EN	11			O	EMAC MII / RMII transmit enable
ESC_TX1_ENA	14			O	EtherCAT MII Transmit-1 Enable
GPIO46	0, 4, 8, 12	E19	128	I/O	General-Purpose Input Output 46
EMIF1_A6	2			O	External memory interface 1 address line 6
SCID_RX	6			I	SCI-D Receive Data
ENET_MII_TX_ERR	11			O	EMAC MII transmit error
ESC_MDIO_CLK	14			O	EtherCAT MDIO Clock
GPIO47	0, 4, 8, 12	E18	129	I/O	General-Purpose Input Output 47
EMIF1_A7	2			O	External memory interface 1 address line 7
SCID_TX	6			O	SCI-D Transmit Data
ENET_PPS0	11			O	EMAC Pulse Per Second Output 0
ESC_MDIO_DATA	14			I/O	EtherCAT MDIO Data

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO48	0, 4, 8, 12	R16	90	I/O	General-Purpose Input Output 48
OUTPUTXBAR3	1			O	Output X-BAR Output 3
EMIF1_A8	2			O	External memory interface 1 address line 8
SCIA_TX	6			O	SCI-A Transmit Data
SD1_D1	7			I	SDFM-1 Channel 1 Data Input
ENET_PPS1	11			O	EMAC Pulse Per Second Output 1
ESC_PHY_CLK	14			O	EtherCAT PHY Clock
GPIO49	0, 4, 8, 12	R17	93	I/O	General-Purpose Input Output 49
OUTPUTXBAR4	1			O	Output X-BAR Output 4
EMIF1_A9	2			O	External memory interface 1 address line 9
SCIA_RX	6			I	SCI-A Receive Data
SD1_C1	7			I	SDFM-1 Channel 1 Clock Input
EMIF1_A5	9			O	External memory interface 1 address line 5
ENET_MII_RX_CLK	11			I	EMAC MII receive clock
SD2_D1	13			I	SDFM-2 Channel 1 Data Input
FSITXA_D0	14			O	FSITX-A Data Output 0
GPIO50	0, 4, 8, 12	R18	94	I/O	General-Purpose Input Output 50
EQEP1_A	1			I	eQEP-1 Input A
EMIF1_A10	2			O	External memory interface 1 address line 10
SPIC_SIMO	6			I/O	SPI-C Slave In, Master Out (SIMO)
SD1_D2	7			I	SDFM-1 Channel 2 Data Input
EMIF1_A6	9			O	External memory interface 1 address line 6
ENET_MII_RX_DV	11			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
SD2_D2	13			I	SDFM-2 Channel 2 Data Input
FSITXA_D1	14			O	FSITX-A Data Output 1
GPIO51	0, 4, 8, 12	R19	95	I/O	General-Purpose Input Output 51
EQEP1_B	1			I	eQEP-1 Input B
EMIF1_A11	2			O	External memory interface 1 address line 11
SPIC_SOMI	6			I/O	SPI-C Slave Out, Master In (SOMI)
SD1_C2	7			I	SDFM-1 Channel 2 Clock Input
EMIF1_A7	9			O	External memory interface 1 address line 7
ENET_MII_RX_ERR	11			I	EMAC MII / RMII receive error
SD2_D3	13			I	SDFM-2 Channel 3 Data Input
FSITXA_CLK	14			O	FSITX-A Output Clock
GPIO52	0, 4, 8, 12	P16	96	I/O	General-Purpose Input Output 52
EQEP1_STROBE	1			I/O	eQEP-1 Strobe
EMIF1_A12	2			O	External memory interface 1 address line 12
SPIC_CLK	6			I/O	SPI-C Clock
SD1_D3	7			I	SDFM-1 Channel 3 Data Input
EMIF1_A8	9			O	External memory interface 1 address line 8
ENET_MII_RX_DATA0	11			I	EMAC MII / RMII receive data 0
SD2_D4	13			I	SDFM-2 Channel 4 Data Input
FSIRXA_D0	14			I	FSIRX-A Data Input 0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO53	0, 4, 8, 12	P17	97	I/O	General-Purpose Input Output 53
EQEP1_INDEX	1			I/O	eQEP-1 Index
EMIF1_D31	2			I/O	External memory interface 1 data line 31
EMIF2_D15	3			I/O	External memory interface 2 data line 15
SPIC_STEn	6			I/O	SPI-C Slave Transmit Enable (STE)
SD1_C3	7			I	SDFM-1 Channel 3 Clock Input
EMIF1_A9	9			O	External memory interface 1 address line 9
ENET_MII_RX_DATA1	11			I	EMAC MII / RMII receive data 1
SD1_C1	13			I	SDFM-1 Channel 1 Clock Input
FSIRXA_D1	14			I	FSIRX-A Data Input 1
GPIO54	0, 4, 8, 12	P18	98	I/O	General-Purpose Input Output 54
SPIA_SIMO	1			I/O	SPI-A Slave In, Master Out (SIMO)
EMIF1_D30	2			I/O	External memory interface 1 data line 30
EMIF2_D14	3			I/O	External memory interface 2 data line 14
EQEP2_A	5			I	eQEP-2 Input A
SCIB_TX	6			O	SCI-B Transmit Data
SD1_D4	7			I	SDFM-1 Channel 4 Data Input
EMIF1_A10	9			O	External memory interface 1 address line 10
ENET_MII_RX_DATA2	11			I	EMAC MII receive data 2
SD1_C2	13			I	SDFM-1 Channel 2 Clock Input
FSIRXA_CLK	14			I	FSIRX-A Input Clock
SSIA_TX	15			I/O	SSI-A Serial Data Transmit
GPIO55	0, 4, 8, 12	P19	100	I/O	General-Purpose Input Output 55
SPIA_SOMI	1			I/O	SPI-A Slave Out, Master In (SOMI)
EMIF1_D29	2			I/O	External memory interface 1 data line 29
EMIF2_D13	3			I/O	External memory interface 2 data line 13
EQEP2_B	5			I	eQEP-2 Input B
SCIB_RX	6			I	SCI-B Receive Data
SD1_C4	7			I	SDFM-1 Channel 4 Clock Input
EMIF1_D0	9			I/O	External memory interface 1 data line 0
ENET_MII_RX_DATA3	11			I	EMAC MII receive data 3
SD1_C3	13			I	SDFM-1 Channel 3 Clock Input
FSITXB_D0	14			O	FSITX-B Data Output 0
SSIA_RX	15			I/O	SSI-A Serial Data Receive

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO56	0, 4, 8, 12	N16	101	I/O	General-Purpose Input Output 56
SPIA_CLK	1			I/O	SPI-A Clock
EMIF1_D28	2			I/O	External memory interface 1 data line 28
EMIF2_D12	3			I/O	External memory interface 2 data line 12
EQEP2_STROBE	5			I/O	eQEP-2 Strobe
SCIC_TX	6			O	SCI-C Transmit Data
SD2_D1	7			I	SDFM-2 Channel 1 Data Input
EMIF1_D1	9			I/O	External memory interface 1 data line 1
I2CA_SDA	10			I/OD	I2C-A Open-Drain Bidirectional Data
ENET_MII_TX_EN	11			O	EMAC MII / RMII transmit enable
SD1_C4	13			I	SDFM-1 Channel 4 Clock Input
FSITXB_CLK	14			O	FSITX-B Output Clock
SSIA_CLK	15			I/O	SSI-A Clock
GPIO57	0, 4, 8, 12	N18	102	I/O	General-Purpose Input Output 57
SPIA_STEn	1			I/O	SPI-A Slave Transmit Enable (STE)
EMIF1_D27	2			I/O	External memory interface 1 data line 27
EMIF2_D11	3			I/O	External memory interface 2 data line 11
EQEP2_INDEX	5			I/O	eQEP-2 Index
SCIC_RX	6			I	SCI-C Receive Data
SD2_C1	7			I	SDFM-2 Channel 1 Clock Input
EMIF1_D2	9			I/O	External memory interface 1 data line 2
I2CA_SCL	10			I/OD	I2C-A Open-Drain Bidirectional Clock
ENET_MII_TX_ERR	11			O	EMAC MII transmit error
FSITXB_D1	14			O	FSITX-B Data Output 1
SSIA_FSS	15			I/O	SSI-A Frame Sync
GPIO58	0, 4, 8, 12	N17	103	I/O	General-Purpose Input Output 58
MCLKRA	1			I	McBSP-A Receive Clock
EMIF1_D26	2			I/O	External memory interface 1 data line 26
EMIF2_D10	3			I/O	External memory interface 2 data line 10
OUTPUTXBAR1	5			O	Output X-BAR Output 1
SPIB_CLK	6			I/O	SPI-B Clock
SD2_D2	7			I	SDFM-2 Channel 2 Data Input
EMIF1_D3	9			I/O	External memory interface 1 data line 3
ESC_LED_LINK0_ACTIVE	10			O	EtherCAT Link-0 Active
ENET_MII_TX_CLK	11			I	EMAC MII transmit clock
SD2_C2	13			I	SDFM-2 Channel 2 Clock Input
FSIRXB_D0	14			I	FSIRX-B Data Input 0
SPIA_SIMO	15			I/O	SPI-A Slave In, Master Out (SIMO)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO59	0, 4, 8, 12	M16	104	I/O	General-Purpose Input Output 59
MFSRA	1			I	McBSP-A Receive Frame Sync
EMIF1_D25	2			I/O	External memory interface 1 data line 25
EMIF2_D9	3			I/O	External memory interface 2 data line 9
OUTPUTXBAR2	5			O	Output X-BAR Output 2
SPIB_STEn	6			I/O	SPI-B Slave Transmit Enable (STE)
SD2_C2	7			I	SDFM-2 Channel 2 Clock Input
EMIF1_D4	9			I/O	External memory interface 1 data line 4
ESC_LED_LINK1_ACTIVE	10			O	EtherCAT Link-1 Active
ENET_MII_TX_DATA0	11			O	EMAC MII / RMII transmit data 0
SD2_C3	13			I	SDFM-2 Channel 3 Clock Input
FSIRXB_D1	14			I	FSIRX-B Data Input 1
SPIA_SOMI	15			I/O	SPI-A Slave Out, Master In (SOMI)
GPIO60	0, 4, 8, 12	M17	105	I/O	General-Purpose Input Output 60
MCLKRB	1			I	McBSP-B Receive Clock
EMIF1_D24	2			I/O	External memory interface 1 data line 24
EMIF2_D8	3			I/O	External memory interface 2 data line 8
OUTPUTXBAR3	5			O	Output X-BAR Output 3
SPIB_SIMO	6			I/O	SPI-B Slave In, Master Out (SIMO)
SD2_D3	7			I	SDFM-2 Channel 3 Data Input
EMIF1_D5	9			I/O	External memory interface 1 data line 5
ESC_LED_ERR	10			O	EtherCAT Error LED
ENET_MII_TX_DATA1	11			O	EMAC MII / RMII transmit data 1
SD2_C4	13			I	SDFM-2 Channel 4 Clock Input
FSIRXB_CLK	14			I	FSIRX-B Input Clock
SPIA_CLK	15			I/O	SPI-A Clock
GPIO61	0, 4, 8, 12	L16	107	I/O	General-Purpose Input Output 61
MFSRB	1			I	McBSP-B Receive Frame Sync
EMIF1_D23	2			I/O	External memory interface 1 data line 23
EMIF2_D7	3			I/O	External memory interface 2 data line 7
OUTPUTXBAR4	5			O	Output X-BAR Output 4
SPIB_SOMI	6			I/O	SPI-B Slave Out, Master In (SOMI)
SD2_C3	7			I	SDFM-2 Channel 3 Clock Input
EMIF1_D6	9			I/O	External memory interface 1 data line 6
ESC_LED_RUN	10			O	EtherCAT Run LED
ENET_MII_TX_DATA2	11			O	EMAC MII transmit data 2
CANA_RX	14			I	CAN-A Receive
SPIA_STEn	15			I/O	SPI-A Slave Transmit Enable (STE)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO62	0, 4, 8, 12	J17	108	I/O	General-Purpose Input Output 62
SCIC_RX	1			I	SCI-C Receive Data
EMIF1_D22	2			I/O	External memory interface 1 data line 22
EMIF2_D6	3			I/O	External memory interface 2 data line 6
EQEP3_A	5			I	eQEP-3 Input A
CANA_RX	6			I	CAN-A Receive
SD2_D4	7			I	SDFM-2 Channel 4 Data Input
EMIF1_D7	9			I/O	External memory interface 1 data line 7
ESC_LED_STATE_RUN	10			O	EtherCAT State Run
ENET_MII_TX_DATA3	11			O	EMAC MII transmit data 3
CANA_TX	14			O	CAN-A Transmit
GPIO63	0, 4, 8, 12	J16	109	I/O	General-Purpose Input Output 63
SCIC_TX	1			O	SCI-C Transmit Data
EMIF1_D21	2			I/O	External memory interface 1 data line 21
EMIF2_D5	3			I/O	External memory interface 2 data line 5
EQEP3_B	5			I	eQEP-3 Input B
CANA_TX	6			O	CAN-A Transmit
SD2_C4	7			I	SDFM-2 Channel 4 Clock Input
SSIA_TX	9			I/O	SSI-A Serial Data Transmit
ENET_MII_RX_DATA0	11			I	EMAC MII / RMII receive data 0
SD1_D1	13			I	SDFM-1 Channel 1 Data Input
ESC_RX1_DATA0	14			I	EtherCAT MII Receive-1 Data-0
SPIB_SIMO	15			I/O	SPI-B Slave In, Master Out (SIMO)
GPIO64	0, 4, 8, 12	L17	110	I/O	General-Purpose Input Output 64
EMIF1_D20	2			I/O	External memory interface 1 data line 20
EMIF2_D4	3			I/O	External memory interface 2 data line 4
EQEP3_STROBE	5			I/O	eQEP-3 Strobe
SCIA_RX	6			I	SCI-A Receive Data
SSIA_RX	9			I/O	SSI-A Serial Data Receive
ENET_MII_RX_DV	10			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
ENET_MII_RX_DATA1	11			I	EMAC MII / RMII receive data 1
SD1_C1	13			I	SDFM-1 Channel 1 Clock Input
ESC_RX1_DATA1	14			I	EtherCAT MII Receive-1 Data-1
SPIB_SOMI	15			I/O	SPI-B Slave Out, Master In (SOMI)
GPIO65	0, 4, 8, 12	K16	111	I/O	General-Purpose Input Output 65
EMIF1_D19	2			I/O	External memory interface 1 data line 19
EMIF2_D3	3			I/O	External memory interface 2 data line 3
EQEP3_INDEX	5			I/O	eQEP-3 Index
SCIA_TX	6			O	SCI-A Transmit Data
SSIA_CLK	9			I/O	SSI-A Clock
ENET_MII_RX_ERR	10			I	EMAC MII / RMII receive error
ENET_MII_RX_DATA2	11			I	EMAC MII receive data 2
SD1_D2	13			I	SDFM-1 Channel 2 Data Input
ESC_RX1_DATA2	14			I	EtherCAT MII Receive-1 Data-2
SPIB_CLK	15			I/O	SPI-B Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO66	0, 4, 8, 12	K17	112	I/O	General-Purpose Input Output 66
EMIF1_D18	2			I/O	External memory interface 1 data line 18
EMIF2_D2	3			I/O	External memory interface 2 data line 2
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
SSIA_FSS	9			I/O	SSI-A Frame Sync
ENET_MII_RX_DATA0	10			I	EMAC MII / RMII receive data 0
ENET_MII_RX_DATA3	11			I	EMAC MII receive data 3
SD1_C2	13			I	SDFM-1 Channel 2 Clock Input
ESC_RX1_DATA3	14			I	EtherCAT MII Receive-1 Data-3
SPIB_STEn	15			I/O	SPI-B Slave Transmit Enable (STE)
GPIO67	0, 4, 8, 12	B19	132	I/O	General-Purpose Input Output 67
EMIF1_D17	2			I/O	External memory interface 1 data line 17
EMIF2_D1	3			I/O	External memory interface 2 data line 1
ENET_MII_RX_CLK	10			I	EMAC MII receive clock
ENET_REVMII_MDIO_RST	11			I	EMAC REVMII MDIO reset
SD1_D3	13			I	SDFM-1 Channel 3 Data Input
GPIO68	0, 4, 8, 12	C18	133	I/O	General-Purpose Input Output 68
EMIF1_D16	2			I/O	External memory interface 1 data line 16
EMIF2_D0	3			I/O	External memory interface 2 data line 0
ENET_MII_INTR	11			I/O	EMAC PHY interrupt, Input in MII/RMII mode, Output in RevMII mode
SD1_C3	13			I	SDFM-1 Channel 3 Clock Input
ESC_PHY1_LINKSTATUS	14			I	EtherCAT PHY-1 Link Status
GPIO69	0, 4, 8, 12	B18	134	I/O	General-Purpose Input Output 69
EMIF1_D15	2			I/O	External memory interface 1 data line 15
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
ENET_MII_TX_EN	10			O	EMAC MII / RMII transmit enable
ENET_MII_RX_CLK	11			I	EMAC MII receive clock
SD1_D4	13			I	SDFM-1 Channel 4 Data Input
ESC_RX1_CLK	14			I	EtherCAT MII Receive-1 Clock
SPIC_SIMO	15			I/O	SPI-C Slave In, Master Out (SIMO)
GPIO70	0, 4, 8, 12	A17	135	I/O	General-Purpose Input Output 70
EMIF1_D14	2			I/O	External memory interface 1 data line 14
CANA_RX	5			I	CAN-A Receive
SCIB_TX	6			O	SCI-B Transmit Data
MCAN_RX	9			I	CAN/CAN FD Receive
ENET_MII_RX_DV	11			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
SD1_C4	13			I	SDFM-1 Channel 4 Clock Input
ESC_RX1_DV	14			I	EtherCAT MII Receive-1 Data Valid
SPIC_SOMI	15			I/O	SPI-C Slave Out, Master In (SOMI)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO71	0, 4, 8, 12	B17	136	I/O	General-Purpose Input Output 71
EMIF1_D13	2			I/O	External memory interface 1 data line 13
CANA_TX	5			O	CAN-A Transmit
SCIB_RX	6			I	SCI-B Receive Data
MCAN_TX	9			O	CAN/CAN FD Transmit
ENET_MII_RX_DATA0	10			I	EMAC MII / RMII receive data 0
ENET_MII_RX_ERR	11			I	EMAC MII / RMII receive error
ESC_RX1_ERR	14			I	EtherCAT MII Receive-1 Error
SPIC_CLK	15			I/O	SPI-C Clock
GPIO72	0, 4, 8, 12	B16	139	I/O	General-Purpose Input Output 72
EMIF1_D12	2			I/O	External memory interface 1 data line 12
CANB_TX	5			O	CAN-B Transmit
SCIC_TX	6			O	SCI-C Transmit Data
ENET_MII_RX_DATA1	10			I	EMAC MII / RMII receive data 1
ENET_MII_TX_DATA3	11			O	EMAC MII transmit data 3
ESC_TX1_DATA3	14			O	EtherCAT MII Transmit-1 Data-3
SPIC_STEn	15			I/O	SPI-C Slave Transmit Enable (STE)
GPIO73	0, 4, 8, 12	A16	140	I/O	General-Purpose Input Output 73
EMIF1_D11	2			I/O	External memory interface 1 data line 11
XCLKOUT	3			O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
CANB_RX	5			I	CAN-B Receive
SCIC_RX	6			I	SCI-C Receive Data
ENET_RMII_CLK	10			I/O	EMAC RMII clock
ENET_MII_TX_DATA2	11			O	EMAC MII transmit data 2
SD2_D2	13			I	SDFM-2 Channel 2 Data Input
ESC_TX1_DATA2	14			O	EtherCAT MII Transmit-1 Data-2
GPIO74	0, 4, 8, 12	C17	141	I/O	General-Purpose Input Output 74
EMIF1_D10	2			I/O	External memory interface 1 data line 10
MCAN_TX	9			O	CAN/CAN FD Transmit
ENET_MII_TX_DATA1	11			O	EMAC MII / RMII transmit data 1
SD2_C2	13			I	SDFM-2 Channel 2 Clock Input
ESC_TX1_DATA1	14			O	EtherCAT MII Transmit-1 Data-1
GPIO75	0, 4, 8, 12	D16	142	I/O	General-Purpose Input Output 75
EMIF1_D9	2			I/O	External memory interface 1 data line 9
MCAN_RX	9			I	CAN/CAN FD Receive
ENET_MII_TX_DATA0	11			O	EMAC MII / RMII transmit data 0
SD2_D3	13			I	SDFM-2 Channel 3 Data Input
ESC_TX1_DATA0	14			O	EtherCAT MII Transmit-1 Data-0
GPIO76	0, 4, 8, 12	C16	143	I/O	General-Purpose Input Output 76
EMIF1_D8	2			I/O	External memory interface 1 data line 8
SCID_TX	6			O	SCI-D Transmit Data
ENET_MII_RX_ERR	10			I	EMAC MII / RMII receive error
SD2_C3	13			I	SDFM-2 Channel 3 Clock Input
ESC_PHY_RESETn	14			O	EtherCAT PHY Active Low Reset

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO77	0, 4, 8, 12	A15	144	I/O	General-Purpose Input Output 77
EMIF1_D7	2			I/O	External memory interface 1 data line 7
SCID_RX	6			I	SCI-D Receive Data
SD2_D4	13			I	SDFM-2 Channel 4 Data Input
ESC_RX0_CLK	14			I	EtherCAT MII Receive-0 Clock
GPIO78	0, 4, 8, 12	B15	145	I/O	General-Purpose Input Output 78
EMIF1_D6	2			I/O	External memory interface 1 data line 6
EQEP2_A	6			I	eQEP-2 Input A
SD2_C4	13			I	SDFM-2 Channel 4 Clock Input
ESC_RX0_DV	14			I	EtherCAT MII Receive-0 Data Valid
GPIO79	0, 4, 8, 12	C15	146	I/O	General-Purpose Input Output 79
EMIF1_D5	2			I/O	External memory interface 1 data line 5
EQEP2_B	6			I	eQEP-2 Input B
SD2_D1	13			I	SDFM-2 Channel 1 Data Input
ESC_RX0_ERR	14			I	EtherCAT MII Receive-0 Error
GPIO80	0, 4, 8, 12	D15	148	I/O	General-Purpose Input Output 80
EMIF1_D4	2			I/O	External memory interface 1 data line 4
EQEP2_STROBE	6			I/O	eQEP-2 Strobe
SD2_C1	13			I	SDFM-2 Channel 1 Clock Input
ESC_RX0_DATA0	14			I	EtherCAT MII Receive-0 Data-0
GPIO81	0, 4, 8, 12	A14	149	I/O	General-Purpose Input Output 81
EMIF1_D3	2			I/O	External memory interface 1 data line 3
EQEP2_INDEX	6			I/O	eQEP-2 Index
ESC_RX0_DATA1	14			I	EtherCAT MII Receive-0 Data-1
GPIO82	0, 4, 8, 12	B14	150	I/O	General-Purpose Input Output 82
EMIF1_D2	2			I/O	External memory interface 1 data line 2
ESC_RX0_DATA2	14			I	EtherCAT MII Receive-0 Data-2
GPIO83	0, 4, 8, 12	C14	151	I/O	General-Purpose Input Output 83
EMIF1_D1	2			I/O	External memory interface 1 data line 1
ESC_RX0_DATA3	14			I	EtherCAT MII Receive-0 Data-3
GPIO84	0, 4, 8, 12	A11	154	I/O	General-Purpose Input Output 84
SCIA_TX	5			O	SCI-A Transmit Data
MDXB	6			O	McBSP-B Transmit Serial Data
UARTA_TX	11			I/O	UART-A Serial Data Transmit
ESC_TX0_ENA	14			O	EtherCAT MII Transmit-0 Enable
MDXA	15			O	McBSP-A Transmit Serial Data
GPIO85	0, 4, 8, 12	B11	155	I/O	General-Purpose Input Output 85
EMIF1_D0	2			I/O	External memory interface 1 data line 0
SCIA_RX	5			I	SCI-A Receive Data
MDRB	6			I	McBSP-B Receive Serial Data
UARTA_RX	11			I/O	UART-A Serial Data Receive
ESC_TX0_CLK	14			I	EtherCAT MII Transmit-0 Clock
MDRA	15			I	McBSP-A Receive Serial Data

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO86	0, 4, 8, 12	C11	156	I/O	General-Purpose Input Output 86
EMIF1_A13	2			O	External memory interface 1 address line 13
EMIF1_CAS	3			O	External memory interface 1 column address strobe
SCIB_TX	5			O	SCI-B Transmit Data
MCLKXB	6			O	McBSP-B Transmit Clock
ESC_PHY0_LINKSTATUS	14			I	EtherCAT PHY-0 Link Status
MCLKXA	15			O	McBSP-A Transmit Clock
GPIO87	0, 4, 8, 12	D11	157	I/O	General-Purpose Input Output 87
EMIF1_A14	2			O	External memory interface 1 address line 14
EMIF1_RAS	3			O	External memory interface 1 row address strobe
SCIB_RX	5			I	SCI-B Receive Data
MFSXB	6			O	McBSP-B Transmit Frame Sync
EMIF1_DQM3	9			O	External memory interface 1 Input/output mask for byte 3
ESC_TX0_DATA0	14			O	EtherCAT MII Transmit-0 Data-0
MFSXA	15			O	McBSP-A Transmit Frame Sync
GPIO88	0, 4, 8, 12	C6	170	I/O	General-Purpose Input Output 88
EMIF1_A15	2			O	External memory interface 1 address line 15
EMIF1_DQM0	3			O	External memory interface 1 Input/output mask for byte 0
EMIF1_DQM1	9			O	External memory interface 1 Input/output mask for byte 1
ESC_TX0_DATA1	14			O	EtherCAT MII Transmit-0 Data-1
GPIO89	0, 4, 8, 12	D6	171	I/O	General-Purpose Input Output 89
EMIF1_A16	2			O	External memory interface 1 address line 16
EMIF1_DQM1	3			O	External memory interface 1 Input/output mask for byte 1
SCIC_TX	6			O	SCI-C Transmit Data
EMIF1_CAS	9			O	External memory interface 1 column address strobe
ESC_TX0_DATA2	14			O	EtherCAT MII Transmit-0 Data-2
GPIO90	0, 4, 8, 12	A5	172	I/O	General-Purpose Input Output 90
EMIF1_A17	2			O	External memory interface 1 address line 17
EMIF1_DQM2	3			O	External memory interface 1 Input/output mask for byte 2
SCIC_RX	6			I	SCI-C Receive Data
EMIF1_RAS	9			O	External memory interface 1 row address strobe
ESC_TX0_DATA3	14			O	EtherCAT MII Transmit-0 Data-3
GPIO91	0, 4, 8, 12	B5	173	I/O	General-Purpose Input Output 91
EMIF1_A18	2			O	External memory interface 1 address line 18
EMIF1_DQM3	3			O	External memory interface 1 Input/output mask for byte 3
I2CA_SDA	6			I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_DQM2	9			O	External memory interface 1 Input/output mask for byte 2
PMBUSA_SCL	10			I/OD	PMBus-A Open-Drain Bidirectional Clock
SSIA_TX	11			I/O	SSI-A Serial Data Transmit
FSIRXF_D0	13			I	FSIRX-F Data Input 0
CLB_OUTPUTXBAR1	14			O	CLB Output X-BAR Output 1
SPID_SIMO	15			I/O	SPI-D Slave In, Master Out (SIMO)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO92	0, 4, 8, 12	A4	174	I/O	General-Purpose Input Output 92
EMIF1_A19	2			O	External memory interface 1 address line 19
EMIF1_BA1	3			O	External memory interface 1 bank address 1
I2CA_SCL	6			I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF1_DQM0	9			O	External memory interface 1 Input/output mask for byte 0
PMBUSA_SDA	10			I/OD	PMBus-A Open-Drain Bidirectional Data
SSIA_RX	11			I/O	SSI-A Serial Data Receive
FSIRXF_D1	13			I	FSIRX-F Data Input 1
CLB_OUTPUTXBAR2	14			O	CLB Output X-BAR Output 2
SPID_SOMI	15			I/O	SPI-D Slave Out, Master In (SOMI)
GPIO93	0, 4, 8, 12	B4	175	I/O	General-Purpose Input Output 93
EMIF1_BA0	3			O	External memory interface 1 bank address 0
SCID_TX	6			O	SCI-D Transmit Data
PMBUSA_ALERT	10			I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
SSIA_CLK	11			I/O	SSI-A Clock
FSIRXF_CLK	13			I	FSIRX-F Input Clock
CLB_OUTPUTXBAR3	14			O	CLB Output X-BAR Output 3
SPID_CLK	15			I/O	SPI-D Clock
GPIO94	0, 4, 8, 12	A3	176	I/O	General-Purpose Input Output 94
SCID_RX	6			I	SCI-D Receive Data
EMIF1_BA1	9			O	External memory interface 1 bank address 1
PMBUSA_CTL	10			I	PMBus-A Control Signal
SSIA_FSS	11			I/O	SSI-A Frame Sync
FSIRXG_D0	13			I	FSIRX-G Data Input 0
CLB_OUTPUTXBAR4	14			O	CLB Output X-BAR Output 4
SPID_STEn	15			I/O	SPI-D Slave Transmit Enable (STE)
GPIO95	0, 4, 8, 12	B3		I/O	General-Purpose Input Output 95
EMIF2_A12	3			O	External memory interface 2 address line 12
FSIRXG_D1	13			I	FSIRX-G Data Input 1
CLB_OUTPUTXBAR5	14			O	CLB Output X-BAR Output 5
GPIO96	0, 4, 8, 12	C3		I/O	General-Purpose Input Output 96
EMIF2_DQM1	3			O	External memory interface 2 Input/output mask for byte 1
EQEP1_A	5			I	eQEP-1 Input A
FSIRXG_CLK	13			I	FSIRX-G Input Clock
CLB_OUTPUTXBAR6	14			O	CLB Output X-BAR Output 6
GPIO97	0, 4, 8, 12	A2		I/O	General-Purpose Input Output 97
EMIF2_DQM0	3			O	External memory interface 2 Input/output mask for byte 0
EQEP1_B	5			I	eQEP-1 Input B
FSIRXH_D0	13			I	FSIRX-H Data Input 0
CLB_OUTPUTXBAR7	14			O	CLB Output X-BAR Output 7
GPIO98	0, 4, 8, 12	F1		I/O	General-Purpose Input Output 98
EMIF2_A0	3			O	External memory interface 2 address line 0
EQEP1_STROBE	5			I/O	eQEP-1 Strobe
FSIRXH_D1	13			I	FSIRX-H Data Input 1
CLB_OUTPUTXBAR8	14			O	CLB Output X-BAR Output 8

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO99	0, 4, 8, 12	G1	17	I/O	General-Purpose Input Output 99
EMIF2_A1	3			O	External memory interface 2 address line 1
EQEP1_INDEX	5			I/O	eQEP-1 Index
FSIRXH_CLK	13			I	FSIRX-H Input Clock
GPIO100	0, 4, 8, 12	H1		I/O	General-Purpose Input Output 100
EMIF2_A2	3			O	External memory interface 2 address line 2
EQEP2_A	5			I	eQEP-2 Input A
SPIC_SIMO	6			I/O	SPI-C Slave In, Master Out (SIMO)
ESC_GPI0	10			I	EtherCAT General-Purpose Input 0
FSITXA_D0	13			O	FSITX-A Data Output 0
GPIO101	0, 4, 8, 12	H2		I/O	General-Purpose Input Output 101
EMIF2_A3	3			O	External memory interface 2 address line 3
EQEP2_B	5			I	eQEP-2 Input B
SPIC_SOMI	6			I/O	SPI-C Slave Out, Master In (SOMI)
ESC_GPI1	10			I	EtherCAT General-Purpose Input 1
FSITXA_D1	13			O	FSITX-A Data Output 1
GPIO102	0, 4, 8, 12	H3		I/O	General-Purpose Input Output 102
EMIF2_A4	3			O	External memory interface 2 address line 4
EQEP2_STROBE	5			I/O	eQEP-2 Strobe
SPIC_CLK	6			I/O	SPI-C Clock
ESC_GPI2	10			I	EtherCAT General-Purpose Input 2
FSITXA_CLK	13			O	FSITX-A Output Clock
GPIO103	0, 4, 8, 12	J1		I/O	General-Purpose Input Output 103
EMIF2_A5	3			O	External memory interface 2 address line 5
EQEP2_INDEX	5			I/O	eQEP-2 Index
SPIC_STEn	6			I/O	SPI-C Slave Transmit Enable (STE)
ESC_GPI3	10			I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13			I	FSIRX-A Data Input 0
GPIO104	0, 4, 8, 12	J2		I/O	General-Purpose Input Output 104
I2CA_SDA	1			I/OD	I2C-A Open-Drain Bidirectional Data
EMIF2_A6	3			O	External memory interface 2 address line 6
EQEP3_A	5			I	eQEP-3 Input A
SCID_TX	6			O	SCI-D Transmit Data
ESC_GPI4	10			I	EtherCAT General-Purpose Input 4
CM-I2CA_SDA	11			I/OD	CM-I2C-A Open-Drain Bidirectional Data
FSIRXA_D1	13			I	FSIRX-A Data Input 1
GPIO105	0, 4, 8, 12	J3		I/O	General-Purpose Input Output 105
I2CA_SCL	1			I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF2_A7	3			O	External memory interface 2 address line 7
EQEP3_B	5			I	eQEP-3 Input B
SCID_RX	6			I	SCI-D Receive Data
ESC_GPI5	10			I	EtherCAT General-Purpose Input 5
CM-I2CA_SCL	11			I/OD	CM-I2C-A Open-Drain Bidirectional Clock
FSIRXA_CLK	13			I	FSIRX-A Input Clock
ENET_MDIO_CLK	14			I/O	EMAC management data clock, Output in MII/RMII modes, Input in RevMII mode

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO106	0, 4, 8, 12	L2		I/O	General-Purpose Input Output 106
EMIF2_A8	3			O	External memory interface 2 address line 8
EQEP3_STROBE	5			I/O	eQEP-3 Strobe
SCIC_TX	6			O	SCI-C Transmit Data
ESC_GPI6	10			I	EtherCAT General-Purpose Input 6
FSITXB_D0	13			O	FSITX-B Data Output 0
ENET_MDIO_DATA	14			I/O	EMAC management data
GPIO107	0, 4, 8, 12	L3		I/O	General-Purpose Input Output 107
EMIF2_A9	3			O	External memory interface 2 address line 9
EQEP3_INDEX	5			I/O	eQEP-3 Index
SCIC_RX	6			I	SCI-C Receive Data
ESC_GPI7	10			I	EtherCAT General-Purpose Input 7
FSITXB_D1	13			O	FSITX-B Data Output 1
ENET_REVMII_MDIO_RST	14			I	EMAC REVMII MDIO reset
GPIO108	0, 4, 8, 12	L4		I/O	General-Purpose Input Output 108
EMIF2_A10	3			O	External memory interface 2 address line 10
ESC_GPI8	10			I	EtherCAT General-Purpose Input 8
FSITXB_CLK	13			O	FSITX-B Output Clock
ENET_MII_INTR	14			I/O	EMAC PHY interrupt, Input in MII/RMII mode, Output in RevMII mode
GPIO109	0, 4, 8, 12	N2		I/O	General-Purpose Input Output 109
EMIF2_A11	3			O	External memory interface 2 address line 11
ESC_GPI9	10			I	EtherCAT General-Purpose Input 9
ENET_MII_CRS	14			I	EMAC MII carrier sense
GPIO110	0, 4, 8, 12	M2		I/O	General-Purpose Input Output 110
EMIF2_WAIT	3			I	External memory interface 2 Asynchronous SRAM WAIT
ESC_GPI10	10			I	EtherCAT General-Purpose Input 10
FSIRXB_D0	13			I	FSIRX-B Data Input 0
ENET_MII_COL	14			I	EMAC MII collision detect
GPIO111	0, 4, 8, 12	M4		I/O	General-Purpose Input Output 111
EMIF2_BA0	3			O	External memory interface 2 bank address 0
ESC_GPI11	10			I	EtherCAT General-Purpose Input 11
FSIRXB_D1	13			I	FSIRX-B Data Input 1
ENET_MII_RX_CLK	14			I	EMAC MII receive clock
GPIO112	0, 4, 8, 12	M3		I/O	General-Purpose Input Output 112
EMIF2_BA1	3			O	External memory interface 2 bank address 1
ESC_GPI12	10			I	EtherCAT General-Purpose Input 12
FSIRXB_CLK	13			I	FSIRX-B Input Clock
ENET_MII_RX_DV	14			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
GPIO113	0, 4, 8, 12	N4		I/O	General-Purpose Input Output 113
EMIF2_CAS	3			O	External memory interface 2 column address strobe
ESC_GPI13	10			I	EtherCAT General-Purpose Input 13
ENET_MII_RX_ERR	14			I	EMAC MII / RMII receive error

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO114	0, 4, 8, 12	N3		I/O	General-Purpose Input Output 114
EMIF2_RAS	3			O	External memory interface 2 row address strobe
ESC_GPI14	10			I	EtherCAT General-Purpose Input 14
ENET_MII_RX_DATA0	14			I	EMAC MII / RMII receive data 0
GPIO115	0, 4, 8, 12	V12		I/O	General-Purpose Input Output 115
EMIF2_CS0n	3			O	External memory interface 2 chip select 0
OUTPUTXBAR5	5			O	Output X-BAR Output 5
ESC_GPI15	10			I	EtherCAT General-Purpose Input 15
FSIRXC_D0	13			I	FSIRX-C Data Input 0
ENET_MII_RX_DATA1	14			I	EMAC MII / RMII receive data 1
GPIO116	0, 4, 8, 12	W10		I/O	General-Purpose Input Output 116
EMIF2_CS2n	3			O	External memory interface 2 chip select 2
OUTPUTXBAR6	5			O	Output X-BAR Output 6
ESC_GPI16	10			I	EtherCAT General-Purpose Input 16
FSIRXC_D1	13			I	FSIRX-C Data Input 1
ENET_MII_RX_DATA2	14			I	EMAC MII receive data 2
GPIO117	0, 4, 8, 12	U12		I/O	General-Purpose Input Output 117
EMIF2_SDCKE	3			O	External memory interface 2 SDRAM clock enable
ESC_GPI17	10			I	EtherCAT General-Purpose Input 17
FSIRXC_CLK	13			I	FSIRX-C Input Clock
ENET_MII_RX_DATA3	14			I	EMAC MII receive data 3
GPIO118	0, 4, 8, 12	T12		I/O	General-Purpose Input Output 118
EMIF2_CLK	3			O	External memory interface 2 clock
ESC_GPI18	10			I	EtherCAT General-Purpose Input 18
FSIRXD_D0	13			I	FSIRX-D Data Input 0
ENET_MII_TX_EN	14			O	EMAC MII / RMII transmit enable
GPIO119	0, 4, 8, 12	T15		I/O	General-Purpose Input Output 119
EMIF2_RNW	3			O	External memory interface 2 read not write
ESC_GPI19	10			I	EtherCAT General-Purpose Input 19
FSIRXD_D1	13			I	FSIRX-D Data Input 1
ENET_MII_TX_ERR	14			O	EMAC MII transmit error
GPIO120	0, 4, 8, 12	U15		I/O	General-Purpose Input Output 120
EMIF2_WEn	3			O	External memory interface 2 write enable
ESC_GPI20	10			I	EtherCAT General-Purpose Input 20
FSIRXD_CLK	13			I	FSIRX-D Input Clock
ENET_MII_TX_CLK	14			I	EMAC MII transmit clock
GPIO121	0, 4, 8, 12	W16		I/O	General-Purpose Input Output 121
EMIF2_OEn	3			O	External memory interface 2 output enable
ESC_GPI21	10			I	EtherCAT General-Purpose Input 21
FSIRXE_D0	13			I	FSIRX-E Data Input 0
ENET_MII_TX_DATA0	14			O	EMAC MII / RMII transmit data 0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO122	0, 4, 8, 12	T8		I/O	General-Purpose Input Output 122
EMIF2_D15	3			I/O	External memory interface 2 data line 15
SPIC_SIMO	6			I/O	SPI-C Slave In, Master Out (SIMO)
SD1_D1	7			I	SDFM-1 Channel 1 Data Input
ESC_GPI22	10			I	EtherCAT General-Purpose Input 22
ENET_MII_TX_DATA1	14			O	EMAC MII / RMII transmit data 1
GPIO123	0, 4, 8, 12	U8		I/O	General-Purpose Input Output 123
EMIF2_D14	3			I/O	External memory interface 2 data line 14
SPIC_SOMI	6			I/O	SPI-C Slave Out, Master In (SOMI)
SD1_C1	7			I	SDFM-1 Channel 1 Clock Input
ESC_GPI23	10			I	EtherCAT General-Purpose Input 23
ENET_MII_TX_DATA2	14			O	EMAC MII transmit data 2
GPIO124	0, 4, 8, 12	V8		I/O	General-Purpose Input Output 124
EMIF2_D13	3			I/O	External memory interface 2 data line 13
SPIC_CLK	6			I/O	SPI-C Clock
SD1_D2	7			I	SDFM-1 Channel 2 Data Input
ESC_GPI24	10			I	EtherCAT General-Purpose Input 24
ENET_MII_TX_DATA3	14			O	EMAC MII transmit data 3
GPIO125	0, 4, 8, 12	T9		I/O	General-Purpose Input Output 125
EMIF2_D12	3			I/O	External memory interface 2 data line 12
SPIC_STEn	6			I/O	SPI-C Slave Transmit Enable (STE)
SD1_C2	7			I	SDFM-1 Channel 2 Clock Input
ESC_GPI25	10			I	EtherCAT General-Purpose Input 25
FSIRXE_D1	13			I	FSIRX-E Data Input 1
ESC_LATCH0	14			I	EtherCAT LatchSignal Input 0
GPIO126	0, 4, 8, 12	U9		I/O	General-Purpose Input Output 126
EMIF2_D11	3			I/O	External memory interface 2 data line 11
SD1_D3	7			I	SDFM-1 Channel 3 Data Input
ESC_GPI26	10			I	EtherCAT General-Purpose Input 26
FSIRXE_CLK	13			I	FSIRX-E Input Clock
ESC_LATCH1	14			I	EtherCAT LatchSignal Input 1
GPIO127	0, 4, 8, 12	V9		I/O	General-Purpose Input Output 127
EMIF2_D10	3			I/O	External memory interface 2 data line 10
SD1_C3	7			I	SDFM-1 Channel 3 Clock Input
ESC_GPI27	10			I	EtherCAT General-Purpose Input 27
ESC_SYNC0	14			O	EtherCAT SyncSignal Output 0
GPIO128	0, 4, 8, 12	W9		I/O	General-Purpose Input Output 128
EMIF2_D9	3			I/O	External memory interface 2 data line 9
SD1_D4	7			I	SDFM-1 Channel 4 Data Input
ESC_GPI28	10			I	EtherCAT General-Purpose Input 28
ESC_SYNC1	14			O	EtherCAT SyncSignal Output 1
GPIO129	0, 4, 8, 12	T10		I/O	General-Purpose Input Output 129
EMIF2_D8	3			I/O	External memory interface 2 data line 8
SD1_C4	7			I	SDFM-1 Channel 4 Clock Input
ESC_GPI29	10			I	EtherCAT General-Purpose Input 29
ESC_TX1_ENA	14			O	EtherCAT MII Transmit-1 Enable

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO130	0, 4, 8, 12	U10		I/O	General-Purpose Input Output 130
EMIF2_D7	3			I/O	External memory interface 2 data line 7
SD2_D1	7			I	SDFM-2 Channel 1 Data Input
ESC_GPI30	10			I	EtherCAT General-Purpose Input 30
ESC_TX1_CLK	14			I	EtherCAT MII Transmit-1 Clock
GPIO131	0, 4, 8, 12	V10		I/O	General-Purpose Input Output 131
EMIF2_D6	3			I/O	External memory interface 2 data line 6
SD2_C1	7			I	SDFM-2 Channel 1 Clock Input
ESC_GPI31	10			I	EtherCAT General-Purpose Input 31
ESC_TX1_DATA0	14			O	EtherCAT MII Transmit-1 Data-0
GPIO132	0, 4, 8, 12	W18		I/O	General-Purpose Input Output 132
EMIF2_D5	3			I/O	External memory interface 2 data line 5
SD2_D2	7			I	SDFM-2 Channel 2 Data Input
ESC_GPO0	10			O	EtherCAT General-Purpose Output 0
ESC_TX1_DATA1	14			O	EtherCAT MII Transmit-1 Data-1
GPIO133	0, 4, 8, 12	G18	118	I/O	General-Purpose Input Output 133
SD2_C2	7			I	SDFM-2 Channel 2 Clock Input
AUXCLKIN	ALT			I	Auxiliary Clock Input
GPIO134	0, 4, 8, 12	V18		I/O	General-Purpose Input Output 134
EMIF2_D4	3			I/O	External memory interface 2 data line 4
SD2_D3	7			I	SDFM-2 Channel 3 Data Input
ESC_GPO1	10			O	EtherCAT General-Purpose Output 1
ESC_TX1_DATA2	14			O	EtherCAT MII Transmit-1 Data-2
GPIO135	0, 4, 8, 12	U18		I/O	General-Purpose Input Output 135
EMIF2_D3	3			I/O	External memory interface 2 data line 3
SCIA_TX	6			O	SCI-A Transmit Data
SD2_C3	7			I	SDFM-2 Channel 3 Clock Input
ESC_GPO2	10			O	EtherCAT General-Purpose Output 2
ESC_TX1_DATA3	14			O	EtherCAT MII Transmit-1 Data-3
GPIO136	0, 4, 8, 12	T17		I/O	General-Purpose Input Output 136
EMIF2_D2	3			I/O	External memory interface 2 data line 2
SCIA_RX	6			I	SCI-A Receive Data
SD2_D4	7			I	SDFM-2 Channel 4 Data Input
ESC_GPO3	10			O	EtherCAT General-Purpose Output 3
ESC_RX1_DV	14			I	EtherCAT MII Receive-1 Data Valid
GPIO137	0, 4, 8, 12	T18		I/O	General-Purpose Input Output 137
EPWM13A	1			O	ePWM-13 Output A (High-res available on ePWM1-8)
EMIF2_D1	3			I/O	External memory interface 2 data line 1
SCIB_TX	6			O	SCI-B Transmit Data
SD2_C4	7			I	SDFM-2 Channel 4 Clock Input
ESC_GPO4	10			O	EtherCAT General-Purpose Output 4
ESC_RX1_CLK	14			I	EtherCAT MII Receive-1 Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO138	0, 4, 8, 12	T19		I/O	General-Purpose Input Output 138
EPWM13B	1			O	ePWM-13 Output B (High-res available on ePWM1-8)
EMIF2_D0	3			I/O	External memory interface 2 data line 0
SCIB_RX	6			I	SCI-B Receive Data
ESC_GPO5	10			O	EtherCAT General-Purpose Output 5
ESC_RX1_ERR	14			I	EtherCAT MII Receive-1 Error
GPIO139	0, 4, 8, 12	N19		I/O	General-Purpose Input Output 139
EPWM14A	1			O	ePWM-14 Output A (High-res available on ePWM1-8)
SCIC_RX	6			I	SCI-C Receive Data
ESC_GPO6	10			O	EtherCAT General-Purpose Output 6
ESC_RX1_DATA0	14			I	EtherCAT MII Receive-1 Data-0
GPIO140	0, 4, 8, 12	M19		I/O	General-Purpose Input Output 140
EPWM14B	1			O	ePWM-14 Output B (High-res available on ePWM1-8)
SCIC_TX	6			O	SCI-C Transmit Data
ESC_GPO7	10			O	EtherCAT General-Purpose Output 7
ESC_RX1_DATA1	14			I	EtherCAT MII Receive-1 Data-1
GPIO141	0, 4, 8, 12	M18		I/O	General-Purpose Input Output 141
EPWM15A	1			O	ePWM-15 Output A (High-res available on ePWM1-8)
SCID_RX	6			I	SCI-D Receive Data
ESC_GPO8	10			O	EtherCAT General-Purpose Output 8
ESC_RX1_DATA2	14			I	EtherCAT MII Receive-1 Data-2
GPIO142	0, 4, 8, 12	L19		I/O	General-Purpose Input Output 142
EPWM15B	1			O	ePWM-15 Output B (High-res available on ePWM1-8)
SCID_TX	6			O	SCI-D Transmit Data
ESC_GPO9	10			O	EtherCAT General-Purpose Output 9
ESC_RX1_DATA3	14			I	EtherCAT MII Receive-1 Data-3
GPIO143	0, 4, 8, 12	F18		I/O	General-Purpose Input Output 143
EPWM16A	1			O	ePWM-16 Output A (High-res available on ePWM1-8)
ESC_GPO10	10			O	EtherCAT General-Purpose Output 10
ESC_LED_LINK0_ACTIVE	14			O	EtherCAT Link-0 Active
GPIO144	0, 4, 8, 12	F17		I/O	General-Purpose Input Output 144
EPWM16B	1			O	ePWM-16 Output B (High-res available on ePWM1-8)
ESC_GPO11	10			O	EtherCAT General-Purpose Output 11
ESC_LED_LINK1_ACTIVE	14			O	EtherCAT Link-1 Active
GPIO145	0, 4, 8, 12	E17		I/O	General-Purpose Input Output 145
EPWM1A	1			O	ePWM-1 Output A (High-res available on ePWM1-8)
ESC_GPO12	10			O	EtherCAT General-Purpose Output 12
ESC_LED_ERR	14			O	EtherCAT Error LED
GPIO146	0, 4, 8, 12	D18		I/O	General-Purpose Input Output 146
EPWM1B	1			O	ePWM-1 Output B (High-res available on ePWM1-8)
ESC_GPO13	10			O	EtherCAT General-Purpose Output 13
ESC_LED_RUN	14			O	EtherCAT Run LED
GPIO147	0, 4, 8, 12	D17		I/O	General-Purpose Input Output 147
EPWM2A	1			O	ePWM-2 Output A (High-res available on ePWM1-8)
ESC_GPO14	10			O	EtherCAT General-Purpose Output 14
ESC_LED_STATE_RUN	14			O	EtherCAT State Run

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO148	0, 4, 8, 12	D14		I/O	General-Purpose Input Output 148
EPWM2B	1			O	ePWM-2 Output B (High-res available on ePWM1-8)
ESC_GPO15	10			O	EtherCAT General-Purpose Output 15
ESC_PHY0_LINKSTATUS	14			I	EtherCAT PHY-0 Link Status
GPIO149	0, 4, 8, 12	A13		I/O	General-Purpose Input Output 149
EPWM3A	1			O	ePWM-3 Output A (High-res available on ePWM1-8)
ESC_GPO16	10			O	EtherCAT General-Purpose Output 16
ESC_PHY1_LINKSTATUS	14			I	EtherCAT PHY-1 Link Status
GPIO150	0, 4, 8, 12	B13		I/O	General-Purpose Input Output 150
EPWM3B	1			O	ePWM-3 Output B (High-res available on ePWM1-8)
ESC_GPO17	10			O	EtherCAT General-Purpose Output 17
ESC_I2C_SDA	14			I/OC	EtherCAT I2C Data
GPIO151	0, 4, 8, 12	C13		I/O	General-Purpose Input Output 151
EPWM4A	1			O	ePWM-4 Output A (High-res available on ePWM1-8)
ESC_GPO18	10			O	EtherCAT General-Purpose Output 18
ESC_I2C_SCL	14			I/OC	EtherCAT I2C Clock
GPIO152	0, 4, 8, 12	D13		I/O	General-Purpose Input Output 152
EPWM4B	1			O	ePWM-4 Output B (High-res available on ePWM1-8)
ESC_GPO19	10			O	EtherCAT General-Purpose Output 19
ESC_MDIO_CLK	14			O	EtherCAT MDIO Clock
GPIO153	0, 4, 8, 12	A12		I/O	General-Purpose Input Output 153
EPWM5A	1			O	ePWM-5 Output A (High-res available on ePWM1-8)
ESC_GPO20	10			O	EtherCAT General-Purpose Output 20
ESC_MDIO_DATA	14			I/O	EtherCAT MDIO Data
GPIO154	0, 4, 8, 12	B12		I/O	General-Purpose Input Output 154
EPWM5B	1			O	ePWM-5 Output B (High-res available on ePWM1-8)
ESC_GPO21	10			O	EtherCAT General-Purpose Output 21
ESC_PHY_CLK	14			O	EtherCAT PHY Clock
GPIO155	0, 4, 8, 12	C12		I/O	General-Purpose Input Output 155
EPWM6A	1			O	ePWM-6 Output A (High-res available on ePWM1-8)
ESC_GPO22	10			O	EtherCAT General-Purpose Output 22
ESC_PHY_RESETn	14			O	EtherCAT PHY Active Low Reset
GPIO156	0, 4, 8, 12	D12		I/O	General-Purpose Input Output 156
EPWM6B	1			O	ePWM-6 Output B (High-res available on ePWM1-8)
ESC_GPO23	10			O	EtherCAT General-Purpose Output 23
ESC_TX0_ENA	14			O	EtherCAT MII Transmit-0 Enable
GPIO157	0, 4, 8, 12	B10		I/O	General-Purpose Input Output 157
EPWM7A	1			O	ePWM-7 Output A (High-res available on ePWM1-8)
ESC_GPO24	10			O	EtherCAT General-Purpose Output 24
ESC_TX0_CLK	14			I	EtherCAT MII Transmit-0 Clock
GPIO158	0, 4, 8, 12	C10		I/O	General-Purpose Input Output 158
EPWM7B	1			O	ePWM-7 Output B (High-res available on ePWM1-8)
ESC_GPO25	10			O	EtherCAT General-Purpose Output 25
ESC_TX0_DATA0	14			O	EtherCAT MII Transmit-0 Data-0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO159	0, 4, 8, 12	D10		I/O	General-Purpose Input Output 159
EPWM8A	1			O	ePWM-8 Output A (High-res available on ePWM1-8)
ESC_GPO26	10			O	EtherCAT General-Purpose Output 26
ESC_TX0_DATA1	14			O	EtherCAT MII Transmit-0 Data-1
GPIO160	0, 4, 8, 12	B9		I/O	General-Purpose Input Output 160
EPWM8B	1			O	ePWM-8 Output B (High-res available on ePWM1-8)
ESC_GPO27	10			O	EtherCAT General-Purpose Output 27
ESC_TX0_DATA2	14			O	EtherCAT MII Transmit-0 Data-2
GPIO161	0, 4, 8, 12	C9		I/O	General-Purpose Input Output 161
EPWM9A	1			O	ePWM-9 Output A (High-res available on ePWM1-8)
ESC_GPO28	10			O	EtherCAT General-Purpose Output 28
ESC_TX0_DATA3	14			O	EtherCAT MII Transmit-0 Data-3
GPIO162	0, 4, 8, 12	D9		I/O	General-Purpose Input Output 162
EPWM9B	1			O	ePWM-9 Output B (High-res available on ePWM1-8)
ESC_GPO29	10			O	EtherCAT General-Purpose Output 29
ESC_RX0_DV	14			I	EtherCAT MII Receive-0 Data Valid
GPIO163	0, 4, 8, 12	A8		I/O	General-Purpose Input Output 163
EPWM10A	1			O	ePWM-10 Output A (High-res available on ePWM1-8)
ESC_GPO30	10			O	EtherCAT General-Purpose Output 30
ESC_RX0_CLK	14			I	EtherCAT MII Receive-0 Clock
GPIO164	0, 4, 8, 12	B8		I/O	General-Purpose Input Output 164
EPWM10B	1			O	ePWM-10 Output B (High-res available on ePWM1-8)
ESC_GPO31	10			O	EtherCAT General-Purpose Output 31
ESC_RX0_ERR	14			I	EtherCAT MII Receive-0 Error
GPIO165	0, 4, 8, 12	C5		I/O	General-Purpose Input Output 165
EPWM11A	1			O	ePWM-11 Output A (High-res available on ePWM1-8)
MDXA	10			O	McBSP-A Transmit Serial Data
ESC_RX0_DATA0	14			I	EtherCAT MII Receive-0 Data-0
GPIO166	0, 4, 8, 12	D5		I/O	General-Purpose Input Output 166
EPWM11B	1			O	ePWM-11 Output B (High-res available on ePWM1-8)
MDRA	10			I	McBSP-A Receive Serial Data
ESC_RX0_DATA1	14			I	EtherCAT MII Receive-0 Data-1
GPIO167	0, 4, 8, 12	C4		I/O	General-Purpose Input Output 167
EPWM12A	1			O	ePWM-12 Output A (High-res available on ePWM1-8)
MCLKXA	10			O	McBSP-A Transmit Clock
ESC_RX0_DATA2	14			I	EtherCAT MII Receive-0 Data-2
GPIO168	0, 4, 8, 12	D4		I/O	General-Purpose Input Output 168
EPWM12B	1			O	ePWM-12 Output B (High-res available on ePWM1-8)
MFSXA	10			O	McBSP-A Transmit Frame Sync
ESC_RX0_DATA3	14			I	EtherCAT MII Receive-0 Data-3
TEST, JTAG, AND RESET					
ERRORSTS		U19	92	O	Error Status Output. When used, this signal requires an external pulldown.
FLT1		W12	73	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
FLT2		V13	74	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.
NC1		H4			No Connection. This pin is not internally connected to the device. This pin may be left open or connected to any voltage within the maximum operating conditions.
NC2		J18	119		No Connection. This pin is not internally connected in the device and may be left open or tied to VSS or VDDIO. NOTE: On other C2000 devices with an internal voltage regulator (VREG), this pin will be VREGENZ (internal voltage regulator enable). To enable PCB compatibility across C2000 devices this pin should be connected to VDDIO (3.3v). This will ensure the internal VREG, when present on other devices, would be disabled and not conflict with an external VREG which must be used with this device.
TCK		V15	81	I	JTAG test clock with internal pullup.
TDI		W13	77	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO		W15	78	O	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.
TMS		W14	80	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
TRSTn		V14	79	I	JTAG test reset with internal pulldown. TRST, when driven high, gives the scan system control of the operations of the device. If this signal is driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: TRST must be maintained low at all times during normal device operation, so an external pulldown resistor is required on this pin for protection against noise spikes. The value of this resistor should be as small as possible, so long as the JTAG debug probe is still able to drive the TRST pin high. A resistor between 2.2 kΩ and 10 kΩ generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debug probe and the application. This pin has an internal 50-ns (nominal) glitch filter.
X1		G19	123	I	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.
X2		J19	121	O	Crystal oscillator output.

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
XRSn		F19	124	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open-drain with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.
POWER AND GROUND					
VDD		E9, E11, F9, F11, G14, G15, J14, J15, K5, K6, P10, P13, R10, R13	61, 76, 117, 126, 137, 153, 158, 169, 16, 21		1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution. A single 56Ω resistor (10% tolerance) should be placed between VDD and VSS. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.
VDD3VFL		R11, R12	72		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin
VDDA		P6, R6	54, 36		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin.
VDDIO		A9, A18, B1, E7, E10, E13, F7, F10, F13, G5, G6, H5, H6, L14, L15, M1, M5, M6, N14, N15, P9, R9, V19, W8, F4, G4, E16, F16	62, 68, 75, 82, 88, 91, 99, 106, 114, 116, 127, 138, 147, 152, 159, 168, 3, 11, 15, 20, 26		3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin.
VDDOSC		H16, H17	120, 125		Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-µF (minimum) decoupling capacitor on each pin.

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
VSS		A1, A10, A19, E5, E6, E8, E12, E14, E15, F5, F6, F8, F12, F14, F15, G16, G17, H8, H9, H10, H11, H12, H14, H15, J5, J6, J8, J9, J10, J11, J12, K8, K9, K10, K11, K12, K14, K15, L5, L6, L8, L9, L10, L11, L12, L18, M8, M9, M10, M11, M12, M14, M15, N1, N5, N6, P7, P8, P11, P12, P14, P15, R7, R8, R14, R15, W7, W19	PAD		Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB.
VSSA		P1, P5, R5, V7, W1	52, 34		Analog Ground
VSSOSC		H18, H19	122		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.

6.3 Signal Descriptions

6.3.1 Analog Signals

Table 6-2. Analog Signals

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ADCIN14	Input 14 to all ADCs. This pin can be used as a general purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference	I		T4	44
ADCIN15	Input 15 to all ADCs. This pin can be used as a general purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference	I		U4	45
ADCINA0	ADC-A Input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.	I		U1	43
ADCINA1	ADC-A Input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.	I		T1	42
ADCINA2	ADC-A Input 2	I		U2	41
ADCINA3	ADC-A Input 3	I		T2	40
ADCINA4	ADC-A Input 4	I		U3	39
ADCINA5	ADC-A Input 5	I		T3	38
ADCINB0	ADC-B Input 0. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-μF capacitor on this pin.	I		V2	46
ADCINB1	ADC-B Input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.	I		W2	47
ADCINB2	ADC-B Input 2	I		V3	48
ADCINB3	ADC-B Input 3	I		W3	49
ADCINB4	ADC-B Input 4	I		V4	
ADCINB5	ADC-B Input 5	I		W4	
ADCINC2	ADC-C Input 2	I		R3	31
ADCINC3	ADC-C Input 3	I		P3	30
ADCINC4	ADC-C Input 4	I		R4	29
ADCINC5	ADC-C Input 5	I		P4	
ADCIND0	ADC-D Input 0	I		T5	56
ADCIND1	ADC-D Input 1	I		U5	57
ADCIND2	ADC-D Input 2	I		T6	58
ADCIND3	ADC-D Input 3	I		U6	59
ADCIND4	ADC-D Input 4	I		T7	60
ADCIND5	ADC-D Input 5	I		U7	
CMPIN1N	Comparator 1 negative input	I		T2	40
CMPIN1P	Comparator 1 positive input	I		U2	41
CMPIN2N	Comparator 2 negative input	I		T3	38
CMPIN2P	Comparator 2 positive input	I		U3	39
CMPIN3N	Comparator 3 negative input	I		W3	49
CMPIN3P	Comparator 3 positive input	I		V3	48
CMPIN4N	Comparator 4 negative input	I		U4	45

Table 6-2. Analog Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
CMPIN4P	Comparator 4 positive input	I		T4	44
CMPIN5N	Comparator 5 negative input	I		P4	
CMPIN5P	Comparator 5 positive input	I		R4	29
CMPIN6N	Comparator 6 negative input	I		P3	30
CMPIN6P	Comparator 6 positive input	I		R3	31
CMPIN7N	Comparator 7 negative input	I		U5	57
CMPIN7P	Comparator 7 positive input	I		T5	56
CMPIN8N	Comparator 8 negative input	I		U6	59
CMPIN8P	Comparator 8 positive input	I		T6	58
DACOUTA	Buffered DAC-A Output.	O		U1	43
DACOUTB	Buffered DAC-B Output.	O		T1	42
DACOUTC	Buffered DAC-C Output.	O		W2	47
VDAC	Optional external reference voltage for on-chip DACs.	I		V2	46
VREFHIA	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. NOTE: Do not load this pin externally	I		V1	37
VREFHIB	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. NOTE: Do not load this pin externally	I		W5	53
VREFHIC	ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. NOTE: Do not load this pin externally	I		R1	35
VREFHID	ADC-D high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHID and VREFLOD pins. NOTE: Do not load this pin externally	I		V5	55
VREFLOA	ADC-A Low Reference	I		R2	33
VREFLOB	ADC-B Low Reference	I		V6	50
VREFLOC	ADC-C Low Reference	I		P2	32
VREFLOD	ADC-D Low Reference	I		W6	51

6.3.2 Digital Signals

Table 6-3. Digital Signals

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ADCSOCAO	ADC Start of Conversion A Output for External ADC (from ePWM modules)	O	8	G2	18
ADCSOCBO	ADC Start of Conversion B Output for External ADC (from ePWM modules)	O	10	B2	1
AUXCLKIN	Auxiliary Clock Input	I	133	G18	118
CANA_RX	CAN-A Receive	I	18, 30, 36, 5, 61, 62, 70	A17, D7, E3, J17, L16, T11, V16	10, 107, 108, 135, 165, 63, 83
CANA_TX	CAN-A Transmit	O	19, 31, 37, 4, 62, 63, 71	B17, C7, E4, J16, J17, U11, U16	108, 109, 12, 136, 164, 66, 84
CANB_RX	CAN-B Receive	I	10, 13, 17, 21, 39, 7, 73	A16, B2, B6, D1, E2, F3, W17	1, 14, 140, 167, 5, 86, 9
CANB_TX	CAN-B Transmit	O	12, 16, 20, 38, 6, 72, 8	A6, B16, C2, E1, F2, G2, T16	13, 139, 166, 18, 4, 8, 85
CLB_OUTPUTXBAR1	CLB Output X-BAR Output 1	O	32, 91	B5, U13	173, 67
CLB_OUTPUTXBAR2	CLB Output X-BAR Output 2	O	33, 92	A4, T13	174, 69
CLB_OUTPUTXBAR3	CLB Output X-BAR Output 3	O	34, 93	B4, U14	175, 70
CLB_OUTPUTXBAR4	CLB Output X-BAR Output 4	O	35, 94	A3, T14	176, 71
CLB_OUTPUTXBAR5	CLB Output X-BAR Output 5	O	36, 95	B3, V16	83
CLB_OUTPUTXBAR6	CLB Output X-BAR Output 6	O	37, 96	C3, U16	84
CLB_OUTPUTXBAR7	CLB Output X-BAR Output 7	O	38, 97	A2, T16	85
CLB_OUTPUTXBAR8	CLB Output X-BAR Output 8	O	39, 98	F1, W17	86
CM-I2CA_SCL	CM-I2C-A Open-Drain Bidirectional Clock	I/OD	1, 105, 32	D8, J3, U13	161, 67
CM-I2CA_SDA	CM-I2C-A Open-Drain Bidirectional Data	I/OD	104, 31	C8, J2, U11	160, 66
EMIF1_CAS	External memory interface 1 column address strobe	O	23, 86, 89	C11, D6, K4	156, 171, 23
EMIF1_CLK	External memory interface 1 clock	O	30	T11	63
EMIF1_OEn	External memory interface 1 output enable	O	32, 37	U13, U16	67, 84
EMIF1_RAS	External memory interface 1 row address strobe	O	22, 87, 90	A5, D11, J4	157, 172, 22
EMIF1_RNW	External memory interface 1 read not write	O	31, 33	T13, U11	66, 69
EMIF1_SDCKE	External memory interface 1 SDRAM clock enable	O	29	W11	65
EMIF1_WAIT	External memory interface 1 Asynchronous SRAM WAIT	I	36	V16	83
EMIF1_WEn	External memory interface 1 write enable	O	31	U11	66
EMIF2_CAS	External memory interface 2 column address strobe	O	113	N4	
EMIF2_CLK	External memory interface 2 clock	O	118	T12	
EMIF2_OEn	External memory interface 2 output enable	O	121	W16	
EMIF2_RAS	External memory interface 2 row address strobe	O	114	N3	
EMIF2_RNW	External memory interface 2 read not write	O	119	T15	

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
EMIF2_SDCKE	External memory interface 2 SDRAM clock enable	O	117	U12	
EMIF2_WAIT	External memory interface 2 Asynchronous SRAM WAIT	I	110	M2	
EMIF2_WEn	External memory interface 2 write enable	O	120	U15	
EMIF1_A0	External memory interface 1 address line 0	O	35, 38	T14, T16	71, 85
EMIF1_A1	External memory interface 1 address line 1	O	36, 39	V16, W17	83, 86
EMIF1_A2	External memory interface 1 address line 2	O	37, 40	U16, V17	84, 87
EMIF1_A3	External memory interface 1 address line 3	O	38, 41	T16, U17	85, 89
EMIF1_A4	External memory interface 1 address line 4	O	39, 44	K18, W17	113, 86
EMIF1_A5	External memory interface 1 address line 5	O	45, 49	K19, R17	115, 93
EMIF1_A6	External memory interface 1 address line 6	O	46, 50	E19, R18	128, 94
EMIF1_A7	External memory interface 1 address line 7	O	47, 51	E18, R19	129, 95
EMIF1_A8	External memory interface 1 address line 8	O	48, 52	P16, R16	90, 96
EMIF1_A9	External memory interface 1 address line 9	O	49, 53	P17, R17	93, 97
EMIF1_A10	External memory interface 1 address line 10	O	50, 54	P18, R18	94, 98
EMIF1_A11	External memory interface 1 address line 11	O	51	R19	95
EMIF1_A12	External memory interface 1 address line 12	O	52	P16	96
EMIF1_A13	External memory interface 1 address line 13	O	86	C11	156
EMIF1_A14	External memory interface 1 address line 14	O	87	D11	157
EMIF1_A15	External memory interface 1 address line 15	O	88	C6	170
EMIF1_A16	External memory interface 1 address line 16	O	89	D6	171
EMIF1_A17	External memory interface 1 address line 17	O	90	A5	172
EMIF1_A18	External memory interface 1 address line 18	O	91	B5	173
EMIF1_A19	External memory interface 1 address line 19	O	92	A4	174
EMIF1_BA0	External memory interface 1 bank address 0	O	20, 33, 93	B4, F2, T13	13, 175, 69
EMIF1_BA1	External memory interface 1 bank address 1	O	21, 34, 92, 94	A3, A4, F3, U14	14, 174, 176, 70
EMIF1_CS0n	External memory interface 1 chip select 0	O	32	U13	67
EMIF1_CS2n	External memory interface 1 chip select 2	O	18, 28, 34	E3, U14, V11	10, 64, 70
EMIF1_CS3n	External memory interface 1 chip select 3	O	19, 29, 35	E4, T14, W11	12, 65, 71
EMIF1_CS4n	External memory interface 1 chip select 4	O	28, 30	T11, V11	63, 64
EMIF1_D0	External memory interface 1 data line 0	I/O	55, 85	B11, P19	100, 155
EMIF1_D1	External memory interface 1 data line 1	I/O	56, 83	C14, N16	101, 151
EMIF1_D2	External memory interface 1 data line 2	I/O	57, 82	B14, N18	102, 150
EMIF1_D3	External memory interface 1 data line 3	I/O	58, 81	A14, N17	103, 149
EMIF1_D4	External memory interface 1 data line 4	I/O	59, 80	D15, M16	104, 148
EMIF1_D5	External memory interface 1 data line 5	I/O	60, 79	C15, M17	105, 146
EMIF1_D6	External memory interface 1 data line 6	I/O	61, 78	B15, L16	107, 145
EMIF1_D7	External memory interface 1 data line 7	I/O	62, 77	A15, J17	108, 144
EMIF1_D8	External memory interface 1 data line 8	I/O	76	C16	143
EMIF1_D9	External memory interface 1 data line 9	I/O	75	D16	142
EMIF1_D10	External memory interface 1 data line 10	I/O	74	C17	141
EMIF1_D11	External memory interface 1 data line 11	I/O	73	A16	140

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
EMIF1_D12	External memory interface 1 data line 12	I/O	72	B16	139
EMIF1_D13	External memory interface 1 data line 13	I/O	71	B17	136
EMIF1_D14	External memory interface 1 data line 14	I/O	70	A17	135
EMIF1_D15	External memory interface 1 data line 15	I/O	69	B18	134
EMIF1_D16	External memory interface 1 data line 16	I/O	68	C18	133
EMIF1_D17	External memory interface 1 data line 17	I/O	67	B19	132
EMIF1_D18	External memory interface 1 data line 18	I/O	66	K17	112
EMIF1_D19	External memory interface 1 data line 19	I/O	65	K16	111
EMIF1_D20	External memory interface 1 data line 20	I/O	64	L17	110
EMIF1_D21	External memory interface 1 data line 21	I/O	63	J16	109
EMIF1_D22	External memory interface 1 data line 22	I/O	62	J17	108
EMIF1_D23	External memory interface 1 data line 23	I/O	61	L16	107
EMIF1_D24	External memory interface 1 data line 24	I/O	60	M17	105
EMIF1_D25	External memory interface 1 data line 25	I/O	59	M16	104
EMIF1_D26	External memory interface 1 data line 26	I/O	58	N17	103
EMIF1_D27	External memory interface 1 data line 27	I/O	57	N18	102
EMIF1_D28	External memory interface 1 data line 28	I/O	56	N16	101
EMIF1_D29	External memory interface 1 data line 29	I/O	55	P19	100
EMIF1_D30	External memory interface 1 data line 30	I/O	54	P18	98
EMIF1_D31	External memory interface 1 data line 31	I/O	53	P17	97
EMIF1_DQM0	External memory interface 1 Input/output mask for byte 0	O	24, 88, 92	A4, C6, K3	170, 174, 24
EMIF1_DQM1	External memory interface 1 Input/output mask for byte 1	O	25, 88, 89	C6, D6, K2	170, 171, 25
EMIF1_DQM2	External memory interface 1 Input/output mask for byte 2	O	26, 90, 91	A5, B5, K1	172, 173, 27
EMIF1_DQM3	External memory interface 1 Input/output mask for byte 3	O	27, 87, 91	B5, D11, L1	157, 173, 28
EMIF2_A0	External memory interface 2 address line 0	O	98	F1	
EMIF2_A1	External memory interface 2 address line 1	O	99	G1	17
EMIF2_A2	External memory interface 2 address line 2	O	100	H1	
EMIF2_A3	External memory interface 2 address line 3	O	101	H2	
EMIF2_A4	External memory interface 2 address line 4	O	102	H3	
EMIF2_A5	External memory interface 2 address line 5	O	103	J1	
EMIF2_A6	External memory interface 2 address line 6	O	104	J2	
EMIF2_A7	External memory interface 2 address line 7	O	105	J3	
EMIF2_A8	External memory interface 2 address line 8	O	106	L2	
EMIF2_A9	External memory interface 2 address line 9	O	107	L3	
EMIF2_A10	External memory interface 2 address line 10	O	108	L4	
EMIF2_A11	External memory interface 2 address line 11	O	109	N2	
EMIF2_A12	External memory interface 2 address line 12	O	95	B3	
EMIF2_BA0	External memory interface 2 bank address 0	O	111	M4	
EMIF2_BA1	External memory interface 2 bank address 1	O	112	M3	
EMIF2_CS0n	External memory interface 2 chip select 0	O	115	V12	
EMIF2_CS2n	External memory interface 2 chip select 2	O	116	W10	
EMIF2_D0	External memory interface 2 data line 0	I/O	138, 68	C18, T19	133

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
EMIF2_D1	External memory interface 2 data line 1	I/O	137, 67	B19, T18	132
EMIF2_D2	External memory interface 2 data line 2	I/O	136, 66	K17, T17	112
EMIF2_D3	External memory interface 2 data line 3	I/O	135, 65	K16, U18	111
EMIF2_D4	External memory interface 2 data line 4	I/O	134, 64	L17, V18	110
EMIF2_D5	External memory interface 2 data line 5	I/O	132, 63	J16, W18	109
EMIF2_D6	External memory interface 2 data line 6	I/O	131, 62	J17, V10	108
EMIF2_D7	External memory interface 2 data line 7	I/O	130, 61	L16, U10	107
EMIF2_D8	External memory interface 2 data line 8	I/O	129, 60	M17, T10	105
EMIF2_D9	External memory interface 2 data line 9	I/O	128, 59	M16, W9	104
EMIF2_D10	External memory interface 2 data line 10	I/O	127, 58	N17, V9	103
EMIF2_D11	External memory interface 2 data line 11	I/O	126, 57	N18, U9	102
EMIF2_D12	External memory interface 2 data line 12	I/O	125, 56	N16, T9	101
EMIF2_D13	External memory interface 2 data line 13	I/O	124, 55	P19, V8	100
EMIF2_D14	External memory interface 2 data line 14	I/O	123, 54	P18, U8	98
EMIF2_D15	External memory interface 2 data line 15	I/O	122, 53	P17, T8	97
EMIF2_DQM0	External memory interface 2 Input/output mask for byte 0	O	97	A2	
EMIF2_DQM1	External memory interface 2 Input/output mask for byte 1	O	96	C3	
ENET_MDIO_CLK	EMAC management data clock, Output in MII/RMII modes, Input in RevMII mode	I/O	105, 42	D19, J3	130
ENET_MDIO_DATA	EMAC management data	I/O	106, 43	C19, L2	131
ENET_MII_COL	EMAC MII collision detect	I	110, 35, 39, 41	M2, T14, U17, W17	71, 86, 89
ENET_MII_CRS	EMAC MII carrier sense	I	109, 34, 38, 40	N2, T16, U14, V17	70, 85, 87
ENET_MII_INTR	EMAC PHY interrupt, Input in MII/RMII mode, Output in RevMII mode	I/O	108, 68	C18, L4	133
ENET_MII_RX_CLK	EMAC MII receive clock	I	111, 49, 67, 69	B18, B19, M4, R17	132, 134, 93
ENET_MII_RX_DATA0	EMAC MII / RMII receive data 0	I	114, 52, 63, 66, 71	B17, J16, K17, N3, P16	109, 112, 136, 96
ENET_MII_RX_DATA1	EMAC MII / RMII receive data 1	I	115, 53, 64, 72	B16, L17, P17, V12	110, 139, 97
ENET_MII_RX_DATA2	EMAC MII receive data 2	I	116, 54, 65	K16, P18, W10	111, 98
ENET_MII_RX_DATA3	EMAC MII receive data 3	I	117, 55, 66	K17, P19, U12	100, 112
ENET_MII_RX_DV	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid	I	112, 38, 50, 64, 70	A17, L17, M3, R18, T16	110, 135, 85, 94
ENET_MII_RX_ERR	EMAC MII / RMII receive error	I	113, 39, 51, 65, 71, 76	B17, C16, K16, N4, R19, W17	111, 136, 143, 86, 95
ENET_MII_TX_CLK	EMAC MII transmit clock	I	120, 44, 58	K18, N17, U15	103, 113

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ENET_MII_TX_DATA0	EMAC MII / RMII transmit data 0	O	121, 59, 75	D16, M16, W16	104, 142
ENET_MII_TX_DATA1	EMAC MII / RMII transmit data 1	O	122, 60, 74	C17, M17, T8	105, 141
ENET_MII_TX_DATA2	EMAC MII transmit data 2	O	123, 61, 73	A16, L16, U8	107, 140
ENET_MII_TX_DATA3	EMAC MII transmit data 3	O	124, 62, 72	B16, J17, V8	108, 139
ENET_MII_TX_EN	EMAC MII / RMII transmit enable	O	118, 45, 56, 69	B18, K19, N16, T12	101, 115, 134
ENET_MII_TX_ERR	EMAC MII transmit error	O	119, 46, 57	E19, N18, T15	102, 128
ENET_PPS0	EMAC Pulse Per Second Output 0	O	47	E18	129
ENET_PPS1	EMAC Pulse Per Second Output 1	O	48	R16	90
ENET_REVMII_MDIO_RST	EMAC REVMII MDIO reset	I	107, 41, 67	B19, L3, U17	132, 89
ENET_RMII_CLK	EMAC RMII clock	I/O	73	A16	140
EPWM10A	ePWM-10 Output A (High-res available on ePWM1-8)	O	163, 18	A8, E3	10
EPWM10B	ePWM-10 Output B (High-res available on ePWM1-8)	O	164, 19	B8, E4	12
EPWM11A	ePWM-11 Output A (High-res available on ePWM1-8)	O	165, 20	C5, F2	13
EPWM11B	ePWM-11 Output B (High-res available on ePWM1-8)	O	166, 21	D5, F3	14
EPWM12A	ePWM-12 Output A (High-res available on ePWM1-8)	O	167, 22	C4, J4	22
EPWM12B	ePWM-12 Output B (High-res available on ePWM1-8)	O	168, 23	D4, K4	23
EPWM13A	ePWM-13 Output A (High-res available on ePWM1-8)	O	137, 24	K3, T18	24
EPWM13B	ePWM-13 Output B (High-res available on ePWM1-8)	O	138, 25	K2, T19	25
EPWM14A	ePWM-14 Output A (High-res available on ePWM1-8)	O	139, 26	K1, N19	27
EPWM14B	ePWM-14 Output B (High-res available on ePWM1-8)	O	140, 27	L1, M19	28
EPWM15A	ePWM-15 Output A (High-res available on ePWM1-8)	O	141, 28	M18, V11	64
EPWM15B	ePWM-15 Output B (High-res available on ePWM1-8)	O	142, 29	L19, W11	65
EPWM16A	ePWM-16 Output A (High-res available on ePWM1-8)	O	143, 30	F18, T11	63
EPWM16B	ePWM-16 Output B (High-res available on ePWM1-8)	O	144, 31	F17, U11	66
EPWM1A	ePWM-1 Output A (High-res available on ePWM1-8)	O	145	C8, E17	160
EPWM1B	ePWM-1 Output B (High-res available on ePWM1-8)	O	1, 146	D18, D8	161
EPWM2A	ePWM-2 Output A (High-res available on ePWM1-8)	O	147, 2	A7, D17	162
EPWM2B	ePWM-2 Output B (High-res available on ePWM1-8)	O	148, 3	B7, D14	163
EPWM3A	ePWM-3 Output A (High-res available on ePWM1-8)	O	149, 4	A13, C7	164
EPWM3B	ePWM-3 Output B (High-res available on ePWM1-8)	O	150, 5	B13, D7	165
EPWM4A	ePWM-4 Output A (High-res available on ePWM1-8)	O	151, 6	A6, C13	166
EPWM4B	ePWM-4 Output B (High-res available on ePWM1-8)	O	152, 7	B6, D13	167
EPWM5A	ePWM-5 Output A (High-res available on ePWM1-8)	O	153, 8	A12, G2	18
EPWM5B	ePWM-5 Output B (High-res available on ePWM1-8)	O	154, 9	B12, G3	19
EPWM6A	ePWM-6 Output A (High-res available on ePWM1-8)	O	10, 155	B2, C12	1
EPWM6B	ePWM-6 Output B (High-res available on ePWM1-8)	O	11, 156	C1, D12	2
EPWM7A	ePWM-7 Output A (High-res available on ePWM1-8)	O	12, 157	B10, C2	4
EPWM7B	ePWM-7 Output B (High-res available on ePWM1-8)	O	13, 158	C10, D1	5
EPWM8A	ePWM-8 Output A (High-res available on ePWM1-8)	O	14, 159	D10, D2	6

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
EPWM8B	ePWM-8 Output B (High-res available on ePWM1-8)	O	15, 160	B9, D3	7
EPWM9A	ePWM-9 Output A (High-res available on ePWM1-8)	O	16, 161	C9, E1	8
EPWM9B	ePWM-9 Output B (High-res available on ePWM1-8)	O	162, 17	D9, E2	9
EQEP1_A	eQEP-1 Input A	I	10, 20, 50, 96	B2, C3, F2, R18	1, 13, 94
EQEP1_B	eQEP-1 Input B	I	11, 21, 51, 97	A2, C1, F3, R19	14, 2, 95
EQEP1_INDEX	eQEP-1 Index	I/O	13, 23, 53, 99	D1, G1, K4, P17	17, 23, 5, 97
EQEP1_STROBE	eQEP-1 Strobe	I/O	12, 22, 52, 98	C2, F1, J4, P16	22, 4, 96
EQEP2_A	eQEP-2 Input A	I	100, 24, 54, 78	B15, H1, K3, P18	145, 24, 98
EQEP2_B	eQEP-2 Input B	I	101, 25, 55, 79	C15, H2, K2, P19	100, 146, 25
EQEP2_INDEX	eQEP-2 Index	I/O	103, 26, 57, 81	A14, J1, K1, N18	102, 149, 27
EQEP2_STROBE	eQEP-2 Strobe	I/O	102, 27, 56, 80	D15, H3, L1, N16	101, 148, 28
EQEP3_A	eQEP-3 Input A	I	104, 28, 6, 62	A6, J17, J2, V11	108, 166, 64
EQEP3_B	eQEP-3 Input B	I	105, 29, 63, 7	B6, J16, J3, W11	109, 167, 65
EQEP3_INDEX	eQEP-3 Index	I/O	107, 31, 65, 9	G3, K16, L3, U11	111, 19, 66
EQEP3_STROBE	eQEP-3 Strobe	I/O	106, 30, 64, 8	G2, L17, L2, T11	110, 18, 63
ESC_GPI0	EtherCAT General-Purpose Input 0	I	100	C8, H1	160
ESC_GPI1	EtherCAT General-Purpose Input 1	I	1, 101	D8, H2	161
ESC_GPI2	EtherCAT General-Purpose Input 2	I	102, 2	A7, H3	162
ESC_GPI3	EtherCAT General-Purpose Input 3	I	103, 3	B7, J1	163
ESC_GPI4	EtherCAT General-Purpose Input 4	I	104, 4	C7, J2	164
ESC_GPI5	EtherCAT General-Purpose Input 5	I	105, 5	D7, J3	165
ESC_GPI6	EtherCAT General-Purpose Input 6	I	106, 6	A6, L2	166
ESC_GPI7	EtherCAT General-Purpose Input 7	I	107, 7	B6, L3	167
ESC_GPI8	EtherCAT General-Purpose Input 8	I	108	L4	
ESC_GPI9	EtherCAT General-Purpose Input 9	I	109	N2	
ESC_GPI10	EtherCAT General-Purpose Input 10	I	110	M2	
ESC_GPI11	EtherCAT General-Purpose Input 11	I	111	M4	
ESC_GPI12	EtherCAT General-Purpose Input 12	I	112	M3	
ESC_GPI13	EtherCAT General-Purpose Input 13	I	113	N4	
ESC_GPI14	EtherCAT General-Purpose Input 14	I	114	N3	
ESC_GPI15	EtherCAT General-Purpose Input 15	I	115	V12	
ESC_GPI16	EtherCAT General-Purpose Input 16	I	116	W10	
ESC_GPI17	EtherCAT General-Purpose Input 17	I	117	U12	
ESC_GPI18	EtherCAT General-Purpose Input 18	I	118	T12	
ESC_GPI19	EtherCAT General-Purpose Input 19	I	119	T15	
ESC_GPI20	EtherCAT General-Purpose Input 20	I	120	U15	

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ESC_GPI21	EtherCAT General-Purpose Input 21	I	121	W16	
ESC_GPI22	EtherCAT General-Purpose Input 22	I	122	T8	
ESC_GPI23	EtherCAT General-Purpose Input 23	I	123	U8	
ESC_GPI24	EtherCAT General-Purpose Input 24	I	124	V8	
ESC_GPI25	EtherCAT General-Purpose Input 25	I	125	T9	
ESC_GPI26	EtherCAT General-Purpose Input 26	I	126	U9	
ESC_GPI27	EtherCAT General-Purpose Input 27	I	127	V9	
ESC_GPI28	EtherCAT General-Purpose Input 28	I	128	W9	
ESC_GPI29	EtherCAT General-Purpose Input 29	I	129	T10	
ESC_GPI30	EtherCAT General-Purpose Input 30	I	130	U10	
ESC_GPI31	EtherCAT General-Purpose Input 31	I	131	V10	
ESC_GPO0	EtherCAT General-Purpose Output 0	O	132, 8	G2, W18	18
ESC_GPO1	EtherCAT General-Purpose Output 1	O	134, 9	G3, V18	19
ESC_GPO2	EtherCAT General-Purpose Output 2	O	10, 135	B2, U18	1
ESC_GPO3	EtherCAT General-Purpose Output 3	O	11, 136	C1, T17	2
ESC_GPO4	EtherCAT General-Purpose Output 4	O	12, 137	C2, T18	4
ESC_GPO5	EtherCAT General-Purpose Output 5	O	13, 138	D1, T19	5
ESC_GPO6	EtherCAT General-Purpose Output 6	O	139, 14	D2, N19	6
ESC_GPO7	EtherCAT General-Purpose Output 7	O	140, 15	D3, M19	7
ESC_GPO8	EtherCAT General-Purpose Output 8	O	141	M18	
ESC_GPO9	EtherCAT General-Purpose Output 9	O	142	L19	
ESC_GPO10	EtherCAT General-Purpose Output 10	O	143	F18	
ESC_GPO11	EtherCAT General-Purpose Output 11	O	144	F17	
ESC_GPO12	EtherCAT General-Purpose Output 12	O	145	E17	
ESC_GPO13	EtherCAT General-Purpose Output 13	O	146	D18	
ESC_GPO14	EtherCAT General-Purpose Output 14	O	147	D17	
ESC_GPO15	EtherCAT General-Purpose Output 15	O	148	D14	
ESC_GPO16	EtherCAT General-Purpose Output 16	O	149	A13	
ESC_GPO17	EtherCAT General-Purpose Output 17	O	150	B13	
ESC_GPO18	EtherCAT General-Purpose Output 18	O	151	C13	
ESC_GPO19	EtherCAT General-Purpose Output 19	O	152	D13	
ESC_GPO20	EtherCAT General-Purpose Output 20	O	153	A12	
ESC_GPO21	EtherCAT General-Purpose Output 21	O	154	B12	
ESC_GPO22	EtherCAT General-Purpose Output 22	O	155	C12	
ESC_GPO23	EtherCAT General-Purpose Output 23	O	156	D12	
ESC_GPO24	EtherCAT General-Purpose Output 24	O	157	B10	
ESC_GPO25	EtherCAT General-Purpose Output 25	O	158	C10	
ESC_GPO26	EtherCAT General-Purpose Output 26	O	159	D10	
ESC_GPO27	EtherCAT General-Purpose Output 27	O	160	B9	
ESC_GPO28	EtherCAT General-Purpose Output 28	O	161	C9	
ESC_GPO29	EtherCAT General-Purpose Output 29	O	162	D9	
ESC_GPO30	EtherCAT General-Purpose Output 30	O	163	A8	
ESC_GPO31	EtherCAT General-Purpose Output 31	O	164	B8	
ESC_I2C_SCL	EtherCAT I2C Clock	I/OC	151, 30, 41	C13, T11, U17	63, 89

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ESC_I2C_SDA	EtherCAT I2C Data	I/OC	150, 29, 40	B13, V17, W11	65, 87
ESC_LATCH0	EtherCAT LatchSignal Input 0	I	125, 29, 34	T9, U14, W11	65, 70
ESC_LATCH1	EtherCAT LatchSignal Input 1	I	126, 30, 35	T11, T14, U9	63, 71
ESC_LED_ERR	EtherCAT Error LED	O	145, 60	E17, M17	105
ESC_LED_LINK0_ACTIVE	EtherCAT Link-0 Active	O	143, 58	F18, N17	103
ESC_LED_LINK1_ACTIVE	EtherCAT Link-1 Active	O	144, 59	F17, M16	104
ESC_LED_RUN	EtherCAT Run LED	O	146, 61	D18, L16	107
ESC_LED_STATE_RUN	EtherCAT State Run	O	147, 62	D17, J17	108
ESC_MDIO_CLK	EtherCAT MDIO Clock	O	152, 26, 46	D13, E19, K1	128, 27
ESC_MDIO_DATA	EtherCAT MDIO Data	I/O	153, 27, 47	A12, E18, L1	129, 28
ESC_PHY0_LINKSTATUS	EtherCAT PHY-0 Link Status	I	148, 86	C11, D14	156
ESC_PHY1_LINKSTATUS	EtherCAT PHY-1 Link Status	I	149, 68	A13, C18	133
ESC_PHY_CLK	EtherCAT PHY Clock	O	154, 48	B12, R16	90
ESC_PHY_RESETn	EtherCAT PHY Active Low Reset	O	155, 76	C12, C16	143
ESC_RX0_CLK	EtherCAT MII Receive-0 Clock	I	163, 77	A15, A8	144
ESC_RX0_DV	EtherCAT MII Receive-0 Data Valid	I	162, 78	B15, D9	145
ESC_RX0_ERR	EtherCAT MII Receive-0 Error	I	164, 79	B8, C15	146
ESC_RX1_CLK	EtherCAT MII Receive-1 Clock	I	137, 69	B18, T18	134
ESC_RX1_DV	EtherCAT MII Receive-1 Data Valid	I	136, 70	A17, T17	135
ESC_RX1_ERR	EtherCAT MII Receive-1 Error	I	138, 71	B17, T19	136
ESC_RX0_DATA0	EtherCAT MII Receive-0 Data-0	I	165, 80	C5, D15	148
ESC_RX0_DATA1	EtherCAT MII Receive-0 Data-1	I	166, 81	A14, D5	149
ESC_RX0_DATA2	EtherCAT MII Receive-0 Data-2	I	167, 82	B14, C4	150
ESC_RX0_DATA3	EtherCAT MII Receive-0 Data-3	I	168, 83	C14, D4	151
ESC_RX1_DATA0	EtherCAT MII Receive-1 Data-0	I	139, 63	J16, N19	109
ESC_RX1_DATA1	EtherCAT MII Receive-1 Data-1	I	140, 64	L17, M19	110
ESC_RX1_DATA2	EtherCAT MII Receive-1 Data-2	I	141, 65	K16, M18	111
ESC_RX1_DATA3	EtherCAT MII Receive-1 Data-3	I	142, 66	K17, L19	112
ESC_SYNC0	EtherCAT SyncSignal Output 0	O	127, 29, 34	U14, V9, W11	65, 70
ESC_SYNC1	EtherCAT SyncSignal Output 1	O	128, 30, 35	T11, T14, W9	63, 71
ESC_TX0_CLK	EtherCAT MII Transmit-0 Clock	I	157, 85	B10, B11	155
ESC_TX0_ENA	EtherCAT MII Transmit-0 Enable	O	156, 84	A11, D12	154
ESC_TX1_CLK	EtherCAT MII Transmit-1 Clock	I	130, 44	K18, U10	113
ESC_TX1_ENA	EtherCAT MII Transmit-1 Enable	O	129, 45	K19, T10	115
ESC_TX0_DATA0	EtherCAT MII Transmit-0 Data-0	O	158, 87	C10, D11	157
ESC_TX0_DATA1	EtherCAT MII Transmit-0 Data-1	O	159, 88	C6, D10	170
ESC_TX0_DATA2	EtherCAT MII Transmit-0 Data-2	O	160, 89	B9, D6	171
ESC_TX0_DATA3	EtherCAT MII Transmit-0 Data-3	O	161, 90	A5, C9	172
ESC_TX1_DATA0	EtherCAT MII Transmit-1 Data-0	O	131, 75	D16, V10	142

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ESC_TX1_DATA1	EtherCAT MII Transmit-1 Data-1	O	132, 74	C17, W18	141
ESC_TX1_DATA2	EtherCAT MII Transmit-1 Data-2	O	134, 73	A16, V18	140
ESC_TX1_DATA3	EtherCAT MII Transmit-1 Data-3	O	135, 72	B16, U18	139
EXTSYNCOUT	External ePWM Synchronization Pulse	O	6	A6	166
FSIRXA_CLK	FSIRX-A Input Clock	I	105, 13, 5, 54, 9	D1, D7, G3, J3, P18	165, 19, 5, 98
FSIRXA_D0	FSIRX-A Data Input 0	I	103, 12, 3, 52, 8	B7, C2, G2, J1, P16	163, 18, 4, 96
FSIRXA_D1	FSIRX-A Data Input 1	I	10, 104, 11, 4, 53	B2, C1, C7, J2, P17	1, 164, 2, 97
FSIRXB_CLK	FSIRX-B Input Clock	I	11, 112, 60	C1, M17, M3	105, 2
FSIRXB_D0	FSIRX-B Data Input 0	I	110, 58, 9	G3, M2, N17	103, 19
FSIRXB_D1	FSIRX-B Data Input 1	I	10, 111, 59	B2, M16, M4	1, 104
FSIRXC_CLK	FSIRX-C Input Clock	I	117, 14	D2, U12	6
FSIRXC_D0	FSIRX-C Data Input 0	I	115, 12	C2, V12	4
FSIRXC_D1	FSIRX-C Data Input 1	I	116, 13	D1, W10	5
FSIRXD_CLK	FSIRX-D Input Clock	I	120, 17	E2, U15	9
FSIRXD_D0	FSIRX-D Data Input 0	I	118, 15	D3, T12	7
FSIRXD_D1	FSIRX-D Data Input 1	I	119, 16	E1, T15	8
FSIRXE_CLK	FSIRX-E Input Clock	I	126, 20	F2, U9	13
FSIRXE_D0	FSIRX-E Data Input 0	I	121, 18	E3, W16	10
FSIRXE_D1	FSIRX-E Data Input 1	I	125, 19	E4, T9	12
FSIRXF_CLK	FSIRX-F Input Clock	I	23, 93	B4, K4	175, 23
FSIRXF_D0	FSIRX-F Data Input 0	I	21, 91	B5, F3	14, 173
FSIRXF_D1	FSIRX-F Data Input 1	I	22, 92	A4, J4	174, 22
FSIRXG_CLK	FSIRX-G Input Clock	I	26, 96	C3, K1	27
FSIRXG_D0	FSIRX-G Data Input 0	I	24, 94	A3, K3	176, 24
FSIRXG_D1	FSIRX-G Data Input 1	I	25, 95	B3, K2	25
FSIRXH_CLK	FSIRX-H Input Clock	I	29, 99	G1, W11	17, 65
FSIRXH_D0	FSIRX-H Data Input 0	I	27, 97	A2, L1	28
FSIRXH_D1	FSIRX-H Data Input 1	I	28, 98	F1, V11	64
FSITXA_CLK	FSITX-A Output Clock	O	10, 102, 2, 27, 51	A7, B2, H3, L1, R19	1, 162, 28, 95
FSITXA_D0	FSITX-A Data Output 0	O	100, 26, 49, 9	C8, G3, H1, K1, R17	160, 19, 27, 93
FSITXA_D1	FSITX-A Data Output 1	O	1, 101, 25, 50, 8	D8, G2, H2, K2, R18	161, 18, 25, 94
FSITXB_CLK	FSITX-B Output Clock	O	108, 56, 8	G2, L4, N16	101, 18

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
FSITXB_D0	FSITX-B Data Output 0	O	106, 55, 6	A6, L2, P19	100, 166
FSITXB_D1	FSITX-B Data Output 1	O	107, 57, 7	B6, L3, N18	102, 167
GPIO0	General-Purpose Input Output 0	I/O		C8	160
GPIO1	General-Purpose Input Output 1	I/O	1	D8	161
GPIO2	General-Purpose Input Output 2	I/O	2	A7	162
GPIO3	General-Purpose Input Output 3	I/O	3	B7	163
GPIO4	General-Purpose Input Output 4	I/O	4	C7	164
GPIO5	General-Purpose Input Output 5	I/O	5	D7	165
GPIO6	General-Purpose Input Output 6	I/O	6	A6	166
GPIO7	General-Purpose Input Output 7	I/O	7	B6	167
GPIO8	General-Purpose Input Output 8	I/O	8	G2	18
GPIO9	General-Purpose Input Output 9	I/O	9	G3	19
GPIO10	General-Purpose Input Output 10	I/O	10	B2	1
GPIO11	General-Purpose Input Output 11	I/O	11	C1	2
GPIO12	General-Purpose Input Output 12	I/O	12	C2	4
GPIO13	General-Purpose Input Output 13	I/O	13	D1	5
GPIO14	General-Purpose Input Output 14	I/O	14	D2	6
GPIO15	General-Purpose Input Output 15	I/O	15	D3	7
GPIO16	General-Purpose Input Output 16	I/O	16	E1	8
GPIO17	General-Purpose Input Output 17	I/O	17	E2	9
GPIO18	General-Purpose Input Output 18	I/O	18	E3	10
GPIO19	General-Purpose Input Output 19	I/O	19	E4	12
GPIO100	General-Purpose Input Output 100	I/O	100	H1	
GPIO101	General-Purpose Input Output 101	I/O	101	H2	
GPIO102	General-Purpose Input Output 102	I/O	102	H3	
GPIO103	General-Purpose Input Output 103	I/O	103	J1	
GPIO104	General-Purpose Input Output 104	I/O	104	J2	
GPIO105	General-Purpose Input Output 105	I/O	105	J3	
GPIO106	General-Purpose Input Output 106	I/O	106	L2	
GPIO107	General-Purpose Input Output 107	I/O	107	L3	
GPIO108	General-Purpose Input Output 108	I/O	108	L4	
GPIO109	General-Purpose Input Output 109	I/O	109	N2	
GPIO110	General-Purpose Input Output 110	I/O	110	M2	
GPIO111	General-Purpose Input Output 111	I/O	111	M4	
GPIO112	General-Purpose Input Output 112	I/O	112	M3	
GPIO113	General-Purpose Input Output 113	I/O	113	N4	
GPIO114	General-Purpose Input Output 114	I/O	114	N3	
GPIO115	General-Purpose Input Output 115	I/O	115	V12	
GPIO116	General-Purpose Input Output 116	I/O	116	W10	
GPIO117	General-Purpose Input Output 117	I/O	117	U12	
GPIO118	General-Purpose Input Output 118	I/O	118	T12	
GPIO119	General-Purpose Input Output 119	I/O	119	T15	
GPIO120	General-Purpose Input Output 120	I/O	120	U15	

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
GPIO121	General-Purpose Input Output 121	I/O	121	W16	
GPIO122	General-Purpose Input Output 122	I/O	122	T8	
GPIO123	General-Purpose Input Output 123	I/O	123	U8	
GPIO124	General-Purpose Input Output 124	I/O	124	V8	
GPIO125	General-Purpose Input Output 125	I/O	125	T9	
GPIO126	General-Purpose Input Output 126	I/O	126	U9	
GPIO127	General-Purpose Input Output 127	I/O	127	V9	
GPIO128	General-Purpose Input Output 128	I/O	128	W9	
GPIO129	General-Purpose Input Output 129	I/O	129	T10	
GPIO130	General-Purpose Input Output 130	I/O	130	U10	
GPIO131	General-Purpose Input Output 131	I/O	131	V10	
GPIO132	General-Purpose Input Output 132	I/O	132	W18	
GPIO133	General-Purpose Input Output 133	I/O	133	G18	118
GPIO134	General-Purpose Input Output 134	I/O	134	V18	
GPIO135	General-Purpose Input Output 135	I/O	135	U18	
GPIO136	General-Purpose Input Output 136	I/O	136	T17	
GPIO137	General-Purpose Input Output 137	I/O	137	T18	
GPIO138	General-Purpose Input Output 138	I/O	138	T19	
GPIO139	General-Purpose Input Output 139	I/O	139	N19	
GPIO140	General-Purpose Input Output 140	I/O	140	M19	
GPIO141	General-Purpose Input Output 141	I/O	141	M18	
GPIO142	General-Purpose Input Output 142	I/O	142	L19	
GPIO143	General-Purpose Input Output 143	I/O	143	F18	
GPIO144	General-Purpose Input Output 144	I/O	144	F17	
GPIO145	General-Purpose Input Output 145	I/O	145	E17	
GPIO146	General-Purpose Input Output 146	I/O	146	D18	
GPIO147	General-Purpose Input Output 147	I/O	147	D17	
GPIO148	General-Purpose Input Output 148	I/O	148	D14	
GPIO149	General-Purpose Input Output 149	I/O	149	A13	
GPIO150	General-Purpose Input Output 150	I/O	150	B13	
GPIO151	General-Purpose Input Output 151	I/O	151	C13	
GPIO152	General-Purpose Input Output 152	I/O	152	D13	
GPIO153	General-Purpose Input Output 153	I/O	153	A12	
GPIO154	General-Purpose Input Output 154	I/O	154	B12	
GPIO155	General-Purpose Input Output 155	I/O	155	C12	
GPIO156	General-Purpose Input Output 156	I/O	156	D12	
GPIO157	General-Purpose Input Output 157	I/O	157	B10	
GPIO158	General-Purpose Input Output 158	I/O	158	C10	
GPIO159	General-Purpose Input Output 159	I/O	159	D10	
GPIO160	General-Purpose Input Output 160	I/O	160	B9	
GPIO161	General-Purpose Input Output 161	I/O	161	C9	
GPIO162	General-Purpose Input Output 162	I/O	162	D9	
GPIO163	General-Purpose Input Output 163	I/O	163	A8	
GPIO164	General-Purpose Input Output 164	I/O	164	B8	
GPIO165	General-Purpose Input Output 165	I/O	165	C5	

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
GPIO166	General-Purpose Input Output 166	I/O	166	D5	
GPIO167	General-Purpose Input Output 167	I/O	167	C4	
GPIO168	General-Purpose Input Output 168	I/O	168	D4	
GPIO20	General-Purpose Input Output 20	I/O	20	F2	13
GPIO21	General-Purpose Input Output 21	I/O	21	F3	14
GPIO22	General-Purpose Input Output 22	I/O	22	J4	22
GPIO23	General-Purpose Input Output 23	I/O	23	K4	23
GPIO24	General-Purpose Input Output 24	I/O	24	K3	24
GPIO25	General-Purpose Input Output 25	I/O	25	K2	25
GPIO26	General-Purpose Input Output 26	I/O	26	K1	27
GPIO27	General-Purpose Input Output 27	I/O	27	L1	28
GPIO28	General-Purpose Input Output 28	I/O	28	V11	64
GPIO29	General-Purpose Input Output 29	I/O	29	W11	65
GPIO30	General-Purpose Input Output 30	I/O	30	T11	63
GPIO31	General-Purpose Input Output 31	I/O	31	U11	66
GPIO32	General-Purpose Input Output 32	I/O	32	U13	67
GPIO33	General-Purpose Input Output 33	I/O	33	T13	69
GPIO34	General-Purpose Input Output 34	I/O	34	U14	70
GPIO35	General-Purpose Input Output 35	I/O	35	T14	71
GPIO36	General-Purpose Input Output 36	I/O	36	V16	83
GPIO37	General-Purpose Input Output 37	I/O	37	U16	84
GPIO38	General-Purpose Input Output 38	I/O	38	T16	85
GPIO39	General-Purpose Input Output 39	I/O	39	W17	86
GPIO40	General-Purpose Input Output 40	I/O	40	V17	87
GPIO41	General-Purpose Input Output 41	I/O	41	U17	89
GPIO42	General-Purpose Input Output 42	I/O	42	D19	130
GPIO43	General-Purpose Input Output 43	I/O	43	C19	131
GPIO44	General-Purpose Input Output 44	I/O	44	K18	113
GPIO45	General-Purpose Input Output 45	I/O	45	K19	115
GPIO46	General-Purpose Input Output 46	I/O	46	E19	128
GPIO47	General-Purpose Input Output 47	I/O	47	E18	129
GPIO48	General-Purpose Input Output 48	I/O	48	R16	90
GPIO49	General-Purpose Input Output 49	I/O	49	R17	93
GPIO50	General-Purpose Input Output 50	I/O	50	R18	94
GPIO51	General-Purpose Input Output 51	I/O	51	R19	95
GPIO52	General-Purpose Input Output 52	I/O	52	P16	96
GPIO53	General-Purpose Input Output 53	I/O	53	P17	97
GPIO54	General-Purpose Input Output 54	I/O	54	P18	98
GPIO55	General-Purpose Input Output 55	I/O	55	P19	100
GPIO56	General-Purpose Input Output 56	I/O	56	N16	101
GPIO57	General-Purpose Input Output 57	I/O	57	N18	102
GPIO58	General-Purpose Input Output 58	I/O	58	N17	103
GPIO59	General-Purpose Input Output 59	I/O	59	M16	104
GPIO60	General-Purpose Input Output 60	I/O	60	M17	105
GPIO61	General-Purpose Input Output 61	I/O	61	L16	107

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
GPIO62	General-Purpose Input Output 62	I/O	62	J17	108
GPIO63	General-Purpose Input Output 63	I/O	63	J16	109
GPIO64	General-Purpose Input Output 64	I/O	64	L17	110
GPIO65	General-Purpose Input Output 65	I/O	65	K16	111
GPIO66	General-Purpose Input Output 66	I/O	66	K17	112
GPIO67	General-Purpose Input Output 67	I/O	67	B19	132
GPIO68	General-Purpose Input Output 68	I/O	68	C18	133
GPIO69	General-Purpose Input Output 69	I/O	69	B18	134
GPIO70	General-Purpose Input Output 70	I/O	70	A17	135
GPIO71	General-Purpose Input Output 71	I/O	71	B17	136
GPIO72	General-Purpose Input Output 72	I/O	72	B16	139
GPIO73	General-Purpose Input Output 73	I/O	73	A16	140
GPIO74	General-Purpose Input Output 74	I/O	74	C17	141
GPIO75	General-Purpose Input Output 75	I/O	75	D16	142
GPIO76	General-Purpose Input Output 76	I/O	76	C16	143
GPIO77	General-Purpose Input Output 77	I/O	77	A15	144
GPIO78	General-Purpose Input Output 78	I/O	78	B15	145
GPIO79	General-Purpose Input Output 79	I/O	79	C15	146
GPIO80	General-Purpose Input Output 80	I/O	80	D15	148
GPIO81	General-Purpose Input Output 81	I/O	81	A14	149
GPIO82	General-Purpose Input Output 82	I/O	82	B14	150
GPIO83	General-Purpose Input Output 83	I/O	83	C14	151
GPIO84	General-Purpose Input Output 84	I/O	84	A11	154
GPIO85	General-Purpose Input Output 85	I/O	85	B11	155
GPIO86	General-Purpose Input Output 86	I/O	86	C11	156
GPIO87	General-Purpose Input Output 87	I/O	87	D11	157
GPIO88	General-Purpose Input Output 88	I/O	88	C6	170
GPIO89	General-Purpose Input Output 89	I/O	89	D6	171
GPIO90	General-Purpose Input Output 90	I/O	90	A5	172
GPIO91	General-Purpose Input Output 91	I/O	91	B5	173
GPIO92	General-Purpose Input Output 92	I/O	92	A4	174
GPIO93	General-Purpose Input Output 93	I/O	93	B4	175
GPIO94	General-Purpose Input Output 94	I/O	94	A3	176
GPIO95	General-Purpose Input Output 95	I/O	95	B3	
GPIO96	General-Purpose Input Output 96	I/O	96	C3	
GPIO97	General-Purpose Input Output 97	I/O	97	A2	
GPIO98	General-Purpose Input Output 98	I/O	98	F1	
GPIO99	General-Purpose Input Output 99	I/O	99	G1	17
I2CA_SCL	I2C-A Open-Drain Bidirectional Clock	I/OD	1, 105, 32, 33, 43, 57, 92	A4, C19, D8, J3, N18, T13, U13	102, 131, 161, 174, 67, 69
I2CA_SDA	I2C-A Open-Drain Bidirectional Data	I/OD	104, 31, 32, 42, 56, 91	B5, C8, D19, J2, N16, U11, U13	101, 130, 160, 173, 66, 67

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
I2CB_SCL	I2C-B Open-Drain Bidirectional Clock	I/OD	3, 35, 41, 69	B18, B7, T14, U17	134, 163, 71, 89
I2CB_SDA	I2C-B Open-Drain Bidirectional Data	I/OD	2, 34, 40, 66	A7, K17, U14, V17	112, 162, 70, 87
MCAN_RX	CAN/CAN FD Receive	I	10, 18, 23, 30, 36, 5, 70, 75	A17, B2, D16, D7, E3, K4, T11, V16	1, 10, 135, 142, 165, 23, 63, 83
MCAN_TX	CAN/CAN FD Transmit	O	19, 22, 31, 37, 4, 71, 74, 8	B17, C17, C7, E4, G2, J4, U11, U16	12, 136, 141, 164, 18, 22, 66, 84
MCLKRA	McBSP-A Receive Clock	I	58, 7	B6, N17	103, 167
MCLKRB	McBSP-B Receive Clock	I	3, 60	B7, M17	105, 163
MCLKXA	McBSP-A Transmit Clock	O	167, 22, 86	C11, C4, J4	156, 22
MCLKXB	McBSP-B Transmit Clock	O	14, 26, 86	C11, D2, K1	156, 27, 6
MDRA	McBSP-A Receive Serial Data	I	166, 21, 85	B11, D5, F3	14, 155
MDRB	McBSP-B Receive Serial Data	I	13, 25, 85	B11, D1, K2	155, 25, 5
MDXA	McBSP-A Transmit Serial Data	O	165, 20, 84	A11, C5, F2	13, 154
MDXB	McBSP-B Transmit Serial Data	O	12, 24, 84	A11, C2, K3	154, 24, 4
MFSRA	McBSP-A Receive Frame Sync	I	5, 59	D7, M16	104, 165
MFSRB	McBSP-B Receive Frame Sync	I	1, 61	D8, L16	107, 161
MFSXA	McBSP-A Transmit Frame Sync	O	168, 23, 87	D11, D4, K4	157, 23
MFSXB	McBSP-B Transmit Frame Sync	O	15, 27, 87	D11, D3, L1	157, 28, 7
OUTPUTXBAR1	Output X-BAR Output 1	O	2, 24, 34, 58	A7, K3, N17, U14	103, 162, 24, 70
OUTPUTXBAR2	Output X-BAR Output 2	O	25, 3, 37, 59	B7, K2, M16, U16	104, 163, 25, 84
OUTPUTXBAR3	Output X-BAR Output 3	O	14, 26, 4, 48, 5, 60	C7, D2, D7, K1, M17, R16	105, 164, 165, 27, 6, 90
OUTPUTXBAR4	Output X-BAR Output 4	O	15, 27, 49, 6, 61	A6, D3, L1, L16, R17	107, 166, 28, 7, 93
OUTPUTXBAR5	Output X-BAR Output 5	O	115, 28, 7	B6, V11, V12	167, 64
OUTPUTXBAR6	Output X-BAR Output 6	O	116, 29, 9	G3, W10, W11	19, 65
OUTPUTXBAR7	Output X-BAR Output 7	O	11, 16, 30	C1, E1, T11	2, 63, 8
OUTPUTXBAR8	Output X-BAR Output 8	O	17, 31	E2, U11	66, 9
PMBUSA_ALERT	PMBus-A Open-Drain Bidirectional Alert Signal	I/OD	26, 93	B4, K1	175, 27
PMBUSA_CTL	PMBus-A Control Signal	I	27, 94	A3, L1	176, 28
PMBUSA_SCL	PMBus-A Open-Drain Bidirectional Clock	I/OD	24, 91	B5, K3	173, 24

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
PMBUSA_SDA	PMBus-A Open-Drain Bidirectional Data	I/OD	25, 92	A4, K2	174, 25
SCIA_RX	SCI-A Receive Data	I	136, 28, 35, 43, 49, 64, 85, 9	B11, C19, G3, L17, R17, T14, T17, V11	110, 131, 155, 19, 64, 71, 93
SCIA_TX	SCI-A Transmit Data	O	135, 29, 34, 36, 42, 48, 65, 8, 84	A11, D19, G2, K16, R16, U14, U18, V16, W11	111, 130, 154, 18, 65, 70, 83, 90
SCIB_RX	SCI-B Receive Data	I	11, 138, 15, 19, 23, 55, 71, 87	B17, C1, D11, D3, E4, K4, P19, T19	100, 12, 136, 157, 2, 23, 7
SCIB_TX	SCI-B Transmit Data	O	10, 137, 14, 18, 22, 54, 70, 86, 9	A17, B2, C11, D2, E3, G3, J4, P18, T18	1, 10, 135, 156, 19, 22, 6, 98
SCIC_RX	SCI-C Receive Data	I	107, 13, 139, 39, 57, 62, 73, 90	A16, A5, D1, J17, L3, N18, N19, W17	102, 108, 140, 172, 5, 86
SCIC_TX	SCI-C Transmit Data	O	106, 12, 140, 38, 56, 63, 72, 89	B16, C2, D6, J16, L2, M19, N16, T16	101, 109, 139, 171, 4, 85
SCID_RX	SCI-D Receive Data	I	105, 141, 46, 77, 94	A15, A3, E19, J3, M18	128, 144, 176
SCID_TX	SCI-D Transmit Data	O	104, 142, 47, 76, 93	B4, C16, E18, J2, L19	129, 143, 175
SD1_C1	SDFM-1 Channel 1 Clock Input	I	123, 17, 49, 53, 64	E2, L17, P17, R17, U8	110, 9, 93, 97
SD1_C2	SDFM-1 Channel 2 Clock Input	I	125, 19, 51, 54, 66	E4, K17, P18, R19, T9	112, 12, 95, 98
SD1_C3	SDFM-1 Channel 3 Clock Input	I	127, 21, 53, 55, 68	C18, F3, P17, P19, V9	100, 133, 14, 97
SD1_C4	SDFM-1 Channel 4 Clock Input	I	129, 23, 55, 56, 70	A17, K4, N16, P19, T10	100, 101, 135, 23
SD1_D1	SDFM-1 Channel 1 Data Input	I	122, 16, 36, 48, 63	E1, J16, R16, T8, V16	109, 8, 83, 90
SD1_D2	SDFM-1 Channel 2 Data Input	I	124, 18, 37, 50, 65	E3, K16, R18, U16, V8	10, 111, 84, 94
SD1_D3	SDFM-1 Channel 3 Data Input	I	126, 20, 38, 52, 67	B19, F2, P16, T16, U9	13, 132, 85, 96

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
SD1_D4	SDFM-1 Channel 4 Data Input	I	128, 22, 39, 54, 69	B18, J4, P18, W17, W9	134, 22, 86, 98
SD2_C1	SDFM-2 Channel 1 Clock Input	I	131, 25, 57, 80	D15, K2, N18, V10	102, 148, 25
SD2_C2	SDFM-2 Channel 2 Clock Input	I	133, 27, 58, 59, 74	C17, G18, L1, M16, N17	103, 104, 118, 141, 28
SD2_C3	SDFM-2 Channel 3 Clock Input	I	135, 29, 59, 61, 76	C16, L16, M16, U18, W11	104, 107, 143, 65
SD2_C4	SDFM-2 Channel 4 Clock Input	I	137, 31, 60, 63, 78	B15, J16, M17, T18, U11	105, 109, 145, 66
SD2_D1	SDFM-2 Channel 1 Data Input	I	130, 24, 49, 56, 79	C15, K3, N16, R17, U10	101, 146, 24, 93
SD2_D2	SDFM-2 Channel 2 Data Input	I	132, 26, 50, 58, 73	A16, K1, N17, R18, W18	103, 140, 27, 94
SD2_D3	SDFM-2 Channel 3 Data Input	I	134, 28, 51, 60, 75	D16, M17, R19, V11, V18	105, 142, 64, 95
SD2_D4	SDFM-2 Channel 4 Data Input	I	136, 30, 52, 62, 77	A15, J17, P16, T11, T17	108, 144, 63, 96
SPIA_CLK	SPI-A Clock	I/O	18, 34, 56, 60	E3, M17, N16, U14	10, 101, 105, 70
SPIA_SIMO	SPI-A Slave In, Master Out (SIMO)	I/O	16, 32, 54, 58	E1, N17, P18, U13	103, 67, 8, 98
SPIA_SOMI	SPI-A Slave Out, Master In (SOMI)	I/O	17, 33, 55, 59	E2, M16, P19, T13	100, 104, 69, 9
SPIA_STEn	SPI-A Slave Transmit Enable (STE)	I/O	19, 35, 57, 61	E4, L16, N18, T14	102, 107, 12, 71
SPIB_CLK	SPI-B Clock	I/O	22, 26, 58, 65	J4, K1, K16, N17	103, 111, 22, 27
SPIB_SIMO	SPI-B Slave In, Master Out (SIMO)	I/O	24, 60, 63	J16, K3, M17	105, 109, 24
SPIB_SOMI	SPI-B Slave Out, Master In (SOMI)	I/O	25, 61, 64	K2, L16, L17	107, 110, 25
SPIB_STEn	SPI-B Slave Transmit Enable (STE)	I/O	23, 27, 59, 66	K17, K4, L1, M16	104, 112, 23, 28
SPIC_CLK	SPI-C Clock	I/O	102, 124, 22, 52, 71	B17, H3, J4, P16, V8	136, 22, 96
SPIC_SIMO	SPI-C Slave In, Master Out (SIMO)	I/O	100, 122, 20, 50, 69	B18, F2, H1, R18, T8	13, 134, 94
SPIC_SOMI	SPI-C Slave Out, Master In (SOMI)	I/O	101, 123, 21, 51, 70	A17, F3, H2, R19, U8	135, 14, 95
SPIC_STEn	SPI-C Slave Transmit Enable (STE)	I/O	103, 125, 23, 53, 72	B16, J1, K4, P17, T9	139, 23, 97

Table 6-3. Digital Signals (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
SPID_CLK	SPI-D Clock	I/O	32, 93	B4, U13	175, 67
SPID_SIMO	SPI-D Slave In, Master Out (SIMO)	I/O	30, 91	B5, T11	173, 63
SPID_SOMI	SPI-D Slave Out, Master In (SOMI)	I/O	31, 92	A4, U11	174, 66
SPID_STEn	SPI-D Slave Transmit Enable (STE)	I/O	33, 94	A3, T13	176, 69
SSIA_CLK	SSI-A Clock	I/O	18, 56, 65, 93	B4, E3, K16, N16	10, 101, 111, 175
SSIA_FSS	SSI-A Frame Sync	I/O	19, 57, 66, 94	A3, E4, K17, N18	102, 112, 12, 176
SSIA_RX	SSI-A Serial Data Receive	I/O	17, 55, 64, 92	A4, E2, L17, P19	100, 110, 174, 9
SSIA_TX	SSI-A Serial Data Transmit	I/O	16, 54, 63, 91	B5, E1, J16, P18	109, 173, 8, 98
TRACE_CLK	Trace Clock	O	24	K3	24
TRACE_DATA0	Trace Data 0	O	20	F2	13
TRACE_DATA1	Trace Data 1	O	21	F3	14
TRACE_DATA2	Trace Data 2	O	22	J4	22
TRACE_DATA3	Trace Data 3	O	23	K4	23
TRACE_SWO	Trace Single Wire Out	O	25	K2	25
UARTA_RX	UART-A Serial Data Receive	I/O	43, 85	B11, C19	131, 155
UARTA_TX	UART-A Serial Data Transmit	I/O	42, 84	A11, D19	130, 154
USB0DM	USB-0 PHY differential data	O	42	D19	130
USB0DP	USB-0 PHY differential data	O	43	C19	131
XCLKOUT	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.	O	73	A16	140

6.3.3 Power and Ground

Table 6-4. Power and Ground

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
VDD	1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution. A single 56Ω resistor (10% tolerance) should be placed between VDD and VSS. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.			E11, E9, F11, F9, G14, G15, J14, J15, K5, K6, P10, P13, R10, R13	117, 126, 137, 153, 158, 16, 169, 21, 61, 76
VDD3VFL	3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin			R11, R12	72
VDDA	3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin.			P6, R6	36, 54

Table 6-4. Power and Ground (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
VDDIO	3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin.			A18, A9, B1, E10, E13, E16, E7, F10, F13, F16, F4, F7, G4, G5, G6, H5, H6, L14, L15, M1, M5, M6, N14, N15, P9, R9, V19, W8	106, 11, 114, 116, 127, 138, 147, 15, 152, 159, 168, 20, 26, 3, 62, 68, 75, 82, 88, 91, 99
VDDOSC	Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-µF (minimum) decoupling capacitor on each pin.			H16, H17	120, 125
VSS	Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB.			A1, A10, A19, E12, E14, E15, E5, E6, E8, F12, F14, F15, F5, F6, F8, G16, G17, H10, H11, H12, H14, H15, H8, H9, J10, J11, J12, J5, J6, J8, J9, K10, K11, K12, K14, K15, K8, K9, L10, L11, L12, L18, L5, L6, L8, L9, M10, M11, M12, M14, M15, M8, M9, N1, N5, N6, P11, P12, P14, P15, P7, P8, R14, R15, R7, R8, W19, W7	PAD
VSSA	Analog Ground			P1, P5, R5, V7, W1	34, 52

Table 6-4. Power and Ground (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
VSSOSC	Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.			H18, H19	122

6.3.4 Test, JTAG, and Reset

Table 6-5. Test, JTAG, and Reset

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
ERRORSTS	Error Status Output. When used, this signal requires an external pulldown.	O		U19	92
FLT1	Flash test pin 1. Reserved for TI. Must be left unconnected.	I/O		W12	73
FLT2	Flash test pin 2. Reserved for TI. Must be left unconnected.	I/O		V13	74
NC1	No Connection. This pin is not internally connected to the device. This pin may be left open or connected to any voltage within the maximum operating conditions.			H4	
NC2	No Connection. This pin is not internally connected in the device and may be left open or tied to VSS or VDDIO. NOTE: On other C2000 devices with an internal voltage regulator (VREG), this pin will be VREGENZ (internal voltage regulator enable). To enable PCB compatibility across C2000 devices this pin should be connected to VDDIO (3.3v). This will ensure the internal VREG, when present on other devices, would be disabled and not conflict with an external VREG which must be used with this device.			J18	119
TCK	JTAG test clock with internal pullup.	I		V15	81
TDI	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.	I		W13	77
TDO	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.	O		W15	78
TMS	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.	I		W14	80

Table 6-5. Test, JTAG, and Reset (continued)

SIGNAL NAME	DESCRIPTION	PIN TYPE	GPIO PIN	337 BGA PIN	176 Pin PIN
TRSTn	JTAG test reset with internal pulldown. TRST, when driven high, gives the scan system control of the operations of the device. If this signal is driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: TRST must be maintained low at all times during normal device operation, so an external pulldown resistor is required on this pin for protection against noise spikes. The value of this resistor should be as small as possible, so long as the JTAG debug probe is still able to drive the TRST pin high. A resistor between 2.2 kΩ and 10 kΩ generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debug probe and the application. This pin has an internal 50-ns (nominal) glitch filter.	I		V14	79
X1	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.	I		G19	123
X2	Crystal oscillator output.	O		J19	121
XRSn	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open-drain with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.	I/OD		F19	124

6.4 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 6-6 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. In order to avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 6-6 with pullups and pulldowns are always on and cannot be disabled.

Table 6-6. Pins With Internal Pullup and Pulldown

PIN	RESET (XRSn = 0)	DEVICE BOOT	APPLICATION SOFTWARE
GPIOx	Pullup disabled	Pullup disabled(1)	Pullup enable is application-defined
TRSTn	Pulldown active		
TCK	Pullup active		
TMS	Pullup active		
TDI	Pullup active		
XRSn	Pullup active		
ERRORSTS	Pulldown active		
DACOUTx	Pulldown active		
Other pins	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

6.5 Pin Multiplexing

GPIO muxed pins are listed in the GPIO Muxed Pins table in Section 6.5.1.

6.5.1 GPIO Muxed Pins Table

Table 6-7. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1A				I2CA_SDA		CM-I2CA_SDA	ESC_GPI0		FSITXA_D0			
GPIO1	EPWM1B		MFSRB		I2CA_SCL		CM-I2CA_SCL	ESC_GPI1		FSITXA_D1			
GPIO2	EPWM2A			OUTPUTXBAR1	I2CB_SDA			ESC_GPI2		FSITXA_CLK			
GPIO3	EPWM2B	OUTPUTXBAR2	MCLKRB	OUTPUTXBAR2	I2CB_SCL			ESC_GPI3		FSIRXA_D0			
GPIO4	EPWM3A			OUTPUTXBAR3	CANA_TX		MCAN_TX	ESC_GPI4		FSIRXA_D1			
GPIO5	EPWM3B	MFSRA	OUTPUTXBAR3		CANA_RX		MCAN_RX	ESC_GPI5		FSIRXA_CLK			
GPIO6	EPWM4A	OUTPUTXBAR4	EXTSYNCOUT	EQEP3_A	CANB_TX			ESC_GPI6		FSITXB_D0			
GPIO7	EPWM4B	MCLKRA	OUTPUTXBAR5	EQEP3_B	CANB_RX			ESC_GPI7		FSITXB_D1			
GPIO8	EPWM5A	CANB_TX	ADCSOCAO	EQEP3_STROBE	SCIA_TX		MCAN_TX	ESC_GPO0		FSITXB_CLK	FSITXA_D1	FSIRXA_D0	
GPIO9	EPWM5B	SCIB_TX	OUTPUTXBAR6	EQEP3_INDEX	SCIA_RX			ESC_GPO1		FSIRXB_D0	FSITXA_D0	FSIRXA_CLK	
GPIO10	EPWM6A	CANB_RX	ADCSOCBO	EQEP1_A	SCIB_TX		MCAN_RX	ESC_GPO2		FSIRXB_D1	FSITXA_CLK	FSIRXA_D1	
GPIO11	EPWM6B	SCIB_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX			ESC_GPO3		FSIRXB_CLK	FSIRXA_D1		
GPIO12	EPWM7A	CANB_TX	MDXB	EQEP1_STROBE	SCIC_TX			ESC_GPO4		FSIRXC_D0	FSIRXA_D0		
GPIO13	EPWM7B	CANB_RX	MDRB	EQEP1_INDEX	SCIC_RX			ESC_GPO5		FSIRXC_D1	FSIRXA_CLK		
GPIO14	EPWM8A	SCIB_TX	MCLKXB		OUTPUTXBAR3			ESC_GPO6		FSIRXC_CLK			
GPIO15	EPWM8B	SCIB_RX	MFSXB		OUTPUTXBAR4			ESC_GPO7		FSIRXD_D0			
GPIO16	SPIA_SIMO	CANB_TX	OUTPUTXBAR7	EPWM9A		SD1_D1			SSIA_TX	FSIRXD_D1			
GPIO17	SPIA_SOMI	CANB_RX	OUTPUTXBAR8	EPWM9B		SD1_C1			SSIA_RX	FSIRXD_CLK			
GPIO18	SPIA_CLK	SCIB_TX	CANA_RX	EPWM10A		SD1_D2	MCAN_RX	EMIF1_CS2n	SSIA_CLK	FSIRXE_D0			
GPIO19	SPIA_STEn	SCIB_RX	CANA_TX	EPWM10B		SD1_C2	MCAN_TX	EMIF1_CS3n	SSIA_FSS	FSIRXE_D1			
GPIO20	EQEP1_A	MDXA	CANB_TX	EPWM11A		SD1_D3		EMIF1_BA0	TRACE_DATA0	FSIRXE_CLK	SPIC_SIMO		
GPIO21	EQEP1_B	MDRA	CANB_RX	EPWM11B		SD1_C3		EMIF1_BA1	TRACE_DATA1	FSIRXF_D0	SPIC_SOMI		
GPIO22	EQEP1_STROBE	MCLKXA	SCIB_TX	EPWM12A	SPIB_CLK	SD1_D4	MCAN_TX	EMIF1_RAS	TRACE_DATA2	FSIRXF_D1	SPIC_CLK		
GPIO23	EQEP1_INDEX	MFSXA	SCIB_RX	EPWM12B	SPIB_STEn	SD1_C4	MCAN_RX	EMIF1_CAS	TRACE_DATA3	FSIRXF_CLK	SPIC_STEn		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO24	OUTPUTXBAR1	EQEP2_A	MDXB		SPIB_SIMO	SD2_D1	PMBUSA_SCL	EMIF1_DQM0	TRACE_CLK	EPWM13A		FSIRXG_D0	
GPIO25	OUTPUTXBAR2	EQEP2_B	MDRB		SPIB_SOMI	SD2_C1	PMBUSA_SDA	EMIF1_DQM1	TRACE_SWO	EPWM13B	FSITXA_D1	FSIRXG_D1	
GPIO26	OUTPUTXBAR3	EQEP2_INDEX	MCLKXB	OUTPUTXBAR3	SPIB_CLK	SD2_D2	PMBUSA_ALERT	EMIF1_DQM2	ESC_MDIO_CLK	EPWM14A	FSITXA_D0	FSIRXG_CLK	
GPIO27	OUTPUTXBAR4	EQEP2_STROBE	MFSXB	OUTPUTXBAR4	SPIB_STEn	SD2_C2	PMBUSA_CTL	EMIF1_DQM3	ESC_MDIO_DATA	EPWM14B	FSITXA_CLK	FSIRXH_D0	
GPIO28	SCIA_RX	EMIF1_CS4n		OUTPUTXBAR5	EQEP3_A	SD2_D3	EMIF1_CS2n			EPWM15A		FSIRXH_D1	
GPIO29	SCIA_TX	EMIF1_SDCKE		OUTPUTXBAR6	EQEP3_B	SD2_C3	EMIF1_CS3n	ESC_LATCH0	ESC_I2C_SDA	EPWM15B	ESC_SYNC0	FSIRXH_CLK	
GPIO30	CANA_RX	EMIF1_CLK	MCAN_RX	OUTPUTXBAR7	EQEP3_STROBE	SD2_D4	EMIF1_CS4n	ESC_LATCH1	ESC_I2C_SCL	EPWM16A	ESC_SYNC1	SPID_SIMO	
GPIO31	CANA_TX	EMIF1_WEn	MCAN_TX	OUTPUTXBAR8	EQEP3_INDEX	SD2_C4	EMIF1_RNW	I2CA_SDA	CM-I2CA_SDA	EPWM16B		SPID_SOMI	
GPIO32	I2CA_SDA	EMIF1_CS0n	SPIA_SIMO			CLB_OUTPUTXBAR1	EMIF1_OEn	I2CA_SCL	CM-I2CA_SCL			SPID_CLK	
GPIO33	I2CA_SCL	EMIF1_RNW	SPIA_SOMI			CLB_OUTPUTXBAR2	EMIF1_BA0					SPID_STEn	
GPIO34	OUTPUTXBAR1	EMIF1_CS2n	SPIA_CLK		I2CB_SDA	CLB_OUTPUTXBAR3	EMIF1_BA1	ESC_LATCH0	ENET_MII_CRS	SCIA_TX	ESC_SYNC0		
GPIO35	SCIA_RX	EMIF1_CS3n	SPIA_STEn		I2CB_SCL	CLB_OUTPUTXBAR4	EMIF1_A0	ESC_LATCH1	ENET_MII_COL		ESC_SYNC1		
GPIO36	SCIA_TX	EMIF1_WAIT			CANA_RX	CLB_OUTPUTXBAR5	EMIF1_A1	MCAN_RX		SD1_D1			
GPIO37	OUTPUTXBAR2	EMIF1_OEn			CANA_TX	CLB_OUTPUTXBAR6	EMIF1_A2	MCAN_TX		SD1_D2			
GPIO38		EMIF1_A0		SCIC_TX	CANB_TX	CLB_OUTPUTXBAR7	EMIF1_A3	ENET_MII_RX_DV	ENET_MII_CRS	SD1_D3			
GPIO39		EMIF1_A1		SCIC_RX	CANB_RX	CLB_OUTPUTXBAR8	EMIF1_A4	ENET_MII_RX_ERR	ENET_MII_COL	SD1_D4			
GPIO40		EMIF1_A2			I2CB_SDA				ENET_MII_CRS		ESC_I2C_SDA		
GPIO41		EMIF1_A3			I2CB_SCL			ENET_REVMII_MDIO_RST	ENET_MII_COL		ESC_I2C_SCL		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO42					I2CA_SDA			ENET_MDIO_CLK	UARTA_TX			SCIA_TX	USB0DM
GPIO43					I2CA_SCL			ENET_MDIO_DATA	UARTA_RX			SCIA_RX	USB0DP
GPIO44		EMIF1_A4							ENET_MII_TX_CLK		ESC_TX1_CLK		
GPIO45		EMIF1_A5							ENET_MII_TX_EN		ESC_TX1_ENA		
GPIO46		EMIF1_A6			SCID_RX				ENET_MII_TX_ERR		ESC_MDIO_CLK		
GPIO47		EMIF1_A7			SCID_TX				ENET_PPS0		ESC_MDIO_DATA		
GPIO48	OUTPUTXBAR3	EMIF1_A8			SCIA_TX	SD1_D1			ENET_PPS1		ESC_PHY_CLK		
GPIO49	OUTPUTXBAR4	EMIF1_A9			SCIA_RX	SD1_C1	EMIF1_A5		ENET_MII_RX_CLK	SD2_D1	FSITXA_D0		
GPIO50	EQEP1_A	EMIF1_A10			SPIC_SIMO	SD1_D2	EMIF1_A6		ENET_MII_RX_DV	SD2_D2	FSITXA_D1		
GPIO51	EQEP1_B	EMIF1_A11			SPIC_SOMI	SD1_C2	EMIF1_A7		ENET_MII_RX_ERR	SD2_D3	FSITXA_CLK		
GPIO52	EQEP1_STROBE	EMIF1_A12			SPIC_CLK	SD1_D3	EMIF1_A8		ENET_MII_RX_DATA0	SD2_D4	FSIRXA_D0		
GPIO53	EQEP1_INDEX	EMIF1_D31	EMIF2_D15		SPIC_STEn	SD1_C3	EMIF1_A9		ENET_MII_RX_DATA1	SD1_C1	FSIRXA_D1		
GPIO54	SPIA_SIMO	EMIF1_D30	EMIF2_D14	EQEP2_A	SCIB_TX	SD1_D4	EMIF1_A10		ENET_MII_RX_DATA2	SD1_C2	FSIRXA_CLK	SSIA_TX	
GPIO55	SPIA_SOMI	EMIF1_D29	EMIF2_D13	EQEP2_B	SCIB_RX	SD1_C4	EMIF1_D0		ENET_MII_RX_DATA3	SD1_C3	FSITXB_D0	SSIA_RX	
GPIO56	SPIA_CLK	EMIF1_D28	EMIF2_D12	EQEP2_STROBE	SCIC_TX	SD2_D1	EMIF1_D1	I2CA_SDA	ENET_MII_TX_EN	SD1_C4	FSITXB_CLK	SSIA_CLK	
GPIO57	SPIA_STEn	EMIF1_D27	EMIF2_D11	EQEP2_INDEX	SCIC_RX	SD2_C1	EMIF1_D2	I2CA_SCL	ENET_MII_TX_ERR		FSITXB_D1	SSIA_FSS	

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO58	MCLKRA	EMIF1_D26	EMIF2_D10	OUTPUTXBAR1	SPIB_CLK	SD2_D2	EMIF1_D3	ESC_LED_LINK0_ACTIVE	ENET_MII_TX_CLK	SD2_C2	FSIRXB_D0	SPIA_SIMO	
GPIO59	MFSRA	EMIF1_D25	EMIF2_D9	OUTPUTXBAR2	SPIB_STEn	SD2_C2	EMIF1_D4	ESC_LED_LINK1_ACTIVE	ENET_MII_TX_DATA0	SD2_C3	FSIRXB_D1	SPIA_SOMI	
GPIO60	MCLKRB	EMIF1_D24	EMIF2_D8	OUTPUTXBAR3	SPIB_SIMO	SD2_D3	EMIF1_D5	ESC_LED_ERR	ENET_MII_TX_DATA1	SD2_C4	FSIRXB_CLK	SPIA_CLK	
GPIO61	MFSRB	EMIF1_D23	EMIF2_D7	OUTPUTXBAR4	SPIB_SOMI	SD2_C3	EMIF1_D6	ESC_LED_RUN	ENET_MII_TX_DATA2		CANA_RX	SPIA_STEn	
GPIO62	SCIC_RX	EMIF1_D22	EMIF2_D6	EQEP3_A	CANA_RX	SD2_D4	EMIF1_D7	ESC_LED_STATE_RUN	ENET_MII_TX_DATA3		CANA_TX		
GPIO63	SCIC_TX	EMIF1_D21	EMIF2_D5	EQEP3_B	CANA_TX	SD2_C4	SSIA_TX		ENET_MII_RX_DATA0	SD1_D1	ESC_RX1_DATA0	SPIB_SIMO	
GPIO64		EMIF1_D20	EMIF2_D4	EQEP3_STROBE	SCIA_RX		SSIA_RX	ENET_MII_RX_DV	ENET_MII_RX_DATA1	SD1_C1	ESC_RX1_DATA1	SPIB_SOMI	
GPIO65		EMIF1_D19	EMIF2_D3	EQEP3_INDEX	SCIA_TX		SSIA_CLK	ENET_MII_RX_ERR	ENET_MII_RX_DATA2	SD1_D2	ESC_RX1_DATA2	SPIB_CLK	
GPIO66		EMIF1_D18	EMIF2_D2		I2CB_SDA		SSIA_FSS	ENET_MII_RX_DATA0	ENET_MII_RX_DATA3	SD1_C2	ESC_RX1_DATA3	SPIB_STEn	
GPIO67		EMIF1_D17	EMIF2_D1					ENET_MII_RX_CLK	ENET_REVMII_MDIO_RST	SD1_D3			
GPIO68		EMIF1_D16	EMIF2_D0						ENET_MII_INTR	SD1_C3	ESC_PHY1_LINKSTATUS		
GPIO69		EMIF1_D15			I2CB_SCL			ENET_MII_TX_EN	ENET_MII_RX_CLK	SD1_D4	ESC_RX1_CLK	SPIC_SIMO	
GPIO70		EMIF1_D14		CANA_RX	SCIB_TX		MCAN_RX		ENET_MII_RX_DV	SD1_C4	ESC_RX1_DV	SPIC_SOMI	
GPIO71		EMIF1_D13		CANA_TX	SCIB_RX		MCAN_TX	ENET_MII_RX_DATA0	ENET_MII_RX_ERR		ESC_RX1_ERR	SPIC_CLK	
GPIO72		EMIF1_D12		CANB_TX	SCIC_TX			ENET_MII_RX_DATA1	ENET_MII_TX_DATA3		ESC_TX1_DATA3	SPIC_STEn	
GPIO73		EMIF1_D11	XCLKOUT	CANB_RX	SCIC_RX			ENET_RMII_CLK	ENET_MII_TX_DATA2	SD2_D2	ESC_TX1_DATA2		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO74		EMIF1_D10					MCAN_TX		ENET_MII_TX_DATA1	SD2_C2	ESC_TX1_DATA1		
GPIO75		EMIF1_D9					MCAN_RX		ENET_MII_TX_DATA0	SD2_D3	ESC_TX1_DATA0		
GPIO76		EMIF1_D8			SCID_TX			ENET_MII_RX_ERR		SD2_C3	ESC_PHY_RESETn		
GPIO77		EMIF1_D7			SCID_RX					SD2_D4	ESC_RX0_CLK		
GPIO78		EMIF1_D6			EQEP2_A					SD2_C4	ESC_RX0_DV		
GPIO79		EMIF1_D5			EQEP2_B					SD2_D1	ESC_RX0_ERR		
GPIO80		EMIF1_D4			EQEP2_STROBE					SD2_C1	ESC_RX0_DATA0		
GPIO81		EMIF1_D3			EQEP2_INDEX						ESC_RX0_DATA1		
GPIO82		EMIF1_D2									ESC_RX0_DATA2		
GPIO83		EMIF1_D1									ESC_RX0_DATA3		
GPIO84				SCIA_TX	MDXB				UARTA_TX		ESC_TX0_ENA	MDXA	
GPIO85		EMIF1_D0		SCIA_RX	MDRB				UARTA_RX		ESC_TX0_CLK	MDRA	
GPIO86		EMIF1_A13	EMIF1_CAS	SCIB_TX	MCLKXB						ESC_PHY0_LINKSTATUS	MCLKXA	
GPIO87		EMIF1_A14	EMIF1_RAS	SCIB_RX	MFSXB		EMIF1_DQM3				ESC_TX0_DATA0	MFSXA	
GPIO88		EMIF1_A15	EMIF1_DQM0				EMIF1_DQM1				ESC_TX0_DATA1		
GPIO89		EMIF1_A16	EMIF1_DQM1		SCIC_TX		EMIF1_CAS				ESC_TX0_DATA2		
GPIO90		EMIF1_A17	EMIF1_DQM2		SCIC_RX		EMIF1_RAS				ESC_TX0_DATA3		
GPIO91		EMIF1_A18	EMIF1_DQM3		I2CA_SDA		EMIF1_DQM2	PMBUSA_SCL	SSIA_TX	FSIRXF_D0	CLB_OUTPUTXBAR1	SPID_SIMO	

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO92		EMIF1_A19	EMIF1_BA1		I2CA_SCL		EMIF1_DQM0	PMBUSA_SDA	SSIA_RX	FSIRXF_D1	CLB_OUTPUTXBAR2	SPID_SOMI	
GPIO93			EMIF1_BA0		SCID_TX			PMBUSA_ALERT	SSIA_CLK	FSIRXF_CLK	CLB_OUTPUTXBAR3	SPID_CLK	
GPIO94					SCID_RX		EMIF1_BA1	PMBUSA_CTL	SSIA_FSS	FSIRXG_D0	CLB_OUTPUTXBAR4	SPID_STEn	
GPIO95			EMIF2_A12							FSIRXG_D1	CLB_OUTPUTXBAR5		
GPIO96			EMIF2_DQM1	EQEP1_A						FSIRXG_CLK	CLB_OUTPUTXBAR6		
GPIO97			EMIF2_DQM0	EQEP1_B						FSIRXH_D0	CLB_OUTPUTXBAR7		
GPIO98			EMIF2_A0	EQEP1_STROBE						FSIRXH_D1	CLB_OUTPUTXBAR8		
GPIO99			EMIF2_A1	EQEP1_INDEX						FSIRXH_CLK			
GPIO100			EMIF2_A2	EQEP2_A	SPIC_SIMO			ESC_GPI0		FSITXA_D0			
GPIO101			EMIF2_A3	EQEP2_B	SPIC_SOMI			ESC_GPI1		FSITXA_D1			
GPIO102			EMIF2_A4	EQEP2_STROBE	SPIC_CLK			ESC_GPI2		FSITXA_CLK			
GPIO103			EMIF2_A5	EQEP2_INDEX	SPIC_STEn			ESC_GPI3		FSIRXA_D0			
GPIO104	I2CA_SDA		EMIF2_A6	EQEP3_A	SCID_TX			ESC_GPI4	CM-I2CA_SDA	FSIRXA_D1			
GPIO105	I2CA_SCL		EMIF2_A7	EQEP3_B	SCID_RX			ESC_GPI5	CM-I2CA_SCL	FSIRXA_CLK	ENET_MDIO_CLK		
GPIO106			EMIF2_A8	EQEP3_STROBE	SCIC_TX			ESC_GPI6		FSITXB_D0	ENET_MDIO_DATA		
GPIO107			EMIF2_A9	EQEP3_INDEX	SCIC_RX			ESC_GPI7		FSITXB_D1	ENET_REVMII_MDIO_RST		
GPIO108			EMIF2_A10					ESC_GPI8		FSITXB_CLK	ENET_MII_INTR		
GPIO109			EMIF2_A11					ESC_GPI9			ENET_MII_CRS		
GPIO110			EMIF2_WAIT					ESC_GPI10		FSIRXB_D0	ENET_MII_COL		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO111			EMIF2_BA0					ESC_GPI11		FSIRXB_D1	ENET_MII_RX_CLK		
GPIO112			EMIF2_BA1					ESC_GPI12		FSIRXB_CLK	ENET_MII_RX_DV		
GPIO113			EMIF2_CAS					ESC_GPI13			ENET_MII_RX_ERR		
GPIO114			EMIF2_RAS					ESC_GPI14			ENET_MII_RX_DATA0		
GPIO115			EMIF2_CS0n	OUTPUTXBAR5				ESC_GPI15		FSIRXC_D0	ENET_MII_RX_DATA1		
GPIO116			EMIF2_CS2n	OUTPUTXBAR6				ESC_GPI16		FSIRXC_D1	ENET_MII_RX_DATA2		
GPIO117			EMIF2_SDCKE					ESC_GPI17		FSIRXC_CLK	ENET_MII_RX_DATA3		
GPIO118			EMIF2_CLK					ESC_GPI18		FSIRXD_D0	ENET_MII_TX_EN		
GPIO119			EMIF2_RNW					ESC_GPI19		FSIRXD_D1	ENET_MII_TX_ERR		
GPIO120			EMIF2_WEn					ESC_GPI20		FSIRXD_CLK	ENET_MII_TX_CLK		
GPIO121			EMIF2_OEn					ESC_GPI21		FSIRXE_D0	ENET_MII_TX_DATA0		
GPIO122			EMIF2_D15		SPIC_SIMO	SD1_D1		ESC_GPI22			ENET_MII_TX_DATA1		
GPIO123			EMIF2_D14		SPIC_SOMI	SD1_C1		ESC_GPI23			ENET_MII_TX_DATA2		
GPIO124			EMIF2_D13		SPIC_CLK	SD1_D2		ESC_GPI24			ENET_MII_TX_DATA3		
GPIO125			EMIF2_D12		SPIC_STEn	SD1_C2		ESC_GPI25		FSIRXE_D1	ESC_LATCH0		
GPIO126			EMIF2_D11			SD1_D3		ESC_GPI26		FSIRXE_CLK	ESC_LATCH1		
GPIO127			EMIF2_D10			SD1_C3		ESC_GPI27			ESC_SYNC0		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO128			EMIF2_D9			SD1_D4		ESC_GPI28			ESC_SYNC1		
GPIO129			EMIF2_D8			SD1_C4		ESC_GPI29			ESC_TX1_ENA		
GPIO130			EMIF2_D7			SD2_D1		ESC_GPI30			ESC_TX1_CLK		
GPIO131			EMIF2_D6			SD2_C1		ESC_GPI31			ESC_TX1_DATA0		
GPIO132			EMIF2_D5			SD2_D2		ESC_GPO0			ESC_TX1_DATA1		
GPIO133						SD2_C2							AUXCLKIN
GPIO134			EMIF2_D4			SD2_D3		ESC_GPO1			ESC_TX1_DATA2		
GPIO135			EMIF2_D3		SCIA_TX	SD2_C3		ESC_GPO2			ESC_TX1_DATA3		
GPIO136			EMIF2_D2		SCIA_RX	SD2_D4		ESC_GPO3			ESC_RX1_DV		
GPIO137	EPWM13A		EMIF2_D1		SCIB_TX	SD2_C4		ESC_GPO4			ESC_RX1_CLK		
GPIO138	EPWM13B		EMIF2_D0		SCIB_RX			ESC_GPO5			ESC_RX1_ERR		
GPIO139	EPWM14A				SCIC_RX			ESC_GPO6			ESC_RX1_DATA0		
GPIO140	EPWM14B				SCIC_TX			ESC_GPO7			ESC_RX1_DATA1		
GPIO141	EPWM15A				SCID_RX			ESC_GPO8			ESC_RX1_DATA2		
GPIO142	EPWM15B				SCID_TX			ESC_GPO9			ESC_RX1_DATA3		
GPIO143	EPWM16A							ESC_GPO10			ESC_LED_LINK0_ACTIVE		
GPIO144	EPWM16B							ESC_GPO11			ESC_LED_LINK1_ACTIVE		
GPIO145	EPWM1A							ESC_GPO12			ESC_LED_ERR		
GPIO146	EPWM1B							ESC_GPO13			ESC_LED_RUN		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO147	EPWM2A							ESC_GPO14			ESC_LED_STATE_RUN		
GPIO148	EPWM2B							ESC_GPO15			ESC_PHY0_LINKSTATUS		
GPIO149	EPWM3A							ESC_GPO16			ESC_PHY1_LINKSTATUS		
GPIO150	EPWM3B							ESC_GPO17			ESC_I2C_SDA		
GPIO151	EPWM4A							ESC_GPO18			ESC_I2C_SCL		
GPIO152	EPWM4B							ESC_GPO19			ESC_MDIO_CLK		
GPIO153	EPWM5A							ESC_GPO20			ESC_MDIO_DATA		
GPIO154	EPWM5B							ESC_GPO21			ESC_PHY_CLK		
GPIO155	EPWM6A							ESC_GPO22			ESC_PHY_RESETn		
GPIO156	EPWM6B							ESC_GPO23			ESC_TX0_ENA		
GPIO157	EPWM7A							ESC_GPO24			ESC_TX0_CLK		
GPIO158	EPWM7B							ESC_GPO25			ESC_TX0_DATA0		
GPIO159	EPWM8A							ESC_GPO26			ESC_TX0_DATA1		
GPIO160	EPWM8B							ESC_GPO27			ESC_TX0_DATA2		
GPIO161	EPWM9A							ESC_GPO28			ESC_TX0_DATA3		
GPIO162	EPWM9B							ESC_GPO29			ESC_RX0_DV		
GPIO163	EPWM10A							ESC_GPO30			ESC_RX0_CLK		
GPIO164	EPWM10B							ESC_GPO31			ESC_RX0_ERR		
GPIO165	EPWM11A							MDXA			ESC_RX0_DATA0		

Table 6-7. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO166	EPWM11B							MDRA			ESC_RX0_DATA1		
GPIO167	EPWM12A							MCLKXA			ESC_RX0_DATA2		
GPIO168	EPWM12B							MFSXA			ESC_RX0_DATA3		

6.5.2 Input X-BAR

The Input X-BAR is used to route any GPIO input to the ADC, eCAP, and ePWM peripherals as well as to external interrupts (XINT) (see Figure 6-7). Table 6-8 lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

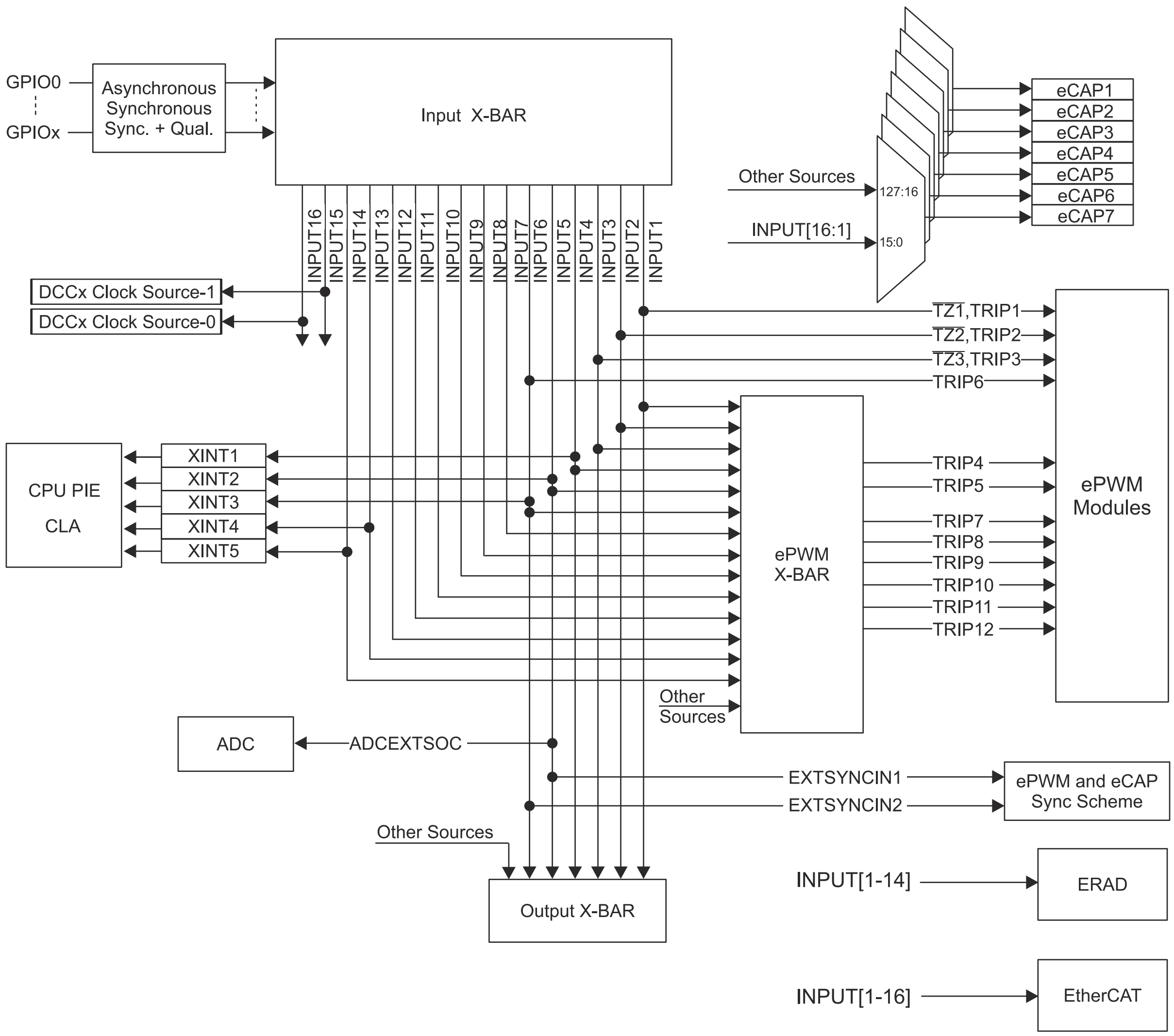


Figure 6-7. Input X-BAR

Table 6-8. Input X-BAR Destinations

INPUT	DESTINATION
INPUT1	eCAPx, ePWM X-BAR, ePWM[TZ1,TRIP1], Output X-BAR, EtherCAT, ERAD
INPUT2	eCAPx, ePWM X-BAR, ePWM[TZ2,TRIP2], Output X-BAR, EtherCAT, ERAD
INPUT3	eCAPx, ePWM X-BAR, ePWM[TZ3,TRIP3], Output X-BAR, EtherCAT, ERAD
INPUT4	eCAPx, ePWM X-BAR, XINT1, Output X-BAR, EtherCAT, ERAD
INPUT5	eCAPx, ePWM X-BAR, XINT2, ADCEXTSOC, EXTSYNCIN1, ePWM SYNC, eCAP SYNC, Output X-BAR, EtherCAT, ERAD
INPUT6	eCAPx, ePWM X-BAR, XINT3, ePWM[TRIP6], EXTSYNCIN2, Output X-BAR, ePWM SYNC, eCAP SYNC, Output X-BAR, EtherCAT, ERAD
INPUT7	eCAPx, ePWM X-BAR, EtherCAT, ERAD, eCAP1 Capture Input
INPUT8	eCAPx, ePWM X-BAR, EtherCAT, ERAD, eCAP2 Capture Input
INPUT9	eCAPx, ePWM X-BAR, EtherCAT, ERAD, eCAP3 Capture Input
INPUT10	eCAPx, ePWM X-BAR, EtherCAT, ERAD, eCAP4 Capture Input
INPUT11	eCAPx, ePWM X-BAR, EtherCAT, ERAD, eCAP5 Capture Input
INPUT12	eCAPx, ePWM X-BAR, EtherCAT, ERAD, eCAP6 Capture Input
INPUT13	eCAPx, ePWM X-BAR, XINT4, EtherCAT
INPUT14	eCAPx, ePWM X-BAR, XINT5, EtherCAT, ERAD
INPUT15	eCAPx, EtherCAT
INPUT16	eCAPx, EtherCAT, DCCx

6.5.3 Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The CLB X-BAR has eight outputs that are connected to the CLB global mux as AUXSIGx. The CLB Output X-BAR has eight outputs that can be selected on the GPIO mux as CLB_OUTPUTXBARx. The ePWM X-BAR has eight outputs that are connected to the TRIPx inputs of the ePWM. The sources for the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR are shown in Figure 6-8. For details on the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

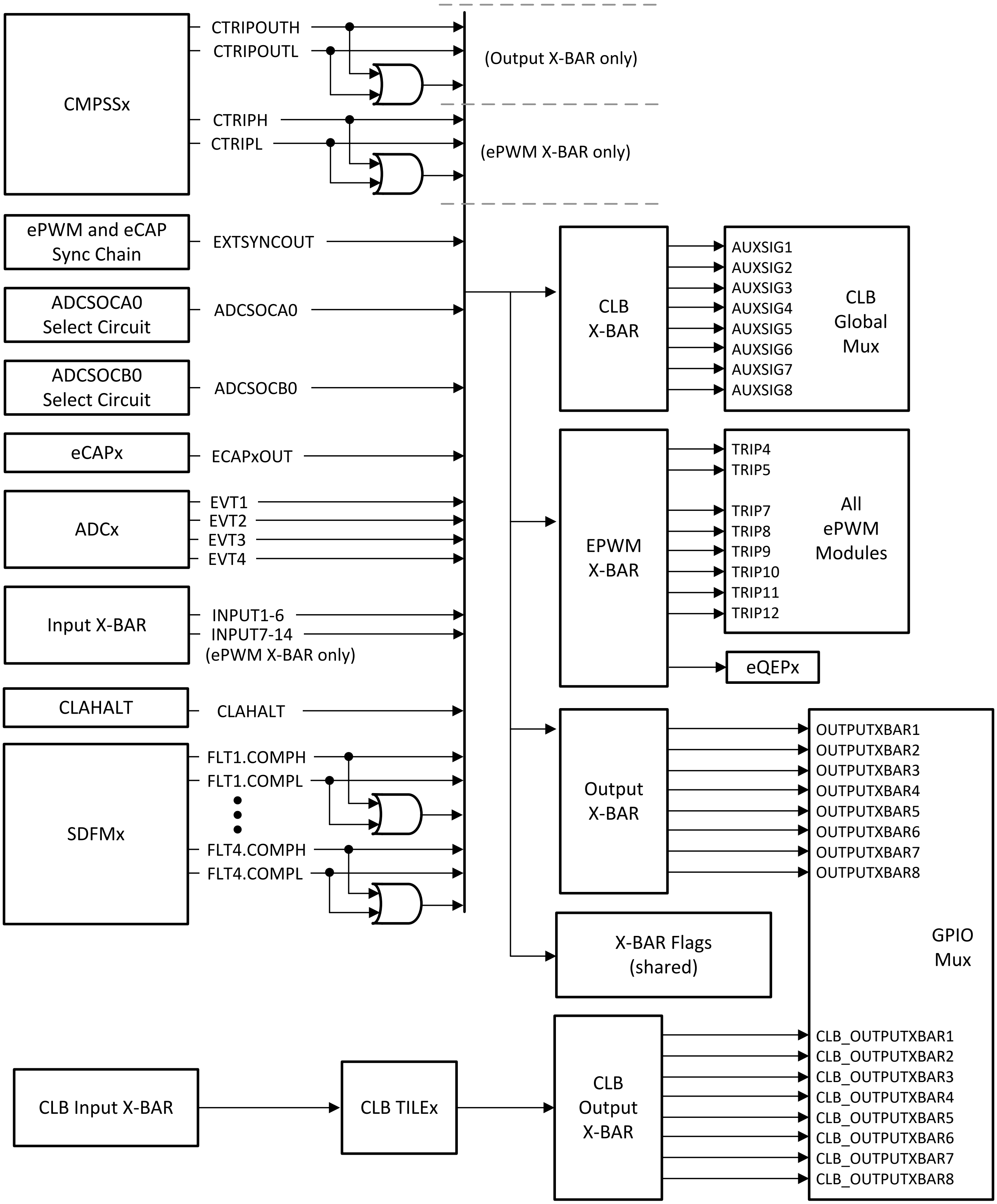


Figure 6-8. Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR Sources

6.5.4 USB Pin Muxing

Table 6-9 lists assignment of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 6-9. Alternate USB Function

GPIO	GPBAMSEL SETTING	USB FUNCTION
GPIO42	GPBAMSEL[10] = 1b	USB0DM
GPIO43	GPBAMSEL[11] = 1b	USB0DP

6.5.5 High-Speed SPI Pin Muxing

The SPI module on this device has a high-speed mode. To achieve the highest possible speed, a special GPIO configuration is used on a single GPIO mux option for each SPI. These GPIOs may also be used by the SPI when not in high-speed mode (HS_MODE = 0).

To select the mux options that enable the SPI high-speed mode, configure the GPyGMUX and GPyMUX registers as shown in Table 6-10.

Table 6-10. GPIO Configuration for High-Speed SPI

GPIO	SPI SIGNAL	MUX CONFIGURATION	
		SPIA	
GPIO58	SPISIMOA	GPBGMUX2[21:20]=11b	GPBMUX2[21:20]=11b
GPIO59	SPISOMIA	GPBGMUX2[23:22]=11b	GPBMUX2[23:22]=11b
GPIO60	SPICLKA	GPBGMUX2[25:24]=11b	GPBMUX2[25:24]=11b
GPIO61	$\overline{\text{SPISTEA}}$	GPBGMUX2[27:26]=11b	GPBMUX2[27:26]=11b
		SPIB	
GPIO63	SPISIMOB	GPBGMUX2[31:30]=11b	GPBMUX2[31:30]=11b
GPIO64	SPISOMIB	GPCGMUX1[1:0]=11b	GPCMUX1[1:0]=11b
GPIO65	SPICLKB	GPCGMUX1[3:2]=11b	GPCMUX1[3:2]=11b
GPIO66	$\overline{\text{SPISTEB}}$	GPCGMUX1[5:4]=11b	GPCMUX1[5:4]=11b
		SPIC	
GPIO69	SPISIMOC	GPCGMUX1[11:10]=11b	GPCMUX1[11:10]=11b
GPIO70	SPISOMIC	GPCGMUX1[13:12]=11b	GPCMUX1[13:12]=11b
GPIO71	SPICLKC	GPCGMUX1[15:14]=11b	GPCMUX1[15:14]=11b
GPIO72	$\overline{\text{SPISTEC}}$	GPCGMUX1[17:16]=11b	GPCMUX1[17:16]=11b
		SPID	
GPIO91	SPISIMOD	GPCGMUX2[23:22]=11b	GPCMUX2[23:22]=11b
GPIO92	SPISOMID	GPCGMUX2[25:24]=11b	GPCMUX2[25:24]=11b
GPIO93	SPICLKD	GPCGMUX2[27:26]=11b	GPCMUX2[27:26]=11b
GPIO94	$\overline{\text{SPISTED}}$	GPCGMUX2[29:28]=11b	GPCMUX2[29:28]=11b

6.5.6 High-Speed SSI Pin Muxing

The SSI module on this device has a high-speed mode. To enable the high-speed mode on the SSI module, enable the high-speed clock and the high-speed capabilities of the SSI module (SSICR1[HSCLKEN] and SSIPP[HSCLK]). The GPIO Configuration for High-Speed SSI table lists the SSI high-speed-capable pinmux options.

Table 6-11. GPIO Configuration for High-Speed SSI

GPIO	SSI SIGNAL	GPIO MUX SELECTION INDEX
GPIO16	SSIA_TX	11
GPIO17	SSIA_RX	11
GPIO18	SSIA_CLK	11
GPIO19	SSIA_FSS	11

6.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 6-12 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 6-12, any are acceptable. Pins not listed in Table 6-12 must be connected according to the Pin Attributes table.

Table 6-12. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
Analog	
VREFHIx	Tie to VDDA
VREFLOx	Tie to VSSA
ADCINx (except DAC pins)	• No Connect • Tie to VSSA
ADCINx (DAC pins)	• No Connect • Pulldown to VSSA through 5-kΩ resistor
Digital	
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
X1	Tie to VSS
X2	No Connect
TCK	• No Connect • Pullup resistor
TDI	• No Connect • Pullup resistor
TDO	No Connect
TMS	No Connect
TRSTn	Pulldown resistor (2.2 kΩ or smaller)
ERRORSTS	No Connect
FLT1	No Connect
FLT2	No Connect
Power and Ground	
VDD	All VDD pins must be connected per the Pin Attributes table.
VDDA	If a dedicated analog supply is not used, tie to VDDIO.
VDDIO	All VDDIO pins must be connected per the Pin Attributes table.
VDD3VFL	Must be tied to VDDIO
VDDOSC	Must be tied to VDDIO
VSS	All VSS pins must be connected to board ground.
VSSA	If a dedicated analog ground is not used, tie to VSS.
VSSOSC	If an external crystal is not used, this pin may be connected to the board ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDDIO with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
	VDD3VFL with respect to VSS	–0.3	4.6	
	VDDOSC with respect to VSS	–0.3	4.6	
	VDD with respect to VSS	–0.3	1.5	
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital/analog input (per pin), I_{IK} (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/ VDDA)(4)	–20	20	mA
	Total for all inputs, $I_{IKTOTAL}$ (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Ambient temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature(3)	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(4) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.

7.2 ESD Ratings – Commercial

				VALUE	UNIT
TMS320F28388D, TMS320F28386D, TMS320F28384D, TMS320F28388S, TMS320F28386S, and TMS320F28384S in 337-ball ZWT package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner balls on 337-ball ZWT: A1, A19, W1, W19	±750	
TMS320F28388D, TMS320F28386D, TMS320F28384D, TMS320F28388S, TMS320F28386S, and TMS320F28384S in 176-pin PTP package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings – Automotive

				VALUE	UNIT
TMS320F28386D-Q1 and TMS320F28384D-Q1 in 337-ball ZWT package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner balls on 337-ball ZWT: A1, A19, W1, W19	±750	
TMS320F28386D-Q1, TMS320F28384D-Q1, TMS320F28386S-Q1, and TMS320F28384S-Q1 in 176-pin PTP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, VDDIO[(1)]		3.14	3.3	3.47	V
Analog supply voltage, VDDA		3.14	3.3	3.47	V
Device supply voltage, VDD		1.14	1.2	1.26	V
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS[(2)]			10^5	V/s
V_{IN}	Digital input voltage	VSS – 0.3		VDDIO + 0.3	V
V_{IN}	Analog input voltage	VSSA – 0.3		VDDA + 0.3	V
Junction temperature, T_J	S version[(3)]	–40		125	°C
Free-Air temperature, T_A	Q version[(3)] (AEC Q100 qualification)	–40		125	°C

(1) VDDIO, VDD3VFL, and VDDOSC should be maintained within 0.3 V of each other.
(2) Supply ramp rate faster than this can trigger the on-chip ESD protection.
(3) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See Calculating Useful Lifetimes of Embedded Processors for more information.

7.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Section 7.5.1 lists the system current consumption values for an external supply.

7.5.1 System Current Consumption (External Supply)

over operating free-air temperature range (unless otherwise noted).
TYP : V_{nom}, 30°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING MODE						
I_{DD}	VDD current consumption during operational usage(3)	See Section 7.5.2.		288	475	mA
I_{DDIO}	VDDIO current consumption during operational usage(2)			45		mA
I_{DDA}	VDDA current consumption during operational usage			8	15	mA
IDLE MODE						
I_{DD}	VDD current consumption while device is in Idle mode(3)	CPU is in IDLE mode • Flash is powered down • XCLKOUT is turned off		90	265	mA
I_{DDIO}	VDDIO current consumption while device is in Idle mode(2)			4	7	mA
I_{DDA}	VDDA current consumption while device is in Idle mode			0.002	0.010	mA
STANDBY MODE						
I_{DD}	VDD current consumption while device is in Standby mode(3)	CPU is in STANDBY mode • Flash is powered down • XCLKOUT is turned off		30	200	mA
I_{DDIO}	VDDIO current consumption while device is in Standby mode(2)			4	7	mA
I_{DDA}	VDDA current consumption while device is in Standby mode			0.002	0.010	mA
FLASH ERASE/PROGRAM						
I_{DD}	VDD Current consumption during Erase/ Program cycle(1) (3)	CPU is running from Flash, performing Erase and Program on the unused sector. • SYSCLK is running at 200 MHz. • I/Os are inputs with pullups enabled. • Peripheral clocks are turned OFF.		242	360	mA
I_{DDIO}	VDDIO Current consumption during Erase/ Program cycle(1) (2)			56	75	mA
I_{DDA}	VDDA Current consumption during Erase/ Program cycle			0.01	0.15	mA
RESET MODE						
I_{DD}	VDD current consumption while held in reset via XRSn(3)	CPU is held in reset via external low signal driven onto XRSn • XRSn held low through power-up		55		mA
I_{DDIO}	VDDIO current consumption while held in reset via XRSn(2)	CPU is held in reset via external low signal driven onto XRSn • XRSn held low through power-up		15		mA
I_{DDA}	VDDA current consumption while held in reset via XRSn	CPU is held in reset via external low signal driven onto XRSn • XRSn held low through power-up		0.05		mA

(1) Brown-out events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brown-out conditions.
(2) Includes current consumption for VDD3VFL supply (VDDIO + VDD3VFL).
(3) VDD current values in this table do not include the 21-mA current from VDD to VSS through the 56Ω resistor that is mentioned in the Signal Descriptions section

7.5.2 Operating Mode Test Description

Section 7.5.1 and the Typical Current Reduction per Disabled Peripheral table list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- CPU1 and CPU2 are operating at 200 MHz and CM is operating at 125 MHz.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

7.5.3 Current Consumption Graphs

Figure 7-1, Figure 7-2, and Figure 7-3 show a typical representation of the relationship between frequency, temperature, core supply, and current consumption on the device. Actual results will vary based on the system implementation and conditions.

Figure 7-1 shows the typical operating current profile across temperature and core supply voltage. Figure 7-2 shows the typical standby current profile across temperature and core supply voltage. Figure 7-3 shows how the typical operating currents change with changing clock frequency of the C28x CPUs and changing clock frequency of the CM module.

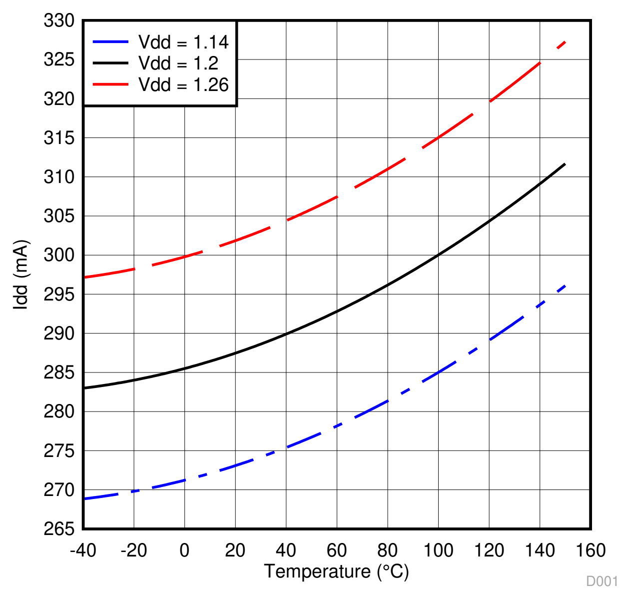


Figure 7-1. Typical Operating Current Versus Temperature

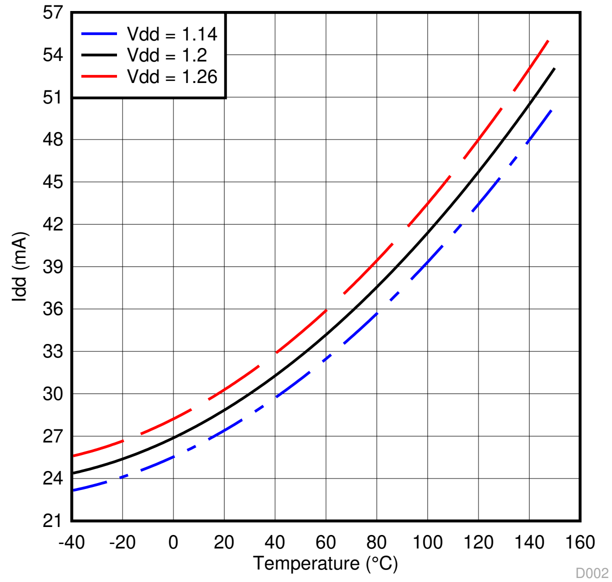


Figure 7-2. Typical Standby Current Versus Temperature

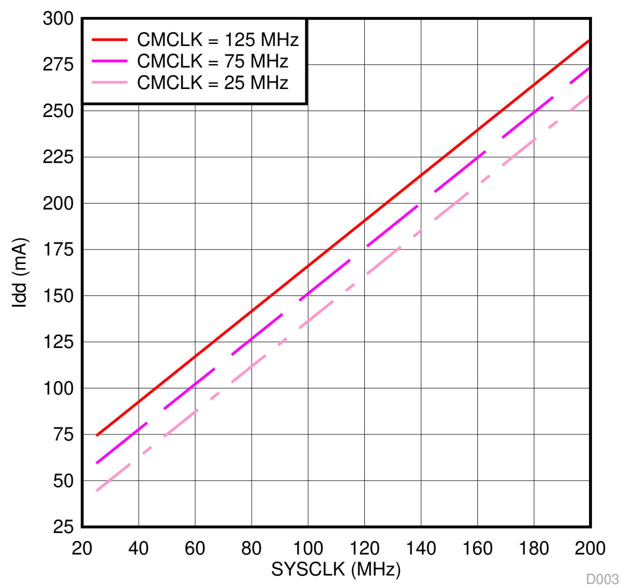


Figure 7-3. Typical Operating Current Versus SYSCLK

7.5.4 Reducing Current Consumption

The F2838x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. The Typical Current Reduction per Disabled Peripheral table lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

7.5.4.1 Typical Current Reduction per Disabled Peripheral

PERIPHERAL[(1)]	I_{DD} CURRENT REDUCTION (mA)
ADC[(2)]	2.6
CLA	1.5
CLA BGCRC	0.3
CLB	1.6
CM - AES	0.4
CM - GCRC	2.4
CM - I2C	1.4
CM - SSI	0.4
CM - uDMA	0.4
CM - UART	0.7
CMPSS[(2)]	0.7
CPU BGCRC	0.5
CPU TIMER	0.1
DAC[(2)]	0.4
DCAN	1.6
DCC	0.2
DMA	1.4
eCAP1 to eCAP5	0.3
eCAP6 to eCAP7[(3)]	0.7
EMIF	1.0
ERAD	4.0
ePWM1 - ePWM8[(4)]	2.0
ePWM9 - ePWM16	1.1
eQEP	0.5
EtherCAT	2.9
Ethernet	3.7
FSI RX	0.7
FSI TX	0.9
I2C	0.4
MCAN (CAN FD)	1.5
McBSP	2.4
PMBUS	0.6
SCI	0.3

7.5.4.1 Typical Current Reduction per Disabled Peripheral (continued)

PERIPHERAL(1)	I_{DD} CURRENT REDUCTION (mA)
SDFM	2.7
SPI	0.7
USB	5.4

(1) All peripherals are disabled upon reset. Use the PCLKCRx register to individually enable peripherals. For peripherals with multiple instances, the current quoted is for a single module.
(2) This current represents the current drawn by the digital portion of the each module.
(3) eCAP6 and eCAP7 can also be configured as HRCAP.
(4) ePWM1 to ePWM8 can also be configured as HRPWM.

7.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}$ MIN	VDDIO * 0.8			V
			I_{OH} = –100 µA	VDDIO – 0.2			V
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}$ MAX			0.4	V
			I_{OL} = 100 µA			0.2	V
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	Group 1(1)	High-level output impedance for group 1 output pins			70		Ω
	Group 2(2)	High-level output impedance for group 2 output pins			35		Ω
	Group 3(3)	High-level output impedance for group 3 output pins			45		Ω
	Group 4(4)	High-level output impedance for group 4 output pins			60		Ω
R_{OL}	Group 1(1)	Low-level output impedance for group 1 output pins			70		Ω
	Group 2(2)	Low-level output impedance for group 2 output pins			35		Ω
	Group 3(3)	Low-level output impedance for group 3 output pins			45		Ω
	Group 4(4)	Low-level output impedance for group 4 output pins			60		Ω
V_{IH}	High-level input voltage (3.3V)	GPIO42, GPIO43		VDDIO * 0.7			V
		All other pins		2.0			V
V_{IL}	Low-level input voltage (3.3V)					0.8	V
$V_{HYSTERESIS}$	Input hysteresis				150		mV
$I_{PULLDOWN}$	Input current	Digital Inputs with pulldown(5)	VDDIO = 3.3 V V_{IN} = VDDIO		120		µA
I_{PULLUP}	Input current	Digital Inputs with pullup enabled(5)	VDDIO = 3.3 V V_{IN} = 0 V		150		µA

7.6 Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	Pin leakage	Digital	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDDIO	-2		2	µA
		Analog (except ADCINB0 or DACOUTx)	0 V ≤ V_{IN} ≤ VDDA	-0.3		0.3	µA
		ADCINB0(6)			2	11	µA
		DACOUTx			66		µA
C_I	Input capacitance(7)				2		pF
$V_{DDIO-POR}$	VDDIO power on reset voltage				2.5		V

(1) Group 1: GPIO0-2, 6, 8-10, 16, 18-29, 31-41, 44-70, 72-117, 119-132, 134-138
(2) Group 2: GPIO3-5, 7, 11-15, 17, 133, 139-168
(3) Group 3: GPIO30, 71, 118
(4) Group 4: USB pins (GPIO42, 43)
(5) See Table 6-6 for a list of pins with a pullup or pulldown.
(6) The MAX input leakage shown on ADCINB0 is at high temperature.
(7) The analog pins are specified separately; see Table 7-12.

7.7 Thermal Resistance Characteristics for ZWT Package

		°C/W[1]	AIR FLOW (lfm)[2]
$R\Theta_{JC}$	Junction-to-case thermal resistance	8.3	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	11.6	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-ambient thermal resistance	20.6	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	18.6	150
		17.4	250
		16.5	500
Psi_{JT}	Junction-to-package top	0.3	0
		0.4	150
		0.5	250
		0.6	500
Psi_{JB}	Junction-to-board	11.4	0
		11.2	150
		11.1	250
		11.1	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

7.8 Thermal Resistance Characteristics for PTP Package

		°C/W[1]	AIR FLOW (lfm)[2]
$R\Theta_{JC}$	Junction-to-case thermal resistance	6.97	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	6.05	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-ambient thermal resistance	17.8	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	12.8	150
		11.4	250
		10.1	500
Psi_{JT}	Junction-to-package top	0.11	0
		0.24	150
		0.33	250
		0.42	500
Psi_{JB}	Junction-to-board	6.1	0
		5.5	150
		5.4	250
		5.3	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

7.9 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

7.10 System

7.10.1 Power Management Module (PMM)

7.10.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

7.10.1.2 Overview

The block diagram of the PMM is shown in PMM Block Diagram. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections. Rise delays, as shown in the figure, represent delays in the release of reset that happen on power up(rising voltage) only. These delays do not exist for power down condition.

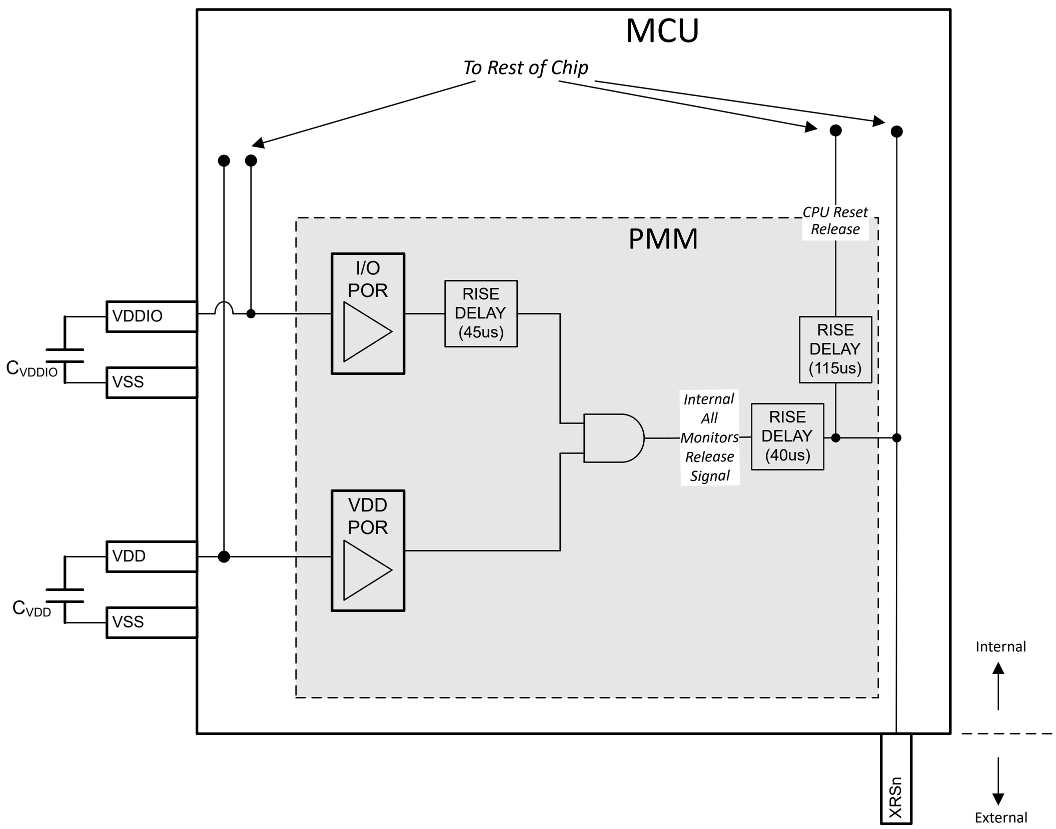


Figure 7-4. PMM Block Diagram

7.10.1.2.1 Power Rail Monitors

The PMM has voltage monitors on both the VDDIO and VDD supply rails that release the XRSn signal high once the supply voltages cross the set thresholds during power up. The role of the PMM on this device is to ensure that IO pins are glitch free during power up and XRSn is held active low during this time. If the minimum rising slew rates are met, then XRSn will be held until the device has proper voltage levels to meet the device's electrical specifications.

However, the detection limits of the PMM are below the minimum operational ranges for the device. If the rising slew rate is not met, XRSn will be released before the supply rails are within specification. Likewise if there is a droop on either of the voltage lines the PMM may not detect an out of range event depending on where the supply voltage settle. As such, an external voltage supervisor is required to monitor the device voltage rails and release reset to the device for these conditions.

Two voltage monitors (I/O POR,VDD POR) both have to detect that their input voltage levels are greater than their respective release thresholds before the PMM will release the drive on the XRSn pin(active low, open-drain input). If the voltage on either supply pin falls below the release point XRSn will be driven low by the device. The I/Os are held in a high impedance state when either of the voltage monitors trip.

7.10.1.2.2 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDDIO.

Note

I/O POR is programmed at a level below the minimum recommended voltage for VDDIO, and therefore it should not be relied upon for sole VDDIO supervision. An external supervisor is recommended for precise monitoring of the VDDIO bus voltage.

7.10.1.2.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for sole VDD supervision. An external supervisor is recommended for precise monitoring of the VDD supply rail.

7.10.1.2.4 External Supervisor Usage

VDDIO Monitoring: An external supervisor is required to monitor the VDDIO rail for in-specification operation. The internal I/O POR is intended to keep the GPIOs from glitching during power up and will hold XRSn active low during this time.

VDD Monitoring: An external supervisor is required to monitor the VDD rail for in-specification operation. The internal VDD POR is intended to keep the GPIOs from glitching during power up and will hold XRSn active low during this time.

7.10.1.2.5 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. These delays ensure that the voltages are stable as both VDDIO and VDD rails ramp up. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in Power Management Module Electrical Data and Timing for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

7.10.1.3 External Components

7.10.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

7.10.1.3.2 VDDIO Decoupling

A minimum amount of decoupling capacitance should be placed on VDDIO. See the C_{VDDIO} parameter in Power Management Module Electrical Data and Timing. The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of C_{VDDIO} * VDDIO pins.

Note

It is critical to have the decoupling capacitor or capacitors close to the supply pins.

7.10.1.4 Power Sequencing

7.10.1.4.1 Supply Pins Ganging

It is strongly recommended that all 3.3-V rails be tied together and supplied from a single source. This list includes:

- VDDIO
- VDDA
- VDD3VFL
- VDDOSC

In addition, no power pin should be left unconnected.

The VDD pins should be tied together and supplied from a single source.

The analog modules on the device have a fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

7.10.1.4.2 Signal Pins Power Sequence

Before powering the device, no voltage larger than 0.3 V above VDDIO or 0.3 V below VSS should be applied to any digital pin; and no voltage larger than 0.3 V above VDDA or 0.3 V below VSSA should be applied to any analog pin (including VREFHI and VDAC). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

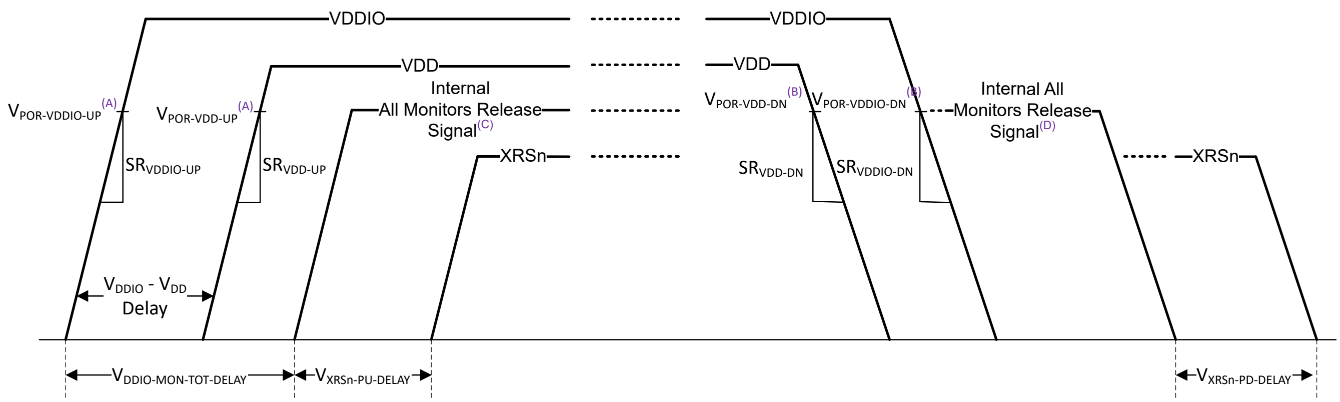
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

7.10.1.4.3 Supply Pins Power Sequence

7.10.1.4.3.1 Power Supply Sequence

Figure 7-5 depicts the power sequencing requirements for the device. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the Power Management Module Characteristics table.
B. This trip point is the trip point after XRSn releases. See the Power Management Module Characteristics table.
C. During power up, the All Monitors Release Signal goes high after all POR monitors are released. See the PMM Block Diagram.
D. During power down, the All Monitors Release Signal goes low if any of the POR monitors are tripped. See the PMM Block Diagram.
E. Above is showing the internal drive on XRSn. An external supervisor can at anytime pull XRSn active low as needed.

Figure 7-5. Power Up/Down Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
  2. VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
  3. The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
  4. After the times specified by $V_{DDIO\text{-}MON\text{-}TOT\text{-}DELAY}$ and $V_{XRSN\text{-}PD\text{-}DELAY}$, XRSn will be released and the device starts the boot-up sequence.

     There is an additional delay between XRSn releasing (that is, going high) and the boot-up sequence starting. See PMM Block Diagram.
  5. During power up, both VDDIO and VDD rails have to be up before XRSn releases.
- **For Power Down:**
  1. There is no requirement between VDDIO and VDD on which should power down first; however, it is recommended that VDD ≤ VDDIO.
  2. Any of the POR monitors that trips during power down will cause XRSn to go low after $V_{XRSN\text{-}PD\text{-}DELAY}$.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

7.10.1.4.3.2 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION
Non-acceptable sequences will lead to reliability concerns and possibly damage.

For simplicity, it is recommended that all 3.3-V rails be tied together, and to follow the descriptions in Supply Pins Power Sequence.

Table 7-1. Sequence Summary

CASE	RAILS POWER-UP ORDER			ACCEPTABLE
	VDDIO	VDDA	VDD	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	-
D	2	3	1	-
E	3	2	1	-
F	3	1	2	-
G	1	1	2	Yes
H	2	2	1	-

Note
The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

7.10.1.4.3.3 Supply Slew Rate

Both VDDIO and VDD have a minimum slew rate requirement. If the minimum slew rate is not met, the device can release from reset and start booting before either VDDIO or VDD has reached the minimum operating voltage, which can result in the device not functioning correctly.

Note
If the minimum slew rate cannot be met, a supervisor must be used on VDDIO and VDD to keep XRSn low until VDD crosses the minimum operating voltage to ensure correct device functionality.

7.10.1.5 Power Management Module Electrical Data and Timing

7.10.1.5.1 Power Management Module Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
C_{VDDIO}	Capacitance on each VDDIO/VDD3FL/ VDDOSC pins	Based on External Supply IC Requirements(1)	0.1			µF
C_{VDDA}	Capacitor on each VDDA pins(5)		2.2			µF
C_{VDD} TOTAL(2)	Total VDD Capacitance(5)		20	22		µF
R_{VDD}TOTAL(7)	Total VDD Resistance to VSS		56			Ω
$SR_{VDDIO-UP}$ (3) (6)	Supply Ramp Up Rate of 3.3V Rail (VDDIO)		8		100	mV/µs
$SR_{VDDIO-DN}$ (3) (6)	Supply Ramp Down Rate of 3.3V Rail (VDDIO)		20		100	mV/µs
SR_{VDD-UP} (3) (6)	Supply Ramp Up Rate of 1.2V Rail (VDD)		3.5		100	mV/µs
SR_{VDD-DN} (3) (6)	Supply Ramp Down Rate of 1.2V Rail (VDD)		10		100	mV/µs
V_{DDIO} - V_{DD} Delay(4)	Ramp Delay Between VDDIO and VDD		0		No Restrictions	µs

(1) Bulk capacitance on this supply should be based on supply IC requirements.
(2) The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
(4) Delay between when the 3.3-V rail ramps up and when the 1.2-V rail ramps up.
(5) Max capacitor tolerance should be 20%.
(6) If an external supervisor is used there is no need to observe the minimum slew rate
(7) A single 56Ω resistor (10% tolerance) should be placed between between VDD and VSS. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.

7.10.1.5.2 Power Management Module Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{POR-VDDIO-UP}$	VDDIO Power on Reset Voltage on Ramp Up	Before XRSn Release		2.5		V
$V_{POR-VDDIO-DN}$	VDDIO Power on Reset Voltage on Ramp Down	After XRSn Release		2.7		V
$V_{POR-VDD-UP}$	VDD Power on Reset Voltage on Ramp Up	Before XRSn Release		1		V
$V_{POR-VDD-DN}$	VDD Power on Reset Voltage on Ramp Down	After XRSn Release		1.047		V
$V_{XRSn-PU-DELAY}$ (1)	XRSn Release Delay after Supplies are Ramped Up During Power Up			40		µs
$V_{XRSn-PD-DELAY}$ (2)	XRSn Trip Delay after Supplies are Ramped Down During Power Down			2		µs
$V_{DDIO-MON-TOT-DELAY}$	Total Delays in Path of VDDIO Monitors (POR)			45		µs
$V_{XRSn-MON-RELEASE-DELAY}$	XRSn Release Delay after a VDD POR Event	Supplies Within Operating Range		40		µs
	XRSn Release Delay after a VDDIO POR Event			85		µs

(1) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect. RC network delay will add to this.
(2) On power down, any of the POR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply. RC network delay will add to this.

7.10.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR). During power up, the POR circuit drives the XRSn pin low. A watchdog or NMI watchdog reset also drives the pin low. An external circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and V_{DDIO}. A capacitor should be placed between XRSn and V_{SS} for noise filtering; the capacitance should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 7-6 shows the recommended reset circuit.

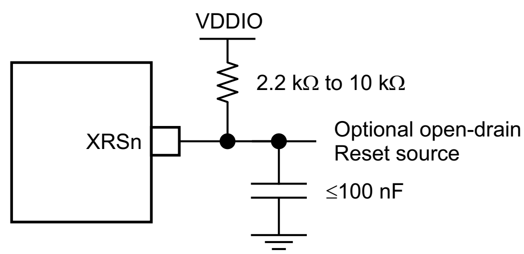


Figure 7-6. Reset Circuit

7.10.2.1 Reset Sources

The Reset Signals table summarizes the various reset signals and their effect on the device. CM subsystem resets are described in the Reset section of the Connectivity Manager System Control and Interrupts chapter in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-2. Reset Signals

Reset Source	CPU1 Core Reset (C28x, TMU, FPU, VCRC)	CPU1 Peripheral Reset	CPU2 Core Reset (C28x, TMU, FPU, VCRC)	CPU2 and CM Peripheral Reset	CPU2 and CM Held In Reset	JTAG / Debug Logic Reset	IOs	XRSn Output
POR	Yes	Yes	Yes	Yes	Yes	Yes	Hi-Z	Yes
XRSn Pin	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1.SIMRESET.XRSn	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1. $\overline{\text{WDRS}}$	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1. $\overline{\text{NMIWDRS}}$	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
CPU1. $\overline{\text{SYSRS}}$ (Debugger Reset)	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1.SIMRESET.CPU1RSn	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1. $\overline{\text{SCCRESET}}$	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	-
CPU1. $\overline{\text{HWBISTRS}}$	Yes	-	-	-	-	-	-	-
CPU2. $\overline{\text{SYSRS}}$ (Debugger Reset)	-	-	Yes	Yes	-	-	-	-
CPU2. $\overline{\text{WDRS}}$	-	-	Yes	Yes	-	-	-	-
CPU2. $\overline{\text{NMIWDRS}}$	-	-	Yes	Yes	-	-	-	-
CPU2. $\overline{\text{SCCRESET}}$	-	-	Yes	Yes	-	-	-	-
CPU2. $\overline{\text{HWBISTRS}}$	-	-	Yes	-	-	-	-	-
ECAT_RESET_OUT	Yes	Yes	Yes	Yes	Yes	-	Hi-Z	Yes
TRSTn	-	-	-	-	-	Yes	-	-

The parameter $t_{h(boot-mode)}$ must account for a reset initiated from any of these sources.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low. Use this to disable any other devices driving the boot pins. The $\overline{\text{SCCRESET}}$ and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP; for more details, see the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

7.10.2.2 Reset Electrical Data and Timing

Section 7.10.2.2.1 lists the reset (XRSn) timing requirements. Section 7.10.2.2.2 lists the reset (XRSn) switching characteristics. Figure 7-7 shows the power-on reset. Figure 7-8 shows the warm reset.

7.10.2.2.1 Reset (XRSn) Timing Requirements

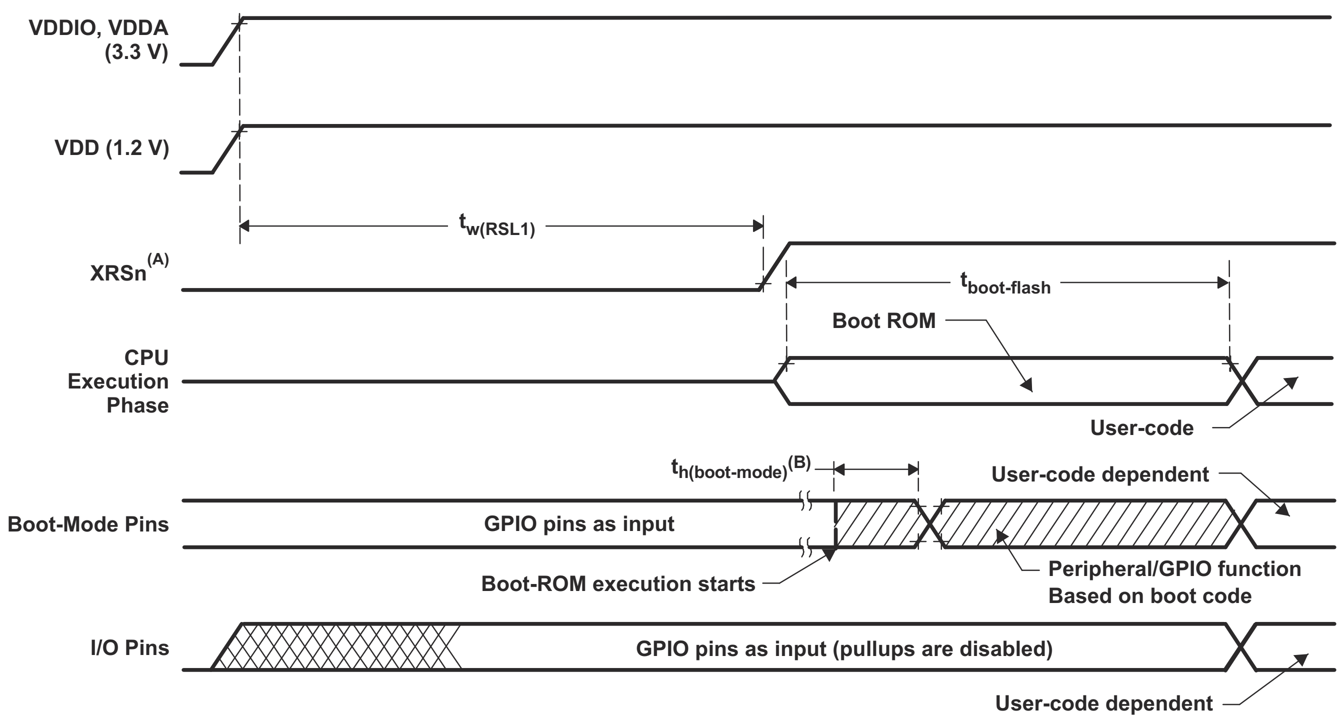
		MIN	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low on warm reset	3.2		µs

7.10.2.2.2 Reset (XRSn) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

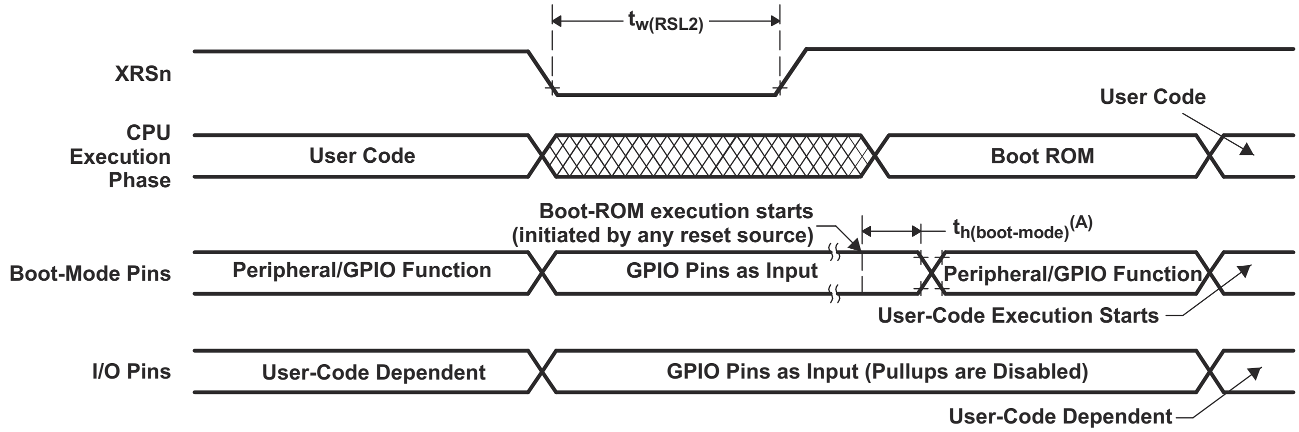
PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, XRSn driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{boot-flash}$	Boot-ROM execution time to first instruction fetch in flash			1.2	ms

7.10.2.2.3 Reset Timing Diagrams



A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the Pin Attributes table.
B. After reset from any source (see Section 7.10.2.1), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 7-7. Power-on Reset



A. After reset from any source (see Section 7.10.2.1), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 7-8. Warm Reset

7.10.3 Clock Specifications

7.10.3.1 Clock Sources

Table 7-3 lists four possible clock sources. Figure 7-9 provides an overview of the device's clocking system.

Table 7-3. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1	Can be used to provide clock for: • Watchdog block • Main PLL • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.
AUXCLKIN	Can be used to provide clock for: • Auxiliary PLL • CPU-Timer 2	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

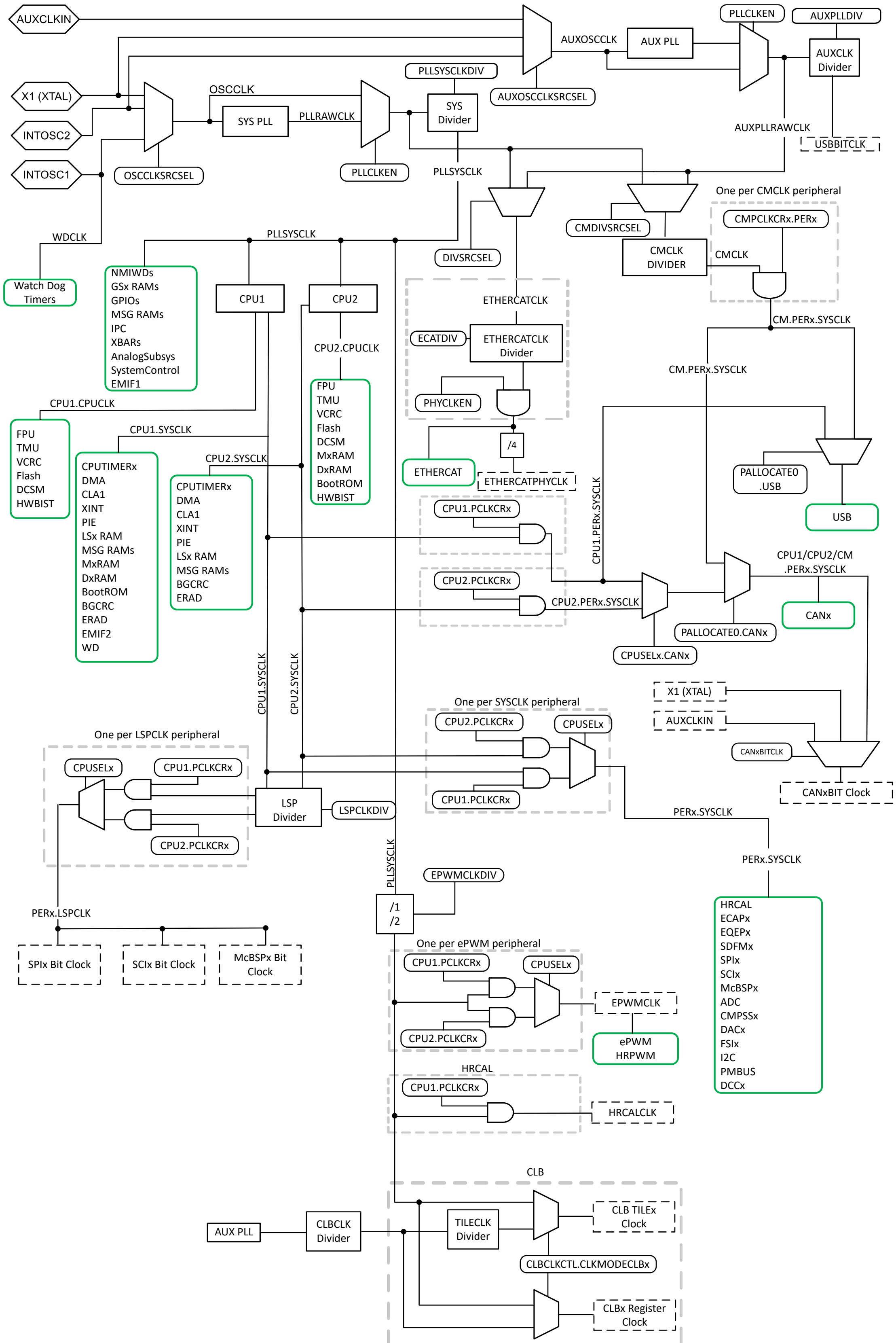


Figure 7-9. Clocking System

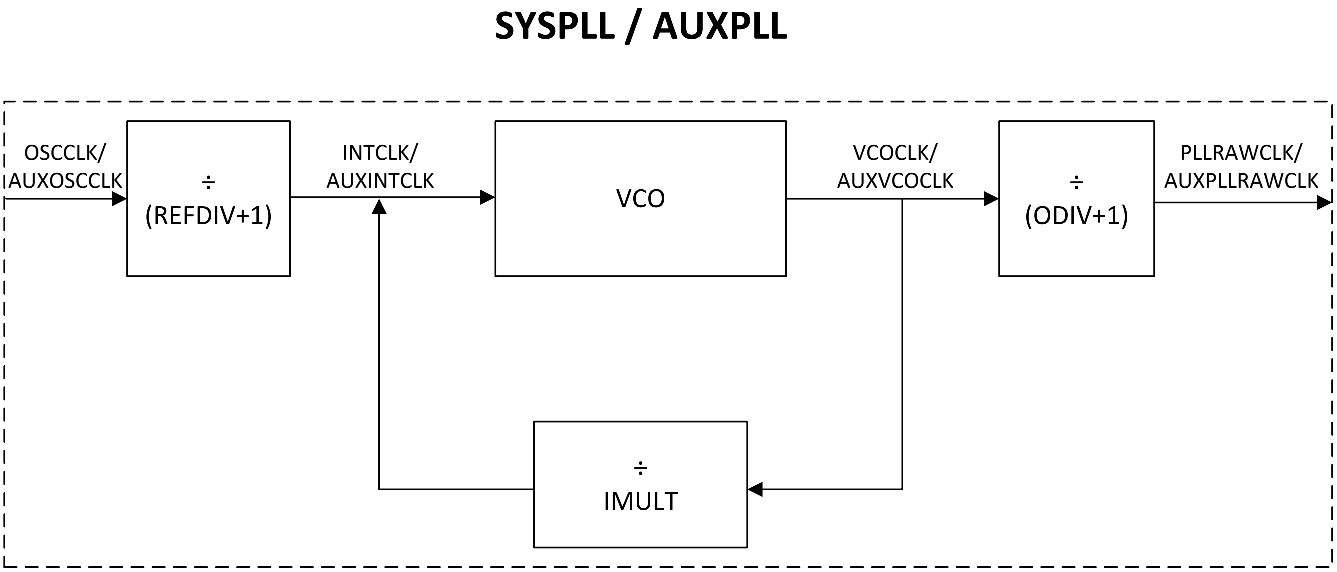


Figure 7-10. SYSPLL/AUXPLL

In Figure 7-10,

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REVDIV + 1)} \times \frac{IMULT}{(ODIV + 1)}$$

$$f_{AUXPLLRAWCLK} = \frac{f_{AUXOSCCLK}}{(REVDIV + 1)} \times \frac{IMULT}{(ODIV + 1)}$$

7.10.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

7.10.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Section 7.10.3.2.1.1 lists the frequency requirements for the input clocks. Section 7.10.3.2.1.2 lists the XTAL oscillator characteristics. Section 7.10.3.2.1.3 and Section 7.10.3.2.1.4 list the timing requirements for the input clocks. Section 7.10.3.2.1.5 lists the PLL lock times for SYSPLL and AUXPLL.

7.10.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	10	25	MHz
$f_{(AUXI)}$	Frequency, AUXCLKIN, from external oscillator	10	60	MHz

7.10.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

7.10.3.2.1.3 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

7.10.3.2.1.4 AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(AUXI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(AUXI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(AUXL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(AUXH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

7.10.3.2.1.5 APLL Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
PLL Lock Time				
SYSPLL / AUXPLL Lock time(1)			5µs + (1024 * (REFDIV + 1) * $t_{c(OSCCLK)}$)	µs

(1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1 or AUXPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock(). For the auxiliary PLL, see InitAuxPll() or SysCtl_setAuxClock().

7.10.3.2.2 Internal Clock Frequencies

The *Internal Clock Frequencies* table provides the clock frequencies for the internal clocks. Up to 1000 ppm of variation is accounted for in the frequencies below when using an external clock source such as a crystal or resonator.

7.10.3.2.2.1 Internal Clock Frequencies

		MIN	TYP	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		200	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	5		500	ns
$f_{(CMCLK)}$	Frequency, Connectivity Manager (CM) clock	2		125	MHz
$t_{c(CMCLK)}$	Period, Connectivity Manager (CM) clock	8		500	ns
$f_{(INTCLK)}$	Frequency, system PLL going into VCO (after REFDIV)[(1)]	2		25	MHz
$f_{(VCOCLK)}$	Frequency, system PLL VCO (before ODIV)	220		600	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	6		400	MHz
$f_{(AUXINTCLK)}$	Frequency, auxiliary PLL going into VCO (after REFDIV)	2		25	MHz
$f_{(AUXVCOCLK)}$	Frequency, auxiliary PLL VCO (before ODIV)	220		600	MHz
$f_{(AUXPLLRAWCLK)}$	Frequency, auxiliary PLL output (before AUXCLK divider)	6		400	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200	MHz
$f_{(PLL\_LIMP)}$	Frequency, PLL Limp Frequency [(2)]		45/(ODIV+1)		MHz
$f_{(AUXPLL)}$	Frequency, AUXPLLCLK	2		150	MHz
$f_{(AUXPLL\_LIMP)}$	Frequency, AUXPLL Limp Frequency [(3)]		45/(ODIV+1)		MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		200	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	5		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)		See respective clock		MHz
$f_{(AUXOSCCLK)}$	Frequency, auxiliary OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1 or AUXCLKIN)		See respective clock		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK			200	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		200	MHz
$f_{(CLBTILECLK)}$	Frequency, CLB tiles clock	100		150	MHz
$f_{(CLBREGCLK)}$	Frequency, CLK registers clock	150		200	MHz

(1) INTOSC1 and INTOSC2 with +/-3% resolution can be used as a Reference Clock to PLL
(2) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp)
(3) PLL output frequency when AUXOSCCLK is dead (Loss of AUXOSCCCLK causes AUXPLL to Limp)

7.10.3.2.3 Output Clock Frequency and Switching Characteristics

Section 7.10.3.2.3.1 lists the frequency and switching characteristics of the output clock, XCLKOUT.

7.10.3.2.3.1 XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)

over recommended operating conditions (unless otherwise noted)

PARAMETER[(1)]		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2[(2)]	H + 2[(2)]	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2[(2)]	H + 2[(2)]	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

7.10.3.3 Input Clocks

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 7-11 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 (also referred to as XTAL) and AUXCLKIN.

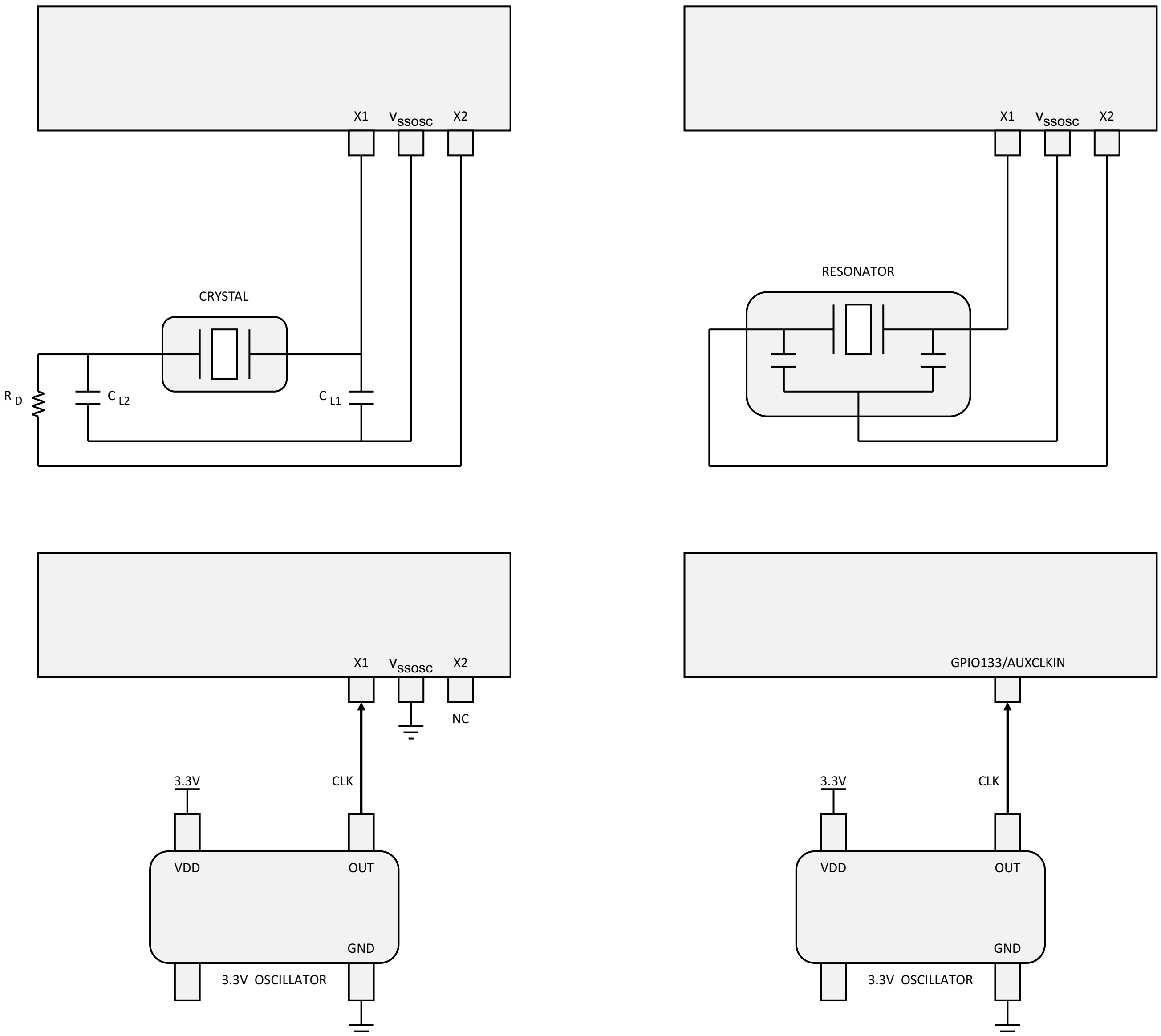


Figure 7-11. Connecting Input Clocks to a 2838x Device

7.10.3.4 XTAL Oscillator

7.10.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

7.10.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

7.10.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 7-12 illustrates the components of the electrical oscillator and the tank circuit.

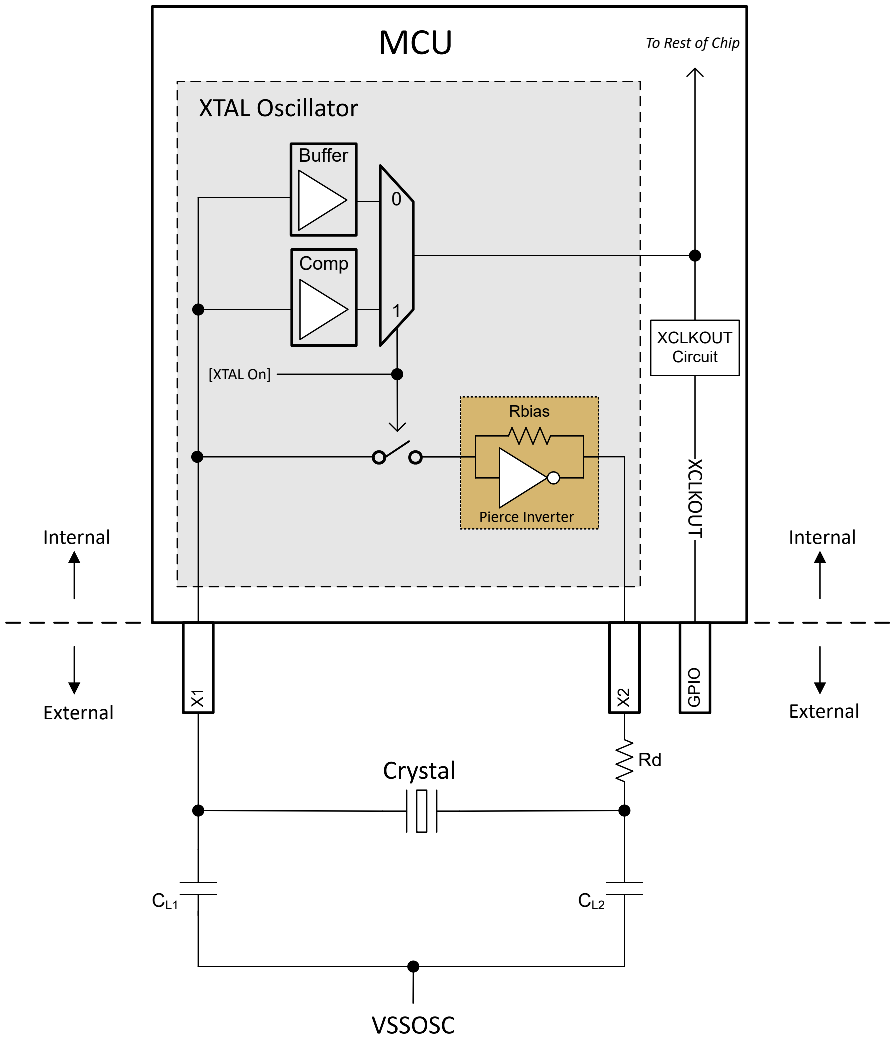


Figure 7-12. Electrical Oscillator Block Diagram

7.10.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

7.10.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when [XTAL On] = 1, which is achieved by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

7.10.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when [XTAL On] = 0, which can be achieved by setting XTALCR.OSCOFF = 1 and XTALCR.SE = 1.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

7.10.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the GPIO Muxed Pins table for a list of GPIOs that XCLKOUT comes out on.

7.10.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 7-13 and explained below.

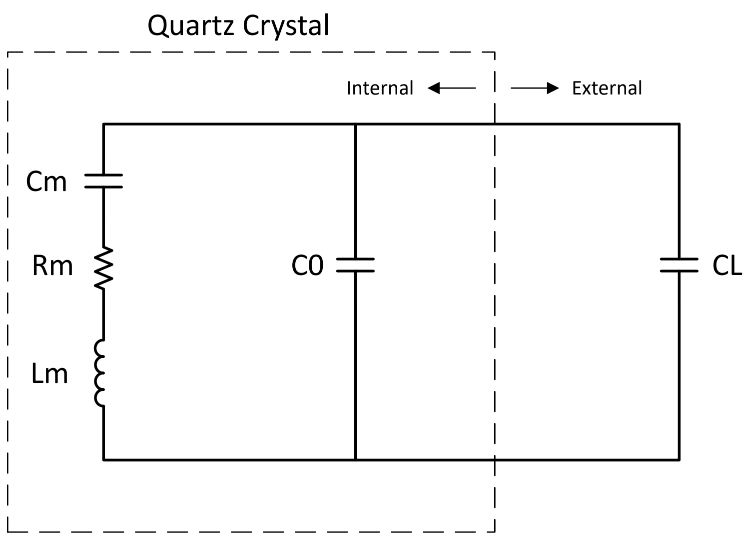


Figure 7-13. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 7-12, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

7.10.3.4.2.3 GPIO Modes of Operation

On this device, X1 and X2 can be used as GPIO19 and GPIO18, respectively, depending on the operating mode of the XTAL. Refer to the External Oscillator (XTAL) section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

7.10.3.4.3 Functional Operation

7.10.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \quad (1)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

7.10.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 7-14 and Figure 7-15 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 7-4 for minimum and maximum values for design considerations.

7.10.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the Rneg – Negative Resistance section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to Crystal Oscillator Specifications for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

7.10.3.4.3.3.1 X1/X2 Precondition

On this device, the GPIO19/18 alternate functionality on X1/X2 can be used to speed up the start-up time of the crystal if needed. This functionality is achieved by preconditioning the load capacitors CL1 and CL2 to a known state before the XTAL is turned on. See the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual* for details.

7.10.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer’s data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

7.10.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
   - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
   - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

7.10.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with <1-pF capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal’s actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

7.10.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the How to Choose a Crystal section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

7.10.3.4.7 Crystal Oscillator Specifications

7.10.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

7.10.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 7-4. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

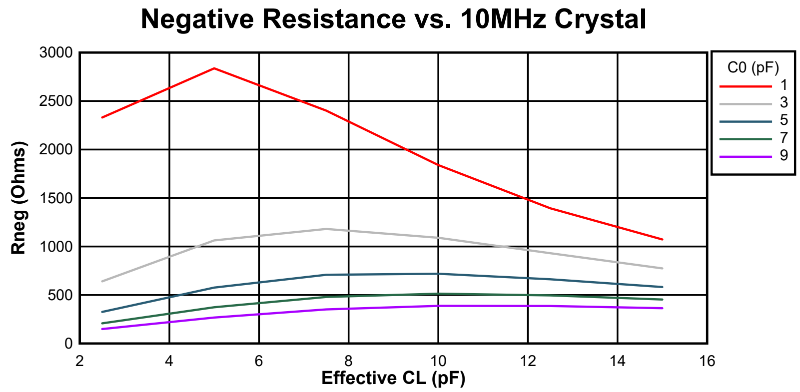


Figure 7-14. Negative Resistance Variation at 10 MHz

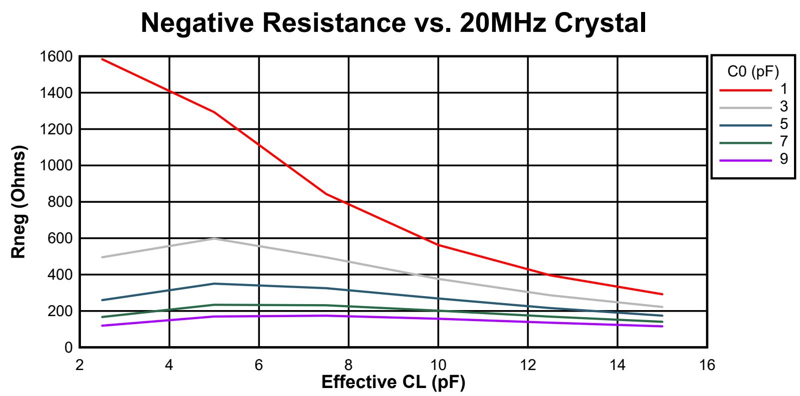


Figure 7-15. Negative Resistance Variation at 20 MHz

7.10.3.4.7.3 Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

7.10.3.4.7.4 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

7.10.3.5 Internal Oscillators

All F2838x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, both oscillators are enabled at power up. INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source. INTOSC1 can also be manually configured as the system reference clock (OSCCLK).

Section 7.10.3.5.1 provides the electrical characteristics of the internal oscillators to determine if this module meets the clocking requirements of the application.

Note

This oscillator cannot be used as the PLL source if the PLLSYSCLK is configured to frequencies above 194 MHz.

7.10.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{INTOSC}	Frequency, INTOSC1 and INTOSC2		9.7	10	10.3	MHz
$f_{INTOSC-STABILITY}$	Frequency stability at room temperature	30°C, Nominal VDD		±0.1		%
	Frequency stability over VDD	30°C		±0.2		%
$t_{INT0SC-ST}$	Start-up and settling time				20	µs

7.10.4 Flash Parameters

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 128-bit-wide prefetch reads and a pipeline buffer. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM.

This device also has an One-Time-Programmable (OTP) sector used for the dual code security module (DCSM), which cannot be erased after it is programmed.

Table 7-5 lists the minimum required flash wait states at different frequencies. The Flash Parameters table lists the flash parameters.

Table 7-5. Flash Wait States

CPUCLK (MHz)		MINIMUM WAIT STATES (1)
EXTERNAL OSCILLATOR OR CRYSTAL	INTOSC1 OR INTOSC2	
150 < CPUCLK ≤ 200	145 < CPUCLK ≤ 194	3
100 < CPUCLK ≤ 150	97 < CPUCLK ≤ 145	2
50 < CPUCLK ≤ 100	48 < CPUCLK ≤ 97	1
CPUCLK ≤ 50	CPUCLK ≤ 48	0

(1) Minimum required FRDCNTL[RWAIT].

7.10.4.1 Flash Parameters

PARAMETER		MIN	TYP	MAX	UNIT
Program Time(1)	128 data bits + 16 ECC bits		40	300	µs
	8KW sector		90	180	ms
Program Time(1)	32KW sector		360	720	ms
EraseTime(2) at < 25 cycles	8KW or 32KW sector		30	55	ms
EraseTime(2) at 1000 cycles	8KW or 32KW sector		40	350	ms
EraseTime(2) at 2000 cycles	8KW or 32KW sector		50	600	ms
EraseTime(2) at 20K cycles	8KW or 32KW sector		110	4000	ms
N_{wec} Write/Erase Cycles per sector				20000	cycles
N_{wec} Write/Erase Cycles for entire Flash (combined all sectors)(3)				100000	cycles
$t_{retention}$ Data retention duration at T_J = 85ºC		20			years
$t_{retention}$ Data retention duration at T_J = 125ºC(4)		10			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
• Code that uses flash API to program the flash
• Flash API itself
• Flash data to be programmed
In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the emulator used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.
(2) Erase time includes Erase verify by the CPU.
(3) Each sector, by itself, can only be erased/programmed 20,000 times. If you choose to use a sector (or multiple sectors) like an EEPROM, you can erase/program only those sectors (still limited to 20,000 cycles) without erasing/programming the entire Flash memory. Therefore, the total number of W/E cycles from a device perspective can exceed 20,000 cycles. However, even this number should not exceed 100,000 cycles.
(4) For de-rating information on operating above 105°C, refer to *Calculating Useful Lifetimes of Embedded Processors*.

Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle. For more details, see the "Flash: Minimum Programming Word Size" advisory in the *TMS320F2838x Real-Time MCUs Silicon Errata*.

7.10.5 RAM Specifications

Table 7-6. CPU1 RAM Parameters

RAM TYPE	SIZE	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH	NUMBER OF BUSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
GS RAM	128KB	2	2	1	16/32	4	0	No
LS RAM	32KB	2	2	1	16/32	2	0	No
M0	2KB	2	2	1	16/32	1	0	No
M1	2KB	2	2	1	16/32	1	0	No
CLA-to-CPU Message RAM	256B	2	2	1	16/32	2	0	No
CPU-to-CLA Message RAM	256B	2	2	1	16/32	2	0	No
CLA-to-DMA Message RAM	256B	2	2	1	16/32	2	0	No
DMA-to-CLA Message RAM	256B	2	2	1	16/32	2	0	No
CM-to-CPU Message RAM	4KB	2	2	1	16/32	4	0	No
CPU-to-CM Message RAM	4KB	2	2	1	16/32	4	0	No
CPU1-to-CPU2 Message RAM	4KB	2	2	1	16/32	4	0	No
CPU2-to-CPU1 Message RAM	4KB	2	2	1	16/32	4	0	No
DX RAM	8KB	2	2	1	16/32	1	0	No

(1) "Number of Buses Available" indicates how many masters (CLA, DMA, CPU) have access to this memory.

Table 7-7. CPU2 RAM Parameters

RAM TYPE	SIZE	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH	NUMBER OF BUSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
GS RAM	128KB	2	2	1	16/32	4	0	No
LS RAM	32KB	2	2	1	16/32	2	0	No
M0	2KB	2	2	1	16/32	1	0	No
M1	2KB	2	2	1	16/32	1	0	No
CLA-to-CPU Message RAM	256B	2	2	1	16/32	2	0	No
CPU-to-CLA Message RAM	256B	2	2	1	16/32	2	0	No
CLA-to-DMA Message RAM	256B	2	2	1	16/32	2	0	No
DMA-to-CLA Message RAM	256B	2	2	1	16/32	2	0	No
CM-to-CPU Message RAM	4KB	2	2	1	16/32	4	0	No
CPU-to-CM Message RAM	4KB	2	2	1	16/32	4	0	No
CPU1-to-CPU2 Message RAM	4KB	2	2	1	16/32	4	0	No
CPU2-to-CPU1 Message RAM	4KB	2	2	1	16/32	4	0	No
DX RAM	8KB	2	2	1	16/32	1	0	No

(1) “Number of Buses Available” indicates how many masters (CLA, DMA, CPU) have access to this memory.

7.10.6 ROM Specifications

Table 7-8. CPU1 ROM Parameters

ROM TYPE	SIZE	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH	NUMBER OF BUSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
Boot ROM	192KB	2	2	1	16/32	1	1	No
Secure ROM	64KB	2	2	1	16/32	1	1	No
CLA Data ROM	8KB	2	2	1	16/32	1	0	No

(1) “Number of Buses Available” indicates how many masters (CLA, DMA, CPU) have access to this memory.

Table 7-9. CPU2 ROM Parameters

ROM TYPE	SIZE	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	BUS WIDTH	NUMBER OF BUSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
Boot ROM	64KB	2	2	1	16/32	1	1	No
Secure ROM	64KB	2	2	1	16/32	1	1	No
CLA Data ROM	8KB	2	2	1	16/32	1	0	No

(1) “Number of Buses Available” indicates how many masters (CLA, DMA, CPU) have access to this memory.

7.10.7 Emulation/JTAG

The JTAG port has five dedicated pins: TRSTn, TMS, TDI, TDO, and TCK. The TRSTn signal should always be pulled down through a 2.2-kΩ pulldown resistor on the board. This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

See Figure 7-16 to see how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 7-17 shows how to connect to the 20-pin header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

The PD (Power Detect) terminal of the JTAG debug probe header should be connected to the board 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the JTAG debug probe). Header terminal RESETn is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header).

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected, 22-Ω resistors should be placed in series on each JTAG signal.

For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints for C28x in CCS.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

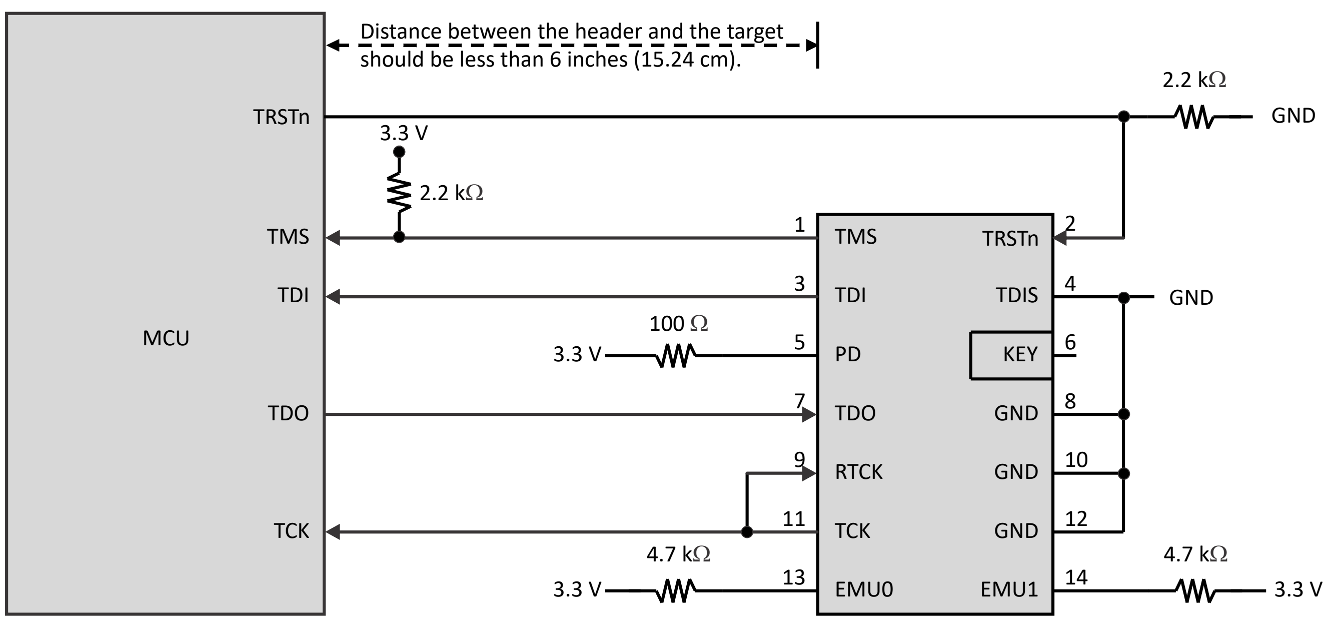


Figure 7-16. Connecting to the 14-Pin JTAG Header

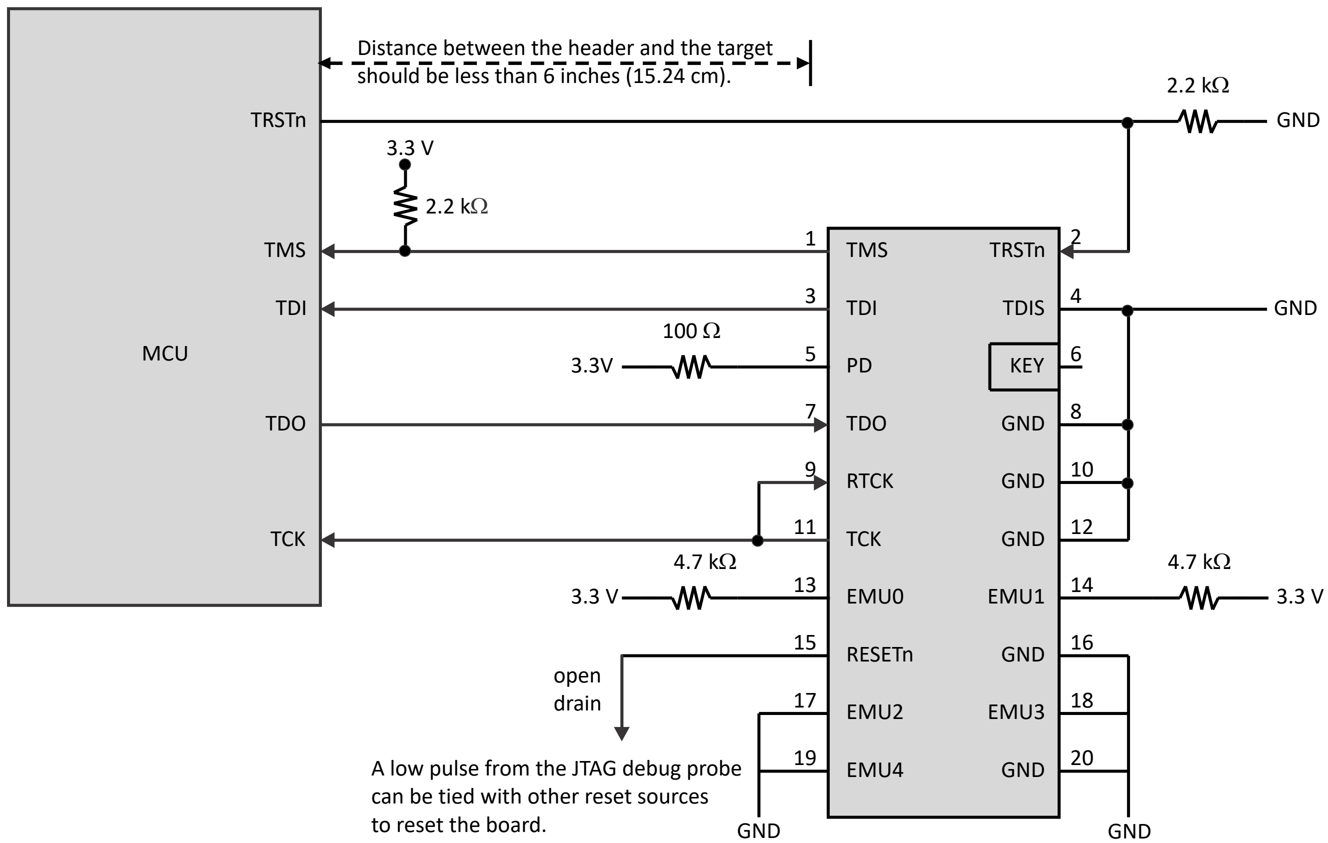


Figure 7-17. Connecting to the 20-Pin JTAG Header

7.10.7.1 JTAG Electrical Data and Timing

Section 7.10.7.1.1 lists the JTAG timing requirements. Section 7.10.7.1.2 lists the JTAG switching characteristics. Figure 7-18 shows the JTAG timing.

7.10.7.1.1 JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	13		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	13		
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	11		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	11		

7.10.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	30	ns

7.10.7.1.3 JTAG Timing

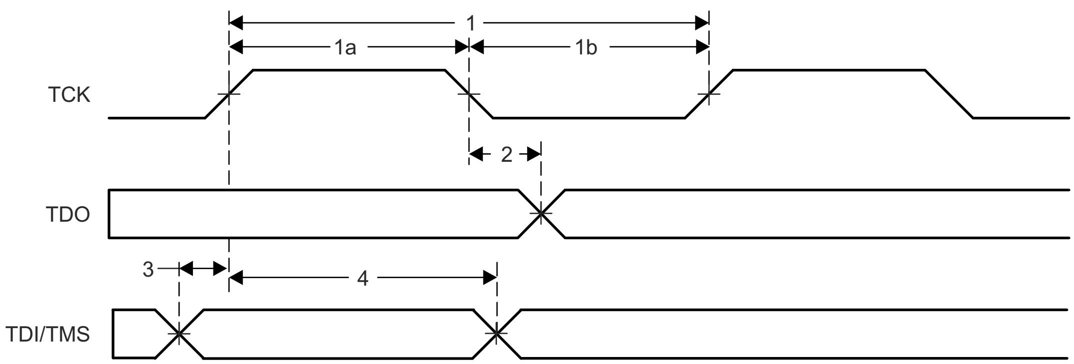


Figure 7-18. JTAG Timing

7.10.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADC(s), eCAP(s), ePWM(s), and external interrupts. For more details, see the X-BAR chapter in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

7.10.8.1 GPIO - Output Timing

Section 7.10.8.1.1 lists the general-purpose output switching characteristics. Figure 7-19 shows the general-purpose output timing.

7.10.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8[(1)]	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8[(1)]	ns
t_{fGPO}	Toggling frequency, GPIO pins			50	MHz

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

7.10.8.1.2 General-Purpose Output Timing

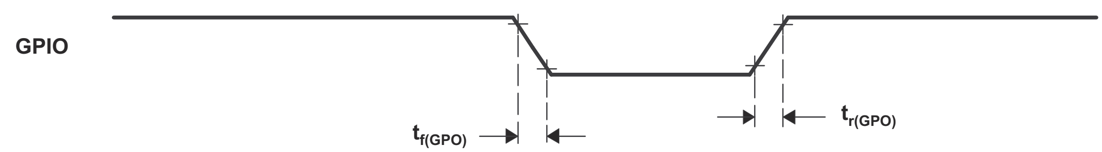


Figure 7-19. General-Purpose Output Timing

7.10.8.2 GPIO - Input Timing

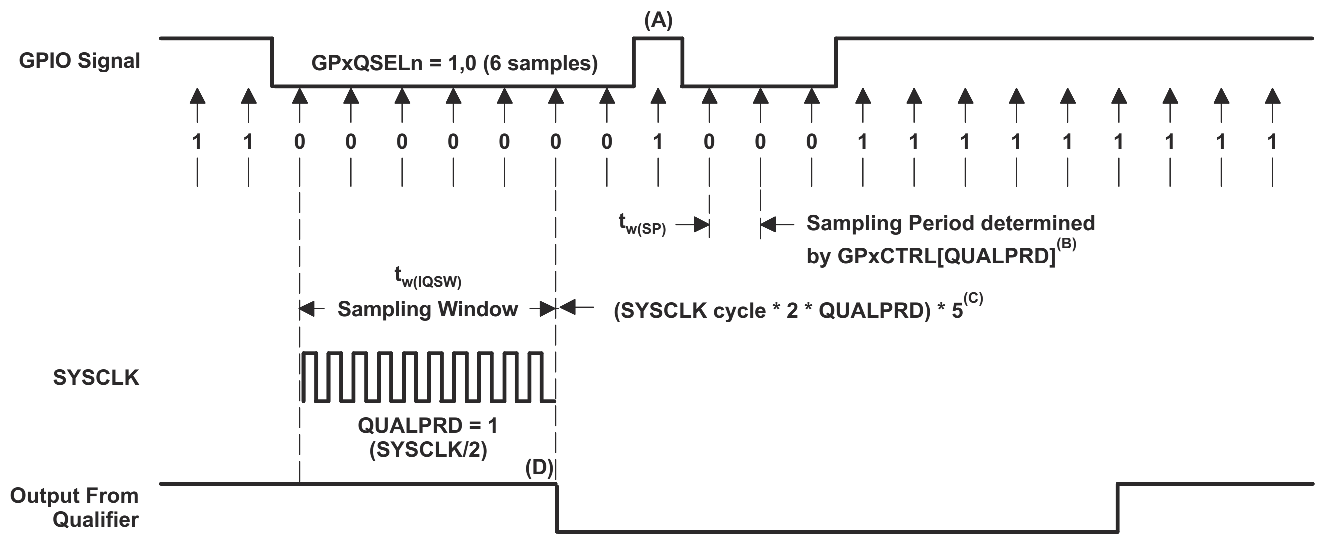
Section 7.10.8.2.1 lists the general-purpose input timing requirements. Figure 7-20 shows the sampling mode.

7.10.8.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

7.10.8.2.2 Sampling Mode



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of 8 GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 7-20. Sampling Mode

7.10.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

$$\text{Sampling frequency} = \text{SYSCLK}/(2 \times \text{QUALPRD}), \text{ if QUALPRD} \neq 0 \tag{2}$$

$$\text{Sampling frequency} = \text{SYSCLK, if QUALPRD} = 0 \tag{3}$$

$$\text{Sampling period} = \text{SYSCLK cycle} \times 2 \times \text{QUALPRD, if QUALPRD} \neq 0 \tag{4}$$

In Equation 2, Equation 3, and Equation 4, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

Figure 7-21 shows the general-purpose input timing.

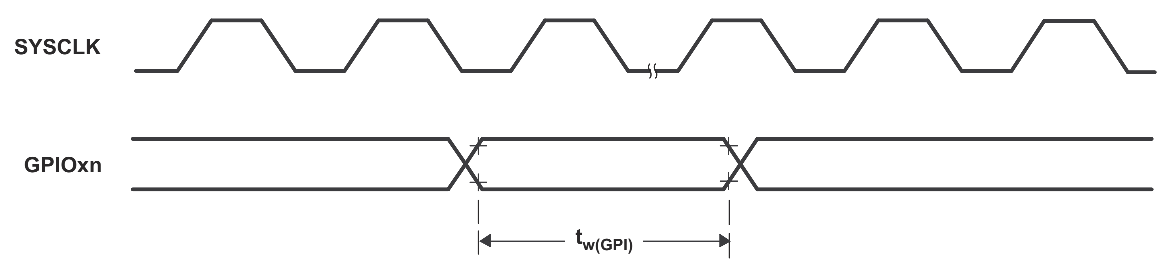


Figure 7-21. General-Purpose Input Timing

7.10.9 Interrupts

Figure 7-22 provides a high-level view of the interrupt architecture.

As shown in Figure 7-22, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, 16 ePIE block interrupts are grouped into 1 CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

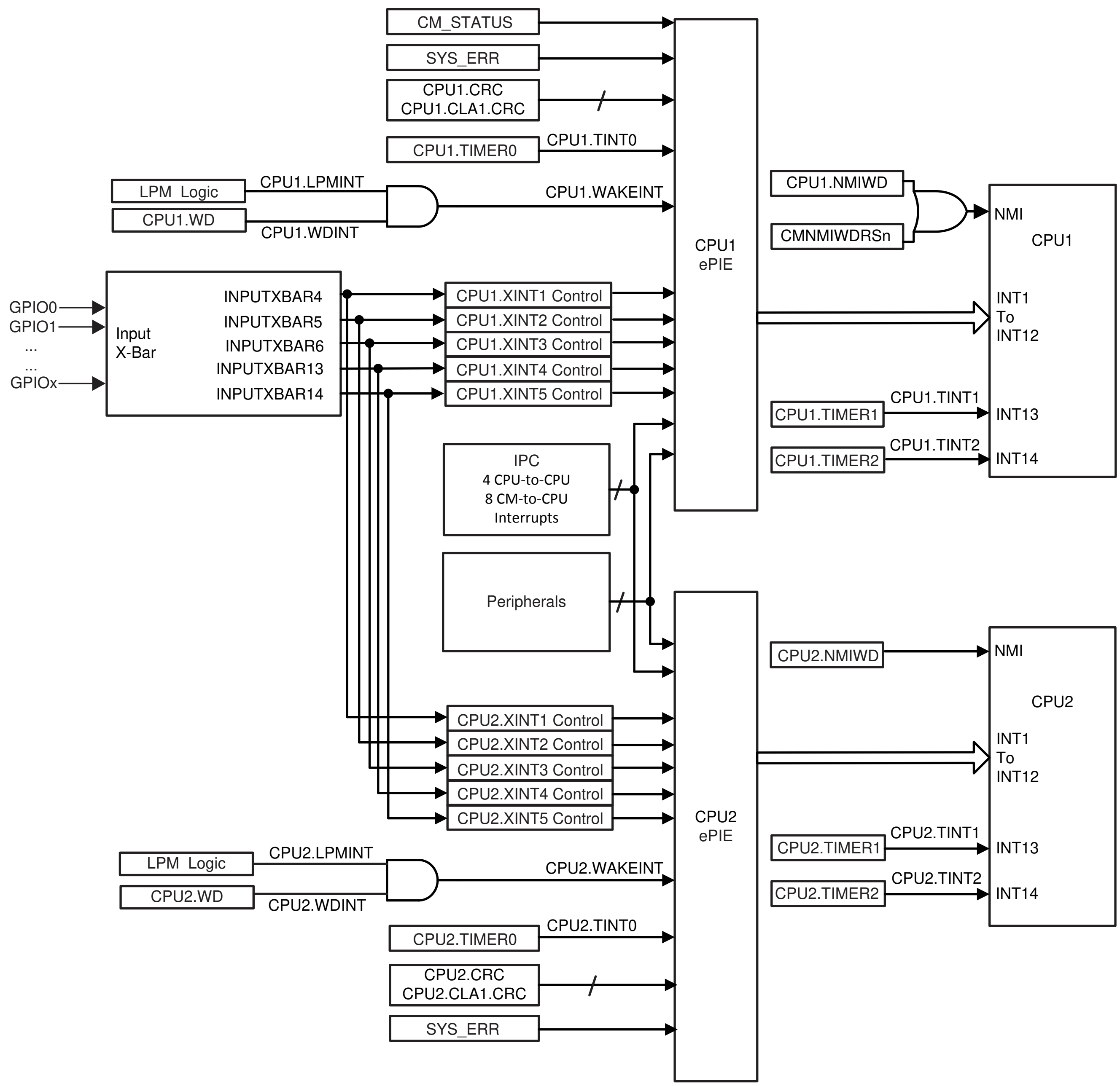


Figure 7-22. External and ePIE Interrupt Sources

7.10.9.1 External Interrupt (XINT) Electrical Data and Timing

Section 7.10.9.1.1 lists the external interrupt timing requirements. Section 7.10.9.1.2 lists the external interrupt switching characteristics. Figure 7-23 shows the external interrupt timing. For an explanation of the input qualifier parameters, see Section 7.10.8.2.1.

7.10.9.1.1 External Interrupt Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

7.10.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch(1)	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) This assumes that the ISR is in a single-cycle memory.

7.10.9.1.3 External Interrupt Timing

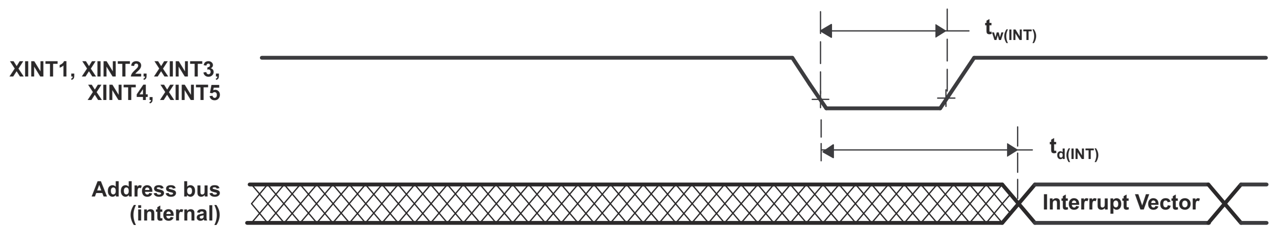


Figure 7-23. External Interrupt Timing

7.10.10 Low-Power Modes

This device has two clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low Power Modes section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

7.10.10.1 Clock-Gating Low-Power Modes

IDLE and STANDBY modes on this device are similar to those on other C28x devices. Table 7-10 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 7-10. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/CLOCK DOMAIN	CPU1 IDLE	CPU1 STANDBY	CPU2 IDLE	CPU2 STANDBY
CPU1.CLKIN	Active	Gated	N/A	N/A
CPU1.SYSCLK	Active	Gated	N/A	N/A
CPU1.CPUCLK	Gated	Gated	N/A	N/A
CPU2.CLKIN	N/A	N/A	Active	Gated
CPU2.SYSCLK	N/A	N/A	Active	Gated
CPU2.CPUCLK	N/A	N/A	Gated	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Gated if CPUSEL.PERx = CPU1	Active	Gated if CPUSEL.PERx = CPU2
CPU1.WDCLK	Active	Active	N/A	N/A
CPU2.WDCLK	N/A	N/A	Active	Active
AUXPLLCLK	Active	Active	Active	Active
PLL	Powered	Powered	Powered	Powered
INTOSC1	Powered	Powered	Powered	Powered
INTOSC2	Powered	Powered	Powered	Powered
Flash[(1)]	Powered	Powered	Powered	Powered
X1/X2 Crystal Oscillator	Powered	Powered	Powered	Powered

(1) Entering any of the low-power modes does not automatically power down the flash. The application should always power down the flash memory before entering a low-power mode.

7.10.10.2 Low-Power Mode Wakeup Timing

Section 7.10.10.2.1 lists the IDLE mode timing requirements, Section 7.10.10.2.2 lists the switching characteristics, and Figure 7-24 shows the timing diagram for IDLE mode. For an explanation of the input qualifier parameters, see Section 7.10.8.2.1.

7.10.10.2.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

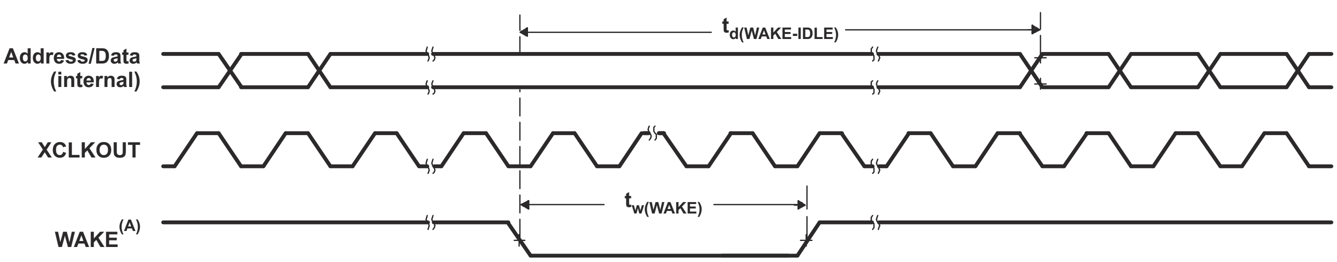
7.10.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume(1)	Wakeup from Flash (Flash module in active state)	Without input qualifier		$40t_{c(SYSCLK)}$	cycles
			With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles
		Wakeup from Flash (Flash module in sleep state)	Without input qualifier		$6700t_{c(SYSCLK)}$ (2)	cycles
			With input qualifier		$6700t_{c(SYSCLK)}$ (2) $+ t_{w(WAKE)}$	cycles
		Wakeup from RAM	Without input qualifier		$25t_{c(SYSCLK)}$	cycles
			With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

7.10.10.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 7-24. IDLE Entry and Exit Timing Diagram

Section 7.10.10.2.4 lists the STANDBY mode timing requirements, Section 7.10.10.2.5 lists the switching characteristics, and Figure 7-25 shows the timing diagram for STANDBY mode.

7.10.10.2.4 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | (2 + QUALSTDBY)$t_{c(OSCCLK)}$ (1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

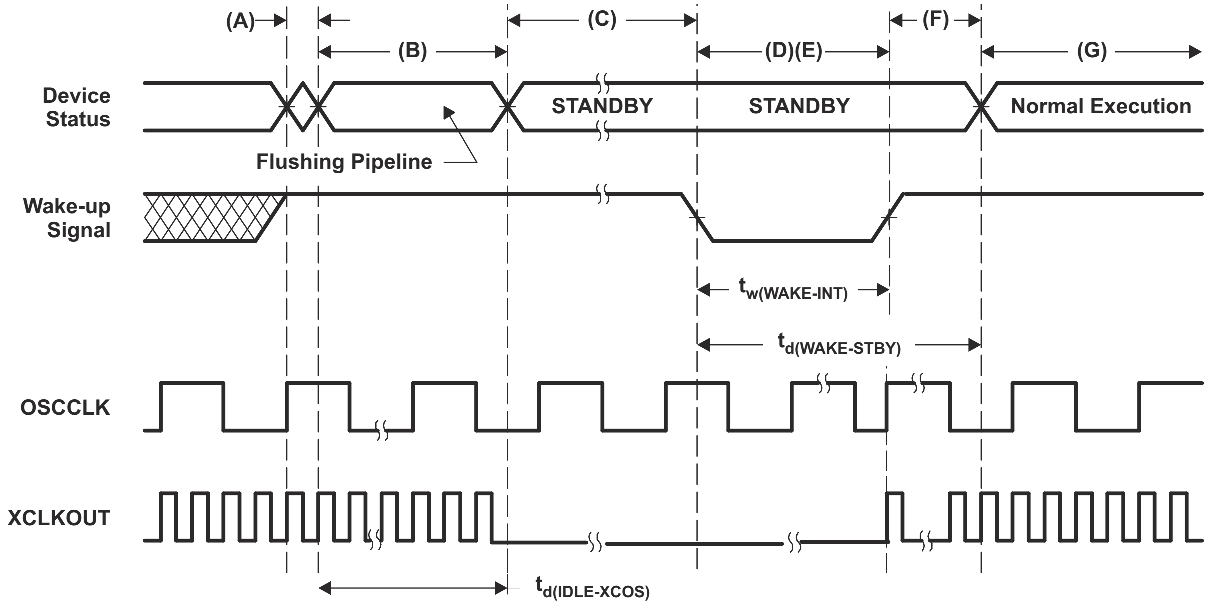
7.10.10.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)	Wakeup from flash (Flash module in active state)		$175t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from flash (Flash module in sleep state)		$6700t_{c(SYSCLK)}$ (2) $+ t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from RAM		$3t_{c(OSC)} + 15t_{c(SYSCLK)} + t_{w(WAKE-INT)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. This value can be realized when SYSCLK is 200 MHz, RWAIT is 3, and FPAC1[PSLEEP] is 0x860.

7.10.10.2.6 STANDBY Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 7-25. STANDBY Entry and Exit Timing Diagram

7.10.11 External Memory Interface (EMIF)

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

7.10.11.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects ($\overline{\text{EMIF\_CS[4:2]}}$). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable time-out
- Select strobe option

7.10.11.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select ($\overline{\text{EMIF\_CS[0]}}$).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in C2000Ware for C2000 MCUs and the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with 8-, 9-, 10-, and 11-column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. The EMIF module does not support mobile SDRAM devices.

On this device, the EMIF does not support burst access for SDRAM configurations. This means every access to an external SDRAM device will have CAS latency.

7.10.11.3 EMIF Electrical Data and Timing

7.10.11.3.1 Asynchronous RAM

7.10.11.3.1.1 EMIF Asynchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
Reads and Writes					
	E	EMIF clock period	$t_{c(SYSCLK)}$		ns
2	$t_{w(EM\_WAIT)}$	Pulse duration, EMxWAIT assertion and deassertion	2E(1)		ns
Reads					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMxD[y:0] valid before $\overline{\text{EMxOE}}$ high	15		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMxD[y:0] valid after $\overline{\text{EMxOE}}$ high	0		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20(1)		ns
Writes					
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20(1)		ns

(1) E = EMxCLK period in ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. Figure 7-27 and Figure 7-29 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

7.10.11.3.1.2 EMIF Asynchronous Memory Switching Characteristics

NO.	PARAMETER(1) (2) (3)		MIN	MAX	UNIT
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E–3	(TA)*E+2	ns
Reads					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E–3	(RS+RST+RH)*E+2	ns
		EMIF read cycle time (EW = 1)(4)	(RS+RST+RH+ (MEWC*16))*E–3	(RS+RST+RH+ (MEWC*16))*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{\text{EMxCS}}$[y:2] low to $\overline{\text{EMxOE}}$ low (SS = 0)	(RS)*E–3	(RS)*E+2	ns
		Output setup time, $\overline{\text{EMxCS}}$[y:2] low to $\overline{\text{EMxOE}}$ low (SS = 1)	–3	2	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{\text{EMxOE}}$ high to $\overline{\text{EMxCS}}$[y:2] high (SS = 0)	(RH)*E–3	(RH)*E	ns
		Output hold time, $\overline{\text{EMxOE}}$ high to $\overline{\text{EMxCS}}$[y:2] high (SS = 1)	–3	0	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{\text{EMxOE}}$ low	(RS)*E–3	(RS)*E+2	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{\text{EMxOE}}$ high to EMxBA[y:0] invalid	(RH)*E–3	(RH)*E	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EMxA[y:0] valid to $\overline{\text{EMxOE}}$ low	(RS)*E–3	(RS)*E+2	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{\text{EMxOE}}$ high to EMxA[y:0] invalid	(RH)*E–3	(RH)*E	ns
10	$t_{w(EMOEL)}$	$\overline{\text{EMxOE}}$ active low width (EW = 0)	(RST)*E–1	(RST)*E+1	ns
		$\overline{\text{EMxOE}}$ active low width (EW = 1)(4)	(RST+(MEWC*16))*E–1	(RST+(MEWC*16))*E+1	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMxWAIT deasserted to $\overline{\text{EMxOE}}$ high	4*E+10	5*E+15	ns
29	$t_{su(EMDQMV-EMOEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{\text{EMxOE}}$ low	(RS)*E–3	(RS)*E+2	ns
30	$t_{h(EMOEH-EMDQMIV)}$	Output hold time, $\overline{\text{EMxOE}}$ high to EMxDQM[y:0] invalid	(RH)*E–3	(RH)*E	ns
Writes					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E–3	(WS+WST+WH)*E+2	ns
		EMIF write cycle time (EW = 1)(4)	(WS+WST+WH+ (MEWC*16))*E–3	(WS+WST+WH+ (MEWC*16))*E+2	ns

7.10.11.3.1.2 EMIF Asynchronous Memory Switching Characteristics (continued)

NO.	PARAMETER(1) (2) (3)		MIN	MAX	UNIT
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{\text{EMxCS[y:2]}}$ low to $\overline{\text{EMxWE}}$ low (SS = 0)	(WS)*E–3	(WS)*E+2	ns
		Output setup time, $\overline{\text{EMxCS[y:2]}}$ low to $\overline{\text{EMxWE}}$ low (SS = 1)	–3	2	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{\text{EMxWE}}$ high to $\overline{\text{EMxCS[y:2]}}$ high (SS = 0)	(WH)*E–3	(WH)*E	ns
		Output hold time, $\overline{\text{EMxWE}}$ high to $\overline{\text{EMxCS[y:2]}}$ high (SS = 1)	–3	0	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{\text{EMxWE}}$ high to EMxDQM[y:0] invalid	(WH)*E–3	(WH)*E	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{\text{EMxWE}}$ high to EMxBA[y:0] invalid	(WH)*E–3	(WH)*E	ns
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMxA[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{\text{EMxWE}}$ high to EMxA[y:0] invalid	(WH)*E–3	(WH)*E	ns
24	$t_{w(EMWEL)}$	$\overline{\text{EMxWE}}$ active low width (EW = 0)	(WST)*E–1	(WST)*E+1	ns
		$\overline{\text{EMxWE}}$ active low width (EW = 1)(4)	(WST+(MEWC*16))*E–1	(WST+(MEWC*16))*E+1	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMxWAIT deasserted to $\overline{\text{EMxWE}}$ high	4*E+10	5*E+15	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMxD[y:0] valid to $\overline{\text{EMxWE}}$ low	(WS)*E–3	(WS)*E+2	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{\text{EMxWE}}$ high to EMxD[y:0] invalid	(WH)*E–3	(WH)*E	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–4], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual* for more information.
(2) E = EMxCLK period in ns.
(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256–1]. The maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual* for more information.
(4) Maximum wait timeout condition.

7.10.11.3.1.3 EMIF Asynchronous Memory Timing Diagrams

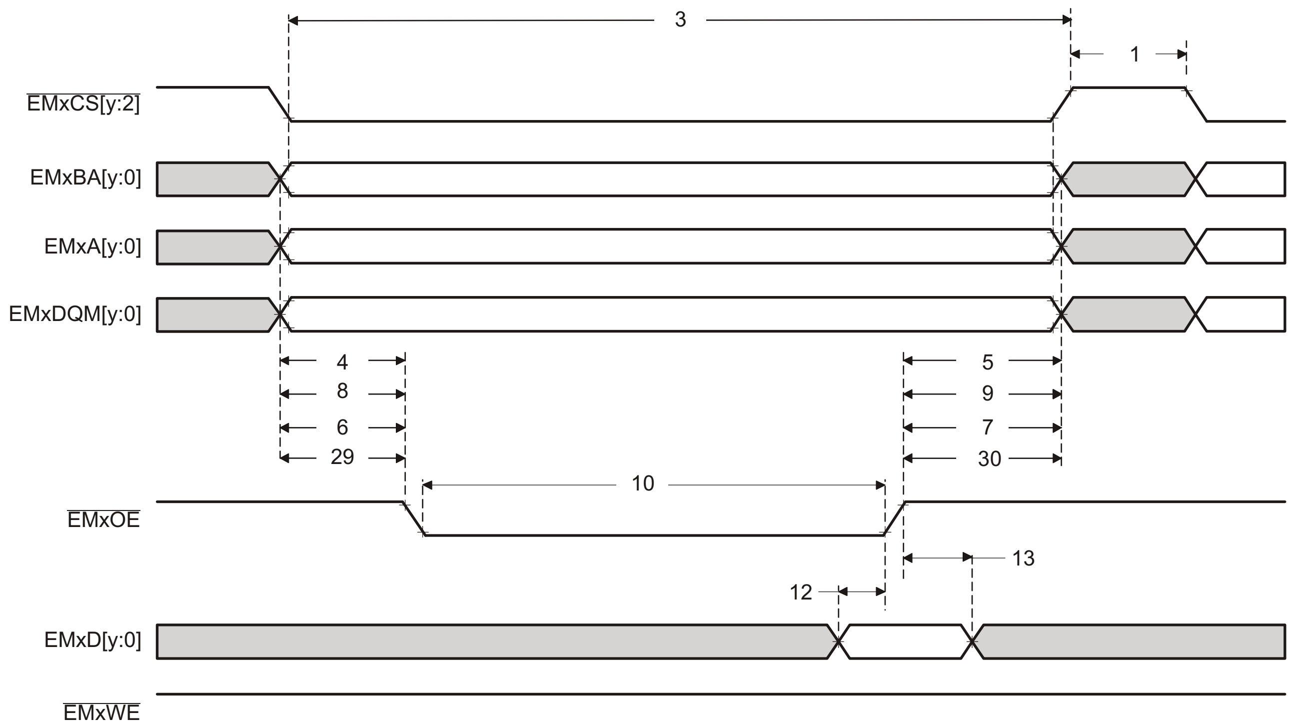


Figure 7-26. Asynchronous Memory Read Timing

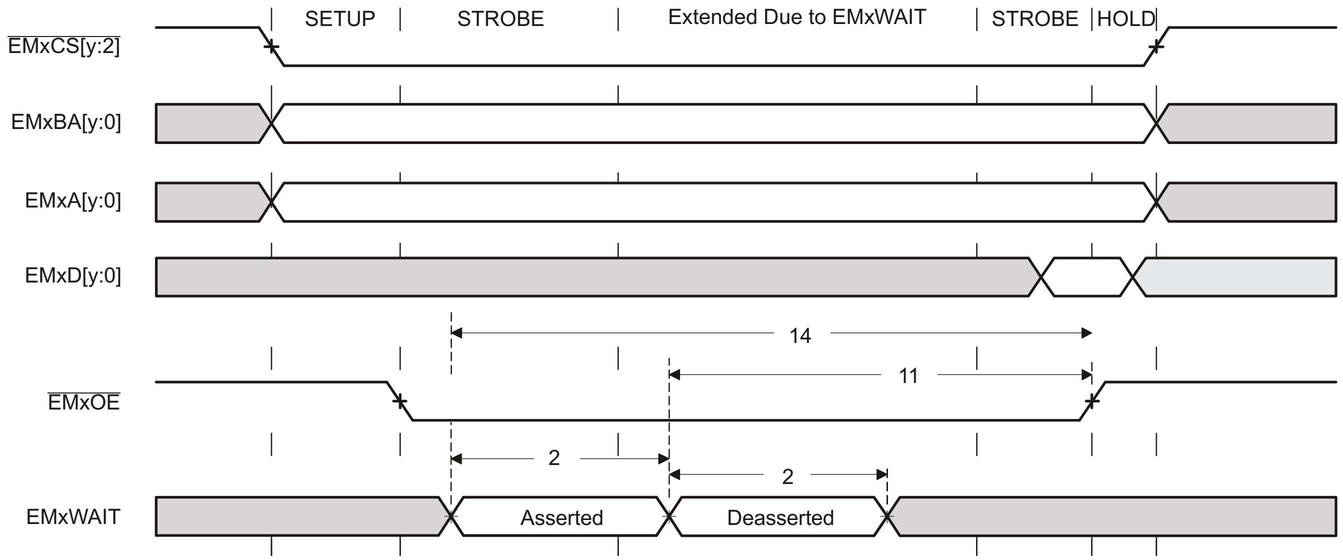


Figure 7-27. EMxWAIT Read Timing Requirements

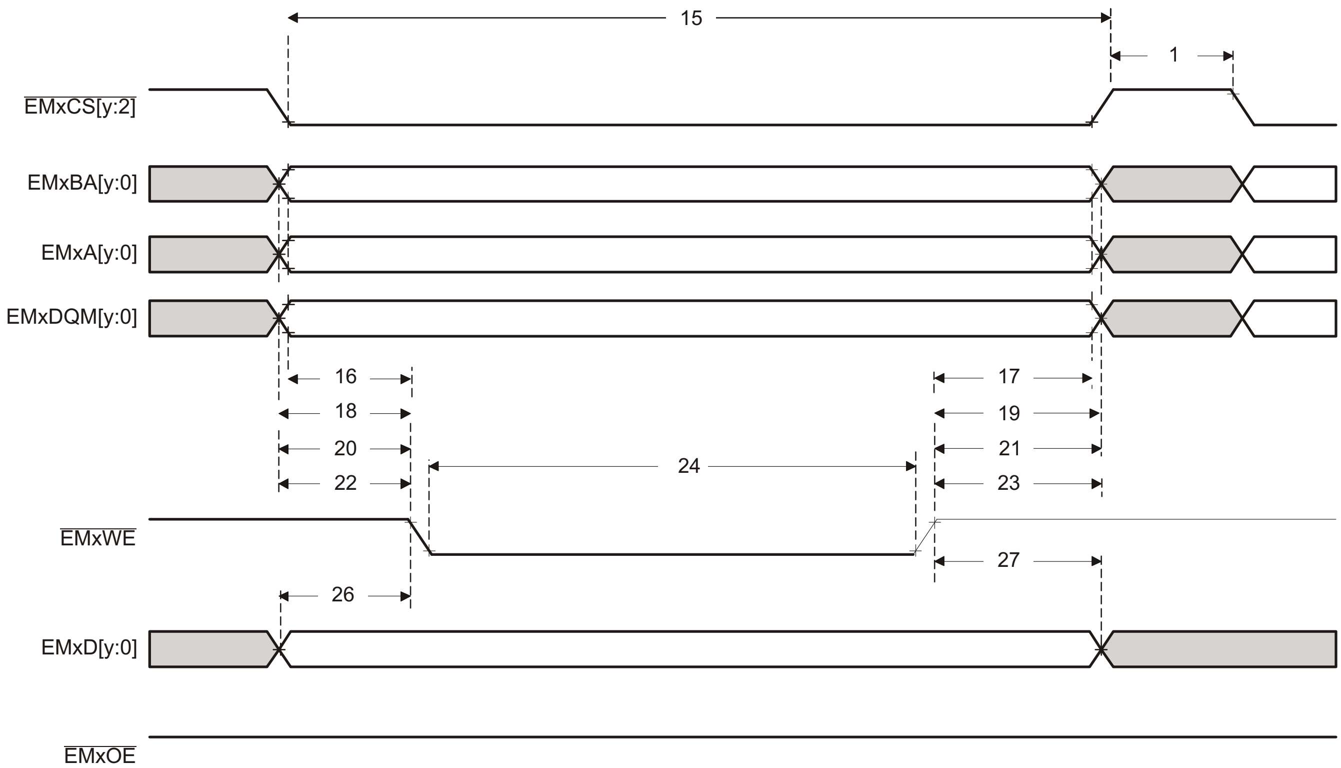


Figure 7-28. Asynchronous Memory Write Timing

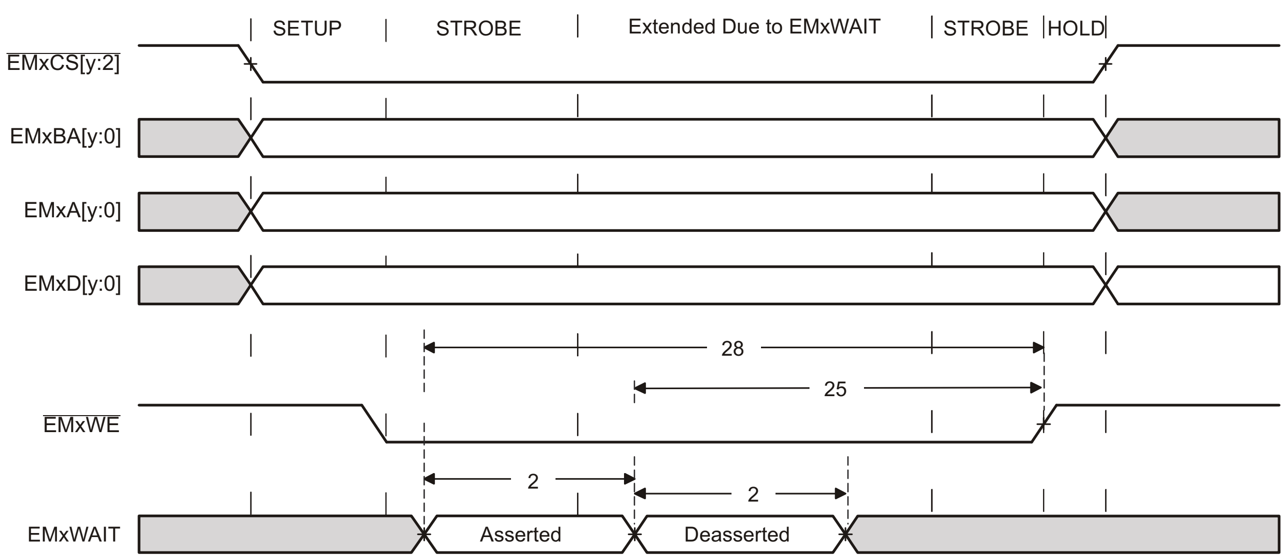


Figure 7-29. EMxWAIT Write Timing Requirements

7.10.11.3.2 Synchronous RAM

Section 7.10.11.3.2.1 lists the EMIF synchronous memory timing requirements. Section 7.10.11.3.2.2 lists the EMIF synchronous memory switching characteristics. Figure 7-30 and Figure 7-31 show the synchronous memory timing diagrams.

7.10.11.3.2.1 EMIF Synchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EMIFDV\text{-}EM\_CLKH)}$	Input setup time, read data valid on EMxD[y:0] before EMxCLK rising	2		ns
20	$t_{h(CLKH\text{-}DIV)}$	Input hold time, read data valid on EMxD[y:0] after EMxCLK rising	1.5		ns

7.10.11.3.2.2 EMIF Synchronous Memory Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK	10		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMxCLK high or low	3		ns
3	$t_{d(CLKH\text{-}CSV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ valid		8	ns
4	$t_{oh(CLKH\text{-}CSIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ invalid	1		ns
5	$t_{d(CLKH\text{-}DQMV)}$	Delay time, EMxCLK rising to EMxDQM[y:0] valid		8	ns
6	$t_{oh(CLKH\text{-}DQMIV)}$	Output hold time, EMxCLK rising to EMxDQM[y:0] invalid	1		ns
7	$t_{d(CLKH\text{-}AV)}$	Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid		8	ns
8	$t_{oh(CLKH\text{-}AIV)}$	Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid	1		ns
9	$t_{d(CLKH\text{-}DV)}$	Delay time, EMxCLK rising to EMxD[y:0] valid		8	ns
10	$t_{oh(CLKH\text{-}DIV)}$	Output hold time, EMxCLK rising to EMxD[y:0] invalid	1		ns
11	$t_{d(CLKH\text{-}RASV)}$	Delay time, EMxCLK rising to EMxRAS valid		8	ns
12	$t_{oh(CLKH\text{-}RASIV)}$	Output hold time, EMxCLK rising to EMxRAS invalid	1		ns
13	$t_{d(CLKH\text{-}CASV)}$	Delay time, EMxCLK rising to EMxCAS valid		8	ns
14	$t_{oh(CLKH\text{-}CASIV)}$	Output hold time, EMxCLK rising to EMxCAS invalid	1		ns
15	$t_{d(CLKH\text{-}WEV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxWE}}$ valid		8	ns
16	$t_{oh(CLKH\text{-}WEIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxWE}}$ invalid	1		ns
17	$t_{d(CLKH\text{-}DHZ)}$	Delay time, EMxCLK rising to EMxD[y:0] tri-stated		8	ns
18	$t_{oh(CLKH\text{-}DLZ)}$	Output hold time, EMxCLK rising to EMxD[y:0] driving	1		ns

7.10.11.3.2.3 EMIF Synchronous Memory Timing Diagrams

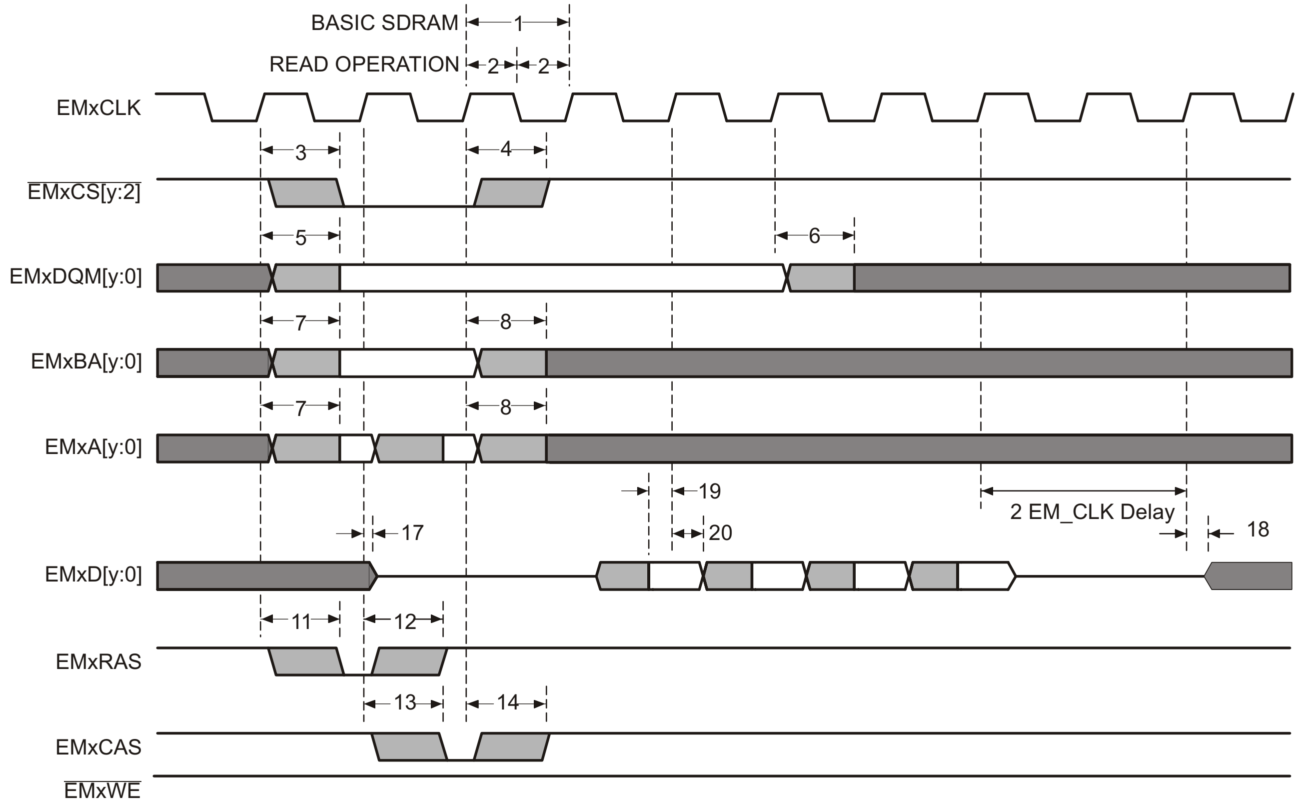


Figure 7-30. Basic SDRAM Read Operation

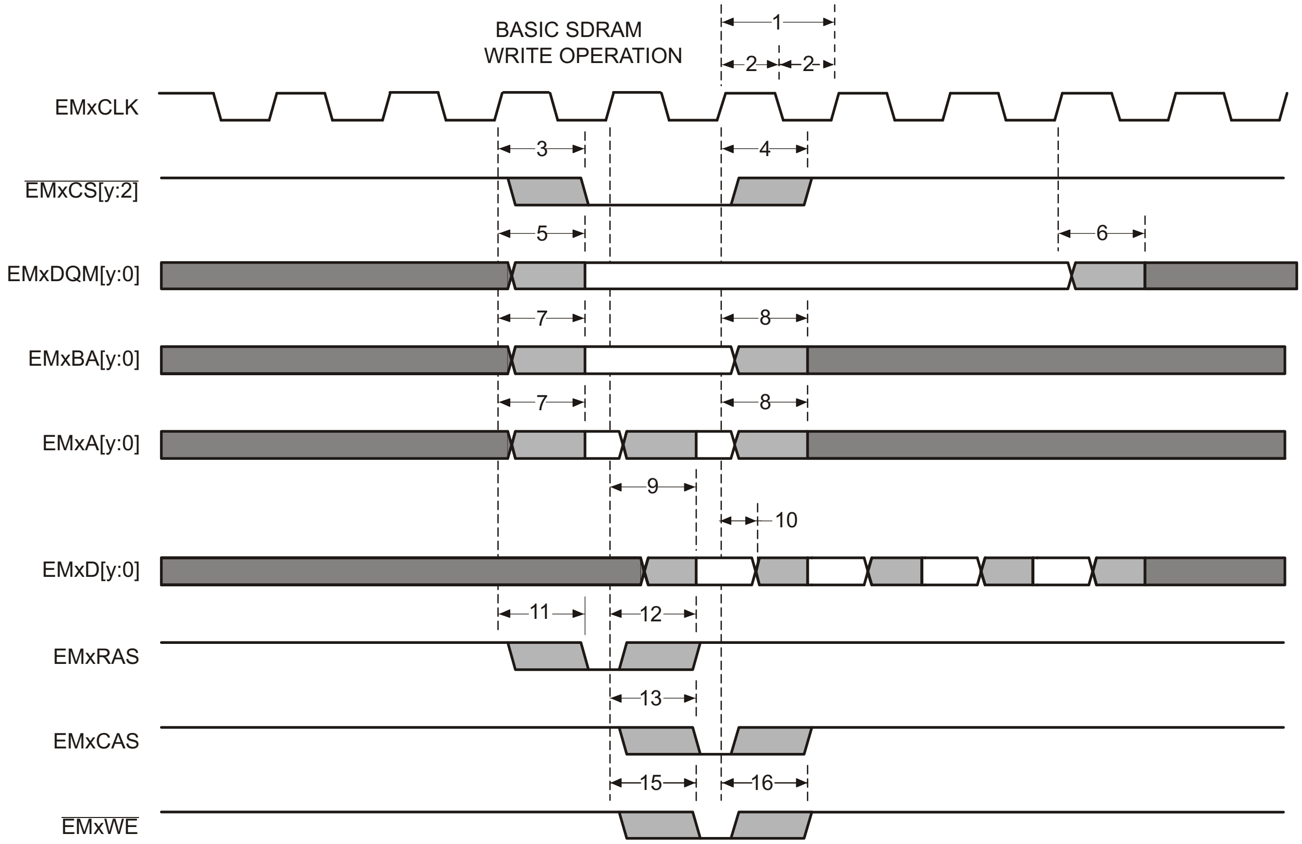


Figure 7-31. Basic SDRAM Write Operation

7.11 C28x Analog Peripherals

7.11.1 Analog Subsystem

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Buffered Digital-to-Analog Converter (DAC), and Comparator Subsystem (CMPSS).

The analog subsystem has the following features:

- Flexible voltage references
  - The ADCs are referenced to VREFHIx and VREFLOx pins
    - VREFHIx pin voltage must be driven in externally
- The buffered DACs are referenced to VREFHIx and VSSA
  - Alternately, these DACs can be referenced to the VDAC pin and VSSA
- The comparator DACs are referenced to VDDA and VSSA
  - Alternately, these DACs can be referenced to the VDAC pin and VSSA
- Flexible pin usage
  - Buffered DAC and comparator subsystem functions multiplexed with ADC inputs
- Internal connection to VREFLO on all ADCs for offset self-calibration

Figure 7-32 shows the Analog Subsystem Block Diagram for the 337-ball ZWT package.

Figure 7-33 shows the Analog Subsystem Block Diagram for the 176-pin PTP package.

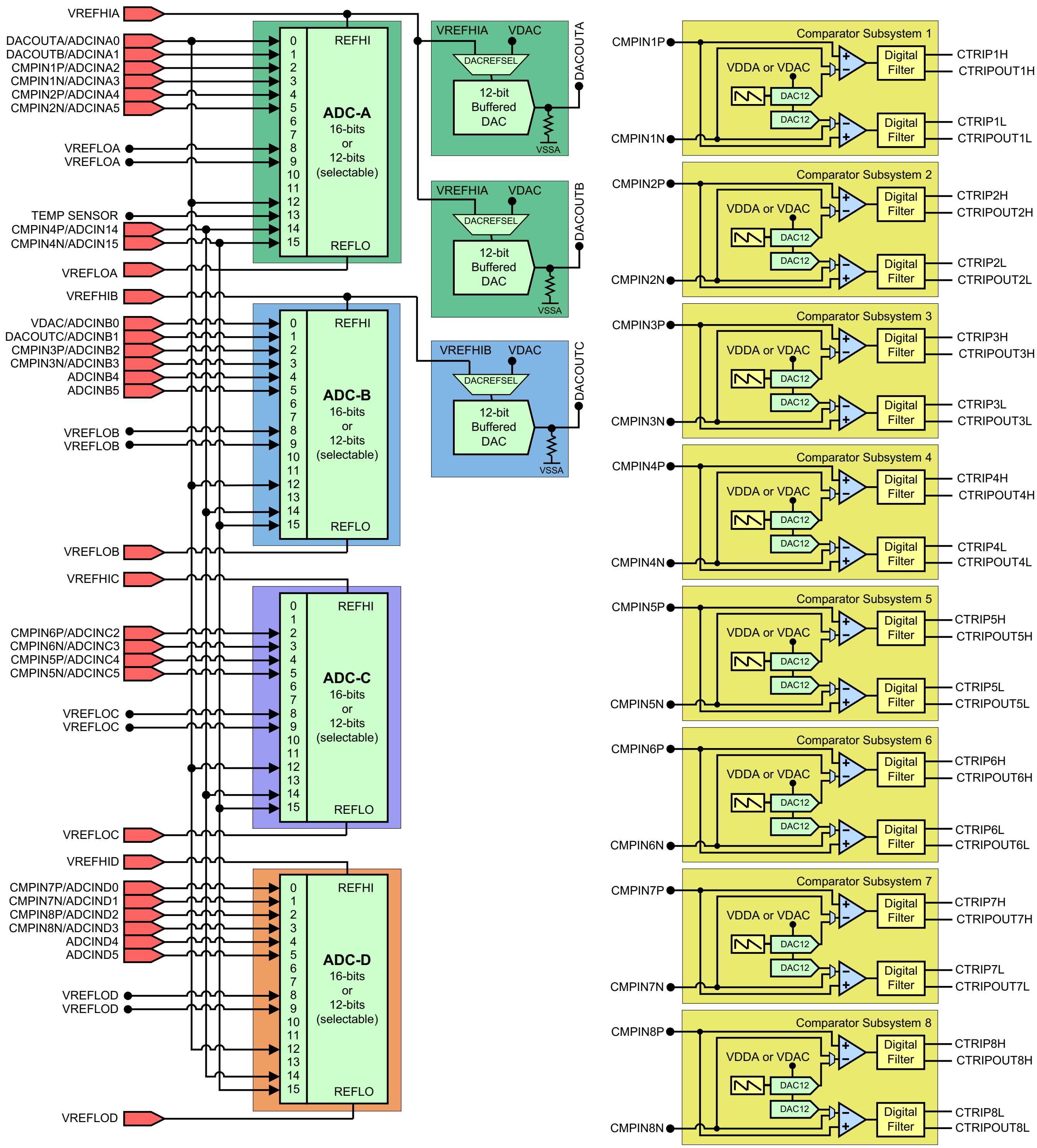


Figure 7-32. Analog Subsystem Block Diagram (337-Ball ZWT)

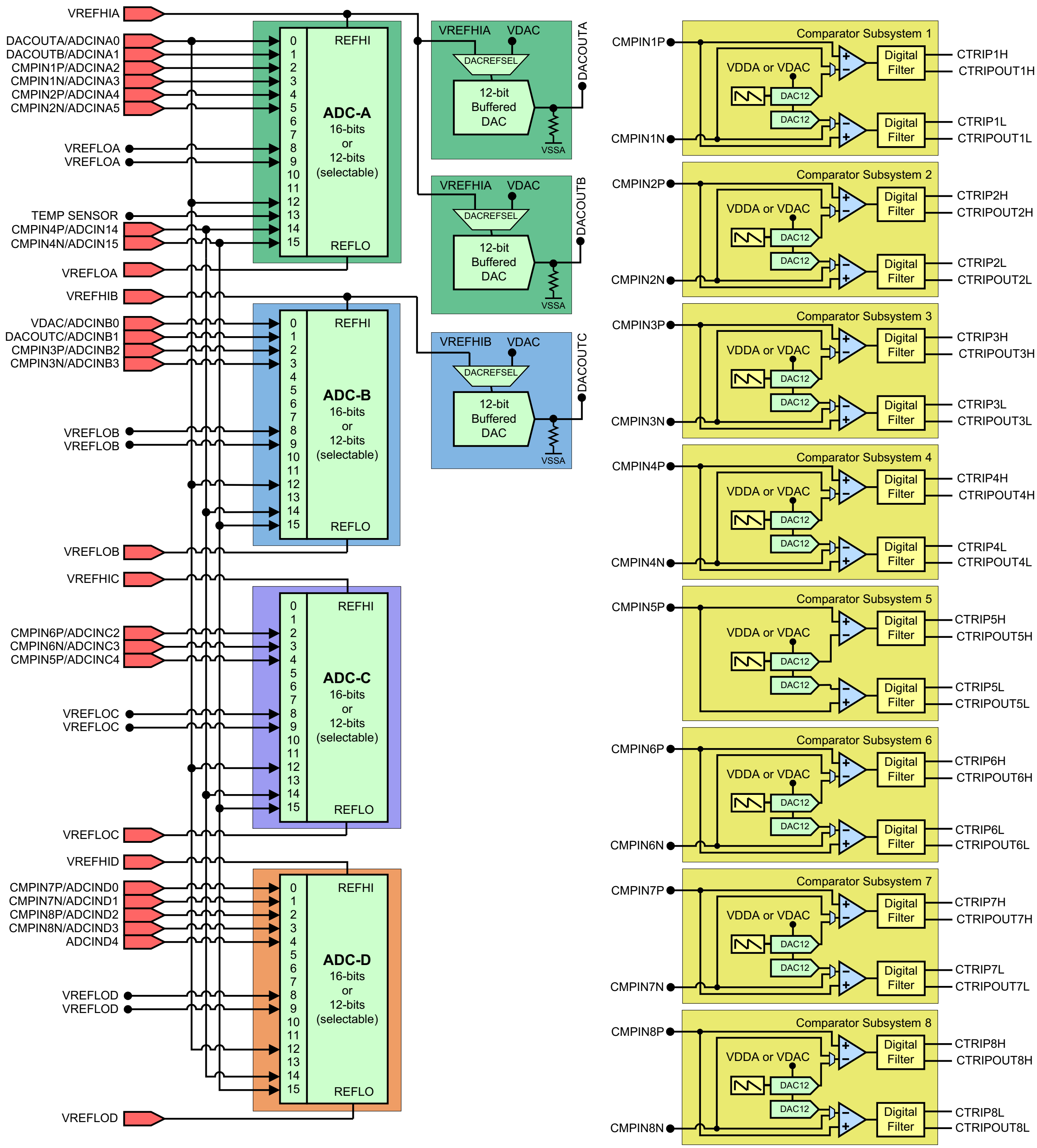


Figure 7-33. Analog Subsystem Block Diagram (176-Pin PTP)

7.11.2 Analog-to-Digital Converter (ADC)

The ADC module is a successive approximation (SAR) style ADC with a selectable resolution of either 16 bits or 12 bits. The ADC is composed of a core and a wrapper. The core is composed of the analog circuits, which include the channel select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The wrapper is composed of the digital circuits that configure and control the ADC. These circuits include the logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC) based (see the SOC Principle of Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*).

Each ADC has the following features:

- Selectable resolution of 12 bits or 16 bits
- Ratiometric external reference set by VREFHI and VREFLO pins
- Differential signal conversions (16-bit mode only)
- Single-ended signal conversions
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - S/W: software immediate start
  - All ePWMs: ADCSOC A or B
  - GPIO Input X-BAR INPUT5
  - CPU Timer 0, CPU Timer 1, CPU Timer 2 (from each C28x core present)
  - ADCINT1, ADCINT2
- Four flexible PIE interrupts
- Configurable interrupt placement
- Burst mode
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

Note

Not every channel may be pinned out from all ADCs. See Section 6 to determine which channels are available.

Figure 7-34 shows the ADC module block diagram.

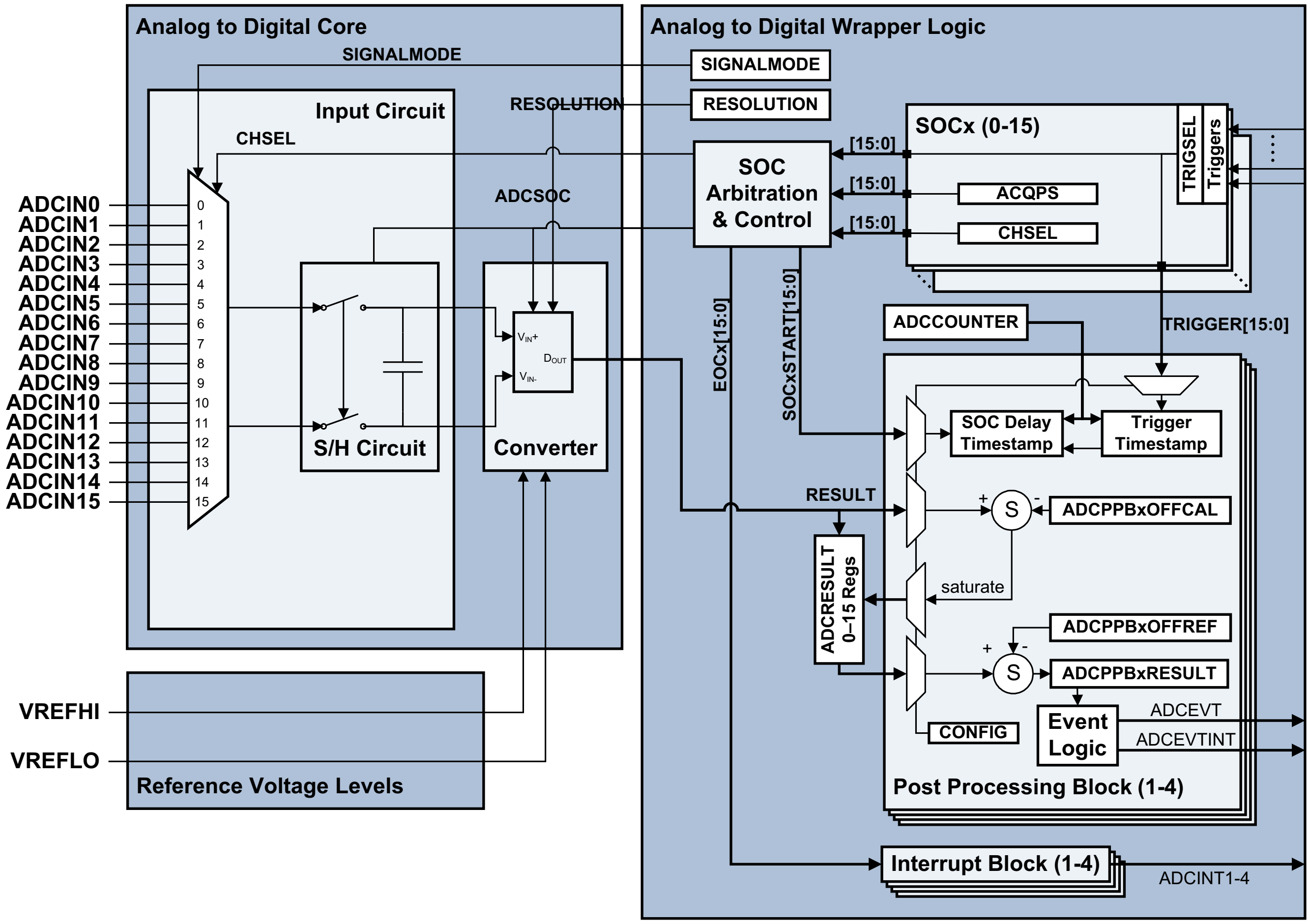


Figure 7-34. ADC Module Block Diagram

7.11.2.1 Result Register Mapping

The ADC results and the ADC PPB results are duplicated for each memory bus controller in the system. Bus controllers include all C28x CPUs, C28x DMAs, and CLAs present on the specific part family and part number. For each bus controller, no access configuration is needed to allow read access to the result registers and no contention occurs in cases where multiple bus controllers try to read the ADC results simultaneously.

7.11.2.2 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 7-11 summarizes the basic ADC options and their level of configurability.

Table 7-11. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	Per module(1)
Resolution	Per module(1)
Signal mode	Per module
Reference voltage source	Not configurable (external reference only)
Trigger source	Per SOC(1)
Converted channel	Per SOC
Acquisition window duration	Per SOC(1)
EOC location	Per module
Burst Mode	Per module(1)

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

7.11.2.2.1 Signal Mode

The ADC supports two signal modes: single-ended and differential. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. In differential signaling mode, the input voltage to the converter is sampled through a pair of input pins, one of which is the positive input (ADCINxP) and the other is the negative input (ADCINxN). The actual input voltage is the difference between the two (ADCINxP – ADCINxN). Figure 7-35 shows the differential signaling mode. Figure 7-36 shows the single-ended signaling mode.

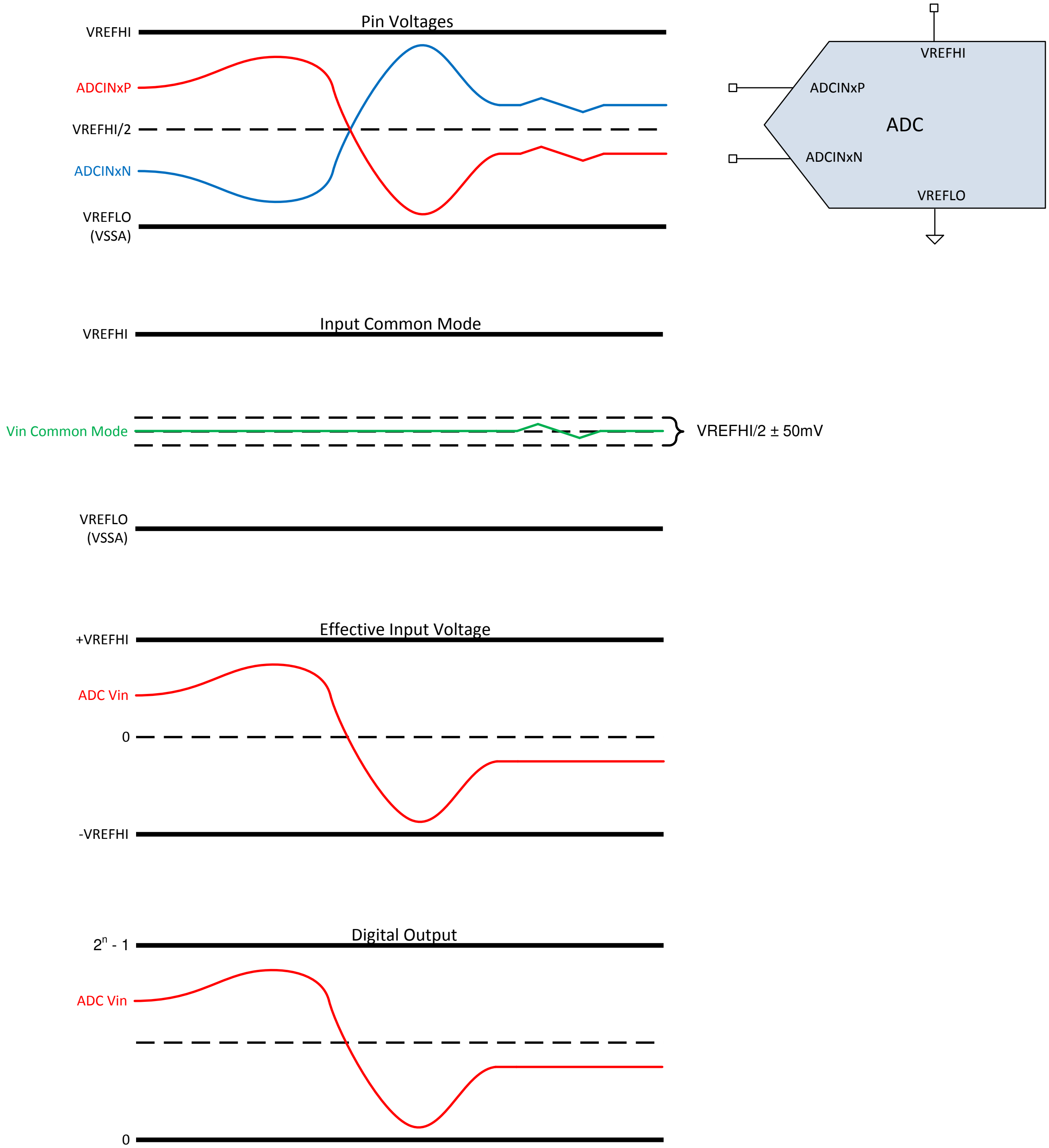


Figure 7-35. Differential Signaling Mode

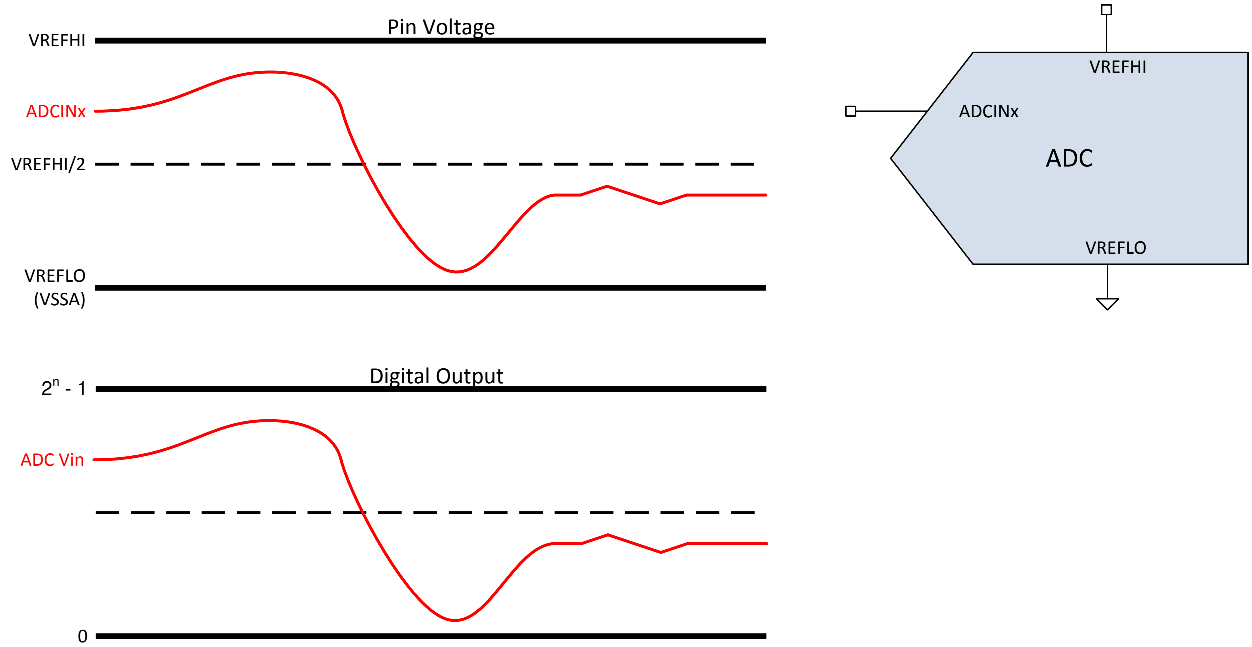


Figure 7-36. Single-ended Signaling Mode

7.11.2.3 ADC Electrical Data and Timing

Section 7.11.2.3.1 lists the ADC operating conditions for the 16-bit differential mode. Section 7.11.2.3.2 lists the ADC characteristics for the 16-bit differential mode. Section 7.11.2.3.3 lists the ADC operating conditions for the 16-bit single-ended mode. Section 7.11.2.3.4 lists the ADC characteristics for the 16-bit single-ended mode. Section 7.11.2.3.5 lists the ADC operating conditions for the 12-bit single-ended mode. Section 7.11.2.3.6 lists the ADC characteristics for the 12-bit single-ended mode. Section 7.11.2.3.7 lists the ADCEXTSOC timing requirements.

7.11.2.3.1 ADC Operating Conditions (16-bit Differential)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		50	MHz
Sample rate	200-MHz SYSCLK			1.1	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	320			ns
VREFHI		2.4	2.5 or 3.0	VDDA	V
VREFLO		VSSA	VSSA	VSSA	V
Conversion range		VREFLO		VREFHI	V
ADC input signal common mode voltage(2) (3)		VREFCM – 50	VREFCM	VREFCM + 50	mV

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) VREFCM = (VREFHI + VREFLO)/2
(3) The VREFCM requirements will not be met if the negative ADC input pin is connected to VSSA or VREFLO.

7.11.2.3.1.1 ADC Operating Conditions (16-bit Differential) Notes

Note

The ADC inputs should be kept below VDDA + 0.3 V during operation. If an ADC input exceeds this level, the VREF internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same VREF.

Note

The VREFHI pin must be kept below VDDA for the ADC and DAC to meet specified performance parameters. The VREFHI pin must be kept below VDDA + 0.3 V for functional operation. If the VREFHI pin exceeds VDDA + 0.3 V, a blocking circuit may activate, causing the interval value of VREFHI to float to 0 V internally, giving improper ADC conversion or DAC output.

7.11.2.3.2 ADC Characteristics (16-bit Differential)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles		29.6		31	ADCCLKs
Power Up Time				500	µs
VREFHI input current [(1)]			190		µA
External Reference Capacitor Value[(2)]		22			µF
DC Characteristics					
Gain Error		–64	±9	64	LSB
Offset Error		–6	±4	6	LSB
Channel-to-Channel Gain Error			±6		LSB
Channel-to-Channel Offset Error			±3		LSB
ADC-to-ADC Gain Error	Identical VREFHI and VREFLO for all ADCs		±6		LSB
ADC-to-ADC Offset Error	Identical VREFHI and VREFLO for all ADCs		±3		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–3.5	±1.0	3.5	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–2		2	LSBs
	VREFHI = 2.5 V, asynchronous ADCs		Not Supported		
AC Characteristics					
SNR[(3)]	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1		90.2		dB
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from INTOSC		90.2		dB
THD[(3)]	VREFHI = 2.5 V, fin = 10 kHz		–105		dB
SFDR[(3)]	VREFHI = 2.5 V, fin = 10 kHz		106		dB
SINAD[(3)]	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1		90.0		dB
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from INTOSC		90.0		
ENOB[(3)]	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1, Single ADC		14.65		bits
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1, synchronous ADCs		14.65		
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		
PSRR	VDD = 1.2-V DC + 200mV DC up to Sine at 1 kHz		77		dB
	VDD = 1.2-V DC + 200 mV Sine at 800 kHz		74		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 800 kHz		77		
	VDDA = 3.3-V DC + 200 mV Sine at 800 kHz		74		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk

7.11.2.3.3 ADC Operating Conditions (16-bit Single-Ended)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		50	MHz
Sample rate	200-MHz SYSCLK			1.1	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	320			ns
VREFHI		2.4	2.5 or 3.0	VDDA	V
VREFLO		VSSA	VSSA	VSSA	V
Conversion range	External reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

7.11.2.3.3.1 ADC Operating Conditions (16-bit Single-Ended) Notes

Note

The ADC inputs should be kept below VDDA + 0.3 V during operation. If an ADC input exceeds this level, the VREF internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same VREF.

Note

The VREFHI pin must be kept below VDDA for the ADC and DAC to meet specified performance parameters. The VREFHI pin must be kept below VDDA + 0.3 V for functional operation. If the VREFHI pin exceeds VDDA + 0.3 V, a blocking circuit may activate, causing the interval value of VREFHI to float to 0 V internally, giving improper ADC conversion or DAC output.

7.11.2.3.4 ADC Characteristics (16-bit Single-Ended)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles		29.6		31	ADCCLKs
Power Up Time				500	µs
VREFHI input current(1)			190		µA
External Reference Capacitor Value(2)		22			µF
DC Characteristics					
Gain Error		–64	±20	64	LSB
Offset Error		–6	±4	6	LSB
Channel-to-Channel Gain Error			±6		LSB
Channel-to-Channel Offset Error			±6		LSB
ADC-to-ADC Gain Error	Identical VREFHI and VREFLO for all ADCs		±6		LSB
ADC-to-ADC Offset Error	Identical VREFHI and VREFLO for all ADCs		±6		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–6	±1.5	6	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–2		2	LSBs
	VREFHI = 2.5 V, asynchronous ADCs		Not Supported		
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1 via PLL		83.5		dB
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from INTOSC via PLL		83.5		dB
THD(3)	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1 via PLL		-94		dB
SFDR(3)	VREFHI = 2.5 V, fin = 10 kHz SYSCLK from X1 via PLL		93		dB
SINAD(3)	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1 via PLL		83.4		dB
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from INTOSC via PLL		83.4		
ENOB(3)	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1, Single ADC		13.5		bits
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1, synchronous ADCs		13.5		
	VREFHI = 2.5 V, fin = 10 kHz, SYSCLK from X1, asynchronous ADCs		Not Supported		
PSRR	VDD = 1.2-V DC + 200mV DC up to Sine at 1 kHz		77		dB
	Sine at 800 kHz		74		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		77		
	Sine at 800 kHz		74		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk

7.11.2.3.5 ADC Operating Conditions (12-bit Single-Ended)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		50	MHz
Sample rate	200-MHz SYSCLK			3.45	MSPS
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	75			ns
VREFHI		2.4	2.5 or 3.0	VDDA	V
VREFLO		VSSA	VSSA	VSSA	V
Conversion range	External reference	VREFLO		VREFHI	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

7.11.2.3.5.1 ADC Operating Conditions (12-bit Single-Ended) Notes

Note

The ADC inputs should be kept below VDDA + 0.3 V during operation. If an ADC input exceeds this level, the VREF internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same VREF.

Note

The VREFHI pin must be kept below VDDA for the ADC and DAC to meet specified performance parameters. The VREFHI pin must be kept below VDDA + 0.3 V for functional operation. If the VREFHI pin exceeds VDDA + 0.3 V, a blocking circuit may activate, causing the interval value of VREFHI to float to 0 V internally, giving improper ADC conversion or DAC output.

7.11.2.3.6 ADC Characteristics (12-bit Single-Ended)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles		10.1		11	ADCCLKs
Power Up Time				500	µs
VREFHI input current(1)			130		µA
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error		–5	±3	5	LSB
Offset Error		–4	±2	4	LSB
Channel-to-Channel Gain Error			±4		LSB
Channel-to-Channel Offset Error			±2		LSB
ADC-to-ADC Gain Error	Identical VREFHI and VREFLO for all ADCs		±4		LSB
ADC-to-ADC Offset Error	Identical VREFHI and VREFLO for all ADCs		±2		LSB
DNL Error		>–1	±0.5	1	LSB
INL Error		–2	±1.0	2	LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs, 337-ball ZWT package	-2		2	LSBs

7.11.2.3.6 ADC Characteristics (12-bit Single-Ended) (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC-to-ADC Isolation	VREFHI = 2.5 V, asynchronous ADCs, 176-pin PTP package	-9		9	LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		69.1		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		69.1		dB
THD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		–88		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		89		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 via PLL		69.0		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC via PLL		69.0		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		11.2		bits
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs		11.2		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs, 337-ball ZWT package		10.9		bits
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs, 176-pin PTP package		9.7		bits
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV Sine at 800 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 800 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk

7.11.2.3.7 ADCEXTSOC Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier(1)	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 7.10.8.2.1.

7.11.2.3.8 ADC Input Models

Note

ADC channels ADCINA0, ADCINA1, and ADCINB1 have a 50-kΩ pulldown resistor to VSSA.

For single-ended operation, the ADC input characteristics are given by Section 7.11.2.3.8.1, Section 7.11.2.3.8.2, and Figure 7-37.

7.11.2.3.8.1 Single-Ended Input Model Parameters (12-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 7-12
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	14.5 pF
R_s	Nominal source impedance	50 Ω

7.11.2.3.8.2 Single-Ended Input Model Parameters (16-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 7-12
R_{on}	Sampling switch resistance	425 Ω
C_h	Sampling capacitor	32.5 pF
R_s	Nominal source impedance	50 Ω

7.11.2.3.8.3 Single-Ended Input Model

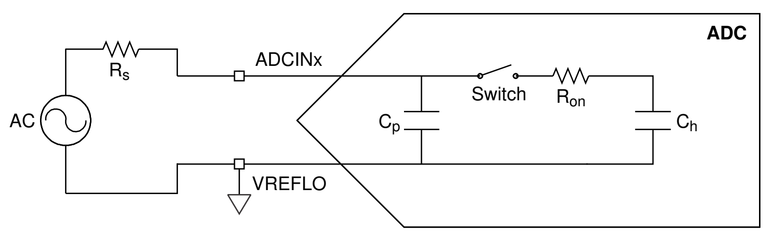


Figure 7-37. Single-Ended Input Model

The user should analyze the ADC input setting assuming worst-case initial conditions on C_h. This will require assuming that C_h could start the S+H window completely charged to VREFHI or completely discharged to VREFLO. When the ADC transitions from an odd-numbered channel to an even-numbered channel, or vice-versa, the actual initial voltage on C_h will be close to being completely discharged to VREFLO. For even-to-even or odd-to-odd channel transitions, the initial voltage on C_h will be close to the voltage of the previously converted channel.

For differential operation, the ADC input characteristics are given by Section 7.11.2.3.8.4 and Figure 7-38.

7.11.2.3.8.4 Differential Input Model Parameters (16-bit Resolution)

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 7-12
R_{on}	Sampling switch resistance	700 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

7.11.2.3.8.5 Differential Input Model

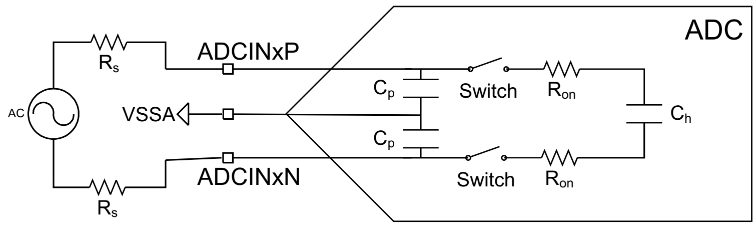


Figure 7-38. Differential Input Model

Table 7-12 lists the parasitic capacitance on each channel. Also, enabling a comparator adds approximately 1.4 pF of capacitance on positive comparator inputs and 2.5 pF of capacitance on negative comparator inputs.

Table 7-12. Per-Channel Parasitic Capacitance

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
ADCINA0	12.9	N/A
ADCINA1	10.3	N/A
ADCINA2	5.9	7.3
ADCINA3	6.3	8.8
ADCINA4	5.9	7.3
ADCINA5	6.3	8.8
ADCINB0(1)	117.0	N/A
ADCINB1	10.6	N/A
ADCINB2	5.9	7.3
ADCINB3	6.2	8.7
ADCINB4	5.2	N/A
ADCINB5	5.1	N/A
ADCINC2	5.5	6.9
ADCINC3	5.8	8.3
ADCINC4	5.0	6.4
ADCINC5	5.3	7.8
ADCIND0	5.3	6.7
ADCIND1	5.7	8.2
ADCIND2	5.3	6.7
ADCIND3	5.6	8.1
ADCIND4	4.3	N/A
ADCIND5	4.3	N/A
ADCIN14	8.6	10.0
ADCIN15	9.0	11.5

(1) The increased capacitance is due to VDAC functionality.

These input models should be used along with actual signal source impedance to determine the acquisition window duration. See the Choosing an Acquisition Window Duration section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual* for more information. See also the *Charge-Sharing Driving Circuits for C2000 ADCs (using TINA-TI simulation tool)* Application Note and the *ADC Input Circuit Evaluation for C2000 MCUs (using TINA-TI simulation tool)* Application Note.

7.11.2.3.9 ADC Timing Diagrams

Section 7.11.2.3.9.1 lists the ADC timings in 12-bit mode (SYSCLK cycles). Section 7.11.2.3.9.2 lists the ADC timings in 16-bit mode. Figure 7-39 and Figure 7-40 show the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 7-13 lists the descriptions of the ADC timing parameters that are in Figure 7-39 and Figure 7-40.

Table 7-13. ADC Timing Parameters

PARAMETER	DESCRIPTION
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} will not necessarily be the same for different SOCs. **Note:** The value on the S+H capacitor will be captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC conversion results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results will be returned.
t_{EOC}	The time from the end of the S+H window until the next ADC conversion S+H window can begin. The subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} will coincide with the conversion results being latched into the result register. If the INTPULSEPOS bit is 0, t_{INT} will coincide with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to ensure the read occurs after the results latch (otherwise, the previous results will be read).

7.11.2.3.9.1 ADC Timings in 12-Bit Mode (SYSCLK Cycles)

ADCCLK PRESCALE		SYSCLK CYCLES				ADCCLK CYCLES
ADCCTL2 [PRESCALE]	RATIO ADCCLK:SYSCLK	t_{EOC}	t_{LAT} (1)	$t_{INT(EARLY)}$ (2)	$t_{INT(LATE)}$	t_{EOC}
0	1	11	13	1	11	11.0
1	1.5	Invalid				
2	2	21	23	1	21	10.5
3	2.5	26	28	1	26	10.4
4	3	31	34	1	31	10.3
5	3.5	36	39	1	36	10.3
6	4	41	44	1	41	10.3
7	4.5	46	49	1	46	10.2
8	5	51	55	1	51	10.2
9	5.5	56	60	1	56	10.2
10	6	61	65	1	61	10.2
11	6.5	66	70	1	66	10.2
12	7	71	76	1	71	10.1
13	7.5	76	81	1	76	10.1
14	8	81	86	1	81	10.1
15	8.5	86	91	1	86	10.1

(1) Refer to the "ADC: DMA Read of Stale Result" advisory in the *TMS320F2838x Real-Time MCUs Silicon Errata*.
(2) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

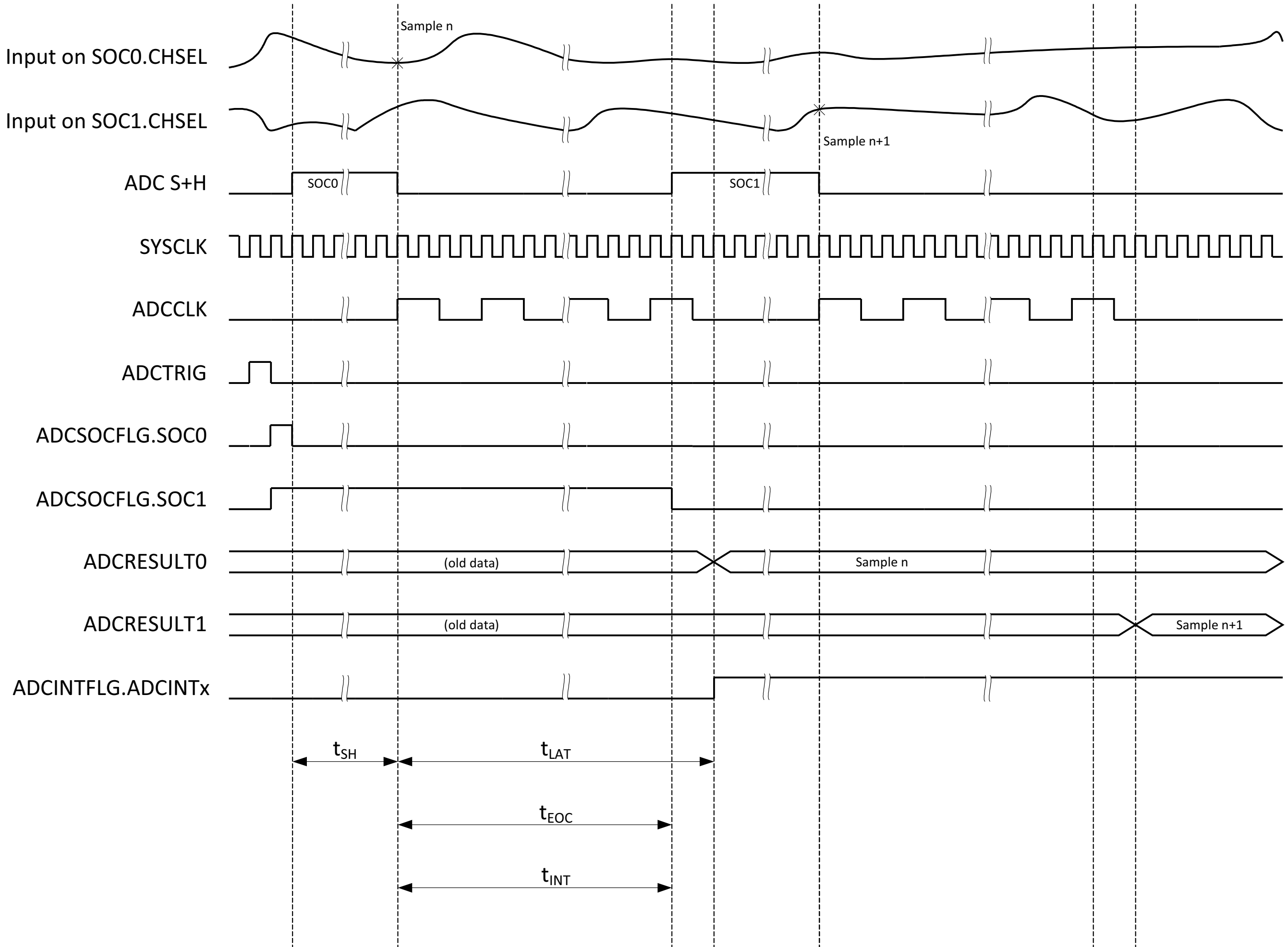


Figure 7-39. ADC Timings for 12-Bit Mode

7.11.2.3.9.2 ADC Timings in 16-Bit Mode

ADCCLK PRESCALE		SYSCLK CYCLES				ADCCLK CYCLES
ADCCTL2 [PRESCALE]	RATIO ADCCLK:SYSCLK	t_{EOC}	t_{LAT} (1)	$t_{INT(EARLY)}$ (2)	$t_{INT(LATE)}$	t_{EOC}
0	1	31	32	1	31	31.0
1	1.5	Invalid				
2	2	60	61	1	60	30.0
3	2.5	75	75	1	75	30.0
4	3	90	91	1	90	30.0
5	3.5	104	106	1	104	29.7
6	4	119	120	1	119	29.8
7	4.5	134	134	1	134	29.8
8	5	149	150	1	149	29.8
9	5.5	163	165	1	163	29.6
10	6	178	179	1	178	29.7
11	6.5	193	193	1	193	29.7
12	7	208	209	1	208	29.7
13	7.5	222	224	1	222	29.6
14	8	237	238	1	237	29.6
15	8.5	252	252	1	252	29.6

(1) Refer to the "ADC: DMA Read of Stale Result" advisory in the *TMS320F2838x Real-Time MCUs Silicon Errata*.
(2) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

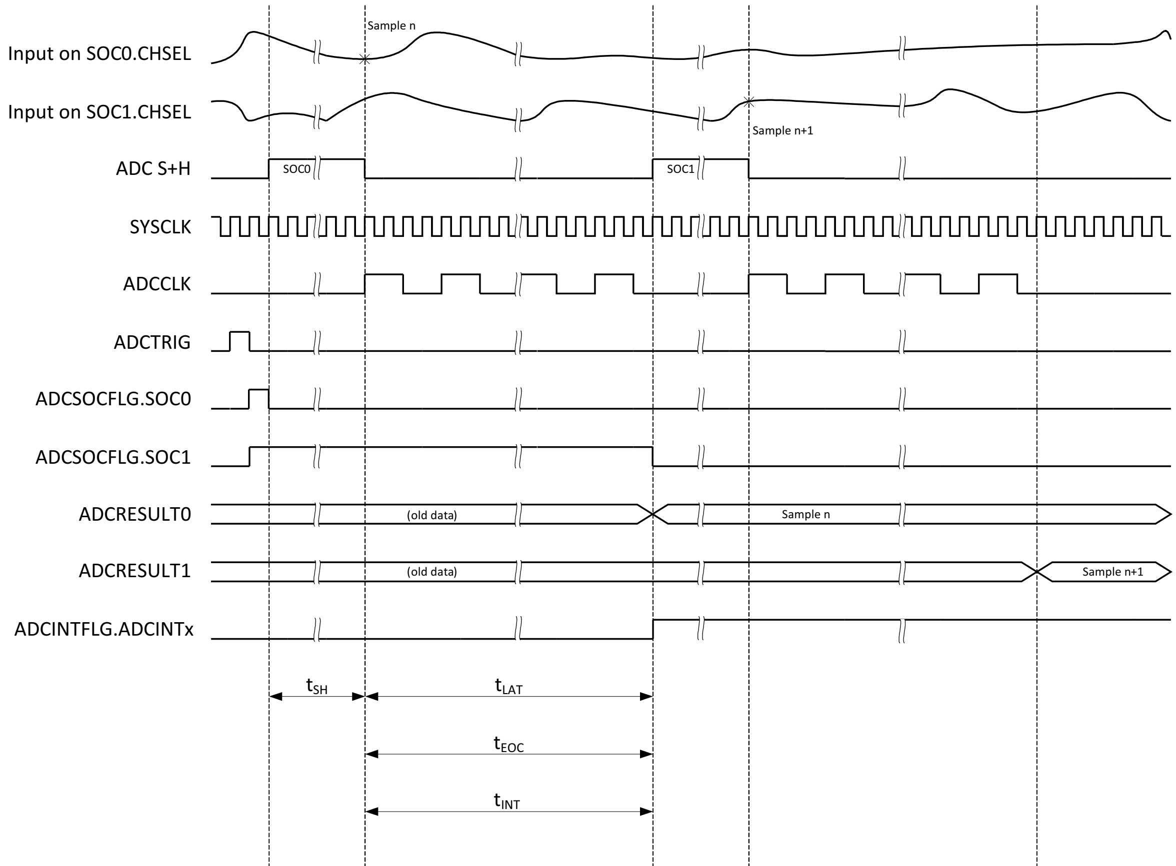


Figure 7-40. ADC Timings for 16-Bit Mode

7.11.2.4 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time listed in Section 7.11.2.4.1.

7.11.2.4.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	External reference		±15		°C
$t_{startup}$	Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)			500		µs
t_{acq}	ADC acquisition time		700			ns

7.11.3 Comparator Subsystem (CMPSS)

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs, two digital filters, and one ramp generator. Comparators are denoted "H" or "L" within each module, where "H" and "L" represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin. The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. A ramp generator circuit is optionally available to control the reference 12-bit DAC value for the high comparator in the subsystem.

Each CMPSS includes:

- Two analog comparators
- Two programmable reference 12-bit DACs
- One ramp generator
- Two digital filters
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option to choose between VDDA or VDAC to be the DAC reference voltage

The block diagram for the CMPSS is shown in Figure 7-41.

- CTRIPx (x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. For more details on the ePWM X-BAR mux configuration, see the Enhanced Pulse Width Modulator (ePWM) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.
- CTRIPxOUTx (x= "H" or "L") signals are connected to the Output X-BAR for external signaling. For more details on the Output X-BAR mux configuration, see the General-Purpose Input/Output (GPIO) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

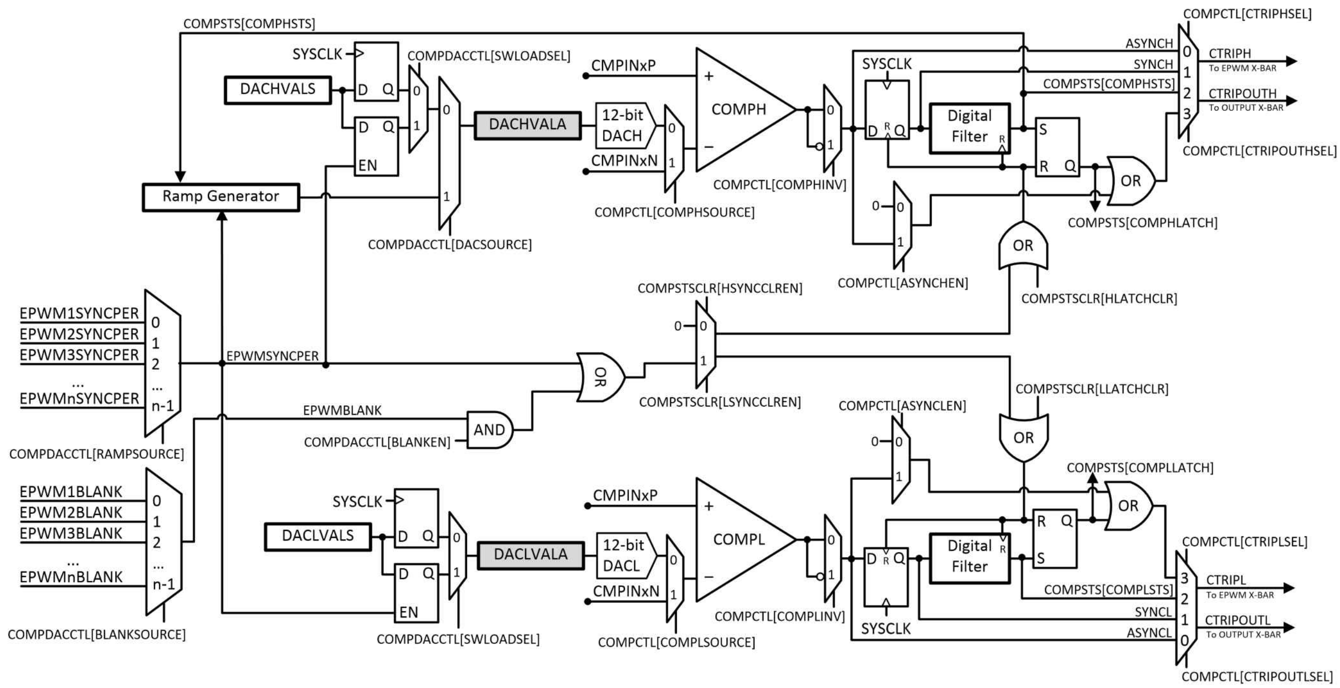


Figure 7-41. CMPSS Module Block Diagram

Figure 7-42 shows the CMPSS connectivity on the 337-ball ZWT and 176-pin PTP packages.

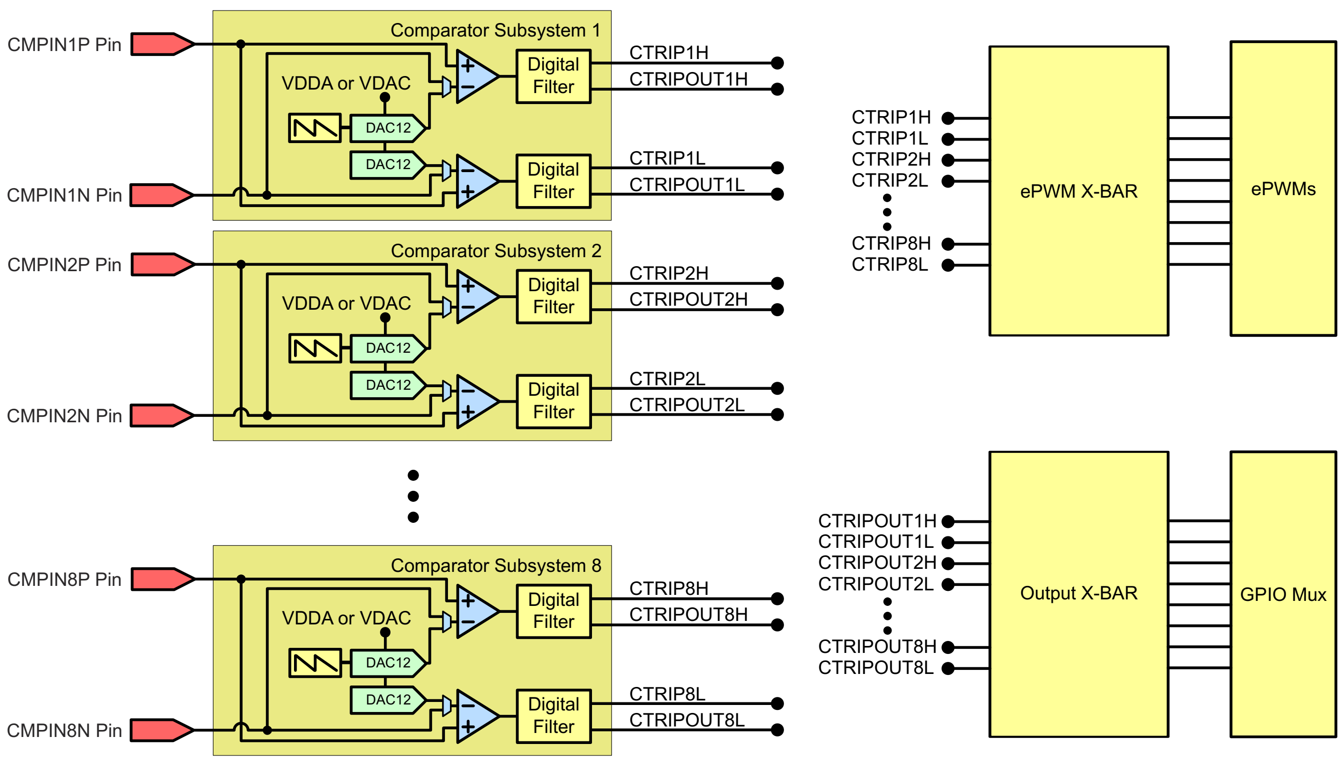


Figure 7-42. CMPSS Connectivity (337-Ball ZWT and 176-Pin PTP)

7.11.3.1 CMPSS Electrical Data and Timing

7.11.3.1.1 Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PU}	Power-up time				500	µs
	Comparator input (CMPINxx) range		0		VDDA	V
	Input referred offset error	Low common mode, inverting input set to 50 mV	–20		20	mV
	Hysteresis(1)	1x	4	12	20	LSB
		2x	17	24	33	
		3x	25	36	50	
		4x	30	48	67	
	Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)	Step response		21	60	ns
		Ramp response (1.65 V/µs)		26		
		Ramp response (8.25 mV/µs)		30		ns
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

7.11.3.1.2 CMPSS Comparator Input Referred Offset and Hysteresis

Note

The CMPSS inputs must be kept below VDDA + 0.3 V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit will isolate the internal comparator from the external pin until the external pin voltage returns below VDDA + 0.3 V. During this time, the internal comparator input will be floating and can decay below VDDA within approximately 0.5 µs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

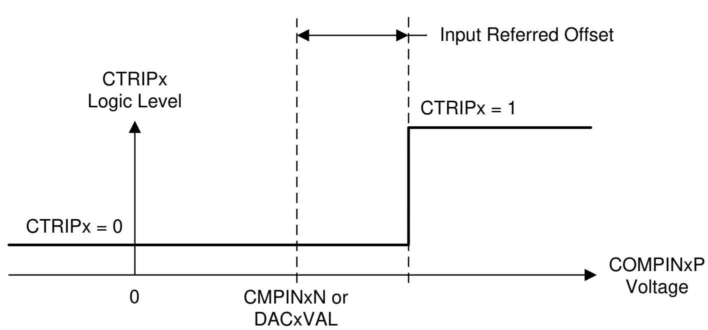


Figure 7-43. CMPSS Comparator Input Referred Offset

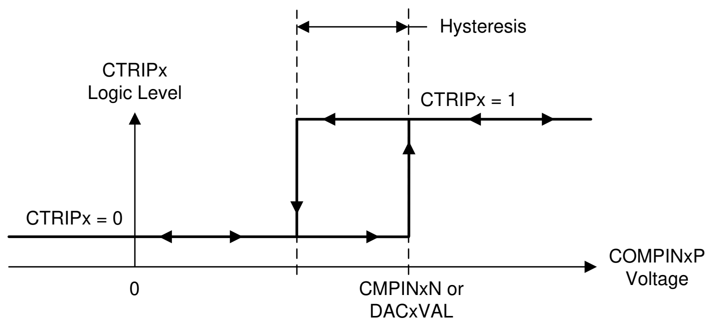


Figure 7-44. CMPSS Comparator Hysteresis

Section 7.11.3.1.3 lists the CMPSS DAC static electrical characteristics.

7.11.3.1.3 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		VDDA	V
	External reference	0		VDAC(4)	
Static offset error(1)		–25		25	mV
Static gain error(1)		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance(2)	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time(2)			200		ns
VDAC reference voltage	When VDAC is reference	2.4	2.5 or 3.0	VDDA	V
VDAC load(3)	When VDAC is reference		6		kΩ

(1) Includes comparator input referred errors.
(2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(3) Per active CMPSS module.
(4) The maximum output voltage is VDDA when VDAC > VDDA.

7.11.3.1.4 CMPSS Illustrative Graphs

Note

The VDAC pin must be kept below VDDA for the DAC and CMPSS to meet specified performance parameters. The VDAC pin must be kept below VDDA + 0.3 V for functional operation. If the VDAC pin exceeds VDDA + 0.3 V, a blocking circuit may activate, causing the interval value of VDAC to float to 0 V internally, giving improper DAC output or CMPSS trips.

Figure 7-45 shows the CMPSS DAC static offset. Figure 7-46 shows the CMPSS DAC static gain. Figure 7-47 shows the CMPSS DAC static linearity.

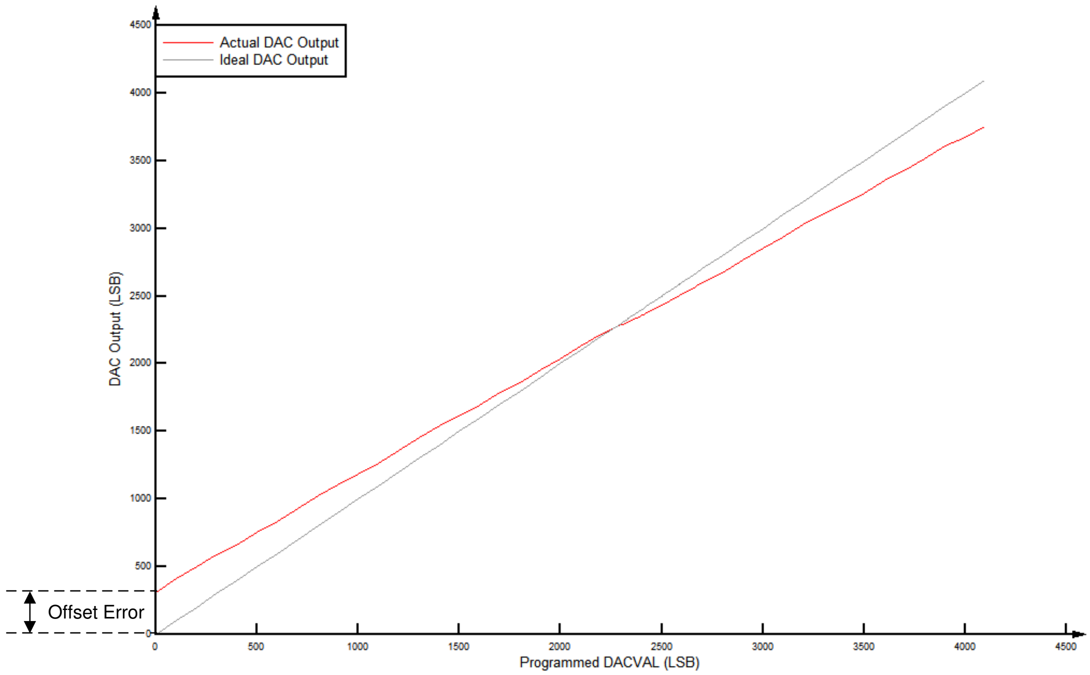


Figure 7-45. CMPSS DAC Static Offset

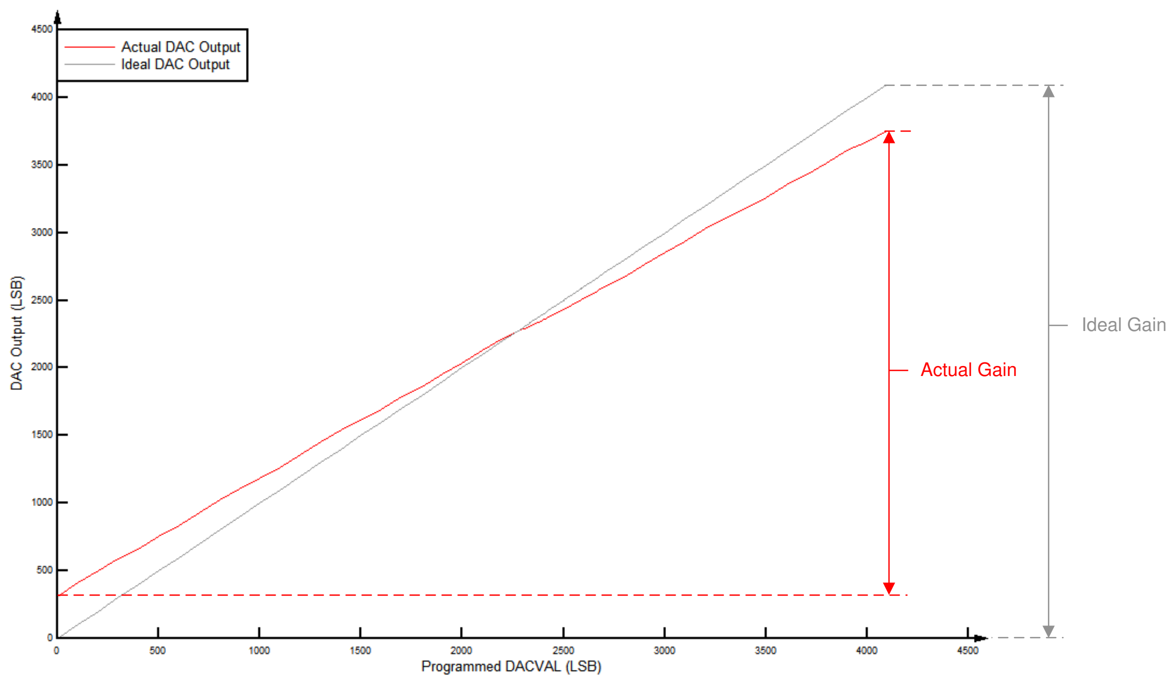


Figure 7-46. CMPSS DAC Static Gain

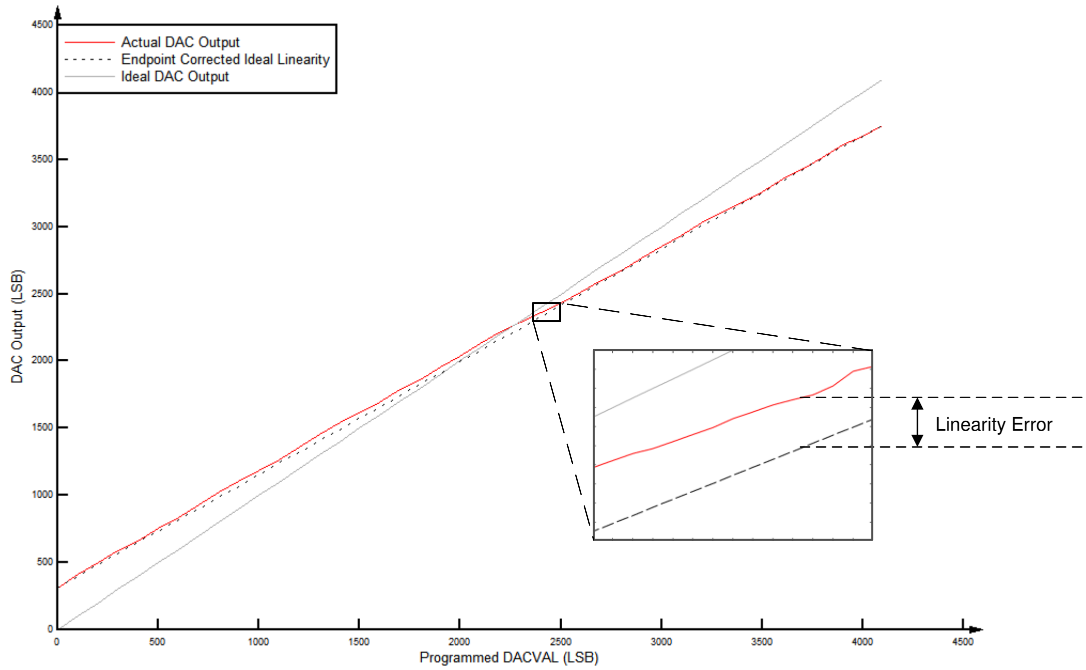


Figure 7-47. CMPSS DAC Static Linearity

7.11.3.1.5 CMPSS DAC Dynamic Error

When using the ramp generator to control the internal DAC, the step size can vary based on the application need. Since the step size of the DAC is less than a full scale transition, the settling time is improved from the electrical specification listed in the *CMPSS DAC Static Electrical Characteristics* table. The equation below and Figure 7-48 can give guidance on the expected voltage error from ideal based on different RAMPxDECVALA values.

$$DYNAMICERROR = (m \times RAMPxDECVALA) + b \quad (5)$$

Table 7-14. DAC Max Dynamic Error Terms

EQUATION PARAMETER	MIN (LSB)	MAX (LSB)
m	0.167	0.30
b	3.7	5.6

Note

Above error terms are based on the max SYSCLK of the target device. If operating below the max SYSCLK then the "m" error term should be scaled accordingly.

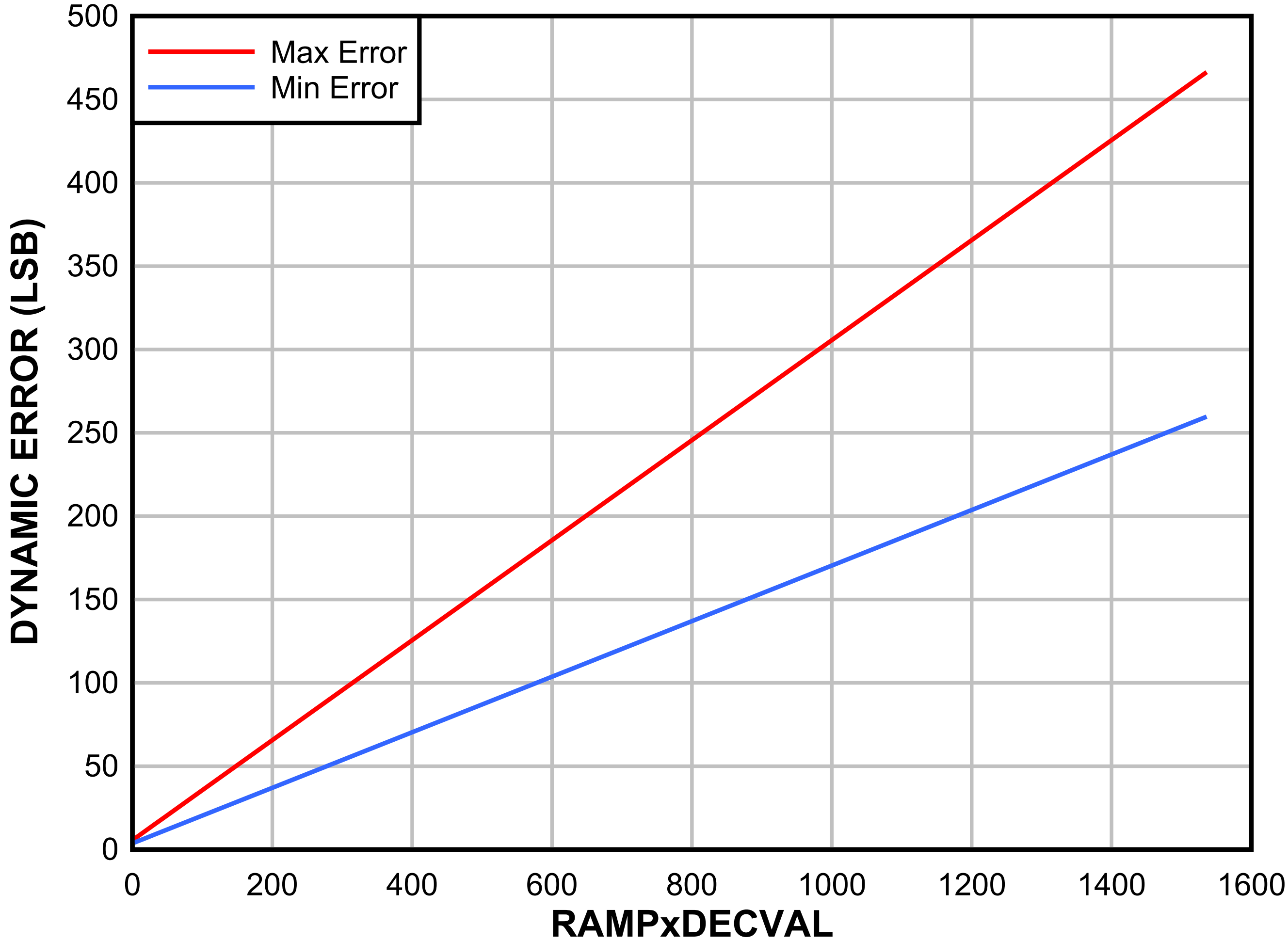


Figure 7-48. CMPSS DAC Dynamic Error

7.11.4 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that is capable of driving an external load. An integrated pulldown resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pulldown resistor cannot be disabled and remains as a passive component on the pin, even for other shared pinmux functions. The buffered DAC is a general-purpose DAC that can be used to generate a DC voltage in addition to AC waveforms such as sine waves, square waves, triangle waves, and so forth. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCPER events.

Each buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage source
- Pulldown resistor on output
- Ability to synchronize with EPWMSYNCPER

The block diagram for the buffered DAC is shown in Figure 7-49.

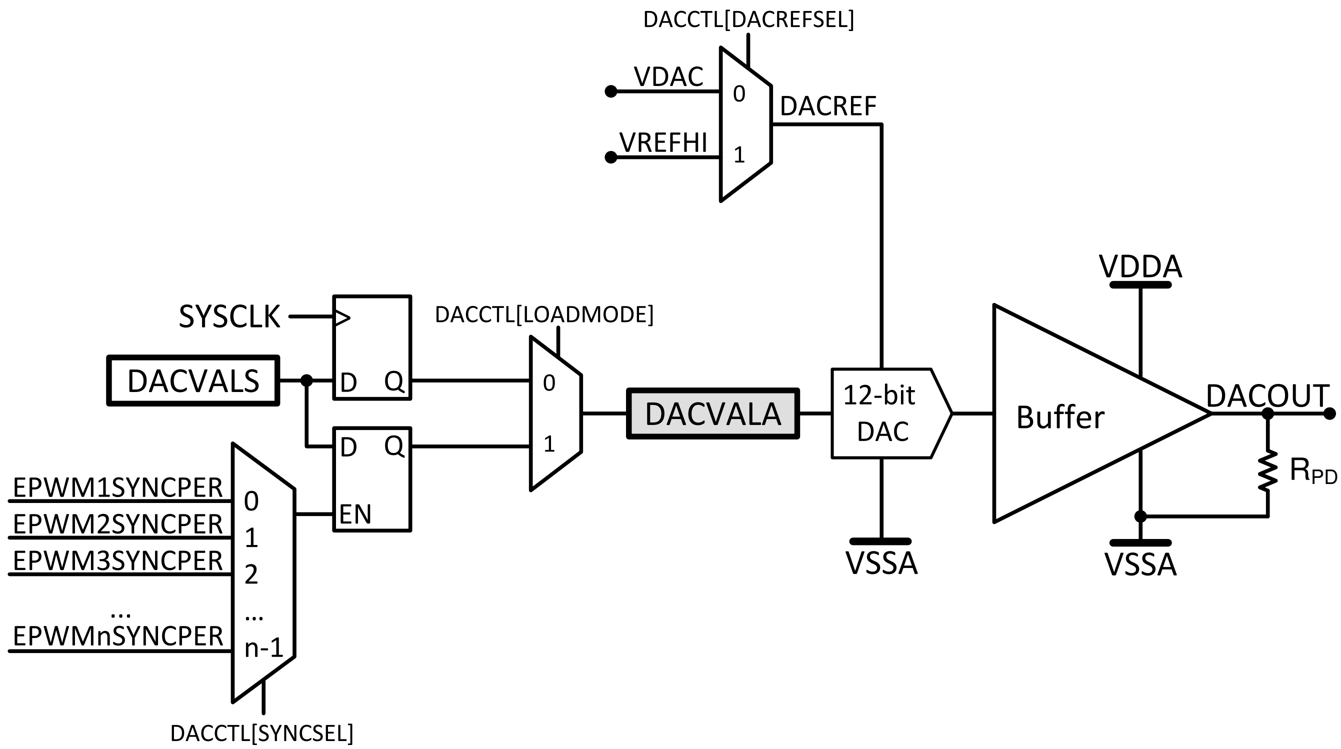


Figure 7-49. DAC Module Block Diagram

7.11.4.1 Buffered DAC Electrical Data and Timing

Section 7.11.4.1.1 lists the buffered DAC operating conditions. Section 7.11.4.1.2 lists the buffered DAC electrical characteristics. Figure 7-50 shows the buffered DAC offset. Figure 7-51 shows the buffered DAC gain. Figure 7-52 shows the buffered DAC linearity.

7.11.4.1.1 Buffered DAC Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN[(1)]	TYP[(1)]	MAX[(1)]	UNIT
R_L	Resistive Load		5			kΩ
C_L	Capacitive Load				100	pF
V_{OUT}	Valid Output Voltage Range[(2)]	R_L = 5 kΩ	0.3		VDDA – 0.3	V
	Reference Voltage[(3)]	VDAC or VREFHI	2.4	2.5 or 3.0	VDDA	V

(1) Typical values are measured with VREFHI = 3.3 V unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V.
(2) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(3) For best PSRR performance, VDAC or VREFHI should be less than VDDA.

7.11.4.1.2 Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(1)	MAX(1)	UNIT
General						
	Resolution			12		bits
R_{PD}	Pulldown Resistor			50		kΩ
	Load Regulation		–1		1	mV/V
	Glitch Energy			1.5		V-ns
	Voltage Output Settling Time Full-Scale	Settling to 2 LSBs after 0.3V-to-3V transition		2		µs
	Voltage Output Settling Time 1/4th Full-Scale	Settling to 2 LSBs after 0.3V-to-0.75V transition		1.6		µs
	Voltage Output Slew Rate	Slew rate from 0.3V-to-3V transition	2.8		4.5	V/µs
	Load Transient Settling Time(6)	5-kΩ Load			328	ns
	Reference Input Resistance(2)	VDAC or VREFHI		170		kΩ
TPU	Power-up Time	External Reference mode			500	µs
DC Characteristics						
Offset	Offset Error	Midpoint	–10		10	mV
Gain	Gain Error(3)		–2.5		2.5	% of FSR
DNL	Differential Non Linearity(4)	Endpoint corrected	> –1	±0.4	1	LSB
INL	Integral Non Linearity	Endpoint corrected	–5	±2	5	LSB
AC Characteristics						
	Output Noise	Integrated noise from 100 Hz to 100 kHz		500		µVrms
		Noise density at 10 kHz		711		nVrms/√Hz
SNR	Signal to Noise Ratio	1020 Hz, 1 MSPS		67		dB
THD	Total Harmonic Distortion	1020 Hz, 1 MSPS		–63		dB
SFDR	Spurious Free Dynamic Range	1020 Hz, 1 MSPS (including harmonics and spurs)		66		dBc
		1020 Hz, 1 MSPS (including only spurs)		104		
PSRR	Power Supply Rejection Ratio(5)	DC		70		dB
		100 kHz		30		

(1) Typical values are measured with VREFHI = 3.3 V unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V.
(2) Per active Buffered DAC module.
(3) Gain error is calculated for linear output range.
(4) The DAC output is monotonic.
(5) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.
(6) Settling to within 3LSBs.

7.11.4.1.3 Buffered DAC Notes and Illustrative Graphs

Note

The VDAC pin must be kept below VDDA for the DAC and CMPSS to meet specified performance parameters. The VDAC pin must be kept below VDDA + 0.3 V for functional operation. If the VDAC pin exceeds VDDA + 0.3 V, a blocking circuit may activate, causing the interval value of VDAC to float to 0 V internally, giving improper DAC output or CMPSS trips.

Note

The VREFHI pin must be kept below VDDA for the ADC and DAC to meet specified performance parameters. The VREFHI pin must be kept below VDDA + 0.3 V for functional operation. If the VREFHI pin exceeds VDDA + 0.3 V, a blocking circuit may activate, causing the interval value of VREFHI to float to 0 V internally, giving improper ADC conversion or DAC output.

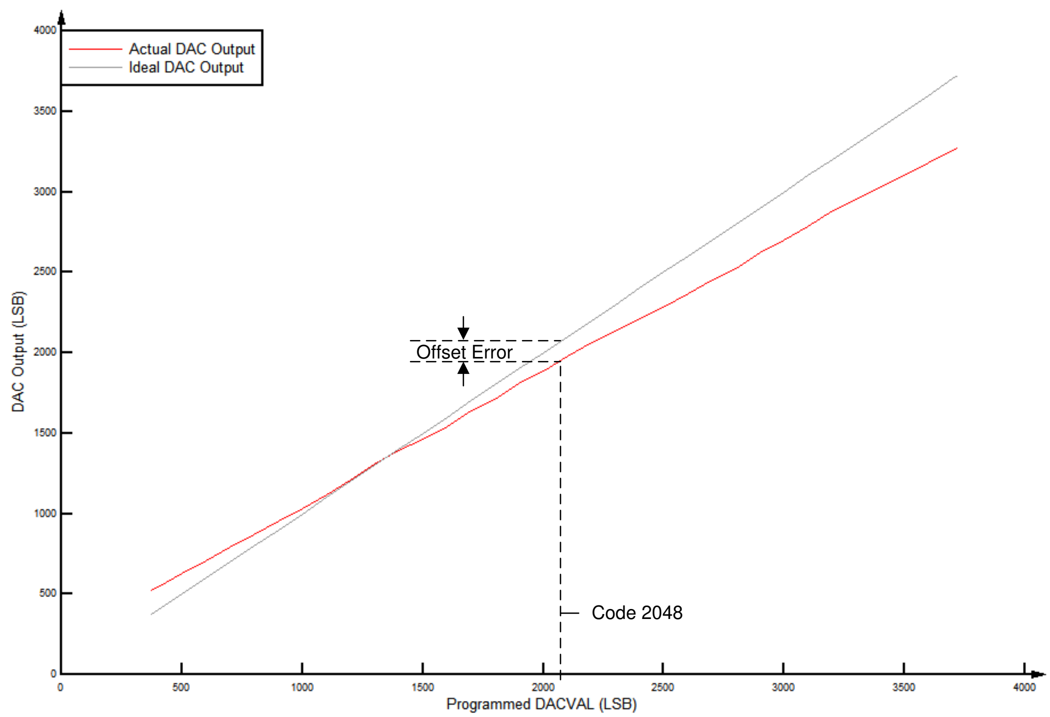


Figure 7-50. Buffered DAC Offset

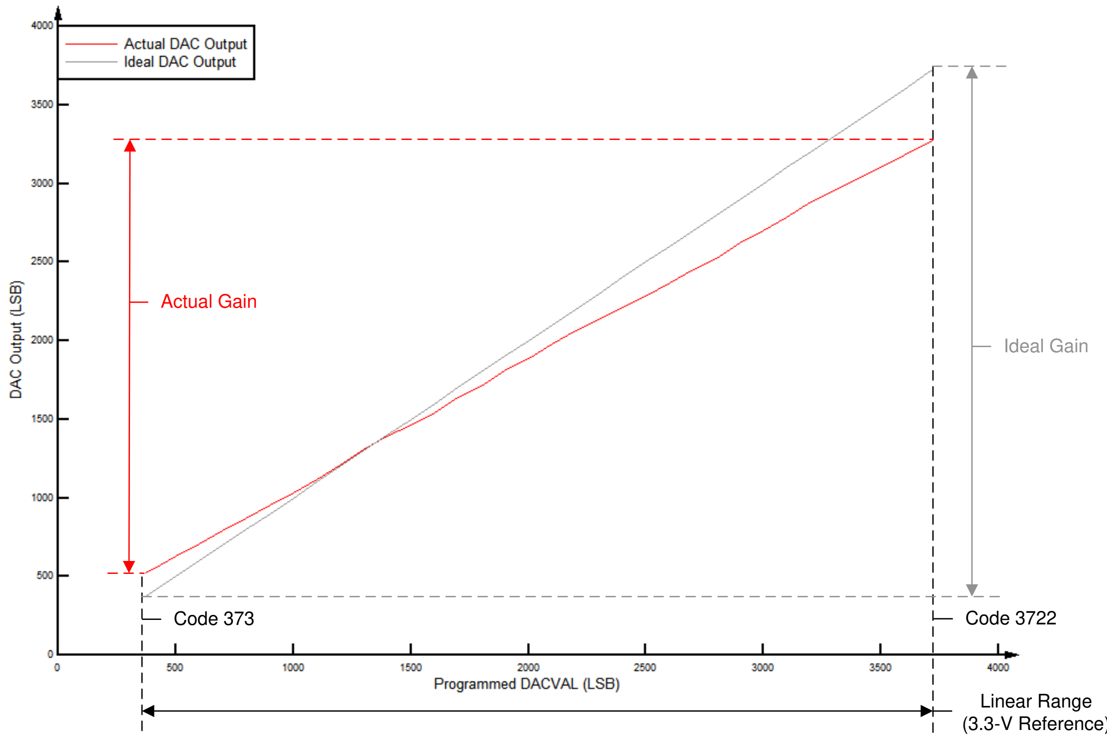


Figure 7-51. Buffered DAC Gain

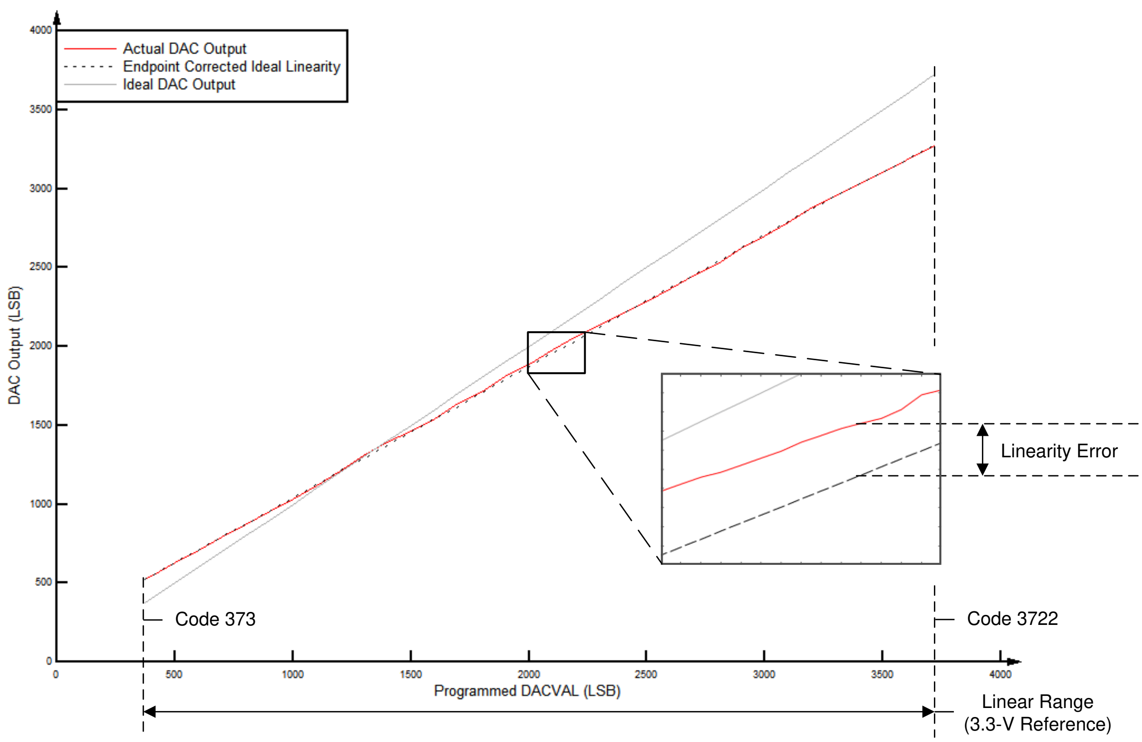


Figure 7-52. Buffered DAC Linearity

7.12 C28x Control Peripherals

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

7.12.1 Enhanced Capture and High-Resolution Capture (eCAP, HRCAP)

The eCAP module can be used in systems where accurate timing of external events is important.

Applications for eCAP include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

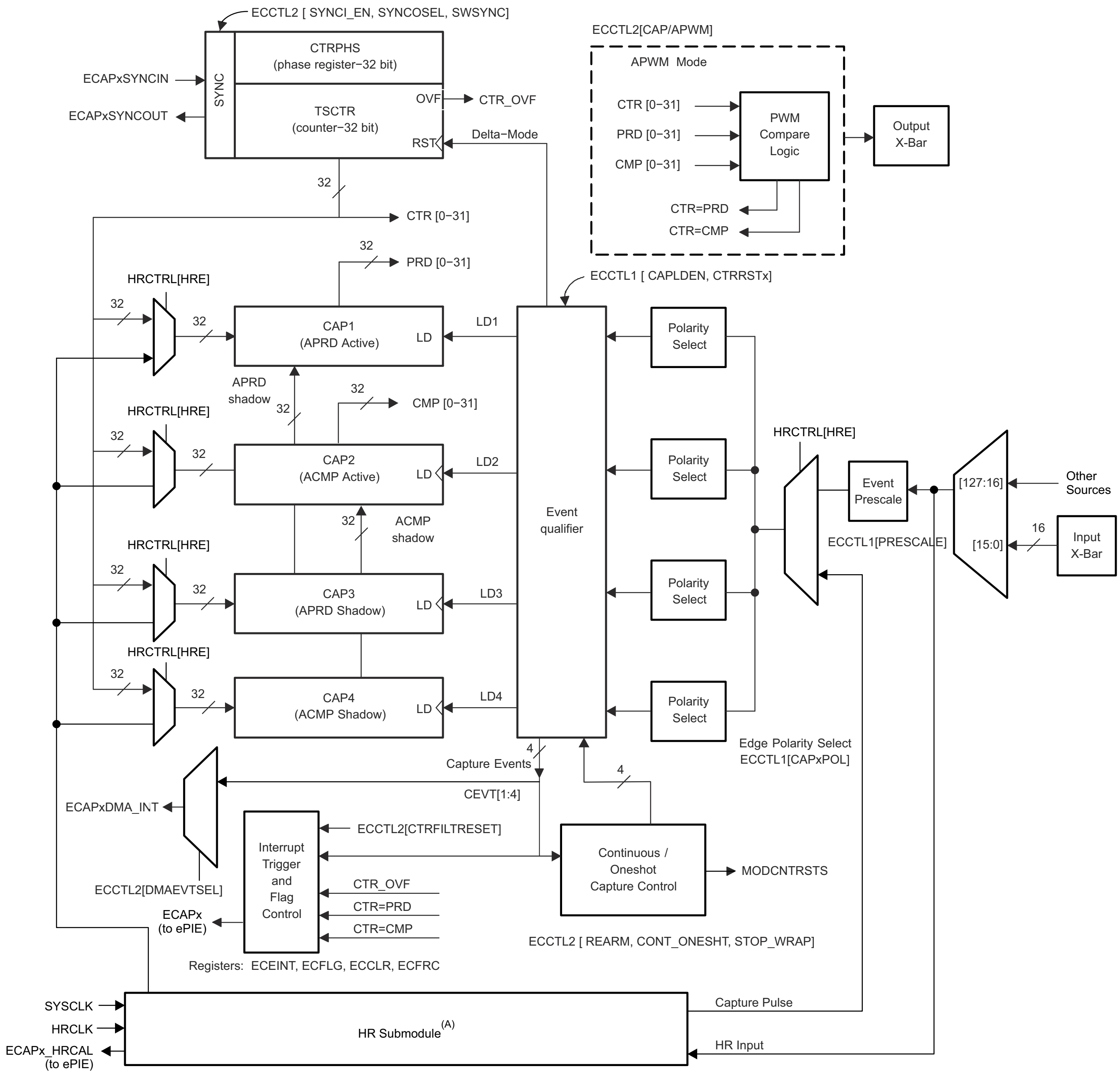
- 4-event time-stamp registers (each 32 bits)
- Edge-polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All of the above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).

The capture functionality of the Type-2 eCAP is enhanced from the Type-0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] will clear the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCTRSTS]) indicates which capture register will be loaded next. In the Type-0 eCAP, it was not possible to know current state of modulo counter.
- DMA trigger source
  - eCAPxDMA is added as a DMA trigger. CEVT[1–4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals.
- EALLOW protection
  - EALLOW protection is added to critical registers. To maintain software compatibility with the Type-0 eCAP, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.
- ECAPxSYNCINSEL register
  - The ECAPSxYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

The eCAP inputs connect to any GPIO input through the Input X-BAR. The APWM outputs connect to GPIO pins through the Output X-BAR to OUTPUTx positions in the GPIO mux. See Section 6.5.2 and Section 6.5.3.

Figure 7-53 shows the eCAP and HRCAP block diagram.



A. The HRCAP submodule is not available on all eCAP modules; in this case, the high-resolution muxes and hardware are not implemented.

Figure 7-53. eCAP and HRCAP Block Diagram

The eCAP module is clocked by PERx.SYSCLK.

The clock enable bits (ECAPx) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

The eCAP6 and eCAP7 modules can be configured as high-resolution capture (HRCAP) submodules. The HRCAP submodule measures the difference, in time, between pulses asynchronously to the system clock. This submodule is new to the eCAP Type 2 module, and features many enhancements over the Type 0 HRCAP module.

Applications for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty-cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance/sonar measurement and scanning
- Flow measurements

The HRCAP submodule includes the following features:

- Pulse-width capture in either non-high-resolution or high-resolution modes
- Absolute mode pulse-width capture
- Continuous or "one-shot" capture
- Capture on either falling or rising edge
- Continuous mode capture of pulse widths in 4-deep buffer
- Hardware calibration logic for precision high-resolution capture
- All of the resources in this list are available on any pin using the Input X-BAR.

The HRCAP submodule includes one high-resolution capture channel in addition to a calibration block. The calibration block allows the HRCAP submodule to be continually recalibrated, at a set interval, with no “down time”. Because the HRCAP submodule now uses the same hardware as its respective eCAP, if the HRCAP is used, the corresponding eCAP will be unavailable.

Each high-resolution-capable channel has the following independent key resources.

- All hardware of the respective eCAP
- High-resolution calibration logic
- Dedicated calibration interrupt

7.12.1.1 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM or eCAP or X-Bar or EtherCAT. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 7-54.

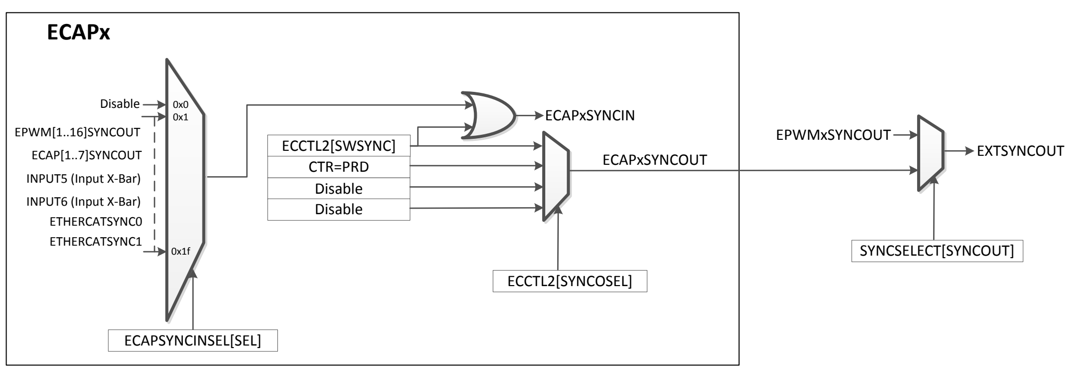


Figure 7-54. eCAPSynchronization Scheme

7.12.1.2 eCAP Electrical Data and Timing

Section 7.12.1.2.1 lists the eCAP timing requirements and Section 7.12.1.2.2 lists the eCAP switching characteristics.

7.12.1.2.1 eCAP Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$			ns
		Synchronous	$2t_{c(SYSCLK)}$			
		With input qualifier	$1t_{c(SYSCLK)} + t_{w\_(IQSW)}$			

7.12.1.2.2 eCAP Switching Charcteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

7.12.1.3 HRCAP Electrical Data and Timing

Section 7.12.1.3.1 lists the HRCAP switching characteristics. Figure 7-55 shows the HRCAP accuracy precision and resolution. Figure 7-56 shows the HRCAP standard deviation characteristics.

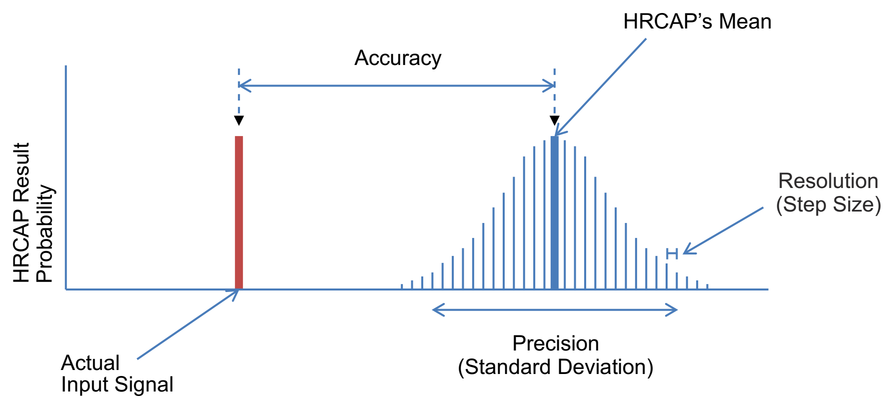
7.12.1.3.1 HRCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input pulse width		110			ns
Accuracy(1) (2) (3) (4)	Measurement length ≤ 5 µs		±390	540	ps
	Measurement length > 5 µs		±450	1450	ps
Standard deviation			See Figure 7-56		
Resolution			300		ps

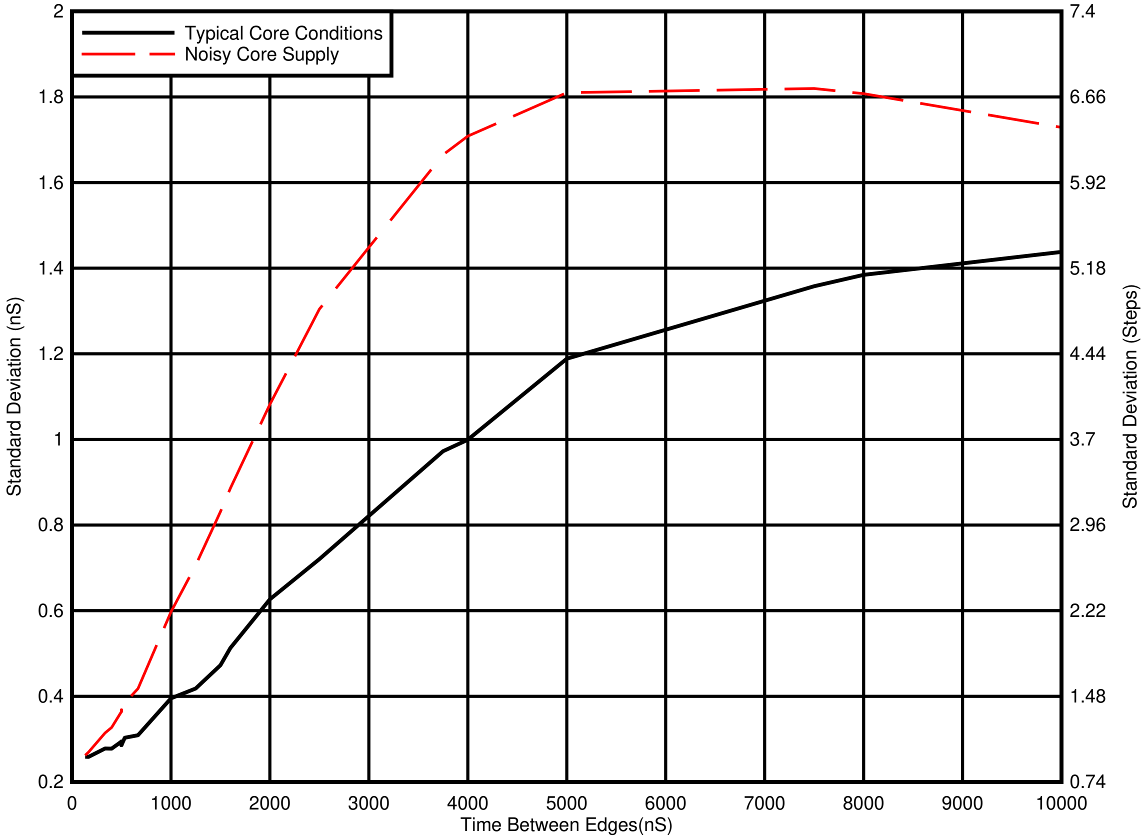
(1) Value obtained using an oscillator of 100 PPM, oscillator accuracy directly affects the HRCAP accuracy.
(2) Measurement is completed using rising-rising or falling-falling edges
(3) Opposite polarity edges will have an additional inaccuracy due to the difference between V_{IH} and V_{IL}. This effect is dependent on the signal's slew rate.
(4) Accuracy only applies to time-converted measurements.

7.12.1.3.2 HRCAP Graphs



A. The HRCAP has some variation in performance, this results in a probability distribution which is described using the following terms:
   - Accuracy: The time difference between the input signal and the mean of the HRCAP's distribution.
   - Precision: The width of the HRCAP's distribution, this is given as a standard deviation.
   - Resolution: The minimum measurable increment.

Figure 7-55. HRCAP Accuracy Precision and Resolution



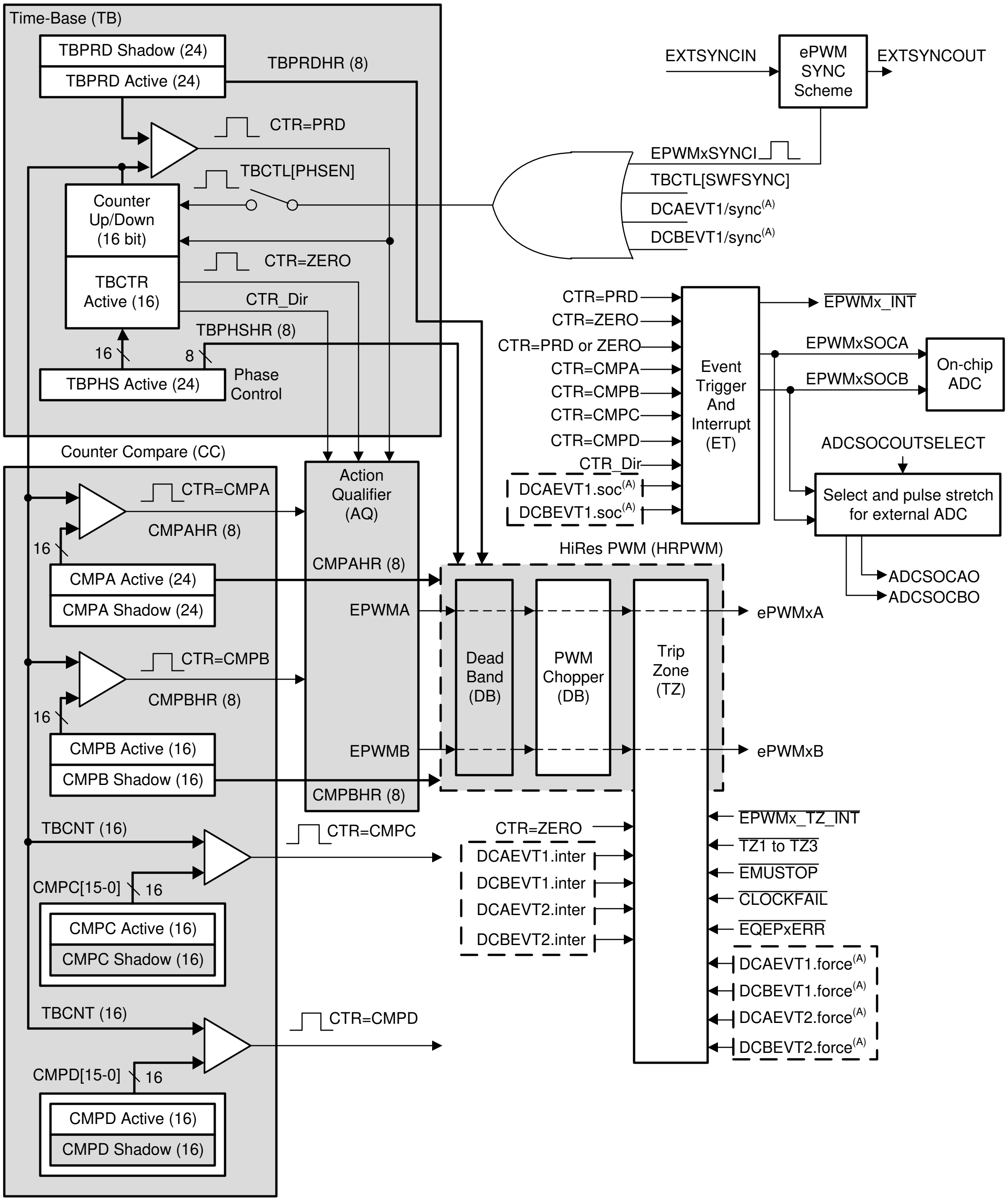
A. Typical core conditions: All peripheral clocks are enabled.
B. Noisy core supply: All core clocks are enabled and disabled with a regular period during the measurement. This resulted in the 1.2-V rail experiencing a 18.5-mA swing during the measurement.
C. Fluctuations in current and voltage on the 1.2-V rail cause the standard deviation of the HRCAP to rise. Care should be taken to ensure that the 1.2-V supply is clean, and that noisy internal events, such as enabling and disabling clock trees, have been minimized while using the HRCAP.

Figure 7-56. HRCAP Standard Deviation Characteristics

7.12.2 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

Figure 7-57 shows the signal interconnections with the ePWM. Figure 7-58 shows the ePWM trip input connectivity.



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 7-57. ePWM Submodules and Critical Internal Signal Interconnects

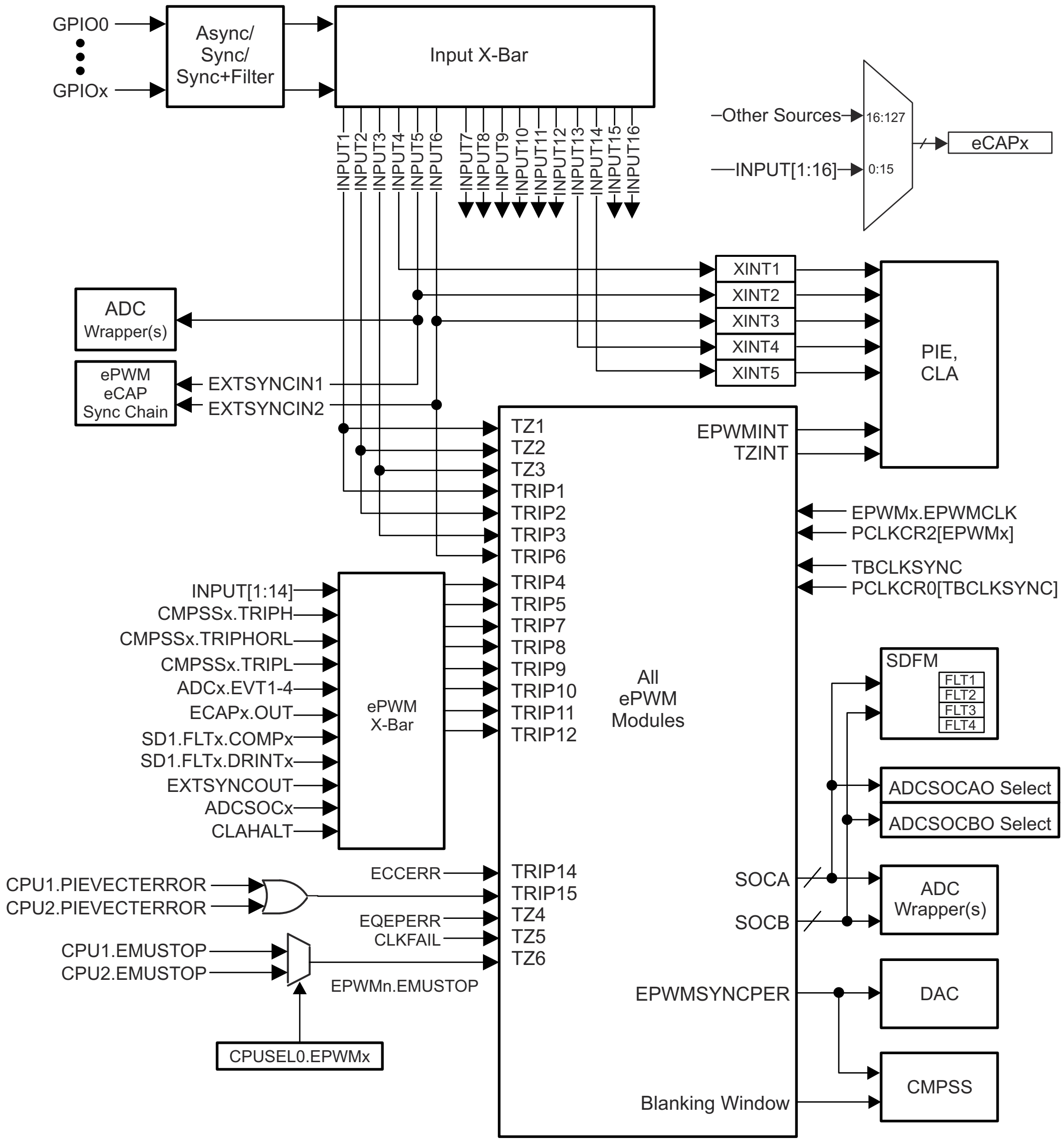


Figure 7-58. ePWM Trip Input Connectivity

7.12.2.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules between CPU1 and CPU2 and allows localized synchronization within the modules belonging to the same CPU. Like the other peripherals, the partitioning of the ePWM and eCAP modules needs to be done using the CPUSELx registers. Figure 7-59 shows the synchronization scheme.

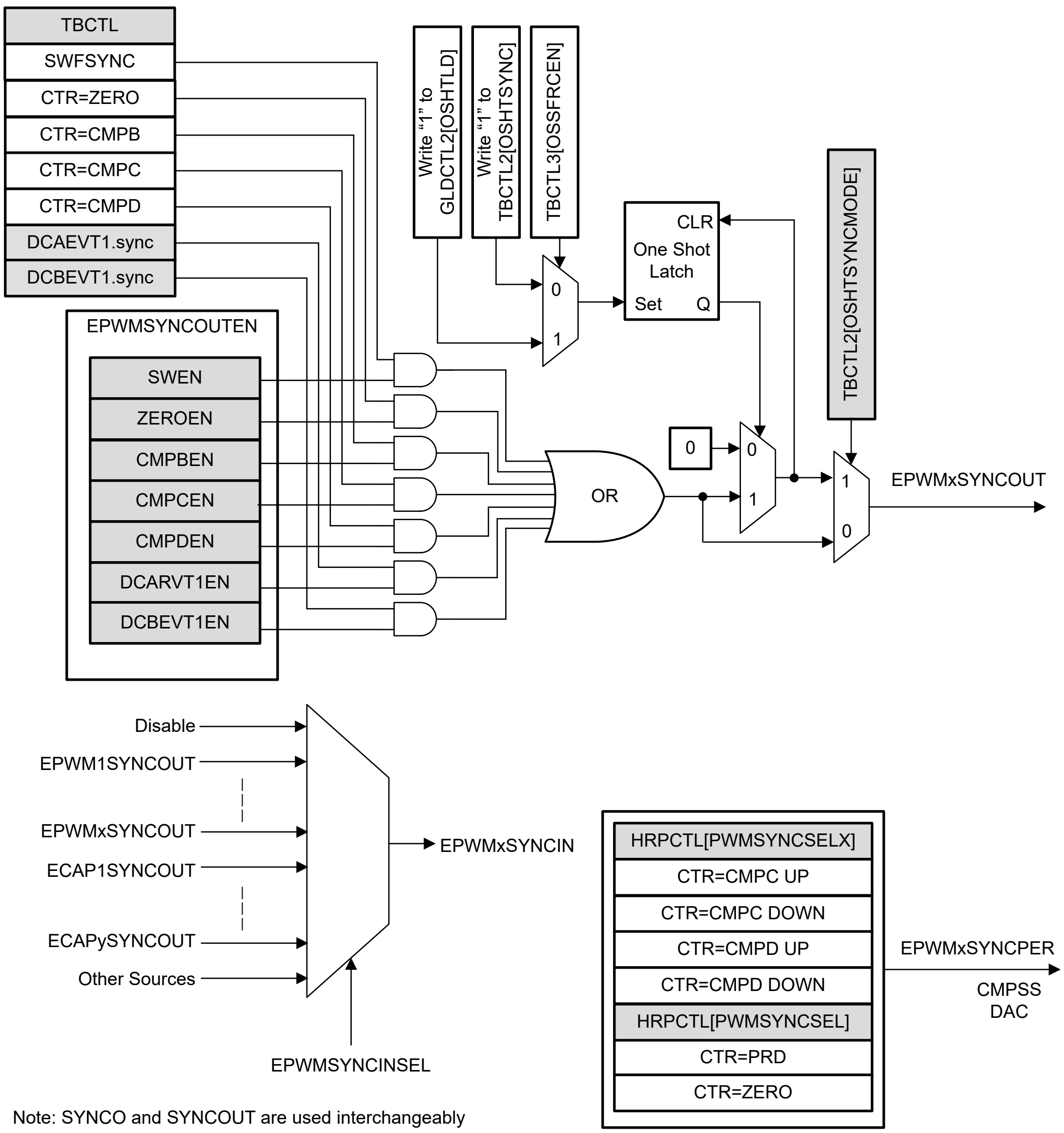


Figure 7-59. Synchronization Chain Architecture

7.12.2.2 ePWM Electrical Data and Timing

Section 7.12.2.2.1 lists the PWM timing requirements and Section 7.12.2.2.2 lists the PWM switching characteristics. For an explanation of the input qualifier parameters, see Section 7.10.8.2.1.

7.12.2.2.1 ePWM Timing Requirements

			MIN	MAX	UNIT
$f_{(EPWM)}$	Frequency, EPWMCLK			200	MHz
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		

7.12.2.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ\text{-}PWM)}$ (1)	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		30	ns
$t_{skew(PWM)}$	Skew between any two PWM outputs		2.5	ns

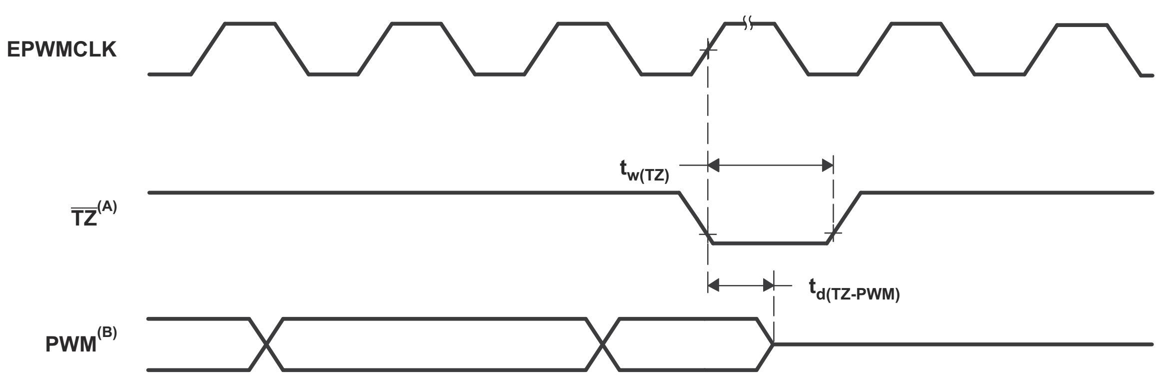
(1) The delay time is only for GPIO sources, it excludes the CMPSS.

7.12.2.2.3 Trip-Zone Input Timing

Section 7.12.2.2.3.1 lists the trip-zone input timing requirements. Figure 7-60 shows the PWM Hi-Z characteristics. For an explanation of the input qualifier parameters, see Section 7.10.8.2.1.

7.12.2.2.3.1 Trip-Zone Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZ}$x input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 7-60. PWM Hi-Z Characteristics

7.12.2.3 External ADC Start-of-Conversion Electrical Data and Timing

Section 7.12.2.3.1 lists the external ADC start-of-conversion switching characteristics. Figure 7-61 shows the $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ timing.

7.12.2.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{\text{ADCSOCxO}}$ low	$32t_{c(SYSCLK)}$		cycles

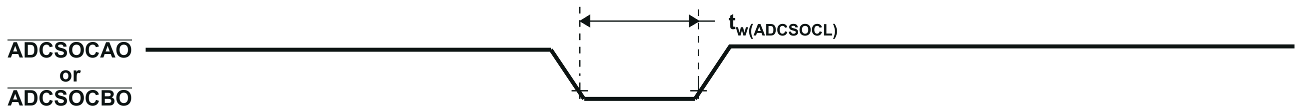


Figure 7-61. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

7.12.3 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

Note

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

7.12.3.1 HRPWM Electrical Data and Timing

Section 7.12.3.1.1 lists the high-resolution PWM switching characteristics.

7.12.3.1.1 High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

7.12.4 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 7-62):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

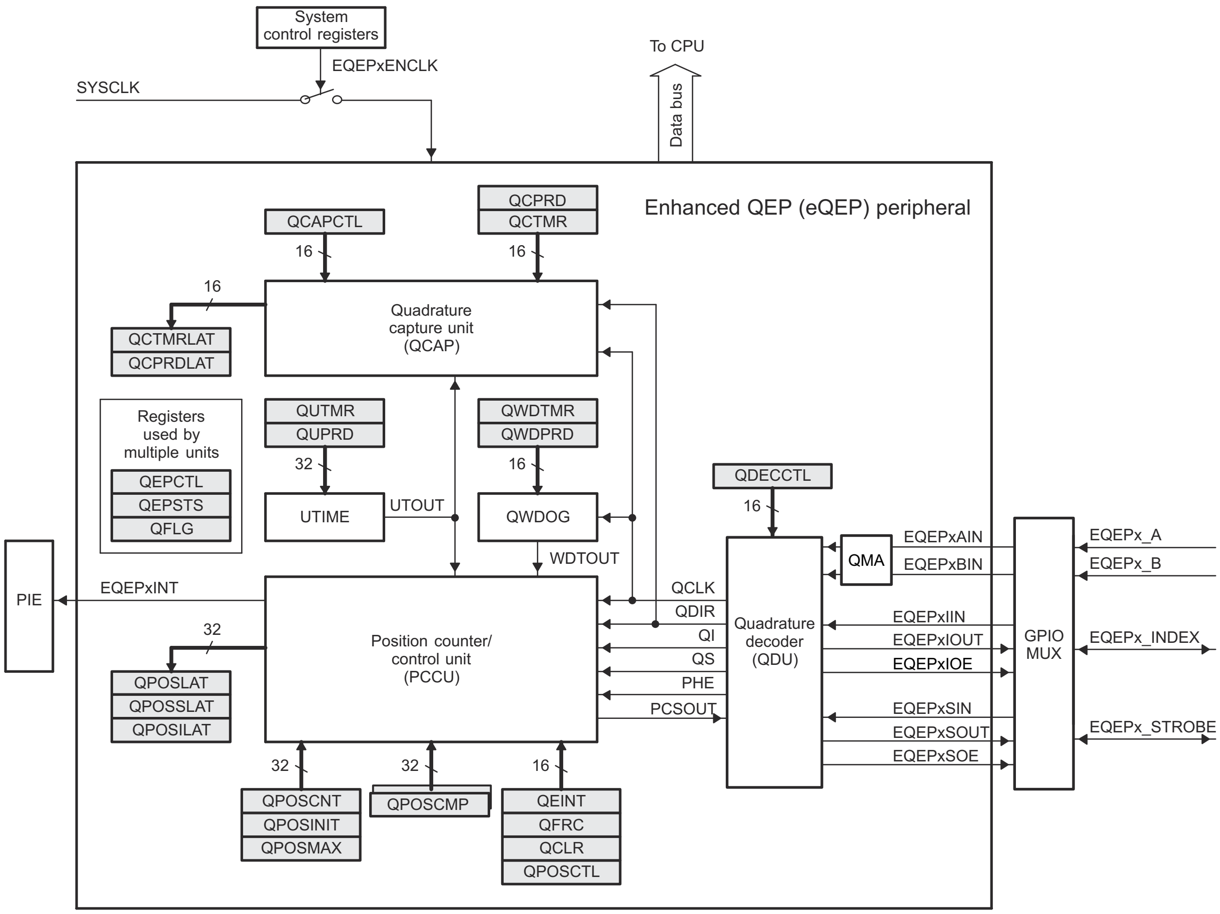


Figure 7-62. eQEP Block Diagram

7.12.4.1 eQEP Electrical Data and Timing

Section 7.12.4.1.1 lists the eQEP timing requirement. GPIO asynchronous mode should not be used for eQEP input pins. For an explanation of the input qualifier parameters, see Section 7.10.8.2.1.

Section 7.12.4.1.2 lists the eQEP switching characteristics.

7.12.4.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous(1)	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

7.12.4.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$4t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$6t_{c(SYSCLK)}$	cycles

7.12.5 Sigma-Delta Filter Module (SDFM)

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each input channel can receive an independent sigma-delta (ΣΔ) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator (secondary filter) for immediate digital threshold comparisons for over-current and under-current monitoring, and zeros-crossing detection. Figure 7-63 shows a block diagram of the SDFMs.

SDFM features include:

- Eight external pins per SDFM module
  - Four sigma-delta data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Configurable modulator clock mode supported:
  - Mode 0: Modulator clock rate equals the modulator data rate.
- Four independent, configurable secondary filter (comparator) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to detect over-value condition, under-value condition, and Threshold-crossing conditions
    1. Two independent Higher Threshold comparators (used to detect over-value condition)
    2. Two independent Lower Threshold comparators (used to detect under-value condition)
    3. One independent Threshold-Crossing comparator (used to measure duty cycle/frequency with eCAP)
  - OSR value for comparator filter unit (COSR) programmable from 1 to 32
- Four independent configurable primary filter (data filter) units per SDFM module:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - OSR value for data filter unit (DOSR) programmable from 1 to 256
  - Ability to enable or disable (or both) individual filter module
  - Ability to synchronize all four independent filters of an SDFM module by using the Master Filter Enable (MFE) bit or by using PWM signals
- Data filter output can be represented in either 16 bits or 32 bits.
- Data filter unit has a programmable mode FIFO to reduce interrupt overhead. The FIFO has the following features:
  - The primary filter (data filter) has a 16-deep x 32-bit FIFO.
  - The FIFO can interrupt the CPU after programmable number of data-ready events.
  - FIFO Wait-for-Sync feature: Ability to ignore data-ready events until the PWM synchronization signal (SDSYNC) is received. Once the SDSYNC event is received, the FIFO is populated on every data-ready event.
  - Data filter output can be represented in either 16 bits or 32 bits.
- PWMx.SOCA/SOCB can be configured to serve as SDSYNC source on a per-data-filter-channel basis.
- PWMs can be used to generate a modulator clock for sigma-delta modulators.
- Configurable Input Qualification available for both SD-Cx and SD-Dx
- Ability to use one filter channel clock (SD-C1) to provide clock to other filter clock channels.
- Configurable digital filter available on comparator filter events to blankout comparator events caused by spurious noise

---

Note

Care should be taken to avoid noise on the SDx_Cy input. If the minimum pulse width requirements are not met (for example, through a noise glitch), then the SDFM results could become undefined.

Figure 7-63 shows the SDFM block diagram.

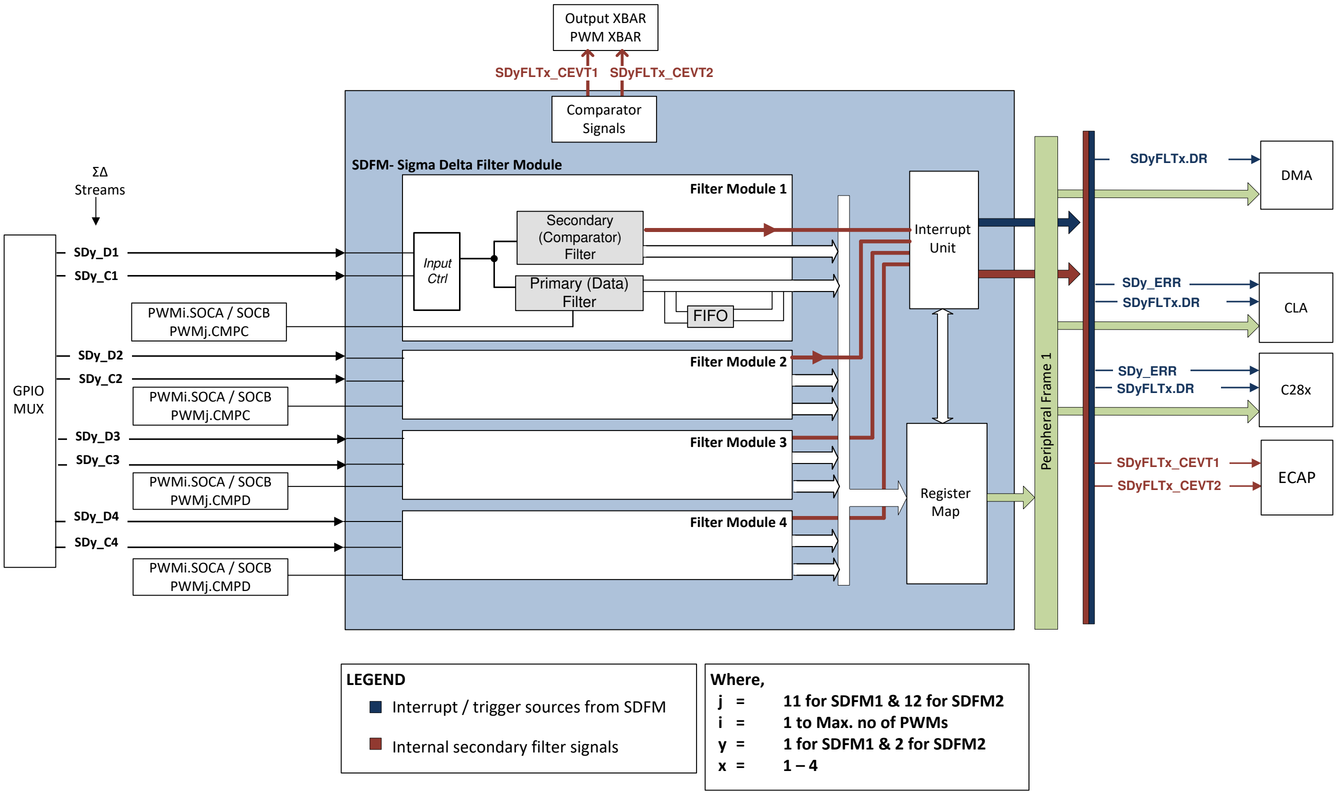


Figure 7-63. SDFM Block Diagram

7.12.5.1 SDFM Electrical Data and Timing (Using ASYNC)

Section 7.12.5.1.1 lists the SDFM timing requirements. The following configurations should be made:

- SDFM GPIO pins should be configured in ASYNC mode only (using GPYQSELn = 0b11).
- Both SDx-Cy and SDx-Dy signals need to be synchronized to PLLRAWCLK (using SDCTLPARMx registers).

Figure 7-64 shows the SDFM timing diagram.

7.12.5.1.1 SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	4 * tc(PLLRAWCLK)	256 * SYSCLK period	ns
$t_{w(SDDHL)M0}$	Pulse duration, SDx_Dy (high / Low)	2 * tc(PLLRAWCLK)		ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	1 * tc(PLLRAWCLK) + 5		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	1 * tc(PLLRAWCLK) + 5		ns

7.12.5.1.2 SDFM Timing Diagram

WARNING

Special precautions should be taken on both SD-Cx and SD-Dx signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination resistors for ringing noise due to any impedance mismatch of clock driver and spacing of traces from other noisy signals are recommended.

Note

The SDFM SD-Cx and SD-Dx signals, when synchronized to PLLRAWCLK, provide protection against SDFM module corruption due to occasional random noise glitches that may result in a false comparator trip and filter output. However, the signals do not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

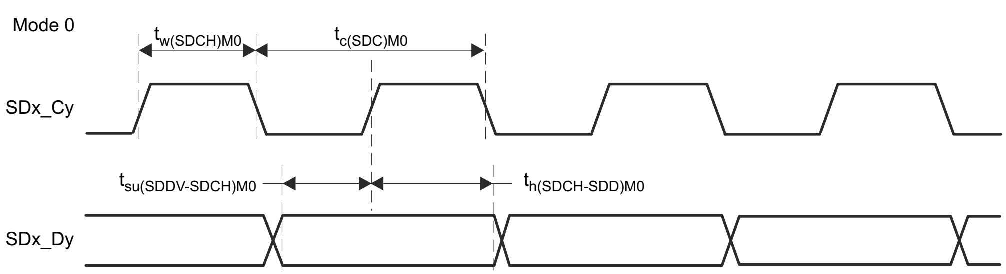


Figure 7-64. SDFM Timing Diagram – Mode 0

7.13 C28x Communications Peripherals

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

7.13.1 Controller Area Network (CAN)

This device uses the CAN IP known as DCAN.

The CAN module performs CAN protocol communication according to ISO 11898-1 (identical to Bosch® CAN protocol specification 2.0 A, B). The bit rate can be programmed to values up to 1 Mbps. A CAN transceiver chip is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message objects can be configured. The message objects and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the message handler. These functions are: acceptance filtering; the transfer of messages between the CAN Core and the Message RAM; and the handling of transmission requests as well as the generation of interrupts or DMA requests.

The register set of the CAN may be accessed directly by the CPU through the module interface. These registers are used to control and configure the CAN core and the message handler, and to access the message RAM.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (mailboxes), each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard (11-bit) or extended (29-bit) identifier
  - Supports programmable identifier receive mask
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus-on, after bus-off state by a programmable 32-bit timer
- Message-RAM parity-check mechanism
- Two interrupt lines
- DMA support

Note

For a CAN bit clock of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

Note

The accuracy of the on-chip zero-pin oscillator is in Section 7.10.3.5.1. Depending on parameters such as the CAN bit timing settings, bit rate, bus length, and propagation delay, the accuracy of this oscillator may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 7-65 shows the CAN block diagram.

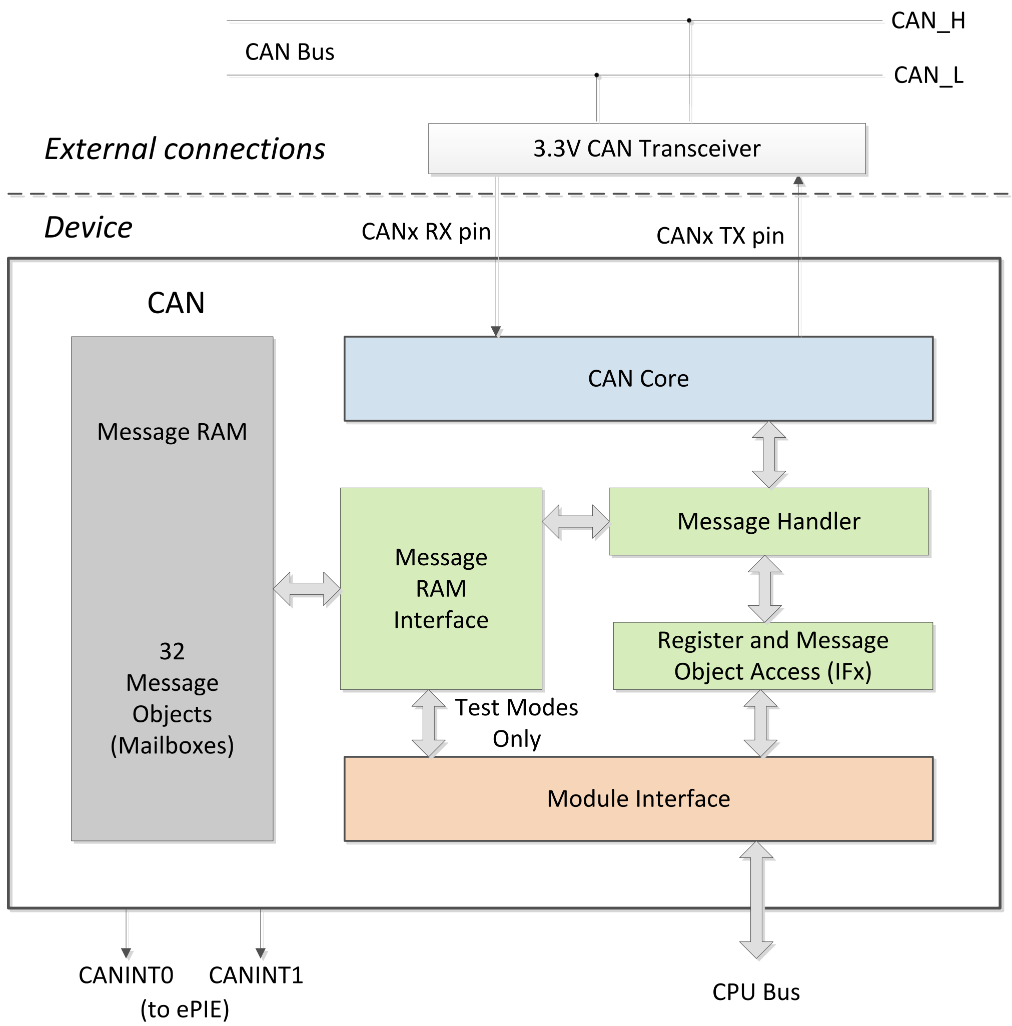


Figure 7-65. CAN Block Diagram

7.13.2 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Double data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- CLA task triggering
- SPI signaling mode (limited features available)

Operating the FSI at maximum speed (50 MHz) at dual data rate (100 Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The *Fast Serial Interface (FSI) Skew Compensation* Application Report provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in Section 7.13.2.1 and Section 7.13.2.2, respectively.

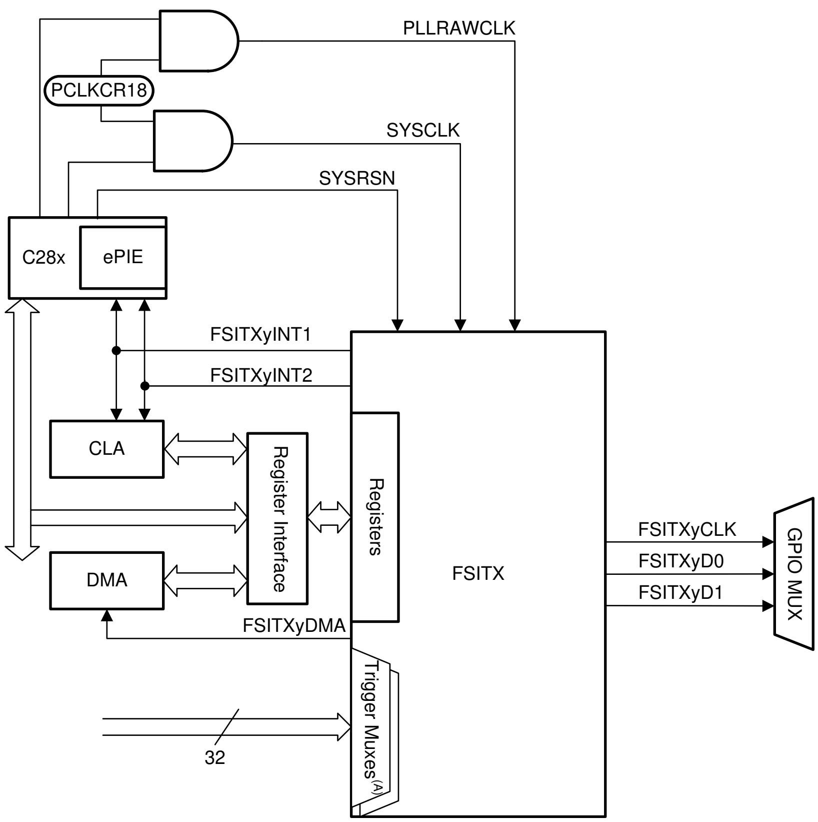
7.13.2.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU (or the CLA) program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU, CLA, and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support
- CLA task triggering

Figure 7-66 shows the FSITX CPU interface. Figure 7-67 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.



A. The signals connected to the trigger muxes are described in the External Frame Trigger Mux section of the Fast Serial Interface (FSI) chapter in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

Figure 7-66. FSITX CPU Interface

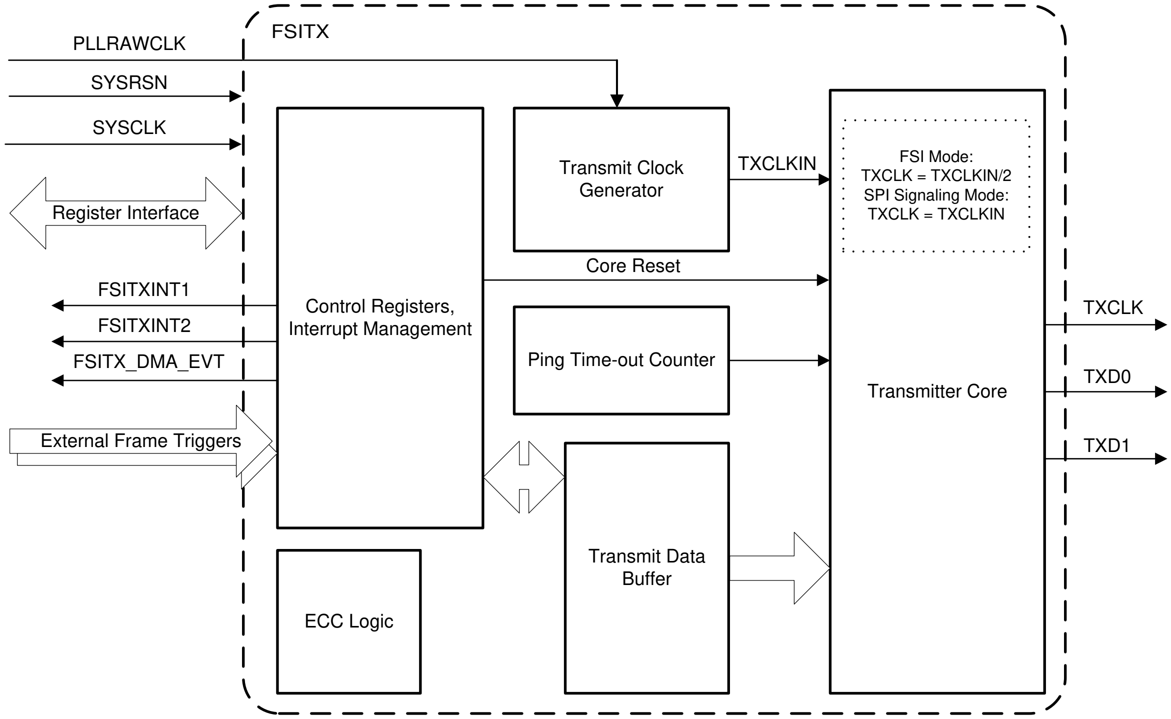


Figure 7-67. FSITX Block Diagram

7.13.2.1.1 FSITX Electrical Data and Timing

Section 7.13.2.1.1.1 lists the FSITX switching characteristics. Figure 7-68 shows the FSITX timings.

7.13.2.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	20		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) - 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLKL-TXD)}$	Delay time, Data valid after TXCLK high or low	$(0.25t_{c(TXCLK)}) - 2$	$(0.25t_{c(TXCLK)}) + 2.5$	ns

7.13.2.1.1.2 FSITX Timings

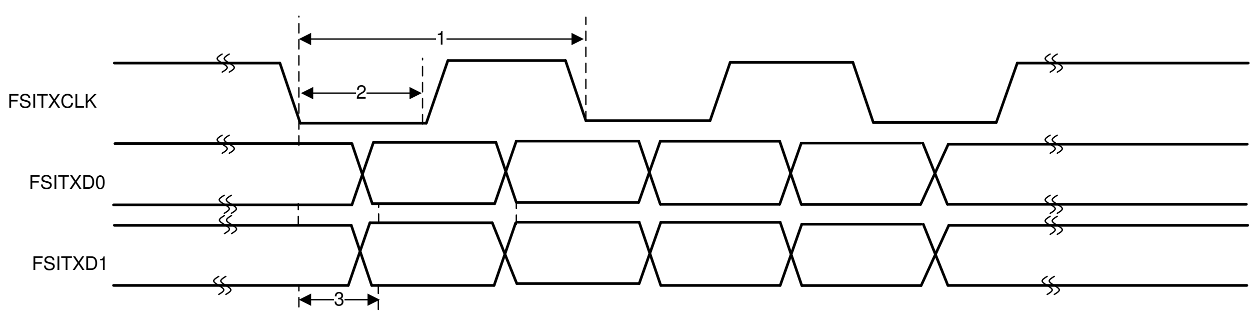


Figure 7-68. FSITX Timings

7.13.2.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK) and the data lines (RXD0 and RXD1) after they pass through the programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU (or the CLA) program, control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, CLA, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- CLA task triggering

Figure 7-69 shows the FSIRX CPU interface. Figure 7-70 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

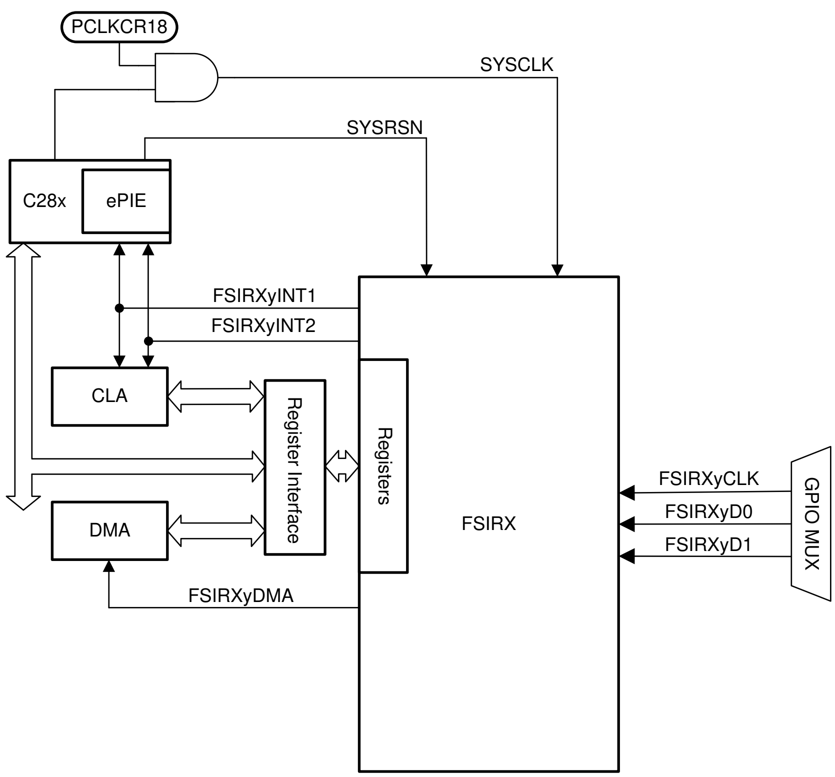


Figure 7-69. FSIRX CPU Interface

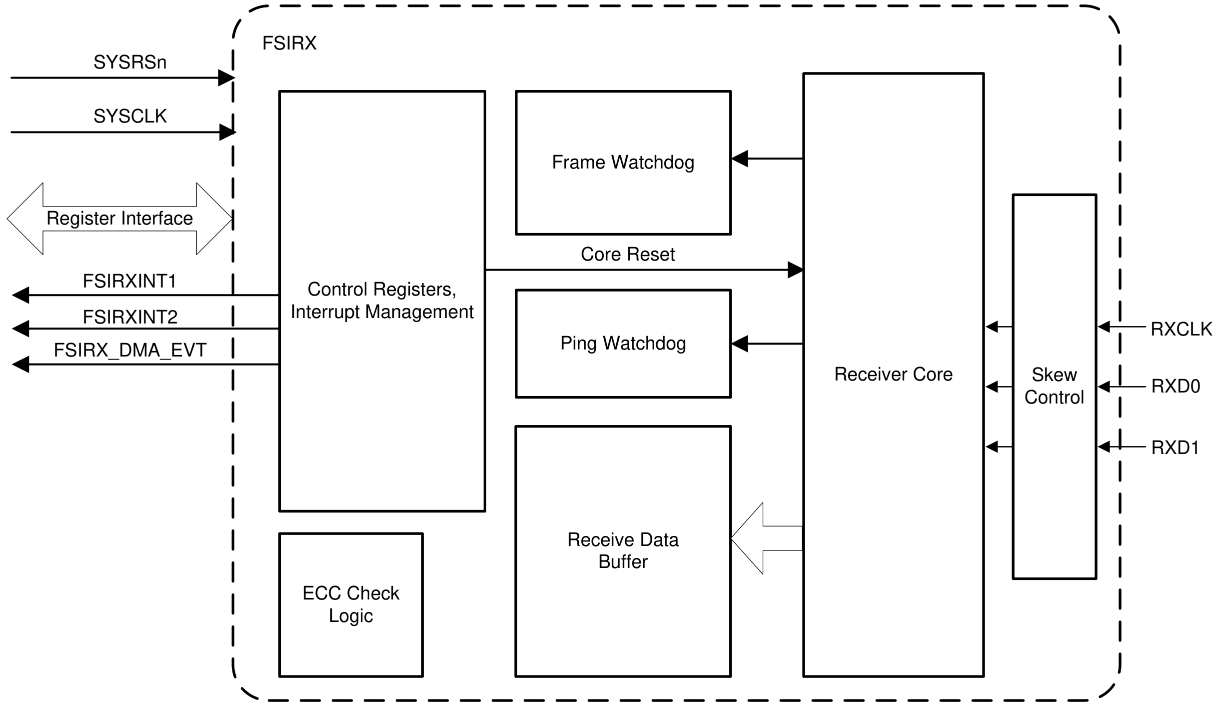


Figure 7-70. FSIRX Block Diagram

7.13.2.2.1 FSIRX Electrical Data and Timing

Section 7.13.2.2.1.1 lists the FSIRX timing requirements. Section 7.13.2.2.1.2 lists the FSIRX electrical characteristics. Figure 7-71 shows the FSIRX timings.

7.13.2.2.1.1 FSIRX Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(RXCLK)}$	Cycle time, RXCLK	20		ns
2	$t_{w(RXCLK)}$	Pulse width, RXCLK low or RXCLK high.	$(0.5t_{c(RXCLK)}) – 1$	$(0.5t_{c(RXCLK)}) + 1$	ns
3	$t_{su(RXCLK–RXD)}$	Setup time with respect to RXCLK, applies to both edges of the clock	3		ns
4	$t_{h(RXCLK–RXD)}$	Hold time with respect to RXCLK, applies to both edges of the clock	2.5		ns

7.13.2.2.1.2 FSIRX Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{d(RXCLK)}$	RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
2	$t_{d(RXD0)}$	RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31	10	30	ns
3	$t_{d(RXD1)}$	RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31	10	30	ns
4	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for RXCLK, RXD0, and RXD1	0.3	1	ns

7.13.2.2.1.3 FSIRX Timing Diagram

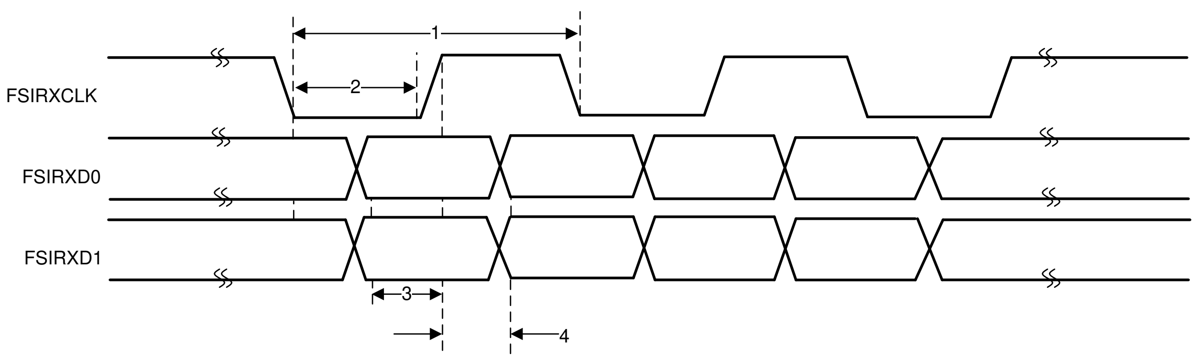


Figure 7-71. FSIRX Timings

7.13.2.3 SPI Signaling Mode

The FSI supports a SPI signaling mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of the SPI signaling mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI slave configuration because the FSI TXCLK cannot take an external clock source.

7.13.2.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Section 7.13.2.3.1.1 lists the FSITX SPI signaling mode switching characteristics. Figure 7-72 shows the FSITX SPI signaling mode timings. Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in Section 7.13.2.2.1.1 are applicable in the SPI signaling mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

7.13.2.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(TXCLK)}$	Cycle time, TXCLK	20		ns
2	$t_{w(TXCLK)}$	Pulse width, TXCLK low or TXCLK high	$(0.5t_{c(TXCLK)}) - 1$	$(0.5t_{c(TXCLK)}) + 1$	ns
3	$t_{d(TXCLKH-TXD0)}$	Delay time, TXD0 valid after TXCLK high		3	ns
4	$t_{d(TXD1-TXCLK)}$	Delay time, TXCLK high after TXD1 low	$t_{w(TXCLK)} - 3$		ns
5	$t_{d(TXCLK-TXD1)}$	Delay time, TXD1 high after TXCLK low	$t_{w(TXCLK)} - 2$		ns

7.13.2.3.1.2 FSITX SPI Signaling Mode Timings

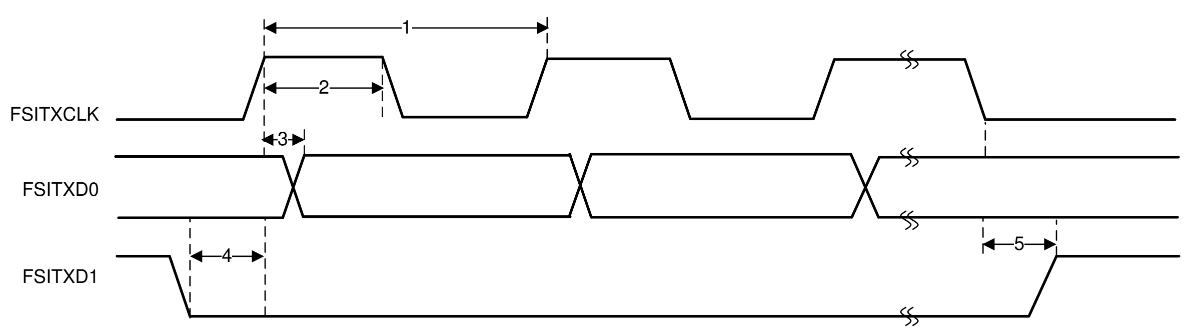


Figure 7-72. FSITX SPI Signaling Mode Timings

7.13.3 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP™ Semiconductors I2C bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate from 10 kbps up to 400 kbps (Fast-mode)
- Receive FIFO and Transmitter FIFO (16-deep x 8-bit FIFO)
- Supports two ePIE interrupts:
  - I2Cx Interrupt – Any of the below events can be configured to generate an I2Cx interrupt:
    - Transmit-data ready
    - Receive-data ready
    - Register-access ready
    - No-acknowledgment received
    - Arbitration lost
    - Stop condition detected
    - Addressed as slave
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable/disable capability
- Free data format mode

Figure 7-73 shows the I2C block diagram.

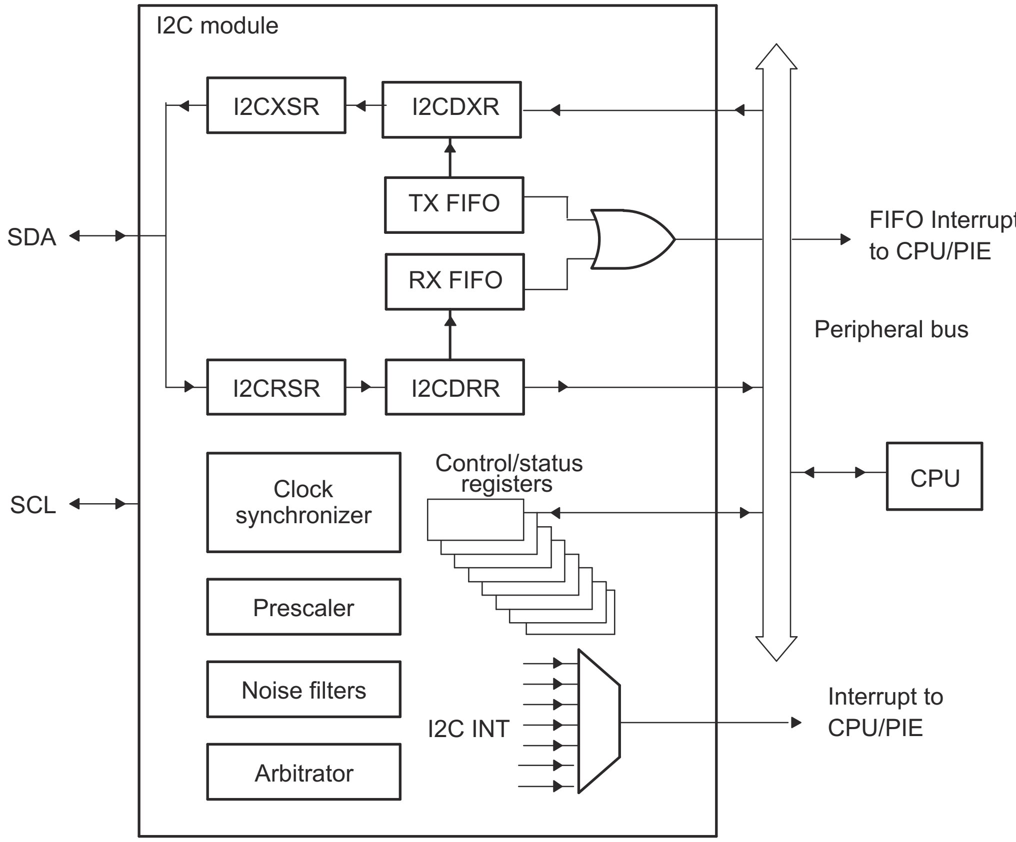


Figure 7-73. I2C Module Conceptual Block Diagram

7.13.3.1 I2C Electrical Data and Timing

Section 7.13.3.1.1 lists the I2C timing requirements. Section 7.13.3.1.2 lists the I2C switching characteristics. Figure 7-74 shows the I2C timing diagram.

Note

To meet all of the I2C protocol timing specifications, the I2C module clock (Fmod) must be configured from 7 MHz to 12 MHz.

7.13.3.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.7		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

7.13.3.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA

7.13.3.1.3 I2C Timing Diagram

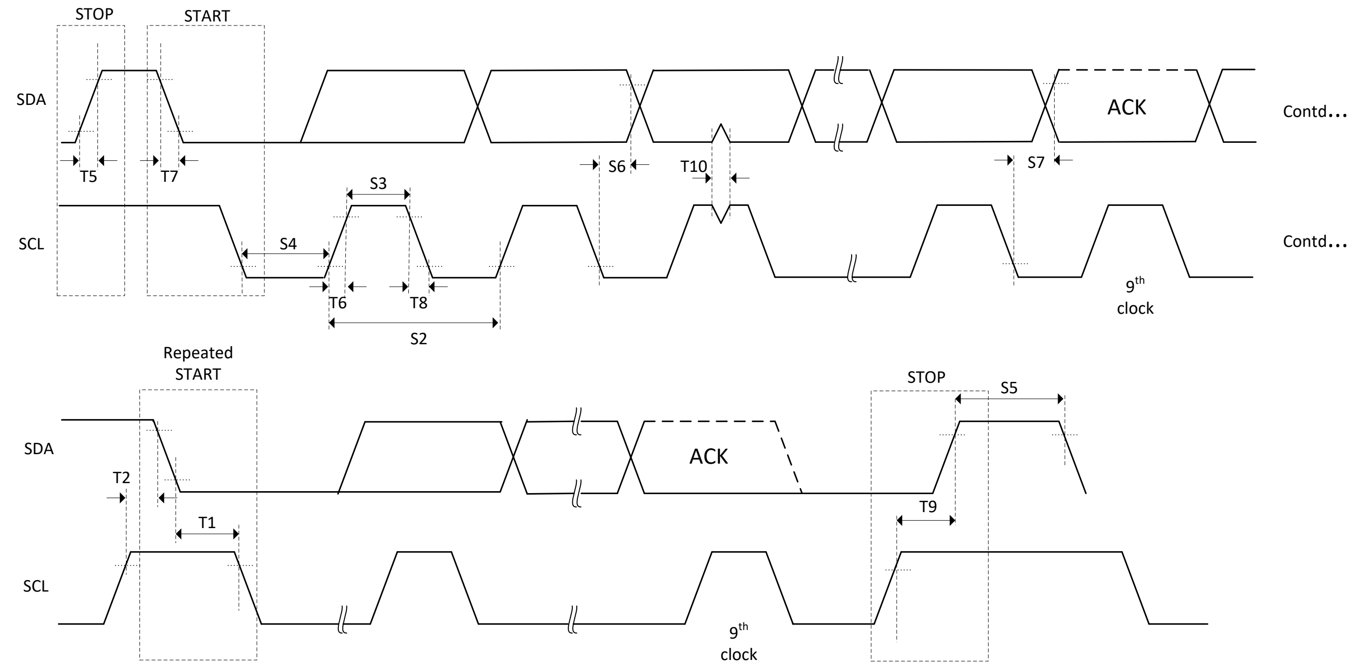


Figure 7-74. I2C Timing Diagram

7.13.4 Multichannel Buffered Serial Port (McBSP)

The McBSPs feature:

- Full-duplex communication
- Double-buffered transmission and triple-buffered reception, allowing a continuous data stream
- Independent clocking and framing for reception and transmission
- The capability to send interrupts to the CPU and to send DMA events to the DMA controller
- 128 channels for transmission and reception
- Multichannel selection modes that enable or disable block transfers in each of the channels
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected A/D and D/A devices
- Support for external generation of clock signals and frame-synchronization signals
- A programmable sample rate generator for internal generation and control of clock signals and frame-synchronization signals
- Programmable polarity for frame-synchronization pulses and clock signals
- Direct interface to:
  - T1/E1 framers
  - IOM-2 compliant devices
  - AC97-compliant devices (the necessary multiphase frame capability is provided)
  - I2S compliant devices
  - SPI devices
- A wide selection of data sizes: 8, 12, 16, 20, 24, and 32 bits

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Note

A value of the chosen data size is referred to as a *serial word* or *word* throughout the McBSP documentation. Elsewhere, *word* is used to describe a 16-bit value.

- μ-law and A-law companding
- The option of transmitting/receiving 8-bit data with the LSB first
- Status bits for flagging exception/error conditions
- ABIS mode is not supported

Figure 7-75 shows the block diagram of the McBSP module.

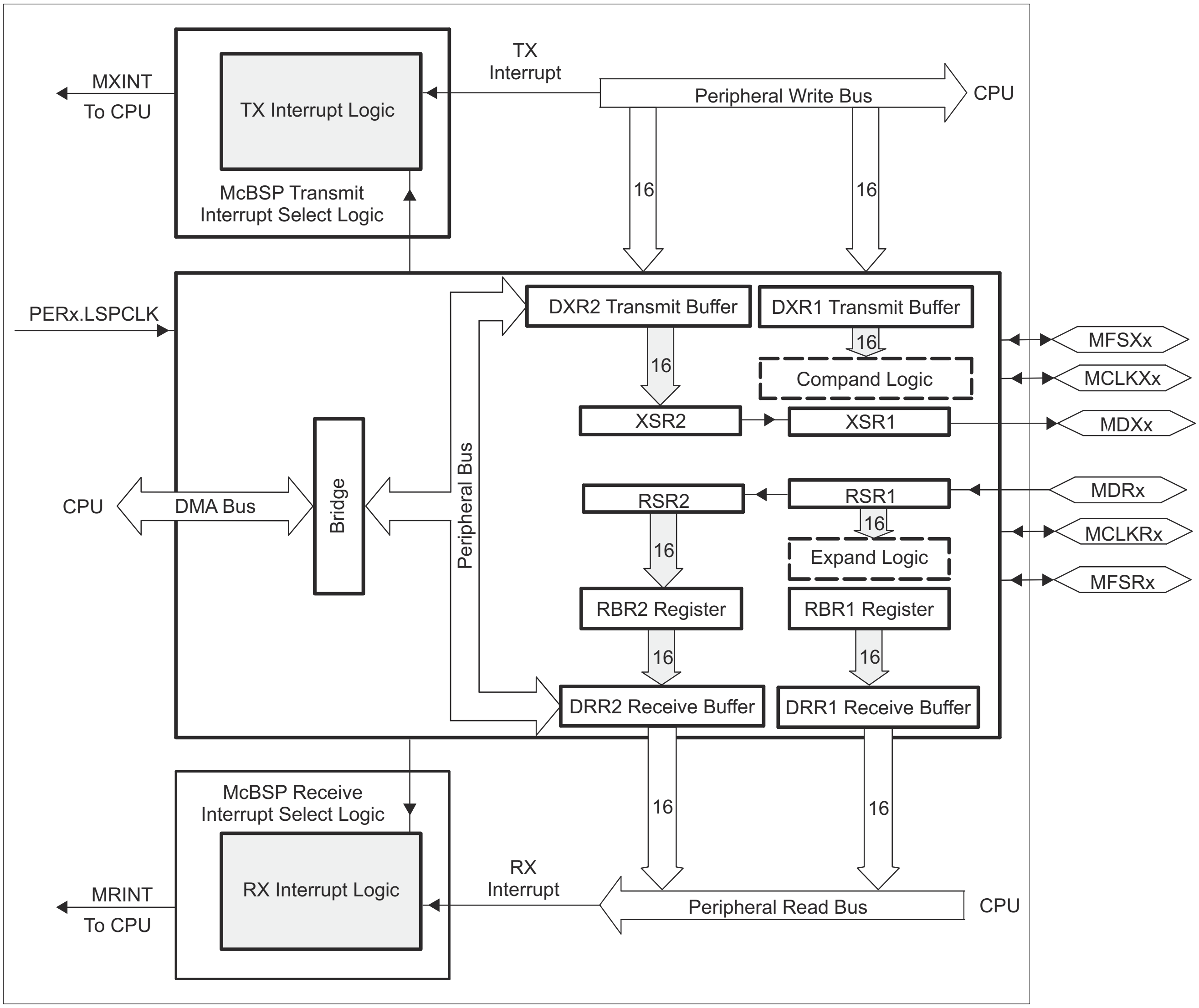


Figure 7-75. McBSP Block Diagram

7.13.4.1 McBSP Electrical Data and Timing

7.13.4.1.1 McBSP Transmit and Receive Timing

Section 7.13.4.1.1.1 lists the McBSP timing requirements:

- Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = CLKSRG / (1 + CLKGDV). CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLK/2).

Section 7.13.4.1.1.2 lists the McBSP switching characteristics:

- Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
- 2P = 1/CLKG in ns.

Figure 7-76 and Figure 7-77 show the McBSP timing diagrams.

7.13.4.1.1.1 McBSP Timing Requirements

NO.				MIN	MAX	UNIT
		McBSP module clock (CLKG, CLKX, CLKR) range		1		kHz
					25	MHz
		McBSP module cycle time (CLKG, CLKX, CLKR) range		40		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P – 7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	21		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	21		ns
			CLKR ext	5		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	3		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	21		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

7.13.4.1.1.2 McBSP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D – 5 (1)	D + 5 (1)	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C – 5 (1)	C + 5 (1)	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	–3	4	ns
				CLKR ext	3	27	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	–3	4	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int	–8	8	ns
				CLKX ext	4	25	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid.		CLKX int	–3	5	ns
		This applies to all bits except the first bit transmitted.		CLKX ext	7	25	
		Delay time, CLKX high to DX valid	DXENA = 0	CLKX int	–3	5	
				CLKX ext	7	25	
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P – 3	P + 5	
				CLKX ext	P + 7	P + 25	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven	DXENA = 0	CLKX int	–8		ns
				CLKX ext	5		
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P – 8		
				CLKX ext	P + 5		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid	DXENA = 0	FSX int		8	ns
				FSX ext		18.5	
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 1	FSX int		P + 8	
				FSX ext		P + 18.5	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven	DXENA = 0	FSX int	–2		ns
				FSX ext	6		
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 1	FSX int	P – 2		
				FSX ext	P + 6		

(1) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

7.13.4.1.1.3 McBSP Receive and Transmit Timing Diagrams

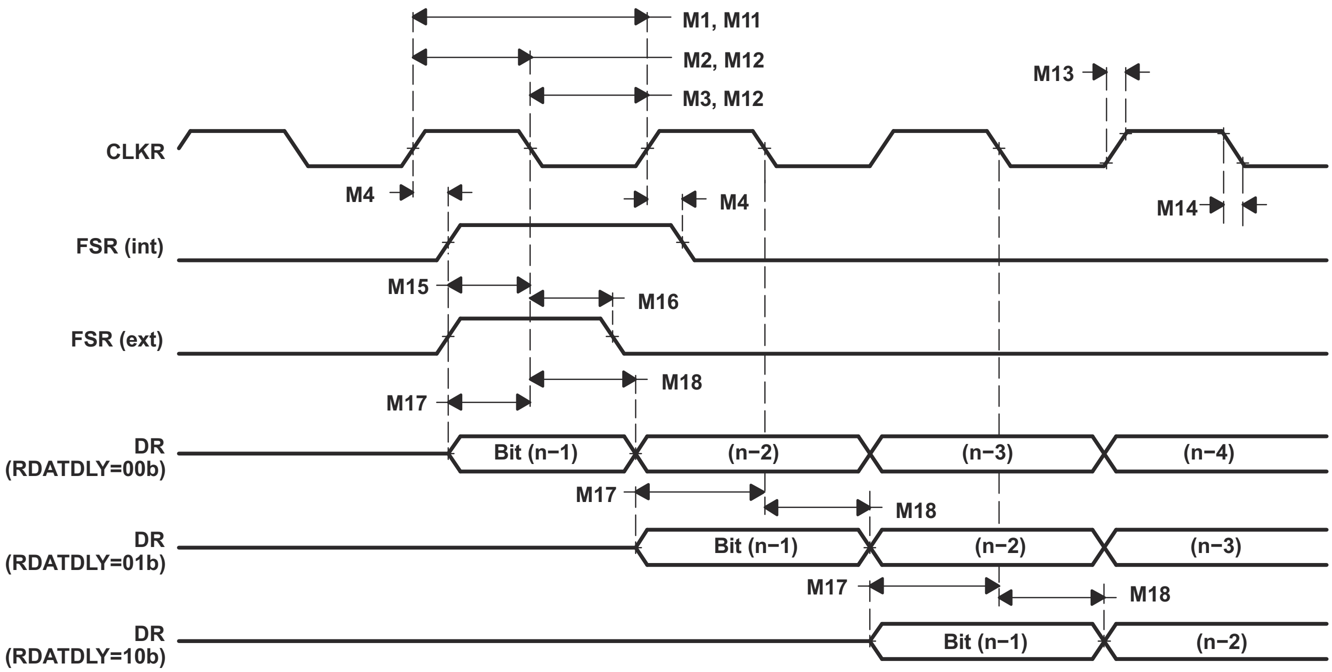


Figure 7-76. McBSP Receive Timing

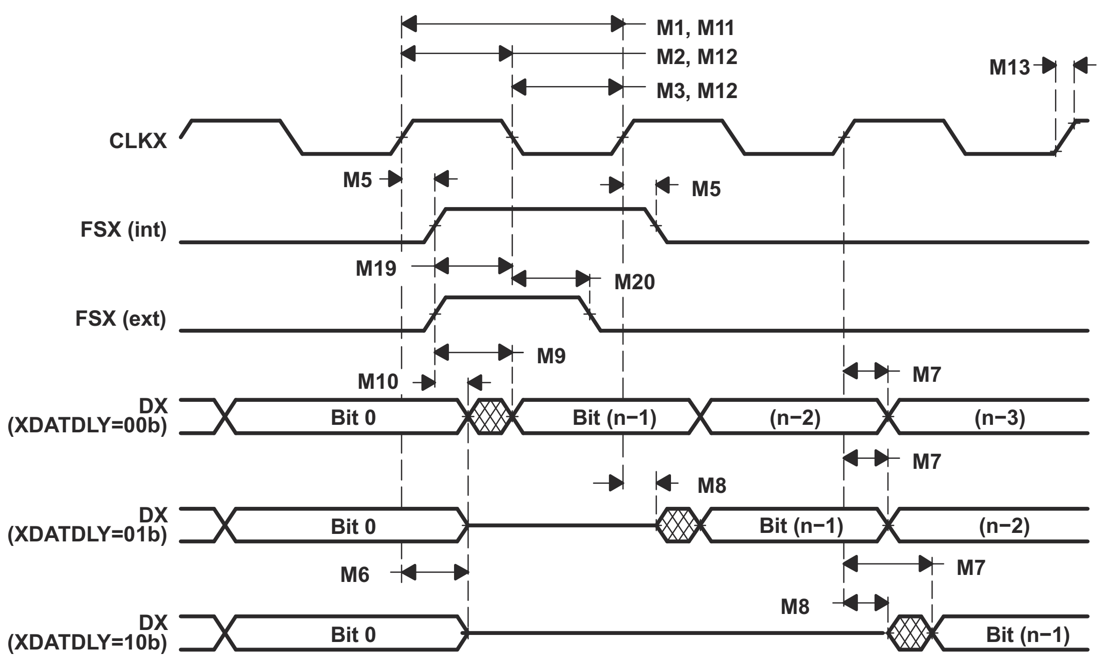


Figure 7-77. McBSP Transmit Timing

7.13.4.1.2 McBSP as SPI Master or Slave Timing

Section 7.13.4.1.2.1 lists the McBSP as SPI master timing requirements. Section 7.13.4.1.2.2 lists the McBSP as SPI master switching characteristics. Section 7.13.4.1.2.3 lists the McBSP as SPI slave timing requirements. Section 7.13.4.1.2.4 lists the McBSP as SPI slave switching characteristics.

Figure 7-78 through Figure 7-81 show the McBSP as SPI master or slave timing diagrams.

7.13.4.1.2.1 McBSP as SPI Master Timing Requirements

NO.			MIN	MAX	UNIT
CLOCK					
	$t_{c(CLKG)}$	Cycle time, CLKG(1)	$2 * t_{c(LSPCLK)}$		ns
	P	Cycle time, LSPCLK(1)	$t_{c(LSPCLK)}$		ns
M33, M42, M52, M61	$t_{c(CKX)}$	Cycle time, CLKX	2P		ns
CLKSTP = 10b, CLKXP = 0					
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		ns
CLKSTP = 11b, CLKXP = 0					
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		ns
CLKSTP = 10b, CLKXP = 1					
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		ns
CLKSTP = 11b, CLKXP = 1					
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		ns

(1) CLKG should be configured to LSPCLK/2 by setting CLKSM = 1 and CLKGDV = 1

7.13.4.1.2.2 McBSP as SPI Master Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
CLOCK						
M33	$t_{c(CLKG)}$	Cycle time, CLKG[(1)] (n * $t_{c(LSPCLK)}$)	40			ns
	P	Half CLKG cycle; 0.5 * $t_{c(CLKG)}$	20			ns
	n	LSPCLK to CLKG divider	2			ns
CLKSTP = 10b, CLKXP = 0						
M24	$t_{h(CKXL-FXL)}$	Hold time, FSX high after CLKX low	2P – 4			ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P - 4			ns
M26	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–3		5	ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P – 8			ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	P – 3		P + 6	ns
CLKSTP = 11b, CLKXP = 0						
M34	$t_{h(CKXL-FXH)}$	Hold time, FSX high after CLKX low	P – 4			ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	2P – 4			ns
M36	$t_{d(CLKXL-DXV)}$	Delay time, CLKX low to DX valid	–3		5	ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P – 8			ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	–3		5	ns
CLKSTP = 10b, CLKXP = 1						
M43	$t_{h(CKXH-FXH)}$	Hold time, FSX high after CLKX high	2P – 4			ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	P – 4			ns
M45	$t_{d(CLKXL-DXV)}$	Delay time, CLKX low to DX valid	–3		5	ns
M47	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P – 8			ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	–3		5	ns
CLKSTP = 11b, CLKXP = 1						
M53	$t_{h(CKXH-FXH)}$	Hold time, FSX high after CLKX high	P – 4			ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	2P – 4			ns
M55	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–3		5	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P – 8			ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	–3		5	ns

(1) CLKG should be configured to LSPCLK/2 by setting CLKSM = 1 and CLKGDV = 1.

7.13.4.1.2.3 McBSP as SPI Slave Timing Requirements

NO.			MIN	MAX	UNIT
CLOCK					
	$t_{c(CLKG)}$	Cycle time, CLKG(1)	2 * $t_{c(LSPCLK)}$		ns
	P	Cycle time, LSPCLK(1)	$t_{c(LSPCLK)}$		ns
M33, M42, M52, M61	$t_{c(CKX)}$	Cycle time, CLKX(2)	16P		ns
CLKSTP = 10b, CLKXP = 0					
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	8P – 10		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	8P – 10		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high	8P+10		ns
CLKSTP = 11b, CLKXP = 0					
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	8P – 10		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	8P – 10		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high	16P+10		ns
CLKSTP = 10b, CLKXP = 1					
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	8P – 10		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	8P – 10		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low	8P+10		ns
CLKSTP = 11b, CLKXP = 1					
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	8P – 10		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	8P – 10		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low	16P+10		ns

(1) CLKG should be configured to LSPCLK/2 by setting CLKSM = 1 and CLKGDV = 1
(2) For SPI slave modes CLKX must be a minimum of 8 CLKG cycles

7.13.4.1.2.4 McBSP as SPI Slave Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
CLOCK						
	2P	Cycle time, CLKG				ns
CLKSTP = 10b, CLKXP = 0						
M26	$t_{d(CLKXH\text{-}DXV)}$	Delay time, CLKX high to DX valid	3P+6		5P+20	ns
M28	$t_{dis(CKXL\text{-}DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	6P+6			ns
M29	$t_{d(FXL\text{-}DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns
CLKSTP = 11b, CLKXP = 0						
M36	$t_{d(CLKXL\text{-}DXV)}$	Delay time, CLKX low to DX valid	3P+6		5P+20	ns
M37	$t_{dis(CKXL\text{-}DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	7P+6			ns
M38	$t_{d(FXL\text{-}DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns
CLKSTP = 10b, CLKXP = 1						
M45	$t_{d(CLKXL\text{-}DXV)}$	Delay time, CLKX low to DX valid	3P+6		5P+20	ns
M47	$t_{dis(CLKXH\text{-}DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	6P+6			ns
M48	$t_{d(FXL\text{-}DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns
CLKSTP = 11b, CLKXP = 1						
M55	$t_{d(CLKXH\text{-}DXV)}$	Delay time, CLKX high to DX valid	3P+6		5P + 20	ns
M56	$t_{dis(CKXH\text{-}DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	7P + 6			ns
M57	$t_{d(FXL\text{-}DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns

7.13.4.1.2.5 McBSP as SPI Master or Slave Timing Diagrams

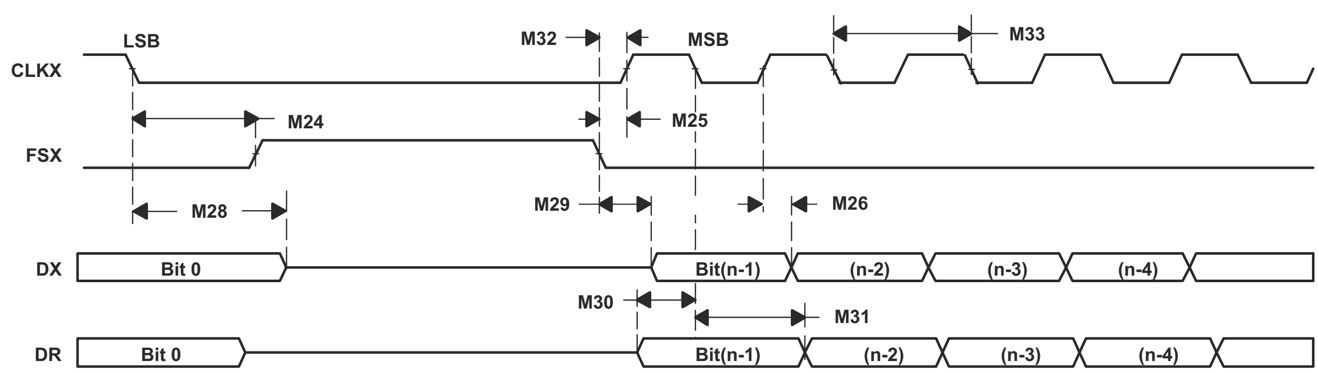


Figure 7-78. McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

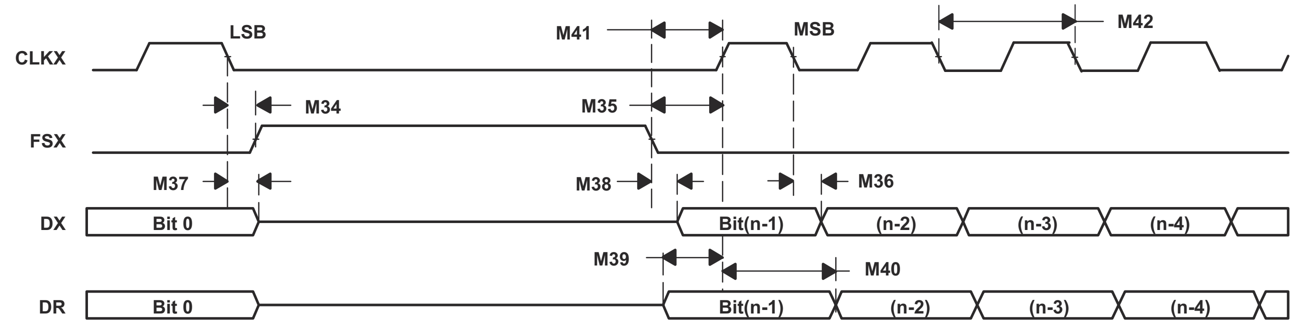


Figure 7-79. McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

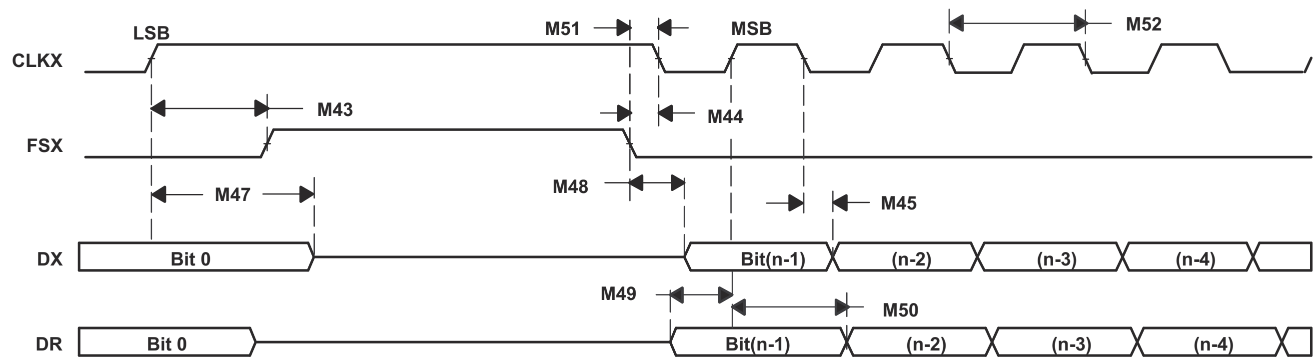


Figure 7-80. McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

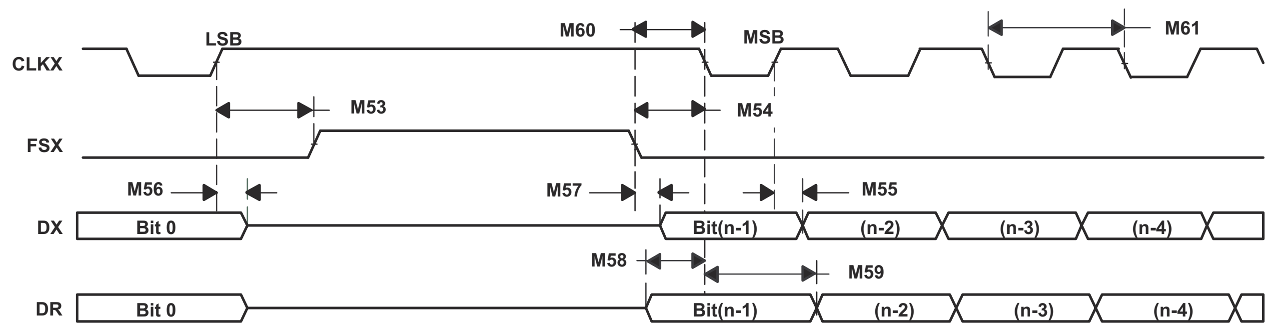


Figure 7-81. McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

7.13.5 Power Management Bus (PMBus)

The PMBus module provides an interface between the microcontroller and devices compliant with the SMI Forum PMBus Specification Part I version 1.0 and Part II version 1.1. PMBus is based on SMBus, which uses a similar physical layer to I2C.

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Support for master and slave modes
- Support for two speeds:
  - Standard Mode: Up to 100 kHz
  - Fast Mode: Up to 400 kHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
  - Receive data ready
  - Transmit buffer empty
  - Slave address received
  - End of message
  - ALERT input asserted
  - Clock low time-out
  - Clock high time-out
  - Bus free

Figure 7-82 shows the PMBus block diagram.

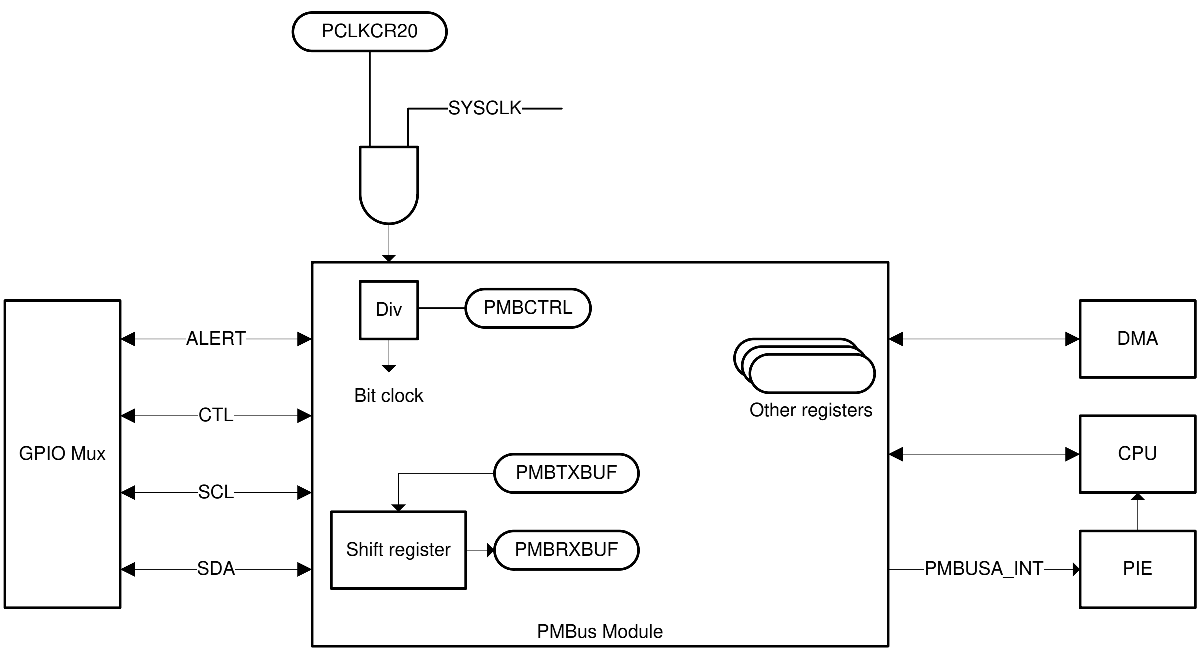


Figure 7-82. PMBus Block Diagram

7.13.5.1 PMBus Electrical Data and Timing

7.13.5.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Valid low-level input voltage				0.8	V
V_{IH}	Valid high-level input voltage		2.1		VDDIO	V
V_{OL}	Low-level output voltage	At I_{pullup} = 4 mA			0.4	V
I_{OL}	Low-level output current	V_{OL} ≤ 0.4 V	4			mA
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0		50	ns
I_i	Input leakage current on each pin	0.1 Vbus < Vi < 0.9 Vbus	–10		10	µA
C_i	Capacitance on each pin				10	pF

7.13.5.1.2 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{mod}	PMBus Module Clock Frequency		f(SYSCLK) /32		10	MHz
f_{SCL}	SCL clock frequency		10		400	kHz
t_{BUF}	Bus free time between STOP and START conditions		1.3			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		0.6			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		0.6			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		0.6			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
$t_{SU;DAT}$	Data setup time before SCL rise		100			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		1.3			µs
t_{HIGH}	High period of the SCL clock		0.6		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (slave device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (master device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL	5% to 95%	20		300	ns
t_f	Fall time of SDA and SCL	95% to 5%	20		300	ns

7.13.5.1.3 PMBus Standard Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{mod}	PMBus Module Clock Frequency		f(SYSCLK) /32		10	MHz
f_{SCL}	SCL clock frequency		10		100	kHz
t_{BUF}	Bus free time between STOP and START conditions		4.7			µs
$t_{HD;STA}$	START condition hold time -- SDA fall to SCL fall delay		4			µs
$t_{SU;STA}$	Repeated START setup time -- SCL rise to SDA fall delay		4.7			µs
$t_{SU;STO}$	STOP condition setup time -- SCL rise to SDA rise delay		4			µs
$t_{HD;DAT}$	Data hold time after SCL fall		300			ns
$t_{SU;DAT}$	Data setup time before SCL rise		250			ns
$t_{Timeout}$	Clock low time-out		25		35	ms
t_{LOW}	Low period of the SCL clock		4.7			µs
t_{HIGH}	High period of the SCL clock		4		50	µs
$t_{LOW;SEXT}$	Cumulative clock low extend time (slave device)	From START to STOP			25	ms
$t_{LOW;MEXT}$	Cumulative clock low extend time (master device)	Within each byte			10	ms
t_r	Rise time of SDA and SCL				1000	ns
t_f	Fall time of SDA and SCL				300	ns

7.13.6 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register. Figure 7-83 shows the SCI block diagram.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
  - Baud rate programmable to 64K different rates
- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wakeup multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

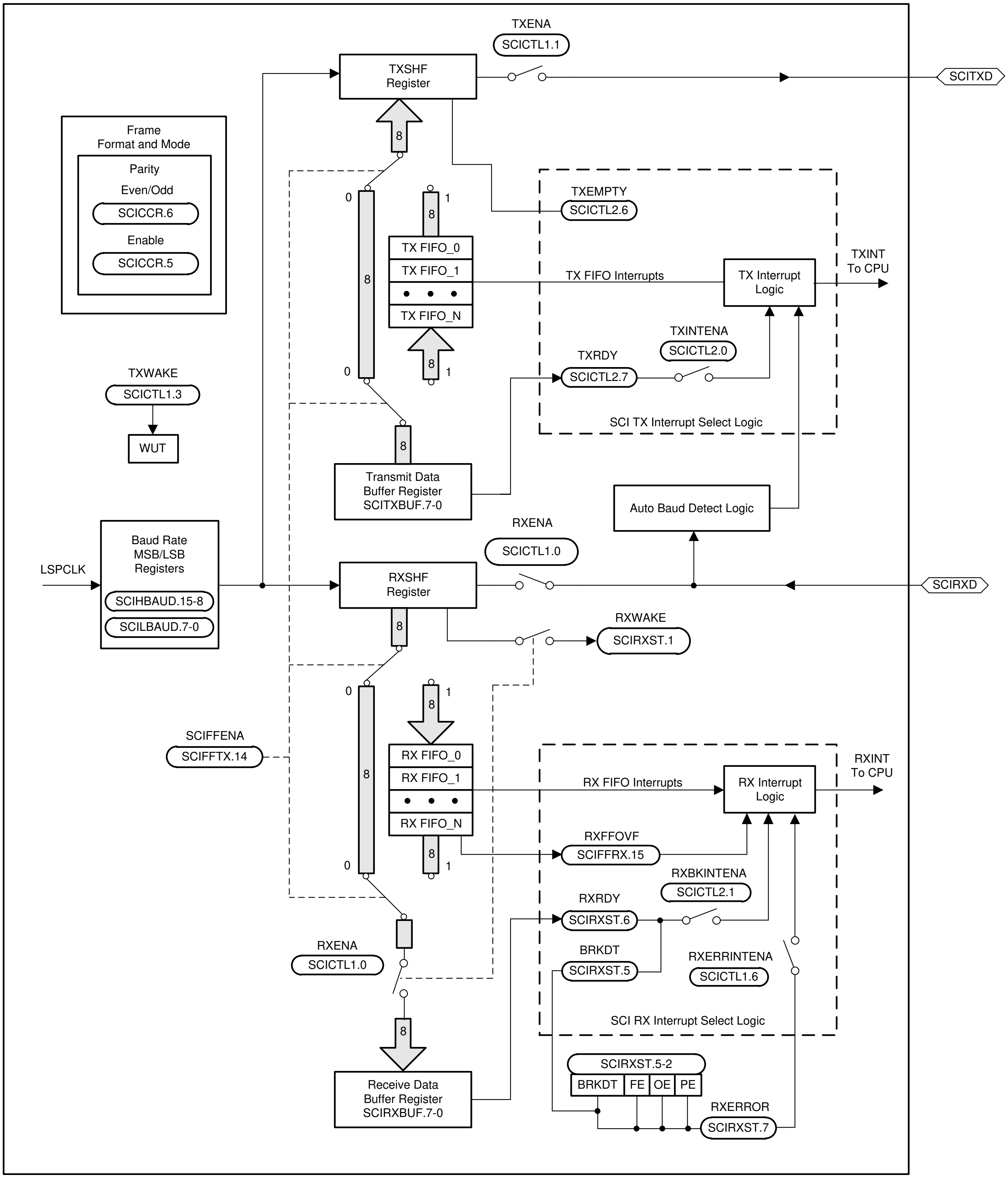


Figure 7-83. SCI Block Diagram

7.13.7 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The port supports 16-level receive and transmit FIFOs for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules
- DMA support
- High-speed mode for up to 50-MHz full-duplex communication

Figure 7-84 shows the SPI CPU Interface.

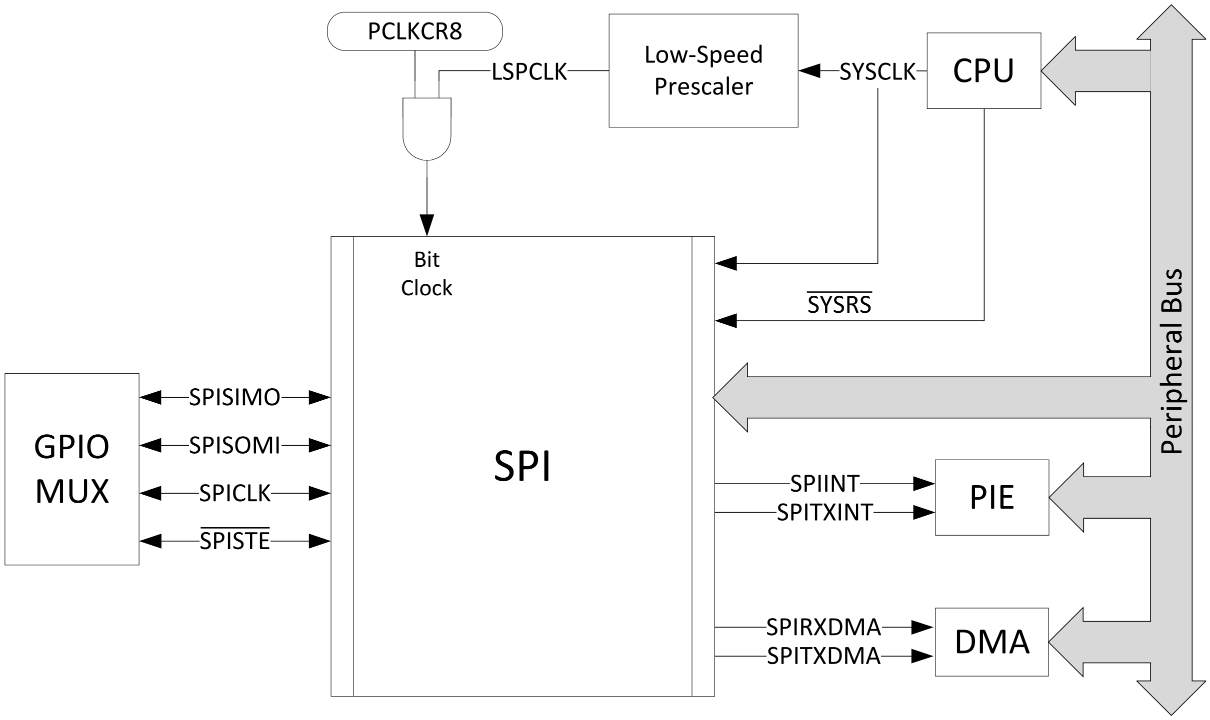


Figure 7-84. SPI CPU Interface

7.13.7.1 SPI Electrical Data and Timing

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

To use the SPI in High-Speed mode, the application must use the high-speed enabled GPIOs (see Section 6.5.5).

7.13.7.1.1 SPI Master Mode Timings

Section 7.13.7.1.1.1 lists the SPI master mode timing requirements. Section 7.13.7.1.1.2 lists the SPI master mode switching characteristics (clock phase = 0). Section 7.13.7.1.1.3 lists the SPI master mode switching characteristics (clock phase = 1). Figure 7-85 shows the SPI master mode external timing where the clock phase = 0. Figure 7-86 shows the SPI master mode external timing where the clock phase = 1.

7.13.7.1.1.1 SPI Master Mode Timing Requirements

NO.			(BRR + 1) CONDITION[(1)]	MIN	MAX	UNIT
High-Speed Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	5		ns
Normal Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	20		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

7.13.7.1.1.2 SPI Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION[1]	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	Even	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
			Odd	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$	
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{\text{SPISTE}}$ inactive	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
High-Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		1	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		5	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

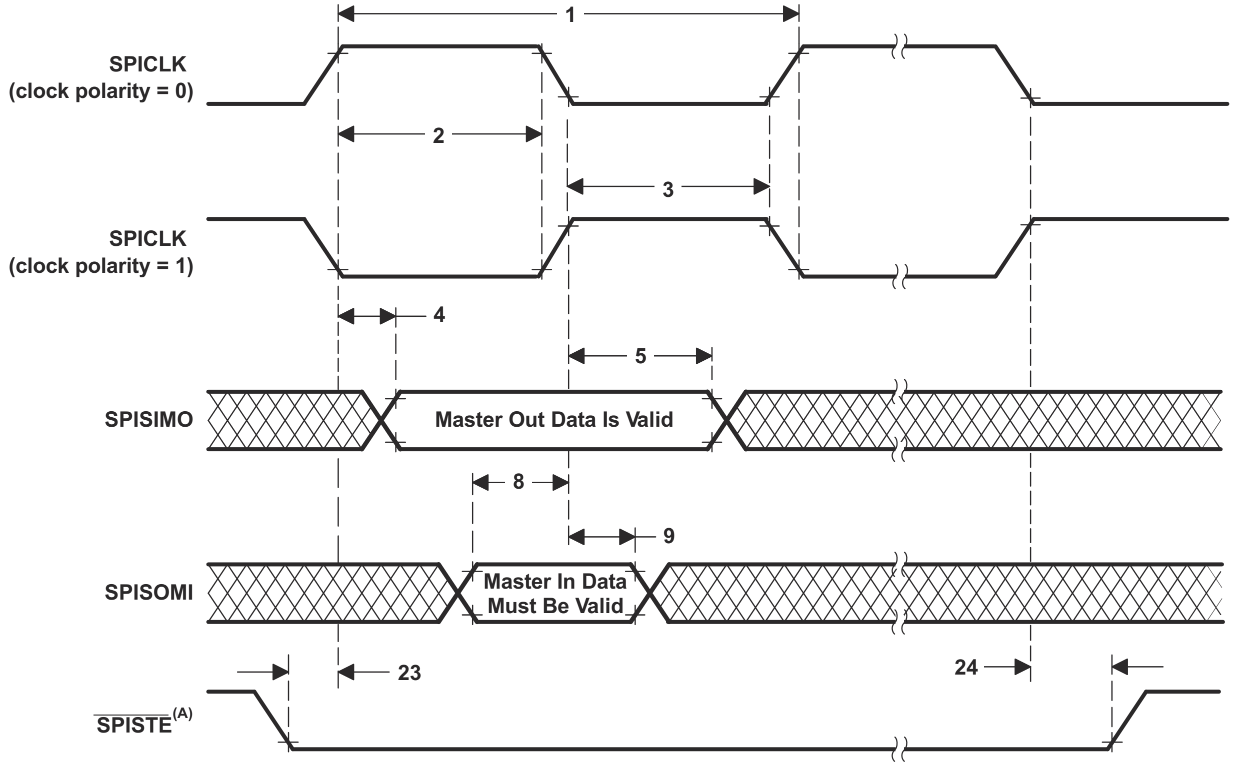
7.13.7.1.1.3 SPI Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ valid to SPICLK	Even, Odd	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{\text{SPISTE}}$ invalid	Even	– 3	+3	ns
			Odd	– 3	+3	
High-Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 5$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 5$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

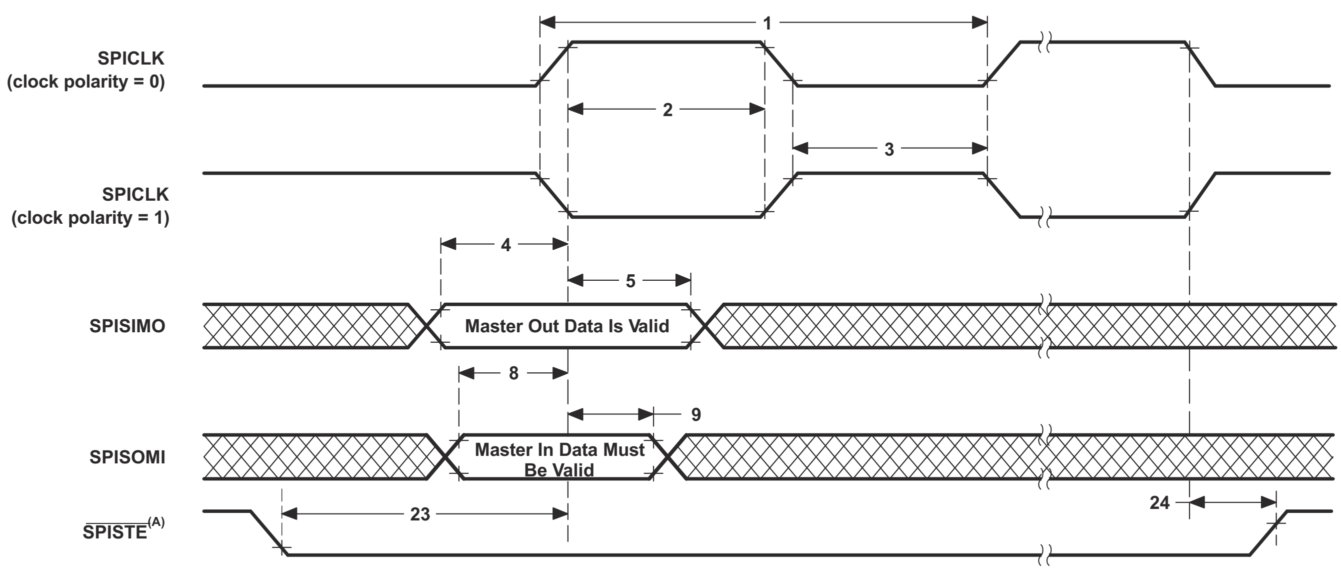
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

7.13.7.1.1.4 SPI Master Mode External Timing



A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 7-85. SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, SPISTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 7-86. SPI Master Mode External Timing (Clock Phase = 1)

7.13.7.1.2 SPI Slave Mode Timings

Section 7.13.7.1.2.1 lists the SPI slave mode timing requirements. Section 7.13.7.1.2.2 lists the SPI slave mode switching characteristics. Figure 7-87 shows the SPI slave mode external timing where the clock phase = 0. Figure 7-88 shows the SPI slave mode external timing where the clock phase = 1.

7.13.7.1.2.1 SPI Slave Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} - 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 11$		ns
		Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 20$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

7.13.7.1.2.2 SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
High-Speed Mode					
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		9	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns
Normal Mode					
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		20	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns

7.13.7.1.2.3 SPI Slave Mode External Timing

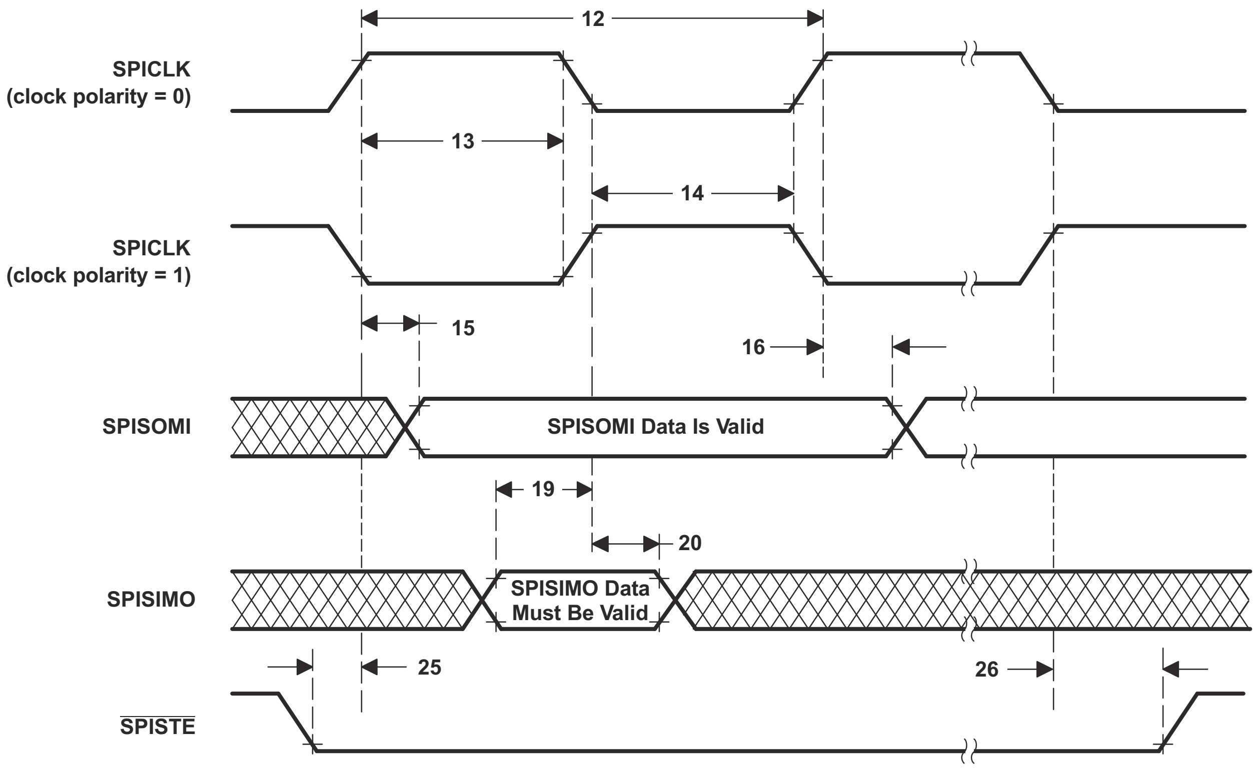


Figure 7-87. SPI Slave Mode External Timing (Clock Phase = 0)

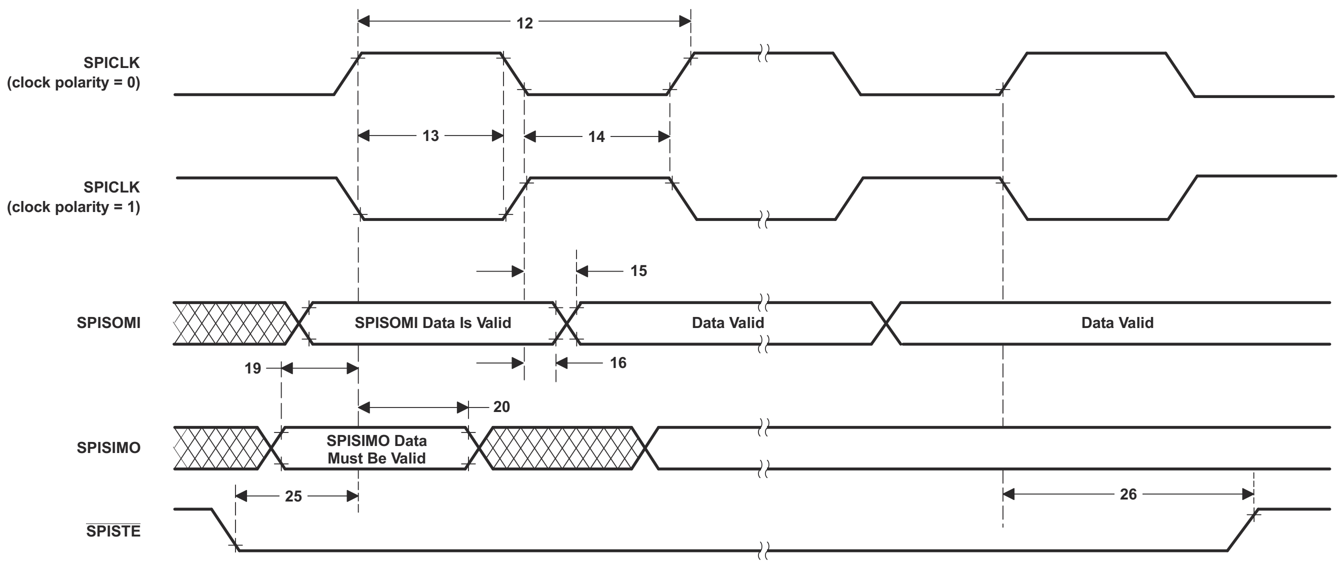


Figure 7-88. SPI Slave Mode External Timing (Clock Phase = 1)

7.13.8 EtherCAT Slave Controller (ESC)

Ethernet for Control Automation Technology (EtherCAT®) is an Ethernet-based fieldbus system, invented by Beckhoff Automation and is standardized in IEC 61158. All the slave nodes connected to the bus interpret, process, and modify the data addressed to them quickly, without having to buffer the frame inside the node. This real-time behavior, frame processing, and forwarding requirements are implemented by the EtherCAT slave controller (ESC) hardware. EtherCAT does not require software interaction for data transmission inside the slaves. EtherCAT only defines the MAC layer while the higher-layer protocols and stack are implemented in software on the microcontrollers connected to the ESC.

The EtherCAT:

- Involves master and slave(s) setup where slave nodes are physically connected daisy-chain style but logically operate on a loop
- Specializes in precise, low-jitter synchronization across slave nodes
- Uses IEEE 802.3 Ethernet physical layer and standard Ethernet frames

7.13.8.1 ESC Features

The ESC on this MCU provides the following functionality:

- Up to 2 MII ports to connect to EtherCAT PHYs
- Process data interface through 16-bit asynchronous interface
- 64-bit distributed clocking
  - Sync output signals to synchronize device events and latch input signals supporting time-stamping for events
  - Distributed clock features of SYNC0/1 (o/ps) and LATCH0/1 able to synchronize GPIOs and allow inputs from any GPIOs as well as other muxing options for internal device events
- 8 Field bus Memory Management Units (FMMUs)
  - Support all native types of RD/, WR/, RDWR, and built-in features of bit- and byte-addressing
- 8 Sync Managers
- I2C EEPROM interface
- Up-to 32 general-purpose inputs (GPIs) and 32 general-purpose outputs (GPOs)
- 2 SYNC and 2 LATCH signals connected to GPIO pads
- 16KB RAM with parity

7.13.8.2 ESC Subsystem Integrated Features

In addition to the ESC features, the following are the device-specific features provided by the integration of the ESC and the MCU:

- ESC access allocation to either the CM subsystem or CPU1 subsystem during initialization
- EtherCAT reset request from master can be routed to NMI or general interrupt controller on MCU
- RAM Parity error routed to NMI on MCU
- DMA access to EtherCAT RAM
- Up to 32 GPIs and up to 32 GPOs feature integrated to 16-bit ASYNC PDI interface
- Interface to CLB
- Distributed clock feature of SYNC0/1 able to synchronize PWMs, generate interrupt/DMA requests, or trigger eCAP capture to allow external component action through GPIO access.
- EtherCAT SYNC0/1 pulse can trigger a CLA task.
- Distributed clock feature of LATCH0/1 allows inputs from any GPIO or PWM crossbar triggers

7.13.8.3 EtherCAT IP Block Diagram

Figure 7-89 shows the general functionality of EtherCAT IP.

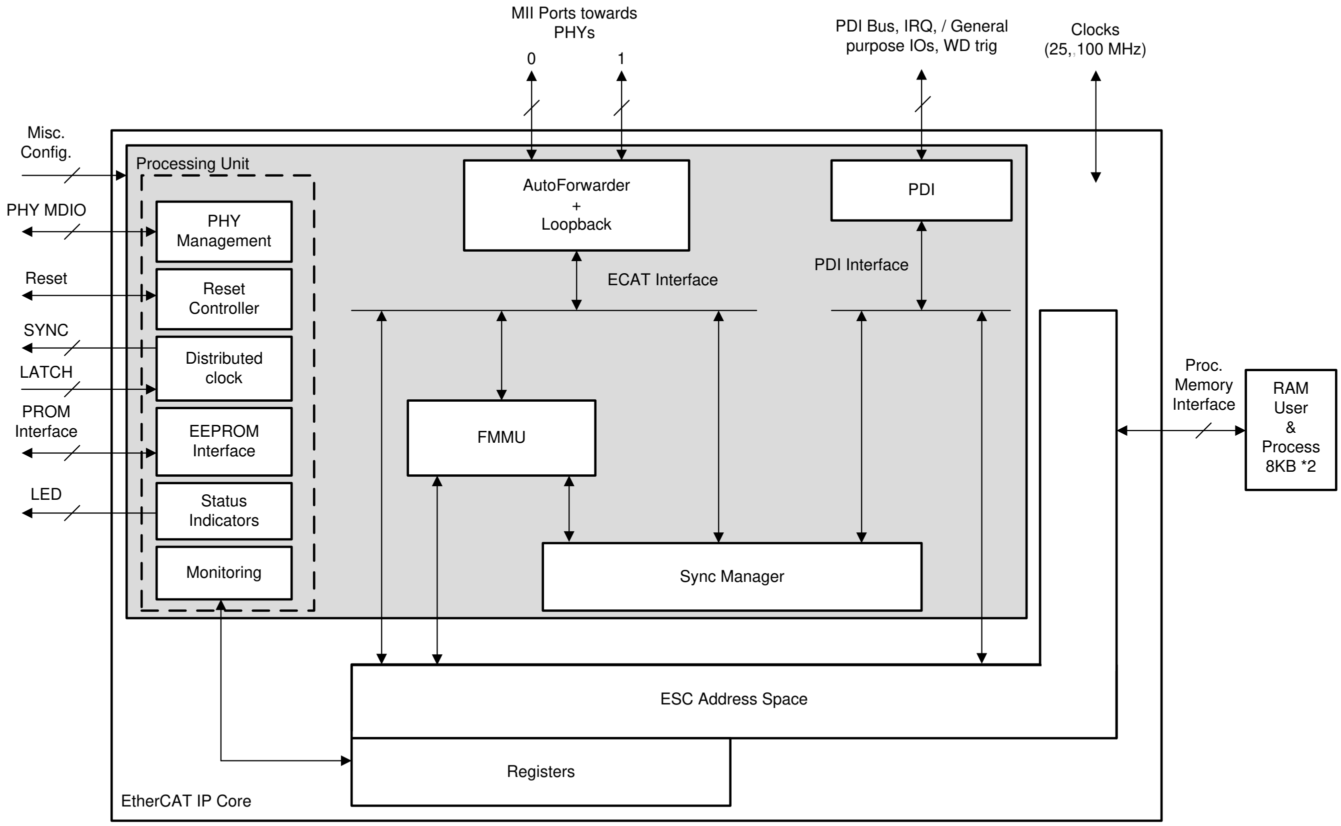


Figure 7-89. EtherCAT IP Block Diagram

7.13.8.4 EtherCAT Electrical Data and Timing

Section 7.13.8.4.1 lists the EtherCAT timing requirements. Section 7.13.8.4.2 lists the EtherCAT switching characteristics. Figure 7-90 through Figure 7-94 show the EtherCAT timing diagrams.

7.13.8.4.1 EtherCAT Timing Requirements

NO.			MIN	NOM	MAX	UNIT
EtherCAT						
	$t_{c(ECATCLK)}$	Cycle time, ECATCLK		10		ns
MII1	$t_{c(TXCLK)}$	Cycle time, ESC_TXy_CLK		40		ns
MII2/MII3	$t_{w(TXCK)}$	Pulse duration, ESC_TXy_CLK high or low	16		24	ns
MII4	$t_{c(RXCK)}$	Cycle time, ESC_RXy_CLK		40		ns
MII5/MII6	$t_{w(RXCK)}$	Pulse duration, ESC_RXy_CLK high or low	16		24	ns
MII8	$t_{su(RXDV-RXCKH)}$	Setup time, receive signals valid before ESC_RXy_CLK high	10			ns
MII9	$t_{h(RXCKH-RXDV)}$	Hold time, receive signals valid after ESC_RXy_CLK high	2			ns
MDIO						
MDIO4	$t_{su(MDV-MCKH)}$	Setup time, ESC_MDIO_DATA valid before ESC_MDIO_CLK high	20			ns
MDIO5	$t_{h(MCKH-MDV)}$	Hold time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	–1			ns

7.13.8.4.2 EtherCAT Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
Auto Shift Compensation						
MII7	$t_{d(TXCLK-TXDV)}$	Delay time, ESC_TXy_CLK to ESC_TXy_DATA[3:0] and ESC_TXy_ENA	20 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK\_100)}$		30 + input_dly + output_dly + TX_SHIFT*$t_{c(CLK\_100)}$	ns
MDIO						
MDIO1	$t_{c(MCK)}$	Cycle time, ESC_MDIO_CLK		400		ns
MDIO2/MDIO3	$t_{w(MCK)}$	Pulse duration, ESC_MDIO_CLK high or low	160		240	ns
MDIO7	$t_{d(MCKH-MDV)}$	Delay time, ESC_MDIO_CLK high to ESC_MDIO_DATA valid			$0.5t_{c(MCK)} + 30$	ns
	$t_{v(MCKH-MDV)}$	Valid time, ESC_MDIO_DATA valid after ESC_MDIO_CLK high	$0.5t_{c(MCK)} - 3.0$			ns

7.13.8.4.3 EtherCAT Timing Diagrams

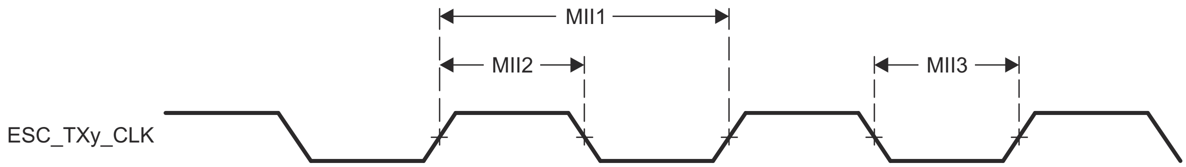


Figure 7-90. EtherCAT Transmit Clock Timing (MII Operation)

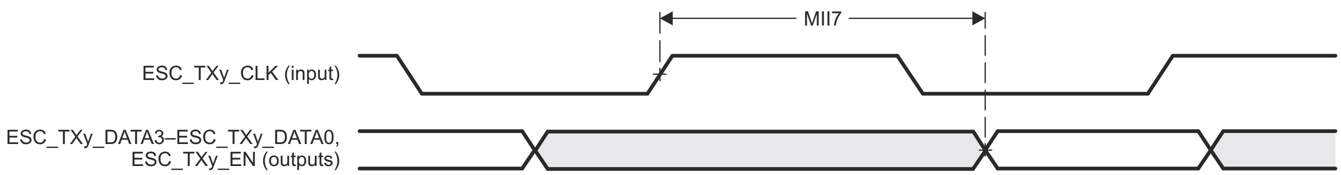


Figure 7-91. EtherCAT Transmit Interface Timing (MII Operation)

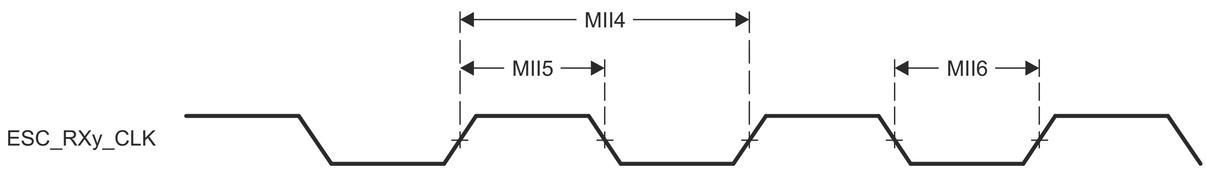


Figure 7-92. EtherCAT Receive Clock Timing (MII Operation)

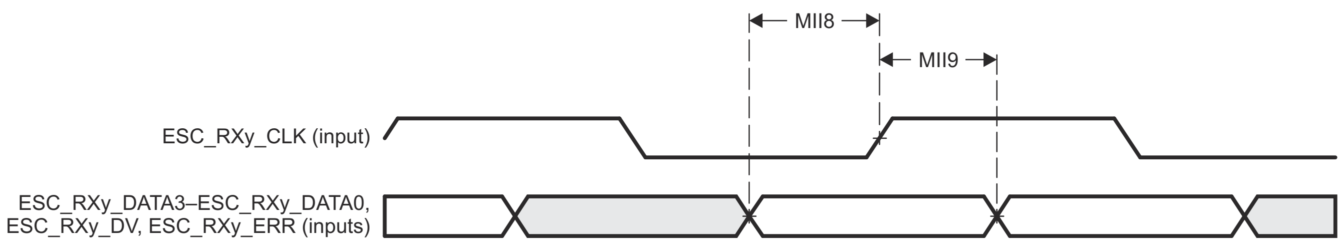


Figure 7-93. EtherCAT Receive Interface Timing (MII Operation)

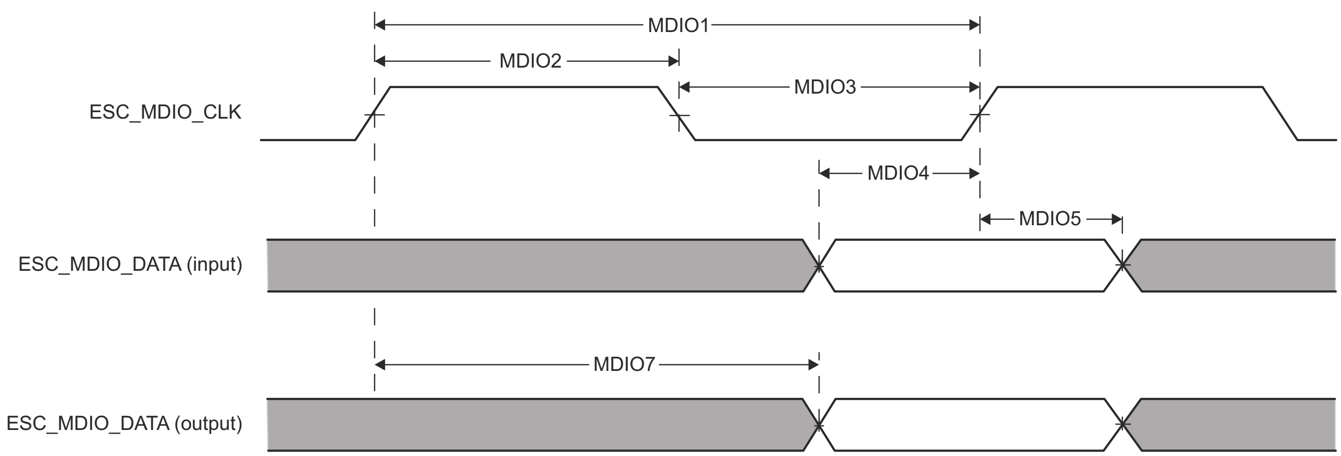


Figure 7-94. EtherCAT MDIO Timing Diagrams

7.13.9 Universal Serial Bus (USB) Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed and low-speed operation
- Integrated PHY
- Three transfer types: control, interrupt, and bulk
- 32 endpoints
  - One dedicated control IN endpoint and one dedicated control OUT endpoint
  - 15 configurable IN endpoints and 15 configurable OUT endpoints
- 4KB of dedicated endpoint memory

Figure 7-95 shows the USB block diagram.

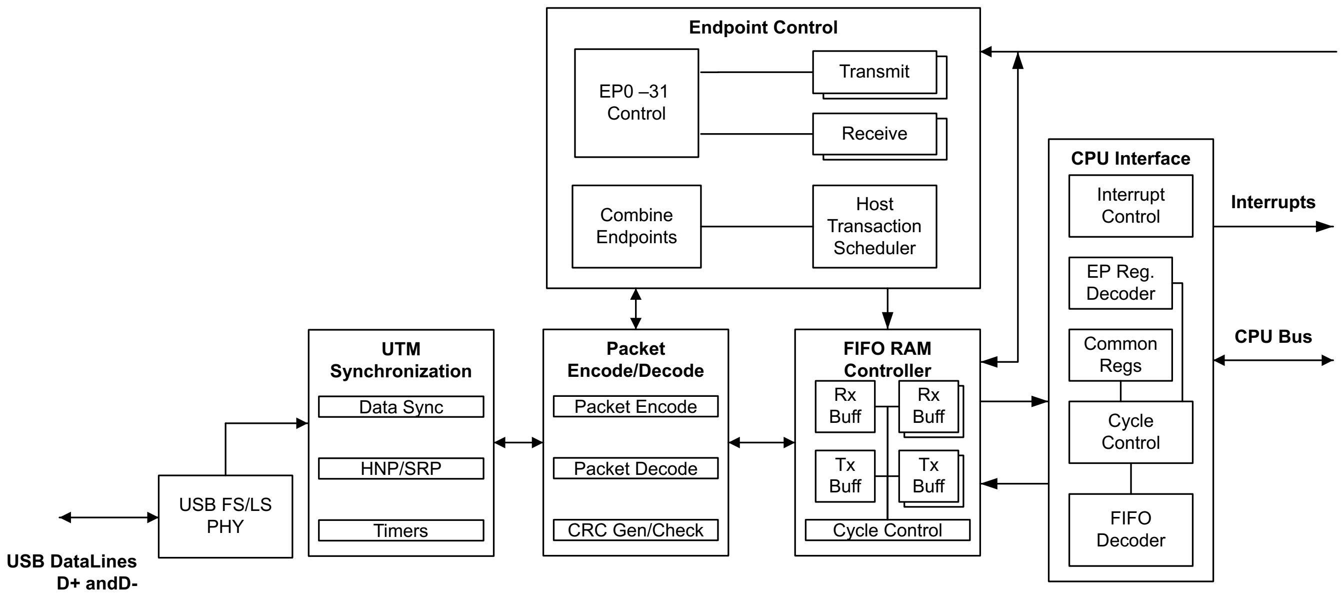


Figure 7-95. USB Block Diagram

Note

The accuracy of the on-chip zero-pin oscillator (Section 7.10.3.5.1, INTOSC Characteristics) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB.

7.13.9.1 USB Electrical Data and Timing

Section 7.13.9.1.1 lists the USB input ports DP and DM timing requirements. Section 7.13.9.1.2 lists the USB output ports DP and DM switching characteristics.

7.13.9.1.1 USB Input Ports DP and DM Timing Requirements

		MIN	MAX	UNIT
V(CM)	Differential input common mode range	0.8	2.5	V
Z(IN)	Input impedance	300		kΩ
VCRS	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic-low level	0.8		V
V_{IH}	Static SE input logic-high level		2.0	V
VDI	Differential input voltage		0.2	V

7.13.9.1.2 USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single-ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single-ended	USB 2.0 load conditions	0	0.3	V
Z(DRV)	D+, D– impedance		28	44	Ω
t_r	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_f	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

7.14 Connectivity Manager (CM) Peripherals

Note

For the actual number of each peripheral on a specific device, see the Device Comparison table.

7.14.1 Modular Controller Area Network (MCAN) [CAN FD]

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices may coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO, up to 32 elements
- Configurable transmit queue, up to 32 elements
- Configurable transmit Event FIFO, up to 32 elements
- Up to 64 dedicated receive buffers
- Two configurable receive FIFOs, up to 64 elements each
- Up to 128 filter elements
- Loop-back mode for self-test
- Maskable interrupt (two configurable interrupt lines, correctable ECC, counter overflow and clock stop/wakeup)
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock/host clock)
- ECC check for Message RAM
- Clock stop and wakeup support
- Timestamp counter

Non-supported features:

- Host bus firewall
- GPIO is not integrated, such as DCAN
- Clock calibration
- Debug over CAN

Figure 7-96 provides an overview of the MCAN module.

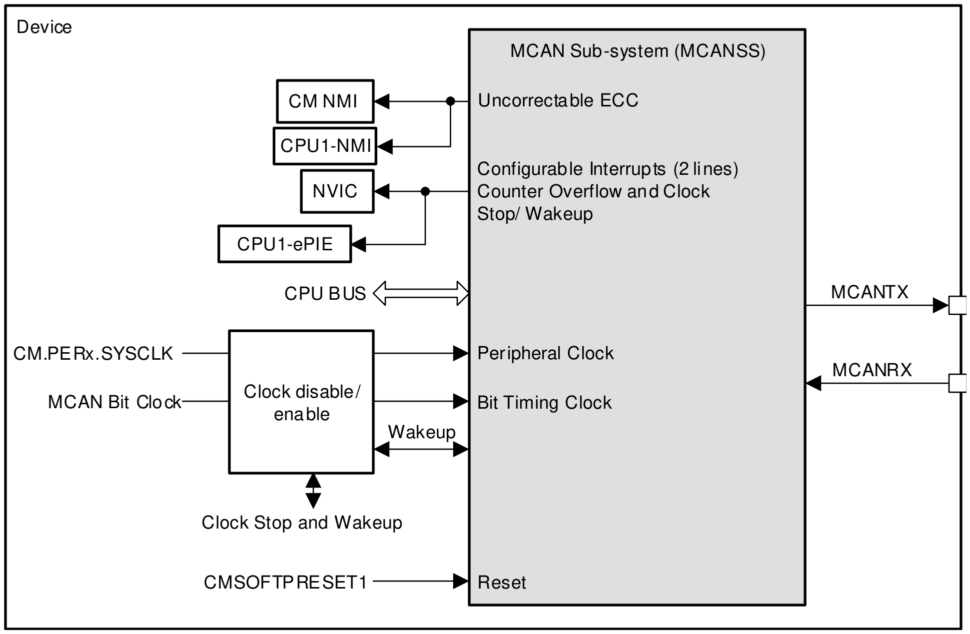


Figure 7-96. MCAN Module Overview

7.14.2 Ethernet Media Access Controller (EMAC)

The Ethernet module enables a host to transmit and receive data over the Ethernet in compliance with IEEE 802.3-2015. The Ethernet module contains the following characteristics:

- IEEE 802.3-2015 for Ethernet MAC, Media Independent Interface (MII)
- IEEE 1588-2008 for precision networked clock synchronization
- IEEE 802.3az-2010 for Energy Efficient Ethernet (EEE)
- Reduced Media Independent Interface (RMII) specification version 1.2 from RMII consortium
- Reverse Media Independent Interface (RevMII)

For more information about the Ethernet module, see the Ethernet chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

7.14.2.1 MAC Features

The Ethernet controller supports a number of Tx and Rx MAC features. The MAC includes the following feature groups:

- MAC Tx and Rx features
- MAC Tx features
- MAC Rx features

7.14.2.1.1 MAC Tx and Rx Features

The combined features for Tx and Rx are as follows:

- Separate transmission, reception, and control interfaces to the application
- Little-endian mode for Transmit and Receive paths
- 10, 100 data transfer rates with the following PHY interfaces:
  - IEEE 802.3-compliant MII (default) interface to communicate with an external Ethernet PHY
  - RMII interface to communicate with an external Fast Ethernet PHY
  - RevMII interface to directly communicate with a remote MAC
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support (based on implementation-specific white papers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in MII PHYs.
- Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- Network statistics with RMON or MIB Counters (RFC2819/RFC2665)
- Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in the TX direction.
- Flexibility to control the Pulse-Per-Second (PPS) output signal
- MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

7.14.2.1.2 MAC Tx Features

The MAC Tx features are as follows:

- Preamble and start-of-packet data (SFD) insertion
- Separate 32-bit status for each packet transmitted from the application
- Automatic CRC and pad generation controllable on a per-packet basis
- Programmable packet length to support Standard or Jumbo Ethernet packets up to 16KB in size
- Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flow control input transitions from assertion to deassertion (in full-duplex mode)
- Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted packets with per-packet or static-global control
- Insertion, replacement, or deletion of up to two VLAN tags
- Insert, replace, or delete queue/channel-based VLAN tags

7.14.2.1.3 MAC Rx Features

The MAC Rx features are as follows:

- Flexible address filtering modes:
  - Destination Address filters with masks for each byte
  - Source Address comparison check with masks for each byte
  - 64-bit Hash filter for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed packets
  - Promiscuous mode to pass all packets without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Additional packet filtering:
  - VLAN tag-based: Perfect match and Hash-based filtering. Filtering based on either outer or inner VLAN tag is possible.
  - Layer 3 and Layer 4-based: TCP or UDP over IPv4 or IPv6
  - Extended VLAN-tag based filtering 4-filter selection
- IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- Module to detect remote wake-up packets and AMD magic packets
- Forwarding of received Pause packets to the application (in full-duplex mode)
- Receive module for Layer-3/Layer-4 checksum offload for received packets
- Stripping of up to two VLAN Tags and providing the tags in the status.

7.14.2.2 Ethernet Electrical Data and Timing

Section 7.14.2.2.1 lists the Ethernet timing requirements. Section 7.14.2.2.2 lists the Ethernet switching characteristics. Figure 7-97 through Figure 7-103 show the Ethernet timing diagrams.

7.14.2.2.1 Ethernet Timing Requirements

NO.			MIN	NOM	MAX	UNIT
MII 100 Mbps						
MII1	$t_{c(TXCK)}$	Cycle time, ENET_MII_TX_CLK		40		ns
MII2/ MII3	$t_{w(TXCK)}$	Pulse duration, ENET_MII_TX_CLK high or low	16		24	ns
MII4	$t_{c(RXCK)}$	Cycle time, ENET_MII_RX_CLK		40		ns
MII5/ MII6	$t_{w(RXCK)}$	Pulse duration, ENET_MII_RX_CLK high or low	16		24	ns
MII8	$t_{su(MRXDV-RXCKH)}$	Setup time, receive signals valid before ENET_MII_RX_CLK high	10			ns
MII9	$t_{h(RXCKH-MRXDV)}$	Hold time, receive signals valid after ENET_MII_RX_CLK high	2			ns
MII 10 Mbps						
MII1	$t_{c(TXCK)}$	Cycle time, ENET_MII_TX_CLK		400		ns
MII2/ MII3	$t_{w(TXCK)}$	Pulse duration, ENET_MII_TX_CLK high or low	160		240	ns
MII4	$t_{c(RXCK)}$	Cycle time, ENET_MII_RX_CLK		400		ns
MII5/ MII6	$t_{w(RXCK)}$	Pulse duration, ENET_MII_RX_CLK high or low	160		240	ns
MII8	$t_{su(MRXDV-RXCKH)}$	Setup time, receive signals valid before ENET_MII_RX_CLK high	10			ns
MII9	$t_{h(RXCKH-MRXDV)}$	Hold time, receive signals valid after ENET_MII_RX_CLK high	2			ns
RMII (Internal Clock) 100 Mbps						
RMII5	$t_{su(MRXDV-RCKH)}$	Setup time, receive signals valid before ENET_RMII_CLK high	4			ns
RMII6	$t_{h(RCKH-MRXDV)}$	Hold time, receive signals valid after ENET_RMII_CLK high	2			ns
RMII (Internal Clock) 10 Mbps						
RMII5	$t_{su(MRXDV-RCKH)}$	Setup time, receive signals valid before ENET_RMII_CLK high	4			ns
RMII6	$t_{h(RCKH-MRXDV)}$	Hold time, receive signals valid after ENET_RMII_CLK high	2			ns
RMII (External Clock) 100 Mbps						
RMII1	$t_{c(RCK)}$	Cycle time, ENET_RMII_CLK		20		ns
RMII2/ RMII3	$t_{w(RCK)}$	Pulse duration, ENET_RMII_CLK high or low	8		12	ns
RMII5	$t_{su(MRXDV-RCKH)}$	Setup time, receive signals valid before ENET_RMII_CLK high	4			ns
RMII6	$t_{h(RCKH-MRXDV)}$	Hold time, receive signals valid after ENET_RMII_CLK high	2			ns
RMII (External Clock) 10 Mbps						
RMII1	$t_{c(RCK)}$	Cycle time, ENET_RMII_CLK		200		ns
RMII2/ RMII3	$t_{w(RCK)}$	Pulse duration, ENET_RMII_CLK high or low	80		120	ns
RMII5	$t_{su(MRXDV-RCKH)}$	Setup time, receive signals valid before ENET_RMII_CLK high	4			ns
RMII6	$t_{h(RCKH-MRXDV)}$	Hold time, receive signals valid after ENET_RMII_CLK high	2			ns
MDIO						
MDIO1	$t_{c(MCK)}$	Cycle time, ENET_MDIO_CLK		400		ns
MDIO2/ MDIO3	$t_{w(MCK)}$	Pulse duration, ENET_MDIO_CLK high or low	160		240	ns
MDIO4	$t_{su(MDV-MCKH)}$	Setup time, ENET_MDIO_DATA valid before ENET_MDIO_CLK high	20			ns

7.14.2.2.1 Ethernet Timing Requirements (continued)

NO.			MIN	NOM	MAX	UNIT
MDIO5	$t_{h(MCKH-MDV)}$	Hold time, ENET_MDIO_DATA valid after ENET_MDIO_CLK high	–1			ns

7.14.2.2.2 Ethernet Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
MII 100 Mbps						
MII7	$t_{d(TXCKH-MTXDV)}$	Delay time, ENET_MII_TX_CLK high to transmit signals valid	0		15	ns
MII 10 Mbps Switching Characteristics						
MII7	$t_{d(TXCKH-MTXDV)}$	Delay time, ENET_MII_TX_CLK high to transmit signals valid	0		15	ns
RMII (Internal Clk) 100 Mbps						
RMII7	$t_{c(RCK)}$	Cycle time, ENET_RMII_CLK		20		ns
RMII8/ RMII9	$t_{w(RCK)}$	Pulse duration, ENET_RMII_CLK high or low	8		12	ns
RMII11	$t_{d(RCKH-MTXDV)}$	Delay time, ENET_RMII_CLK high to transmit signals valid			14	ns
RMII (Internal Clk) 10 Mbps						
RMII7	$t_{c(RCK)}$	Cycle time, ENET_RMII_CLK		200		ns
RMII8/ RMII9	$t_{w(RCK)}$	Pulse duration, ENET_RMII_CLK high or low	80		120	ns
RMII11	$t_{d(RCKH-MTXDV)}$	Delay time, ENET_RMII_CLK high to transmit signals valid	0		14	ns
RMII (External Clk) 100 Mbps						
RMII11	$t_{d(RCKH-MTXDV)}$	Delay time, ENET_RMII_TX_CLK high to transmit signals valid	0		14	ns
RMII (External Clk) 10 Mbps						
RMII11	$t_{d(RCKH-MTXDV)}$	Delay time, ENET_RMII_CLK high to transmit signals valid	0		14	ns
MDIO						
MDIO1	$t_{c(MCK)}$	Cycle time, ENET_MDIO_CLK		400		ns
MDIO2/ MDIO3	$t_{w(MCK)}$	Pulse duration, ENET_MDIO_CLK high or low	160		240	ns
MDIO7	$t_{d(MCKH-MDV)}$	Delay time, ENET_MDIO_CLK high to ENET_MDIO_DATA valid			$0.5t_{c(MCK)} + 30$	ns
	$t_{v(MCKH-MDV)}$	Valid time, ENET_MDIO_DATA valid after ENET_MDIO_CLK high	$0.5t_{c(MCK)}$			ns

7.14.2.2.3 Ethernet Timing Diagrams

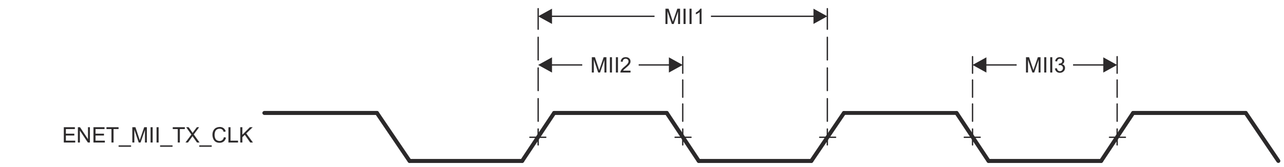


Figure 7-97. Transmit Clock Timing (MII Operation)

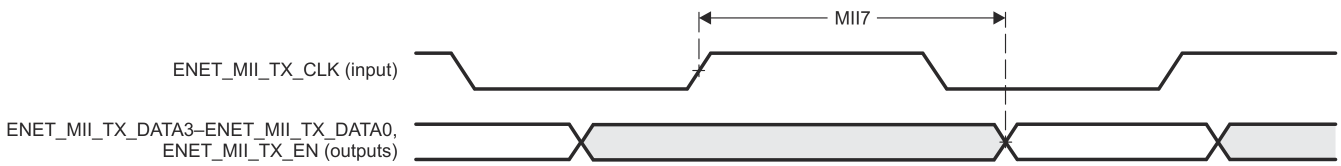


Figure 7-98. Transmit Interface Timing (MII Operation)

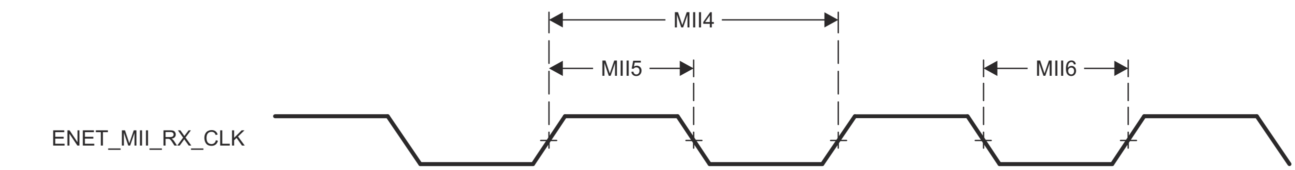


Figure 7-99. Receive Clock Timing (MII Operation)

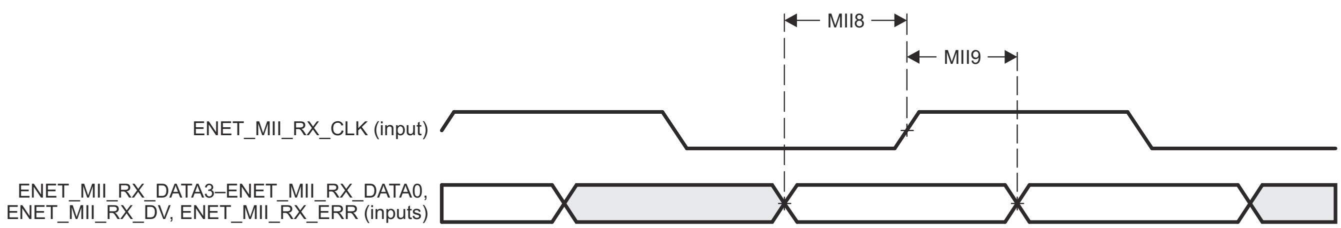


Figure 7-100. Receive Interface Timing (MII Operation)

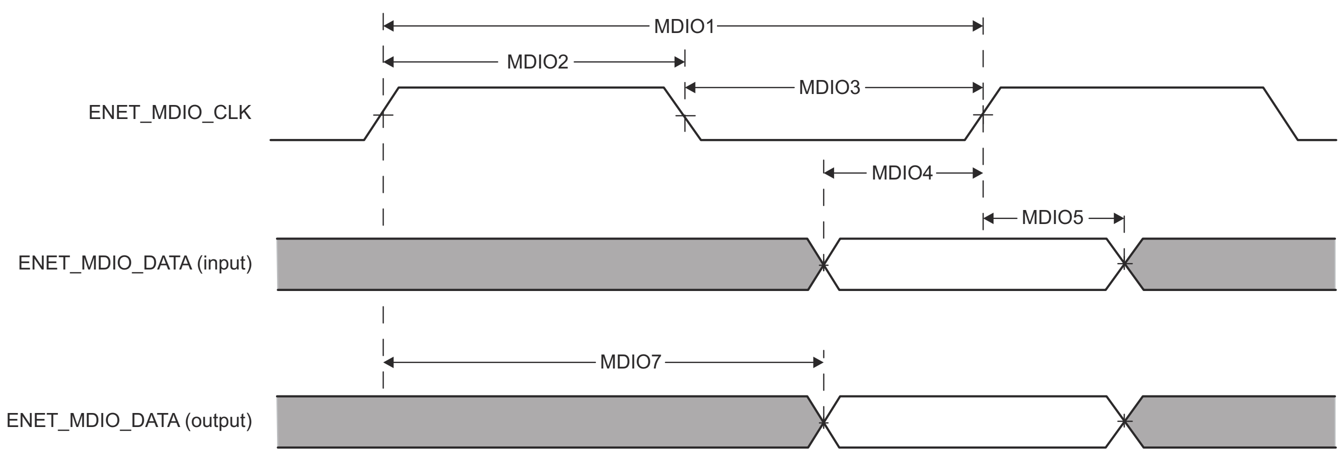


Figure 7-101. MDIO Timing Diagrams

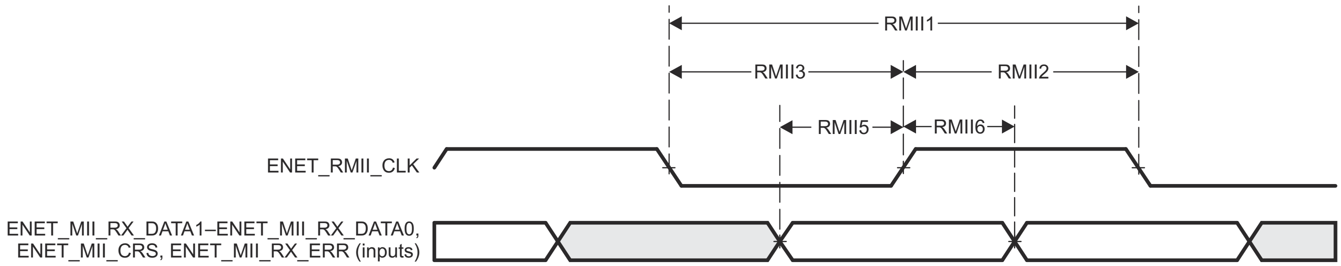


Figure 7-102. Receive Interface Timing (RMII Operation)

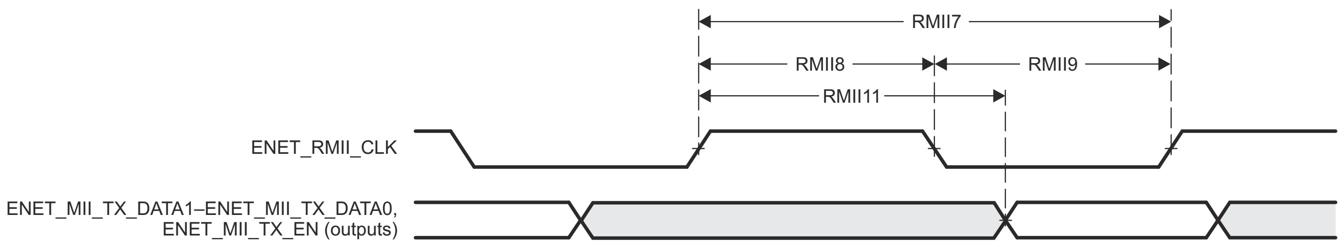


Figure 7-103. Transmit Interface Timing (RMII Operation)

7.14.2.3 Ethernet REVMII Electrical Data and Timing

Section 7.14.2.3.1 lists the Ethernet REVMII timing requirements. Section 7.14.2.3.2 lists the Ethernet REVMII switching characteristics.

7.14.2.3.1 Ethernet REVMII Timing Requirements

		MIN	NOM	MAX	UNIT
REVMII					
$t_{c(RXCK)}$	Cycle time, ENET_MII_RX_CLK		40		ns
$t_{w(RXCK)}$	Pulse duration, ENET_MII_RX_CLK high or low	16		24	ns
$t_{su(MRXDV-RXCKH)}$	Setup time, ENET_MII_RX_DATA[3:0], ENET_MII_RX_EN valid before ENET_MII_RX_CLK high	15			ns
$t_{h(RXCKH-MRXDV)}$	Hold time, ENET_MII_RX_DATA[3:0], ENET_MII_RX_EN valid after ENET_MII_RX_CLK high	0			ns
MDIO					
$t_{c(MCK)}$	Cycle time, ENET_MDIO_CLK		400		ns
$t_{w(MCK)}$	Pulse duration, ENET_MDIO_CLK high or low	160		240	ns
$t_{su(MDV-MCKH)}$	Setup time, ENET_MDIO_DATA valid before ENET_MDIO_CLK high	30			ns
$t_{h(MCKH-MDV)}$	Hold time, ENET_MDIO_DATA valid after ENET_MDIO_CLK high	3			ns

7.14.2.3.2 Ethernet REVMII Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
REVMII					
$t_{c(TXCK)}$	Cycle time, ENET_MII_TX_CLK		40		ns
$t_{w(TXCK)}$	Pulse duration, ENET_MII_TX_CLK high or low	16		24	ns
$t_{d(TXCKH-DV)}$	Delay time, ENET_MII_TX_CLK high to ENET_MII_TX_DATA[3:0], ENET_MII_TX_DV, ENET_MII_TX_ERR valid			10	ns
$t_{v(TXCKH-DV)}$	Valid time, ENET_MII_TX_CLK high to ENET_MII_TX_DATA[3:0], ENET_MII_TX_DV, ENET_MII_TX_ERR invalid	1			ns
MDIO					
$t_{c(MCK)}$	Cycle time, ENET_MDIO_CLK		400		ns
$t_{w(MCK)}$	Pulse duration, ENET_MDIO_CLK high or low	160		240	ns
$t_{d(MCKH-MDV)}$	Delay time, ENET_MDIO_CLK high to ENET_MDIO_DATA valid			40	ns
$t_{v(MCKH-MDV)}$	Valid time, ENET_MDIO_DATA valid after ENET_MDIO_CLK high	1			ns

7.14.3 Inter-Integrated Circuit (CM-I2C)

The CM-I2C bus provides bidirectional data transfer through a two-wire design; a serial data line (SDA) and a serial clock line (SCL); and interfaces to external I2C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The CM-I2C bus can also be used for system testing and diagnostic purposes in product development and manufacturing.

The CM-I2C modules support the following features:

- Devices on the CM-I2C bus can be designated as either a master or a slave.
  - Support both transmitting and receiving data as either a master or a slave
  - Support simultaneous master and slave operation
- Four CM-I2C modes:
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Receive FIFO and Transmitter FIFO (8 deep × 8 bits FIFO)
  - FIFOs can be independently assigned to master or slave
- Three transmission speeds:
  - Standard (100 kbps)
  - Fast mode (400 kbps)
  - Fast-mode plus (1 Mbps)
- Glitch suppression
- SMBus support through software
  - Clock low time-out interrupt
  - Dual slave address capability
  - Quick command capability
- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts because of an error)
  - Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected
- Master with arbitration and clock synchronization, multiple-master support, and 7-bit addressing mode
- Efficient transfers using a Micro Direct Memory Access (µDMA) Controller
  - Separate channels for transmit and receive
  - Ability to execute single data transfers or burst data transfers using the RX and TX FIFOs in the CM-I2C

Figure 7-104 shows the CM-I2C block diagram.

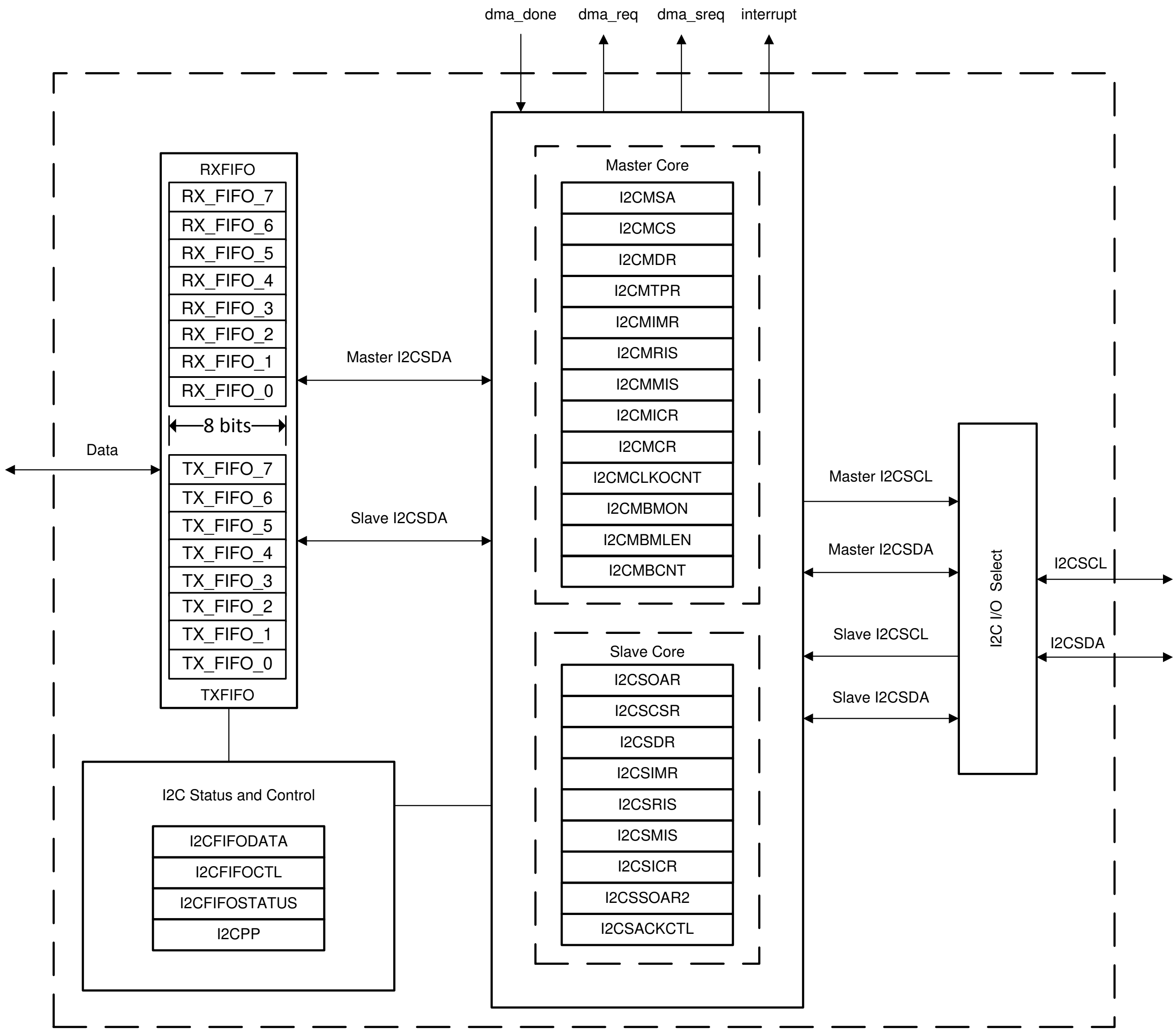


Figure 7-104. CM-I2C Block Diagram

7.14.3.1 CM-I2C Electrical Data and Timing

Section 7.14.3.1.1 lists the CM-I2C timing requirements. Section 7.14.3.1.2 lists the CM-I2C switching characteristics. Figure 7-105 shows the CM-I2C timing diagram.

7.14.3.1.1 CM-I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.7		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	$t_{c(CMCLK)}$	31 * $t_{c(CMCLK)}$	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	$t_{c(CMCLK)}$	31 * $t_{c(CMCLK)}$	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode plus					
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.26		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.26		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	50		ns
T5	$t_{r(SDA)}$	Rise time, SDA		120	ns
T6	$t_{r(SCL)}$	Rise time, SCL		120	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	120	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	120	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.26		µs

7.14.3.1.1 CM-I2C Timing Requirements (continued)

NO.			MIN	MAX	UNIT
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	$t_{c(CMCLK)}$	31 * $t_{c(CMCLK)}$	ns
T11	C_b	capacitance load on each bus line		550	pF

7.14.3.1.2 CM-I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA
Fast mode plus						
S1	f_{SCL}	SCL clock frequency		0	1000	kHz
S2	T_{SCL}	SCL clock period		1		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		0.5		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.26		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		0.5		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.45	µs
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA

7.14.3.1.3 CM-I2C Timing Diagram

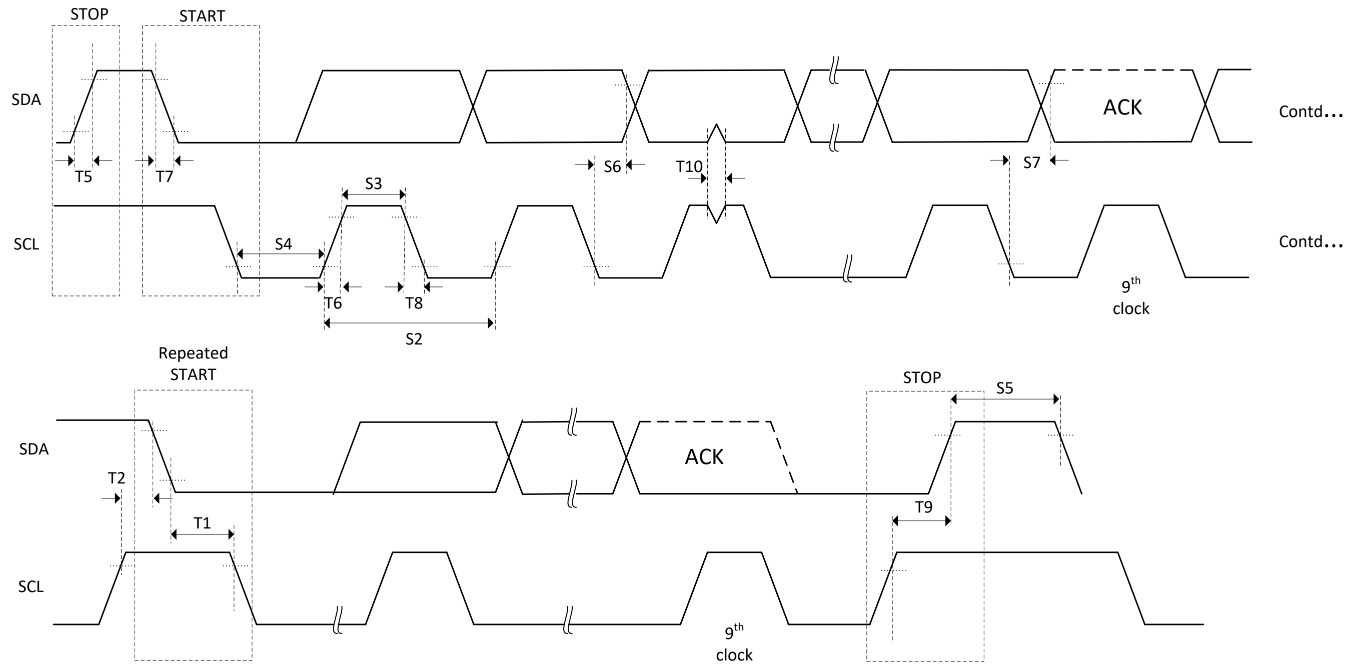


Figure 7-105. CM-I2C Timing Diagram

7.14.4 Synchronous Serial Interface (SSI)

The SSI module includes the following features:

- Programmable interface operation for Freescale® SPI, or Texas Instruments Synchronous Serial Interfaces. In this SSI module, only the Legacy SSI mode is supported.
- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic and debug testing
- Standard FIFO-based interrupts and End-of-Transmission interrupt
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains four entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when FIFO contains four or more entries are available to be written in the FIFO
  - Maskable µDMA interrupts for receive and transmit complete

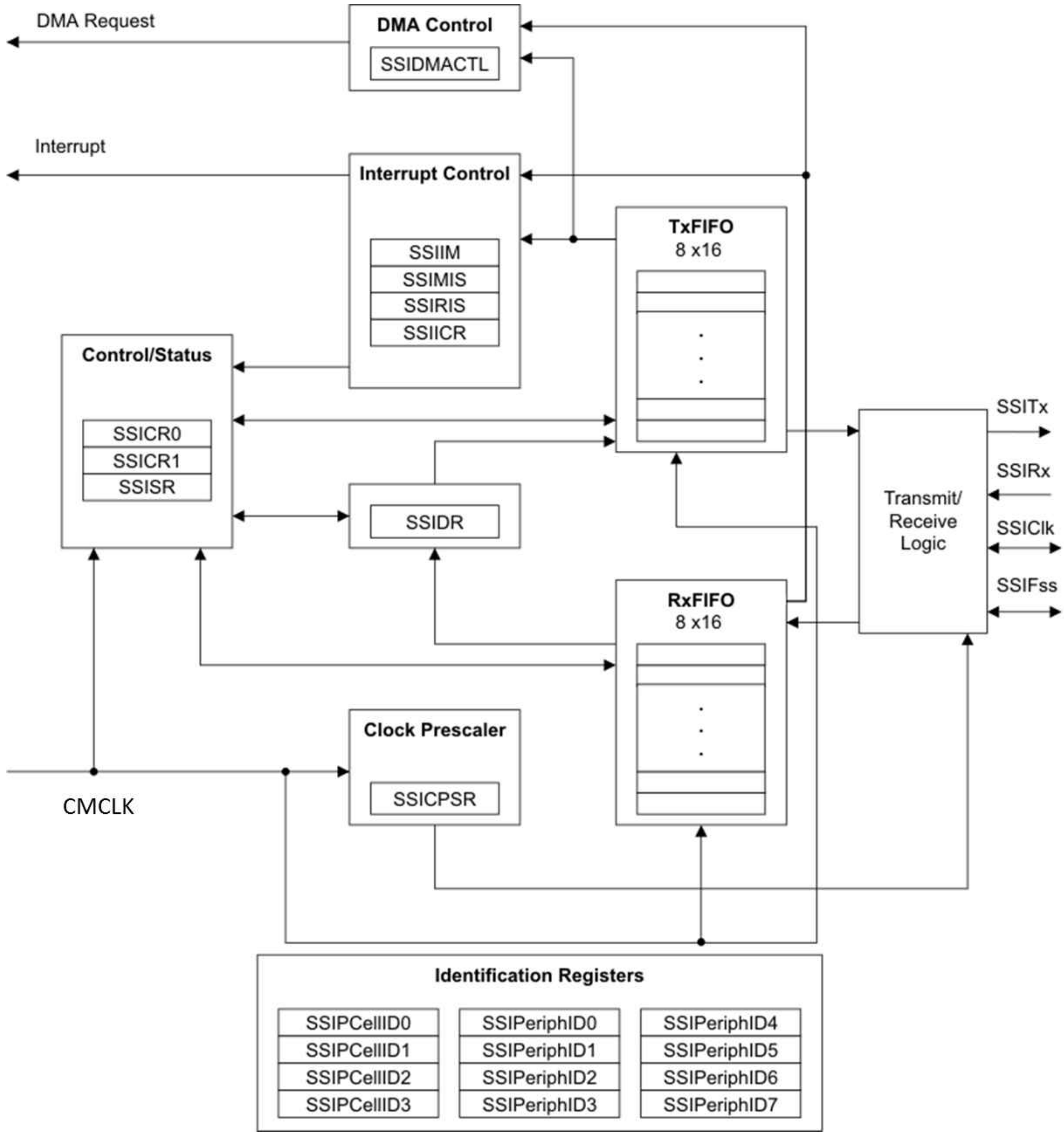


Figure 7-106. SSI Block Diagram

7.14.4.1 SSI Electrical Data and Timing

Section 7.14.4.1.1 lists the SSI timing requirements. Section 7.14.4.1.2 lists the SSI switching characteristics. Figure 7-107 through Figure 7-109 show the SSI timing diagrams.

7.14.4.1.1 SSI Timing Requirements

NO.			MIN	NOM	MAX	UNIT
MASTER MODE						
S8	t_{RXDMS}	Rx Data setup time (high-speed mode)	4			ns
S8	t_{RXDMS}	Rx Data setup time (normal mode)	14			ns
S9	t_{RXDMH}	Rx Data hold time	2			ns
SLAVE MODE						
S1	t_{CLK_PER}	SSIClk cycle time(1)	$12 \times tc_{(CMCLK)}$			ns
S2	t_{CLK_HIGH}	SSIClk high time	$0.4 \times t_{CLK\_PER}$			ns
S3	t_{CLK_LOW}	SSIClk low time	$0.4 \times t_{CLK\_PER}$			ns
S12	t_{RXDSSU}	Rx Data setup time	0			ns
S13	t_{RXDSH}	Rx Data hold time	$4 \times tc_{(CMCLK)}$			ns

(1) In slave mode, the SSICPSR must be configured to set SSICLK to less than one twelfth of CMCLK.

7.14.4.1.2 SSI Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
MASTER MODE						
S1	t_{CLK_PER}	SSIClk cycle time(1)	$2 \times t_{CMCLK}$			ns
S2	t_{CLK_HIGH}	SSIClk high time	$0.4 \times t_{CLK\_PER}$			ns
S3	t_{CLK_LOW}	SSIClk low time	$0.4 \times t_{CLK\_PER}$			ns
S6	t_{TXDMOV}	Tx Data output valid time from SSIClk			6	ns
S7	t_{TXDMOH}	Tx Data output hold time after next SSIClk	0			ns
SLAVE MODE						
S10	t_{TXDSOV}	Tx Data output valid time from edge of SSIClk			$4 \times t_{CMCLK}+14$	ns
S11	t_{TXDSOH}	Tx Data output hold time from next SSIClk	$4 \times t_{CMCLK} + 4$			ns

(1) In master mode, the SSICPSR must be configured to set SSICLK to less than half of CMCLK. For master mode normal mode (non-high speed), a larger SSICPSR divider may be needed to meet the master RX input setup requirements.

7.14.4.1.3 SSI Timing Diagrams

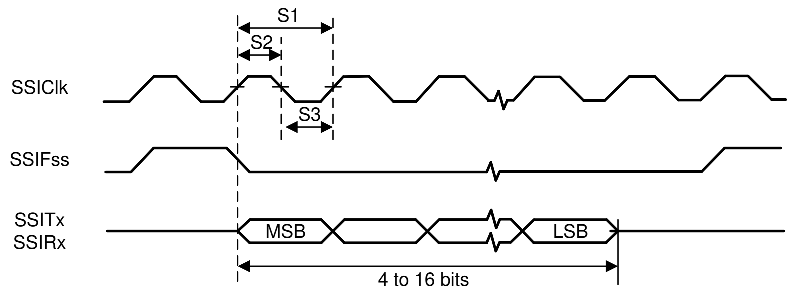


Figure 7-107. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

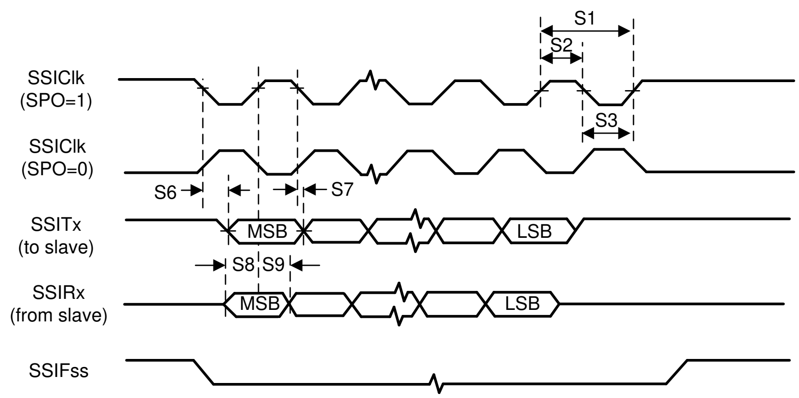


Figure 7-108. Master Mode SSI Timing for SPI Frame Format (FRF = 00), with SPH = 1

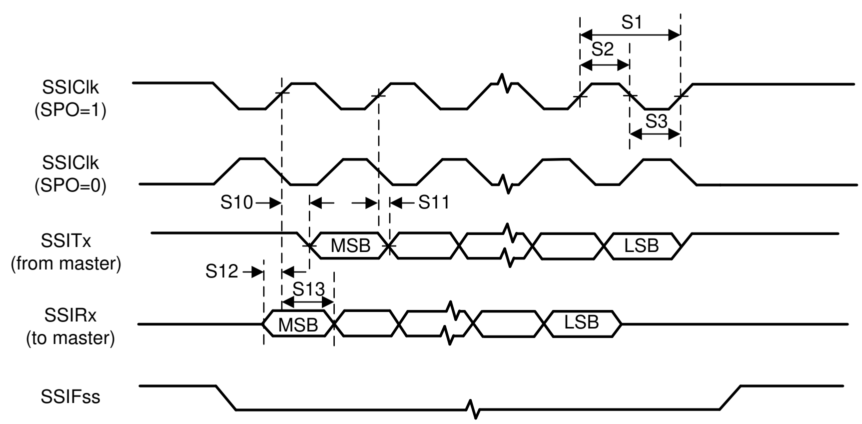


Figure 7-109. Slave Mode SSI Timing for SPI Frame Format (FRF = 00), with SPH = 1

7.14.5 Universal Asynchronous Receiver/Transmitter (CM-UART)

The Universal Asynchronous Receiver/Transmitter (UART) module in this device contains the following features:

- Programmable baud-rate generator allowing speeds of up to 7.8125 Mbps for regular speed (divide by 16) and 15.625 Mbps for high speed (divide by 8)
- Separate 16-level-deep and 8-bit-wide transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of ⅛, ¼, ½, ¾, and ⅞
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity-bit generation and detection
  - 1 or 2 stop-bit generation
- IrDA serial-IR (SIR) encoder and decoder providing:
  - Programmable use of IrDA SIR or UART input/output
  - Support of IrDA SIR encoder and decoder functions for data rates of up to 115.2 kbps half-duplex
  - Support of normal 3/16 and low-power (1.41 to 2.23 μs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power-mode bit duration
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission (EOT) interrupts
- Efficient transfers using Micro Direct Memory Access (μDMA) Controller
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

Figure 7-110 shows the CM-UART module block diagram.

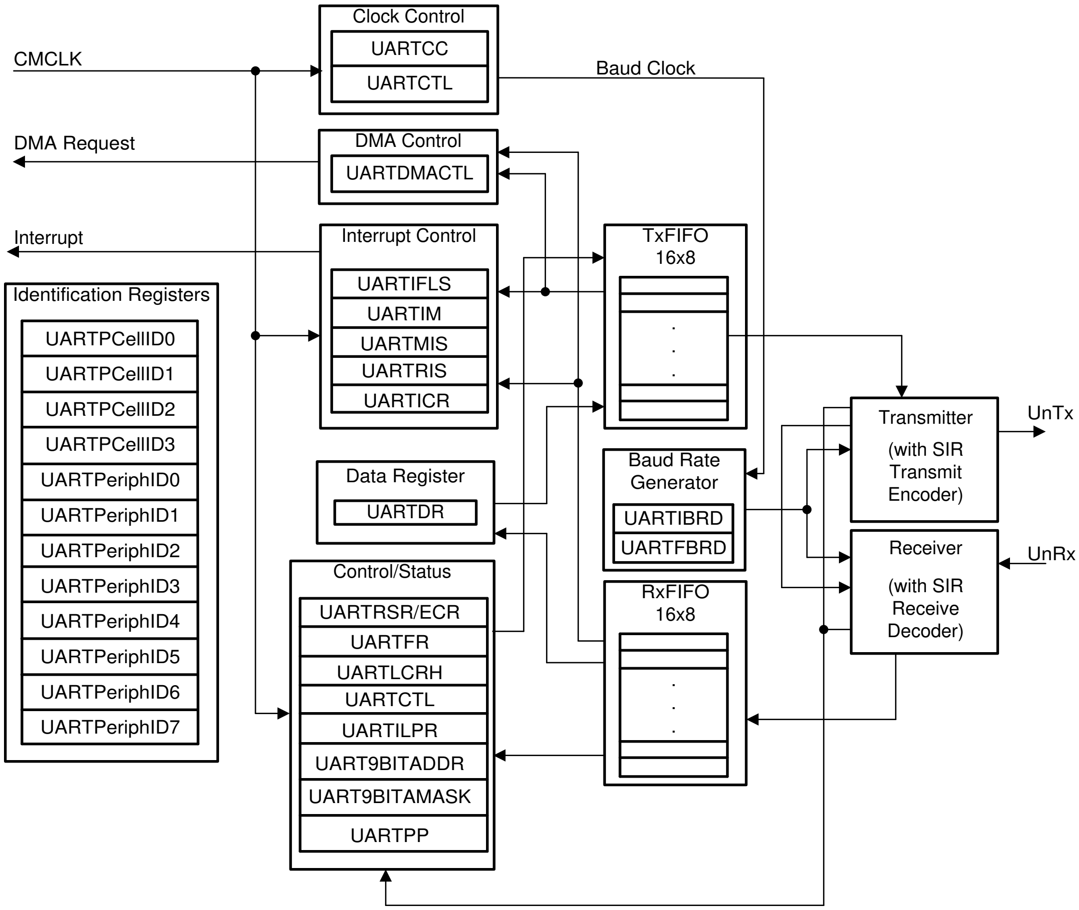


Figure 7-110. CM-UART Module Block Diagram

7.14.6 Trace Port Interface Unit (TPIU)

Trace capability from the Cortex-M4 is supported on the CM subsystem.

The Cortex-M4 supports two trace interfaces:
- Single wire trace, which follows a UART protocol and is asynchronous
- Five-pin (four data pins and one clock pin) and parallel trace

Both options are supported on this device. Figure 7-111 shows the high-level clock and signal hook-up to and from the TPIU.

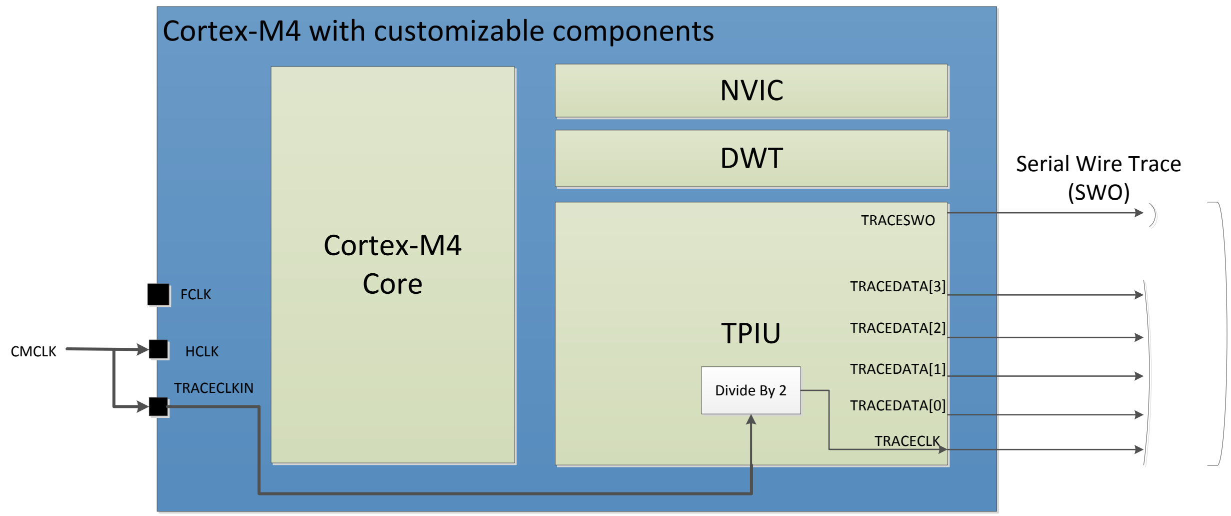


Figure 7-111. Debug Trace

Table 7-15 lists the key attributes of the two trace data export mechanisms. For more details about TPIU and trace mechanisms, see the *Arm Architecture Reference Manual*.

Table 7-15. Key Attributes of Trace Data Export

ATTRIBUTE PARALLEL TRACE	SERIAL WIRE TRACE	PARALLEL TRACE
Protocol	UART Protocol/Manchester-encoded data stream	Trace Data changes on both edges of TRACECLK.
Data throughput rate	Frequency(CMHCLK)/(TPIU_ACPR + 1)	Frequency(CMHCLK)/2

You must configure the GPIO mux to select a trace function on the GPIO pin to use it.

7.14.6.1 TPIU Electrical Data and Timing

Section 7.14.6.1.1 lists the trace port switching characteristics.

7.14.6.1.1 Trace Port Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(TRACE\_CLK)}$	Cycle time, TRACE_CLK		16		ns
$t_{w(TRACE\_CLK)}$	Pulse duration, TRACE_CLK high or low	6		10	ns
$t_{d(TRACE\_DATA, TRACE\_SWO)}$	Delay time, TRACE_CLK high to valid TRACE_DATA	-2		2	ns

8 Detailed Description

8.1 Overview

The TMS320F2838x is a powerful 32-bit floating-point real-time microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; electric vehicles; and DSP and sensing applications. The F2838x supports a dual-core C28x architecture along with a new Connectivity Manager that offloads critical communication tasks, significantly boosting system performance. The integrated analog and control peripherals with advanced connectivity peripherals like EtherCAT and Ethernet also let designers consolidate real-time control and real-time communications architectures reducing requirements for multicontroller systems.

The dual real-time control subsystems are based on TI's 32-bit C28x floating-point CPUs, which provide 200 MHz of signal processing performance in each core. The C28x CPUs are further boosted by the TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations.

The F2838x real-time microcontroller family features two CLA real-time control coprocessors. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics. The dual C28x+CLA architecture enables intelligent partitioning between various system tasks. For example, one C28x+CLA core can be used to track speed and position, while the other C28x+CLA core can be used to control torque and current loops.

The Connectivity Manager subsystem is based on the Cortex-M4 CPU and has access to advanced communication IPs like EtherCAT, Ethernet, MCAN (CAN FD) and AES.

The TMS320F2838x supports up to 1.5MB (512KB per CPU) of flash memory with error correction code (ECC) and up to 312KB (216KB total for C28x CPU1 and CPU2, and 96KB on the Cortex-M4) of SRAM. Two 128-bit secure zones are also available on the device for code protection.

Performance analog and control peripherals are also integrated on the F2838x MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. The sigma-delta filter module (SDFM) works in conjunction with the sigma-delta modulator to enable isolated current shunt measurements. The Comparator Subsystem (CMPSS) with windowed comparators allows for protection of power stages when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Peripherals such as EMIFs, CAN modules (ISO 11898-1/CAN 2.0B-compliant), EtherCAT, Ethernet, and MCAN (CAN FD) extend the connectivity of the F2838x. Lastly, a USB 2.0 port with MAC and PHY lets users easily add universal serial bus (USB) connectivity to their application.

8.2 Functional Block Diagram

Figure 8-1 shows the CPU system and associated peripherals.

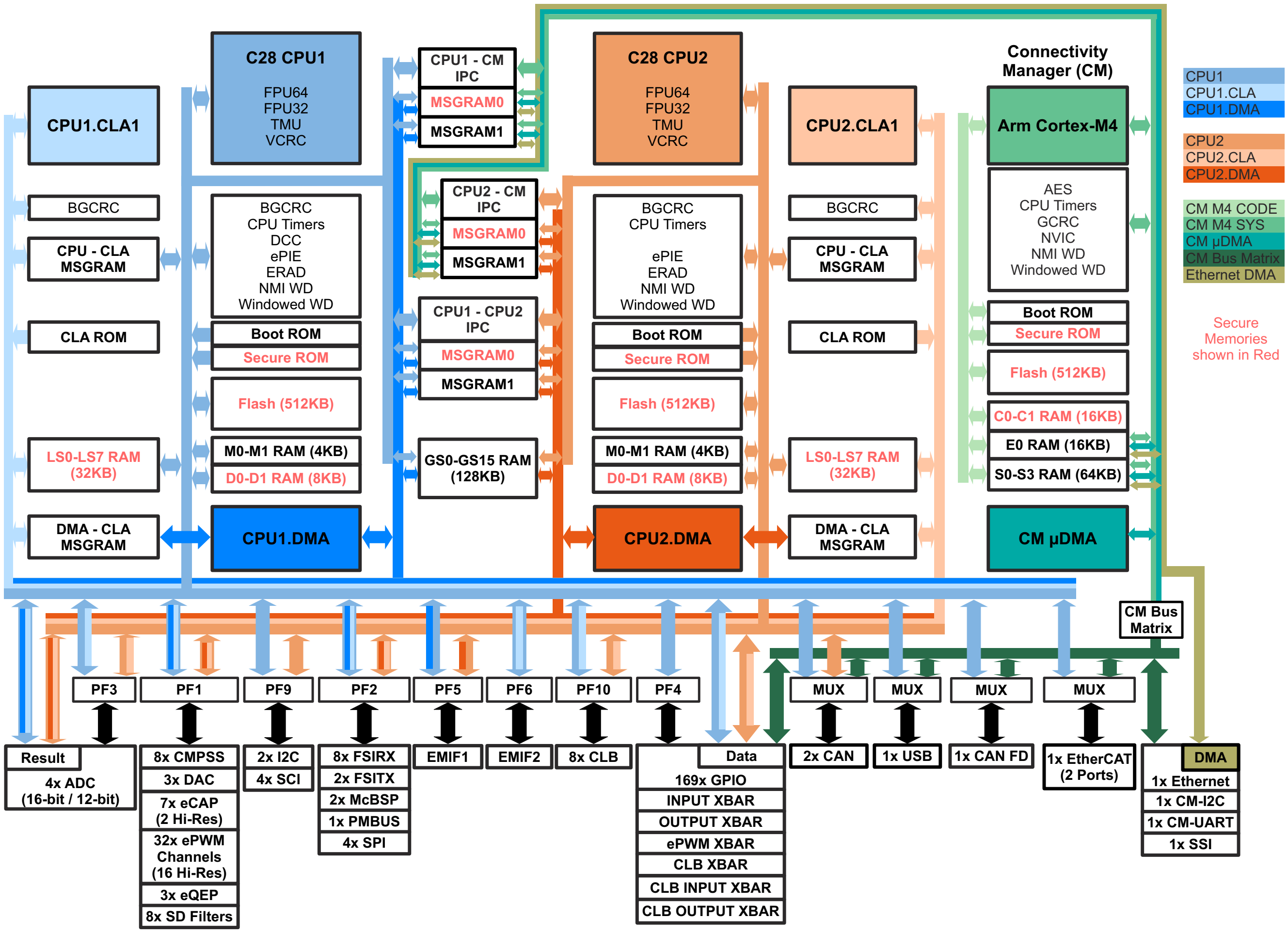


Figure 8-1. Functional Block Diagram

8.3 Memory

8.3.1 C28x Memory Map

Both C28x CPUs on the device have the same memory map except where noted in the C28x Memory Map table. The GSx_RAM (Global Shared RAM) should be assigned to either CPU by the GSxMSEL register. Memories accessible by the CLA or DMA (direct memory access) are noted as well.

Table 8-1. C28x Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
M0 RAM	1K x 16	0x0000 0000	0x0000 03FF			ECC	Yes	
M1 RAM	1K x 16	0x0000 0400	0x0000 07FF			ECC	Yes	
PieVectTable	512 x 16	0x0000 0D00	0x0000 0EFF					
CPUx.CLA1 to CPUx MSGRAM	128 x 16	0x0000 1480	0x0000 14FF	Yes		Parity		
CPUx to CPUx.CLA1 MSGRAM	128 x 16	0x0000 1500	0x0000 157F	Yes		Parity		
CPUx.CLA1 to CPUx.DMA MSGRAM	128 x 16	0x0000 1680	0x0000 16FF	Yes	Yes	Parity		
CPUx.DMA to CPUx.CLA1 MSGRAM	128 x 16	0x0000 1700	0x0000 177F	Yes	Yes	Parity		
LS0 RAM	2K x 16	0x0000 8000	0x0000 87FF	Yes		ECC	Yes	Yes
LS1 RAM	2K x 16	0x0000 8800	0x0000 8FFF	Yes		ECC	Yes	Yes
LS2 RAM	2K x 16	0x0000 9000	0x0000 97FF	Yes		ECC	Yes	Yes
LS3 RAM	2K x 16	0x0000 9800	0x0000 9FFF	Yes		ECC	Yes	Yes
LS4 RAM	2K x 16	0x0000 A000	0x0000 A7FF	Yes		ECC	Yes	Yes
LS5 RAM	2K x 16	0x0000 A800	0x0000 AFFF	Yes		ECC	Yes	Yes
LS6 RAM	2K x 16	0x0000 B000	0x0000 B7FF	Yes		ECC	Yes	Yes
LS7 RAM	2K x 16	0x0000 B800	0x0000 BFFF	Yes		ECC	Yes	Yes
D0 RAM	2K x 16	0x0000 C000	0x0000 C7FF			ECC	Yes	Yes
D1 RAM	2K x 16	0x0000 C800	0x0000 CFFF			ECC	Yes	Yes
GS0 RAM(1)	4K x 16	0x0000 D000	0x0000 DFFF		Yes	Parity	Yes	
GS1 RAM(1)	4K x 16	0x0000 E000	0x0000 EFFF		Yes	Parity	Yes	
GS2 RAM(1)	4K x 16	0x0000 F000	0x0000 FFFF	CLA DATA ROM(5)	Yes	Parity	Yes	
GS3 RAM(1)	4K x 16	0x0001 0000	0x0001 0FFF		Yes	Parity	Yes	
GS4 RAM(1)	4K x 16	0x0001 1000	0x0001 1FFF		Yes	Parity	Yes	
GS5 RAM(1)	4K x 16	0x0001 2000	0x0001 2FFF		Yes	Parity	Yes	
GS6 RAM(1)	4K x 16	0x0001 3000	0x0001 3FFF		Yes	Parity	Yes	
GS7 RAM(1)	4K x 16	0x0001 4000	0x0001 4FFF		Yes	Parity	Yes	
GS8 RAM(1)	4K x 16	0x0001 5000	0x0001 5FFF		Yes	Parity	Yes	
GS9 RAM(1)	4K x 16	0x0001 6000	0x0001 6FFF		Yes	Parity	Yes	
GS10 RAM(1)	4K x 16	0x0001 7000	0x0001 7FFF		Yes	Parity	Yes	
GS11 RAM(1)	4K x 16	0x0001 8000	0x0001 8FFF		Yes	Parity	Yes	

Table 8-1. C28x Memory Map (continued)

MEMORY	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
GS12 RAM(1)	4K x 16	0x0001 9000	0x0001 9FFF		Yes	Parity	Yes	
GS13 RAM(1)	4K x 16	0x0001 A000	0x0001 AFFF		Yes	Parity	Yes	
GS14 RAM(1)	4K x 16	0x0001 B000	0x0001 BFFF		Yes	Parity	Yes	
GS15 RAM(1)	4K x 16	0x0001 C000	0x0001 CFFF		Yes	Parity	Yes	
EtherCAT RAM (direct access) (2)	8K x 16	0x0003 0800	0x0003 27FF		Yes	Parity		
CM to CPUx MSGRAM0	1K x 16	0x0003 8000	0x0003 83FF		Yes	Parity	Yes	Yes
CM to CPUx MSGRAM1	1K x 16	0x0003 8400	0x0003 87FF		Yes	Parity	Yes	
CPUx to CM MSGRAM0	1K x 16	0x0003 9000	0x0003 93FF		Yes	Parity	Yes	Yes
CPUx to CM MSGRAM1	1K x 16	0x0003 9400	0x0003 97FF		Yes	Parity	Yes	
CPU1 to CPU2 MSGRAM0	1K x 16	0x0003 A000	0x0003 A3FF		Yes	Parity	Yes	Yes
CPU1 to CPU2 MSGRAM1	1K x 16	0x0003 A400	0x0003 A7FF		Yes	Parity	Yes	
CPU2 to CPU1 MSGRAM0	1K x 16	0x0003 B000	0x0003 B3FF		Yes	Parity	Yes	Yes
CPU2 to CPU1 MSGRAM1	1K x 16	0x0003 B400	0x0003 B7FF		Yes	Parity	Yes	
USB RAM(2)	2K x 16	0x0004 1000	0x0004 17FF		Yes			
CAN A Message RAM	2K x 16	0x0004 9000	0x0004 97FF			Parity		
CAN B Message RAM	2K x 16	0x0004 B000	0x0004 B7FF			Parity		
MCAN Message RAM	17K x 16	0x0005 8000	0x0005 C3FF			ECC		
TI OTP(4)	1K x 16	0x0007 0000	0x0007 03FF			ECC		
User OTP	1K x 16	0x0007 8000	0x0007 83FF					Yes(3)
Flash	256K x 16	0x0008 0000	0x000B FFFF			ECC		Yes
Secure ROM	32K x 16	0x003E 0000	0x003E 7FFF			Parity		Yes
Boot ROM	96K x 16	0x003E 8000	0x003F FFFF			Parity		
Pie Vector Fetch Error (part of Boot ROM)	1 x 16	0x003F FFBE	0x003F FFBF			Parity		
Default Vectors (part of Boot ROM)	64 x 16	0x003F FFC0	0x003F FFFF			Parity		
CLA Data ROM	4K x 16	0x0100 1000	0x0100 1FFF					

(1) Shared between CPU subsystems.
(2) Only on the CPU1 subsystem.
(3) Only CPU1 User OTP is secure. CPU2 User OTP is non-secure.
(4) TI OTP is for TI internal use only.
(5) CLA has its Data ROM mapped at this address space.

8.3.2 C28x Flash Memory Map

On the F28388D, F28386D, and F28384D devices, each CPU has its own flash bank [512KB (256KW)], the total flash for each device is 1MB (512KW). Only one bank can be programmed or erased at a time and the code to program and erase the flash should be executed out of RAM.

The F28388S, F28386S, and F28384S devices have one flash bank of 512KB (256KW) and the code to program the flash should be executed out of RAM. See Section 7.10.4 for details on flash wait states.

The C28x Flash Memory Map table lists the addresses of the flash sectors.

Table 8-2. C28x Flash Memory Map

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP	1K x 16	0x0007 0000	0x0007 03FF
User OTP(1)	1K x 16	0x0007 8000	0x0007 83FF
Sectors			
Sector 0	8K x 16	0x0008 0000	0x0008 1FFF
Sector 1	8K x 16	0x0008 2000	0x0008 3FFF
Sector 2	8K x 16	0x0008 4000	0x0008 5FFF
Sector 3	8K x 16	0x0008 6000	0x0008 7FFF
Sector 4	32K x 16	0x0008 8000	0x0008 FFFF
Sector 5	32K x 16	0x0009 0000	0x0009 7FFF
Sector 6	32K x 16	0x0009 8000	0x0009 FFFF
Sector 7	32K x 16	0x000A 0000	0x000A 7FFF
Sector 8	32K x 16	0x000A 8000	0x000A FFFF
Sector 9	32K x 16	0x000B 0000	0x000B 7FFF
Sector 10	8K x 16	0x000B 8000	0x000B 9FFF
Sector 11	8K x 16	0x000B A000	0x000B BFFF
Sector 12	8K x 16	0x000B C000	0x000B DFFF
Sector 13	8K x 16	0x000B E000	0x000B FFFF
Flash ECC Locations			
TI OTP ECC	128 x 16	0x0107 0000	0x0107 007F
User OTP ECC	128 x 16	0x0107 1000	0x0107 107F
Flash ECC (Sector 0)	1K x 16	0x0108 0000	0x0108 03FF
Flash ECC (Sector 1)	1K x 16	0x0108 0400	0x0108 07FF
Flash ECC (Sector 2)	1K x 16	0x0108 0800	0x0108 0BFF
Flash ECC (Sector 3)	1K x 16	0x0108 0C00	0x0108 0FFF
Flash ECC (Sector 4)	4K x 16	0x0108 1000	0x0108 1FFF
Flash ECC (Sector 5)	4K x 16	0x0108 2000	0x0108 2FFF
Flash ECC (Sector 6)	4K x 16	0x0108 3000	0x0108 3FFF
Flash ECC (Sector 7)	4K x 16	0x0108 4000	0x0108 4FFF
Flash ECC (Sector 8)	4K x 16	0x0108 5000	0x0108 5FFF
Flash ECC (Sector 9)	4K x 16	0x0108 6000	0x0108 6FFF
Flash ECC (Sector 10)	1K x 16	0x0108 7000	0x0108 73FF

Table 8-2. C28x Flash Memory Map (continued)

SECTOR	SIZE	START ADDRESS	END ADDRESS
Flash ECC (Sector 11)	1K x 16	0x0108 7400	0x0108 77FF
Flash ECC (Sector 12)	1K x 16	0x0108 7800	0x0108 7BFF
Flash ECC (Sector 13)	1K x 16	0x0108 7C00	0x0108 7FFF

(1) CPU1 User OTP is used for security (DCSM) configuration; so, it is not available for general-purpose use. CPU2 User OTP is available for general-purpose use.

8.3.3 Peripheral Registers Memory Map

Table 8-3. Peripheral Registers Memory Map

Bit Field Name		DriverLib Name	Base Address	CPU 1	CPU 2	DM A	CL A	Pipeline Protected
Instance	Structure							
Peripheral Frame 0 (PF0)								
AdcaResultRegs	ADC_RESULT_REGS	ADCARESULT_BASE	0x0000_0B00	YES	YES	YES	YES	-
AdcbResultRegs	ADC_RESULT_REGS	ADCBRESULT_BASE	0x0000_0B20	YES	YES	YES	YES	-
AdccResultRegs	ADC_RESULT_REGS	ADCCRESULT_BASE	0x0000_0B40	YES	YES	YES	YES	-
AdcdResultRegs	ADC_RESULT_REGS	ADCDRESULT_BASE	0x0000_0B60	YES	YES	YES	YES	-
Peripheral Frame 1 (PF1)								
EPwm1Regs	EPWM_REGS	EPWM1_BASE	0x0000_4000	YES	YES	YES	YES	YES
EPwm2Regs	EPWM_REGS	EPWM2_BASE	0x0000_4100	YES	YES	YES	YES	YES
EPwm3Regs	EPWM_REGS	EPWM3_BASE	0x0000_4200	YES	YES	YES	YES	YES
EPwm4Regs	EPWM_REGS	EPWM4_BASE	0x0000_4300	YES	YES	YES	YES	YES
EPwm5Regs	EPWM_REGS	EPWM5_BASE	0x0000_4400	YES	YES	YES	YES	YES
EPwm6Regs	EPWM_REGS	EPWM6_BASE	0x0000_4500	YES	YES	YES	YES	YES
EPwm7Regs	EPWM_REGS	EPWM7_BASE	0x0000_4600	YES	YES	YES	YES	YES
EPwm8Regs	EPWM_REGS	EPWM8_BASE	0x0000_4700	YES	YES	YES	YES	YES
EPwm9Regs	EPWM_REGS	EPWM9_BASE	0x0000_4800	YES	YES	YES	YES	YES
EPwm10Regs	EPWM_REGS	EPWM10_BASE	0x0000_4900	YES	YES	YES	YES	YES
EPwm11Regs	EPWM_REGS	EPWM11_BASE	0x0000_4A00	YES	YES	YES	YES	YES
EPwm12Regs	EPWM_REGS	EPWM12_BASE	0x0000_4B00	YES	YES	YES	YES	YES
EPwm13Regs	EPWM_REGS	EPWM13_BASE	0x0000_4C00	YES	YES	YES	YES	YES
EPwm14Regs	EPWM_REGS	EPWM14_BASE	0x0000_4D00	YES	YES	YES	YES	YES
EPwm15Regs	EPWM_REGS	EPWM15_BASE	0x0000_4E00	YES	YES	YES	YES	YES
EPwm16Regs	EPWM_REGS	EPWM16_BASE	0x0000_4F00	YES	YES	YES	YES	YES
EQep1Regs	EQEP_REGS	EQEP1_BASE	0x0000_5100	YES	YES	YES	YES	YES
EQep2Regs	EQEP_REGS	EQEP2_BASE	0x0000_5140	YES	YES	YES	YES	YES
EQep3Regs	EQEP_REGS	EQEP3_BASE	0x0000_5180	YES	YES	YES	YES	YES
ECap1Regs	ECAP_REGS	ECAP1_BASE	0x0000_5200	YES	YES	YES	YES	YES
ECap2Regs	ECAP_REGS	ECAP2_BASE	0x0000_5240	YES	YES	YES	YES	YES
ECap3Regs	ECAP_REGS	ECAP3_BASE	0x0000_5280	YES	YES	YES	YES	YES
ECap4Regs	ECAP_REGS	ECAP4_BASE	0x0000_52C0	YES	YES	YES	YES	YES
ECap5Regs	ECAP_REGS	ECAP5_BASE	0x0000_5300	YES	YES	YES	YES	YES
ECap6Regs	ECAP_REGS	ECAP6_BASE	0x0000_5340	YES	YES	YES	YES	YES
ECap7Regs	ECAP_REGS	ECAP7_BASE	0x0000_5380	YES	YES	YES	YES	YES
DacaRegs	DAC_REGS	DACA_BASE	0x0000_5C00	YES	YES	YES	YES	YES
DacbRegs	DAC_REGS	DACB_BASE	0x0000_5C10	YES	YES	YES	YES	YES
DaccRegs	DAC_REGS	DACC_BASE	0x0000_5C20	YES	YES	YES	YES	YES
Cmpss1Regs	CMPSS_REGS	CMPSS1_BASE	0x0000_5C80	YES	YES	YES	YES	YES
Cmpss2Regs	CMPSS_REGS	CMPSS2_BASE	0x0000_5CA0	YES	YES	YES	YES	YES
Cmpss3Regs	CMPSS_REGS	CMPSS3_BASE	0x0000_5CC0	YES	YES	YES	YES	YES
Cmpss4Regs	CMPSS_REGS	CMPSS4_BASE	0x0000_5CE0	YES	YES	YES	YES	YES

Table 8-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	CPU 1	CPU 2	DMA	CLA	Pipeline Protected
Instance	Structure							
Cmpss5Regs	CMPSS_REGS	CMPSS5_BASE	0x0000_5D00	YES	YES	YES	YES	YES
Cmpss6Regs	CMPSS_REGS	CMPSS6_BASE	0x0000_5D20	YES	YES	YES	YES	YES
Cmpss7Regs	CMPSS_REGS	CMPSS7_BASE	0x0000_5D40	YES	YES	YES	YES	YES
Cmpss8Regs	CMPSS_REGS	CMPSS8_BASE	0x0000_5D60	YES	YES	YES	YES	YES
Sdfm1Regs	SDFM_REGS	SDFM1_BASE	0x0000_5E00	YES	YES	YES	YES	YES
Sdfm2Regs	SDFM_REGS	SDFM2_BASE	0x0000_5E80	YES	YES	YES	YES	YES
Peripheral Frame 2 (PF2)								
SpiaRegs	SPI_REGS	SPIA_BASE	0x0000_6100	YES	YES	YES	YES	YES
SpibRegs	SPI_REGS	SPIB_BASE	0x0000_6110	YES	YES	YES	YES	YES
SpicRegs	SPI_REGS	SPIC_BASE	0x0000_6120	YES	YES	YES	YES	YES
SpidRegs	SPI_REGS	SPID_BASE	0x0000_6130	YES	YES	YES	YES	YES
PmbusaRegs	PMBUS_REGS	PMBUSA_BASE	0x0000_6400	YES	YES	YES	YES	YES
FsiTxaRegs	FSI_TX_REGS	FSITXA_BASE	0x0000_6600	YES	YES	YES	YES	YES
FsiRxaRegs	FSI_RX_REGS	FSIRXA_BASE	0x0000_6680	YES	YES	YES	YES	YES
FsiTxbRegs	FSI_TX_REGS	FSITXB_BASE	0x0000_6700	YES	YES	YES	YES	YES
FsiRxbRegs	FSI_RX_REGS	FSIRXB_BASE	0x0000_6780	YES	YES	YES	YES	YES
FsiRxcRegs	FSI_RX_REGS	FSIRXC_BASE	0x0000_6880	YES	YES	YES	YES	YES
FsiRxdRegs	FSI_RX_REGS	FSIRXD_BASE	0x0000_6980	YES	YES	YES	YES	YES
FsiRxeRegs	FSI_RX_REGS	FSIRXE_BASE	0x0000_6A80	YES	YES	YES	YES	YES
FsiRxfRegs	FSI_RX_REGS	FSIRXF_BASE	0x0000_6B80	YES	YES	YES	YES	YES
FsiRxgRegs	FSI_RX_REGS	FSIRXG_BASE	0x0000_6C80	YES	YES	YES	YES	YES
FsiRxhRegs	FSI_RX_REGS	FSIRXH_BASE	0x0000_6D80	YES	YES	YES	YES	YES
Peripheral Frame 3 (PF3)								
AdcaRegs	ADC_REGS	ADCA_BASE	0x0000_7400	YES	YES	-	YES	YES
AdcbRegs	ADC_REGS	ADCB_BASE	0x0000_7480	YES	YES	-	YES	YES
AdccRegs	ADC_REGS	ADCC_BASE	0x0000_7500	YES	YES	-	YES	YES
AdcdRegs	ADC_REGS	ADCD_BASE	0x0000_7580	YES	YES	-	YES	YES
Peripheral Frame 4 (PF4)								
InputXbarRegs	INPUT_XBAR_REGS	INPUTXBAR_BASE	0x0000_7900	YES	-	-	-	YES
XbarRegs	XBAR_REGS	XBAR_BASE	0x0000_7920	YES	-	-	-	YES
ClbInputXbarRegs	INPUT_XBAR_REGS	CLBINPUTXBAR_BASE	0x0000_7960	YES	-	-	-	YES
EPwmXbarRegs	EPWM_XBAR_REGS	EPWMXBAR_BASE	0x0000_7A00	YES	-	-	-	YES
CLBXbarRegs	CLB_XBAR_REGS	CLBXBAR_BASE	0x0000_7A40	YES	-	-	-	YES
OutputXbarRegs	OUTPUT_XBAR_REGS	OUTPUTXBAR_BASE	0x0000_7A80	YES	-	-	-	YES
ClbOutputXbarRegs	OUTPUT_XBAR_REGS	CLBOUTPUTXBAR_BASE	0x0000_7BC0	YES	-	-	-	YES
GpioCtrlRegs	GPIO_CTRL_REGS	GPIOCTRL_BASE	0x0000_7C00	YES	-	-	-	YES
Peripheral Frame 5 (PF5)								
Emif1ConfigRegs	EMIF1_CONFIG_REGS	EMIF1CONFIG_BASE	0x0005_F4C0	YES	YES	-	-	YES
Peripheral Frame 6 (PF6)								
Emif2ConfigRegs	EMIF2_CONFIG_REGS	EMIF2CONFIG_BASE	0x0005_F4E0	YES	-	-	-	YES
Peripheral Frame 9 (PF9)								
SciaRegs	SCI_REGS	SCIA_BASE	0x0000_7200	YES	YES	-	-	YES
ScibRegs	SCI_REGS	SCIB_BASE	0x0000_7210	YES	YES	-	-	YES
ScicRegs	SCI_REGS	SCIC_BASE	0x0000_7220	YES	YES	-	-	YES
ScidRegs	SCI_REGS	SCID_BASE	0x0000_7230	YES	YES	-	-	YES
I2caRegs	I2C_REGS	I2CA_BASE	0x0000_7300	YES	YES	-	-	YES
I2cbRegs	I2C_REGS	I2CB_BASE	0x0000_7340	YES	YES	-	-	YES
Peripheral Frame 10 (PF10)								
Clb1LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB1_LOGICCFG_BASE	0x0000_3000	YES	YES	-	YES	-

Table 8-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	CPU 1	CPU 2	DMA	CLA	Pipeline Protected
Instance	Structure							
Clb1LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB1_LOGICCTL_BASE	0x0000_3100	YES	YES	-	YES	-
Clb1DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB1_DATAEXCH_BASE	0x0000_3180	YES	YES	-	YES	-
Clb2LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB2_LOGICCFG_BASE	0x0000_3200	YES	YES	-	YES	-
Clb2LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB2_LOGICCTL_BASE	0x0000_3300	YES	YES	-	YES	-
Clb2DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB2_DATAEXCH_BASE	0x0000_3380	YES	YES	-	YES	-
Clb3LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB3_LOGICCFG_BASE	0x0000_3400	YES	YES	-	YES	-
Clb3LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB3_LOGICCTL_BASE	0x0000_3500	YES	YES	-	YES	-
Clb3DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB3_DATAEXCH_BASE	0x0000_3580	YES	YES	-	YES	-
Clb4LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB4_LOGICCFG_BASE	0x0000_3600	YES	YES	-	YES	-
Clb4LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB4_LOGICCTL_BASE	0x0000_3700	YES	YES	-	YES	-
Clb4DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB4_DATAEXCH_BASE	0x0000_3780	YES	YES	-	YES	-
Clb5LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB5_LOGICCFG_BASE	0x0000_3800	YES	YES	-	YES	-
Clb5LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB5_LOGICCTL_BASE	0x0000_3900	YES	YES	-	YES	-
Clb5DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB5_DATAEXCH_BASE	0x0000_3980	YES	YES	-	YES	-
Clb6LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB6_LOGICCFG_BASE	0x0000_3A00	YES	YES	-	YES	-
Clb6LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB6_LOGICCTL_BASE	0x0000_3B00	YES	YES	-	YES	-
Clb6DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB6_DATAEXCH_BASE	0x0000_3B80	YES	YES	-	YES	-
Clb7LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB7_LOGICCFG_BASE	0x0000_3C00	YES	YES	-	YES	-
Clb7LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB7_LOGICCTL_BASE	0x0000_3D00	YES	YES	-	YES	-
Clb7DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB7_DATAEXCH_BASE	0x0000_3D80	YES	YES	-	YES	-
Clb8LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	CLB8_LOGICCFG_BASE	0x0000_3E00	YES	YES	-	YES	-
Clb8LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	CLB8_LOGICCTL_BASE	0x0000_3F00	YES	YES	-	YES	-
Clb8DataExchRegs	CLB_DATA_EXCHANGE_REGS	CLB8_DATAEXCH_BASE	0x0000_3F80	YES	YES	-	YES	-
System Frame								
-	-	M0_RAM_BASE	0x0000_0000	YES	YES	-	-	-
-	-	M1_RAM_BASE	0x0000_0400	YES	YES	-	-	-
CpuTimer0Regs	CPUTIMER_REGS	CPUTIMER0_BASE	0x0000_0C00	YES	YES	-	-	-
CpuTimer1Regs	CPUTIMER_REGS	CPUTIMER1_BASE	0x0000_0C08	YES	YES	-	-	-
CpuTimer2Regs	CPUTIMER_REGS	CPUTIMER2_BASE	0x0000_0C10	YES	YES	-	-	-
PieCtrlRegs	PIE_CTRL_REGS	PIECTRL_BASE	0x0000_0CE0	YES	YES	-	-	-
PieVectTable	PIE_VECT_TABLE	PIEVECTTABLE_BASE	0x0000_0D00	YES	YES	-	-	-
DmaRegs	DMA_REGS	DMA_BASE	0x0000_1000	YES	YES	-	-	-
Dmach1Regs	DMA_CH_REGS	DMA_CH1_BASE	0x0000_1020	YES	YES	-	-	-
Dmach2Regs	DMA_CH_REGS	DMA_CH2_BASE	0x0000_1040	YES	YES	-	-	-
Dmach3Regs	DMA_CH_REGS	DMA_CH3_BASE	0x0000_1060	YES	YES	-	-	-
Dmach4Regs	DMA_CH_REGS	DMA_CH4_BASE	0x0000_1080	YES	YES	-	-	-
Dmach5Regs	DMA_CH_REGS	DMA_CH5_BASE	0x0000_10A0	YES	YES	-	-	-
Dmach6Regs	DMA_CH_REGS	DMA_CH6_BASE	0x0000_10C0	YES	YES	-	-	-
Cla1Regs	CLA_REGS	CLA1_BASE	0x0000_1400	YES	YES	-	-	-
-	-	CLATOCPU_RAM_BASE	0x0000_1480	YES	YES	-	YES	-
-	-	CPUTOCLA_RAM_BASE	0x0000_1500	YES	YES	-	YES	-
-	-	CLATODMA_RAM_BASE	0x0000_1680	YES	YES	YES	YES	-
-	-	DMATOCLA_RAM_BASE	0x0000_1700	YES	YES	-	YES	-
HRCap6Regs	HRCAP_REGS	HRCAP6_BASE	0x0000_5360	YES	YES	YES	YES	YES
HRCap7Regs	HRCAP_REGS	HRCAP7_BASE	0x0000_53A0	YES	YES	YES	YES	YES
McbspaRegs	McBSP_REGS	MCBSPA_BASE	0x0000_6000	YES	YES	YES	YES	YES
McbspbRegs	McBSP_REGS	MCBSPB_BASE	0x0000_6040	YES	YES	YES	YES	YES
BgcrcCpuRegs	BGCRC_REGS	BGCRC_CPU_BASE	0x0000_6340	YES	YES	-	-	YES
BgcrcCla1Regs	BGCRC_REGS	BGCRC_CLA1_BASE	0x0000_6380	YES	YES	-	YES	YES

Table 8-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	CPU 1	CPU 2	DMA	CLA	Pipeline Protected
Instance	Structure							
WdRegs	WD_REGS	WD_BASE	0x0000_7000	YES	YES	-	-	YES
NmiIntruptRegs	NMI_INTRUPT_REGS	NMI_BASE	0x0000_7060	YES	YES	-	-	YES
XintRegs	XINT_REGS	XINT_BASE	0x0000_7070	YES	YES	-	-	YES
SyncSocRegs	SYNC_SOC_REGS	SYNCSOC_BASE	0x0000_7940	YES	-	-	-	YES
DmaClaSrcSelRegs	DMA_CLA_SRC_SEL_REGS	DMACLASRCSEL_BASE	0x0000_7980	YES	YES	-	-	YES
GpioDataRegs	GPIO_DATA_REGS	GPIODATA_BASE	0x0000_7F00	YES	YES	-	YES	YES
GpioDataReadRegs	GPIO_DATA_READ_REGS	GPIODATAREAD_BASE	0x0000_7F80	YES	YES	-	YES	YES
-	-	LS0_RAM_BASE	0x0000_8000	YES	YES	-	YES	-
-	-	LS1_RAM_BASE	0x0000_8800	YES	YES	-	YES	-
-	-	LS2_RAM_BASE	0x0000_9000	YES	YES	-	YES	-
-	-	LS3_RAM_BASE	0x0000_9800	YES	YES	-	YES	-
-	-	LS4_RAM_BASE	0x0000_A000	YES	YES	-	YES	-
-	-	LS5_RAM_BASE	0x0000_A800	YES	YES	-	YES	-
-	-	LS6_RAM_BASE	0x0000_B000	YES	YES	-	YES	-
-	-	LS7_RAM_BASE	0x0000_B800	YES	YES	-	YES	-
-	-	D0_RAM_BASE	0x0000_C000	YES	YES	-	-	-
-	-	D1_RAM_BASE	0x0000_C800	YES	YES	YES	-	-
-	-	GS0_RAM_BASE	0x0000_D000	YES	YES	YES	-	-
-	-	GS1_RAM_BASE	0x0000_E000	YES	YES	YES	-	-
-	-	GS2_RAM_BASE	0x0000_F000	YES	YES	YES	-	-
-	-	GS3_RAM_BASE	0x0001_0000	YES	YES	YES	-	-
-	-	GS4_RAM_BASE	0x0001_1000	YES	YES	YES	-	-
-	-	GS5_RAM_BASE	0x0001_2000	YES	YES	YES	-	-
-	-	GS6_RAM_BASE	0x0001_3000	YES	YES	YES	-	-
-	-	GS7_RAM_BASE	0x0001_4000	YES	YES	YES	-	-
-	-	GS8_RAM_BASE	0x0001_5000	YES	YES	YES	-	-
-	-	GS9_RAM_BASE	0x0001_6000	YES	YES	YES	-	-
-	-	GS10_RAM_BASE	0x0001_7000	YES	YES	YES	-	-
-	-	GS11_RAM_BASE	0x0001_8000	YES	YES	YES	-	-
-	-	GS12_RAM_BASE	0x0001_9000	YES	YES	YES	-	-
-	-	GS13_RAM_BASE	0x0001_A000	YES	YES	YES	-	-
-	-	GS14_RAM_BASE	0x0001_B000	YES	YES	YES	-	-
-	-	GS15_RAM_BASE	0x0001_C000	YES	YES	YES	-	-
-	-	CMTOCPUXMSGRAM0_BASE	0x0003_8000	YES	YES	YES	-	-
-	-	CMTOCPUXMSGRAM1_BASE	0x0003_8400	YES	YES	YES	-	-
-	-	CPUXTOCMMSGRAM0_BASE	0x0003_9000	YES	YES	YES	-	-
-	-	CPUXTOCMMSGRAM1_BASE	0x0003_9400	YES	YES	YES	-	-
-	-	CPU1TOCPU2MSGRAM0_BASE	0x0003_A000	YES	YES	YES	-	-
-	-	CPU1TOCPU2MSGRAM1_BASE	0x0003_A400	YES	YES	YES	-	-
-	-	CPU2TOCPU1MSGRAM0_BASE	0x0003_B000	YES	YES	YES	-	-
-	-	CPU2TOCPU1MSGRAM1_BASE	0x0003_B400	YES	YES	YES	-	-
UsbRegs	USB_REGS	USBA_BASE	0x0004_0000	YES	-	YES	-	YES
Emif1Regs	EMIF_REGS	EMIF1_BASE	0x0004_7000	YES	YES	-	-	YES
Emif2Regs	EMIF_REGS	EMIF2_BASE	0x0004_7800	YES	-	-	-	YES

Table 8-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	CPU 1	CPU 2	DMA	CLA	Pipeline Protected
Instance	Structure							
CanaRegs	CAN_REGS	CANA_BASE	0x0004_8000	YES	YES	YES	-	YES
CanbRegs	CAN_REGS	CANB_BASE	0x0004_A000	YES	YES	YES	-	YES
EscssRegs	ESCSS_REGS	ESC_SS_BASE	0x0005_7E00	YES	-	-	-	YES
EscssConfigRegs	ESCSS_CONFIG_REGS	ESC_SS_CONFIG_BASE	0x0005_7F00	YES	-	-	-	YES
-	-	MCANA_DRIVER_BASE	0x0005_8000	YES	-	-	-	YES
McanaSsRegs	MCANSS_REGS	MCANASS_BASE	0x0005_C400	YES	-	-	-	YES
McanaRegs	MCAN_REGS	MCANA_BASE	0x0005_C600	YES	-	-	-	YES
McanaErrRegs	MCAN_ERROR_REGS	MCANA_ERROR_BASE	0x0005_C800	YES	-	-	-	YES
Cpu2toCpu1IpcRegs	CPU1TOCPU2_IPC_REGS_CPU2VIEW	-	0x0005_CE00	-	YES	-	-	YES
Cpu1toCpu2IpcRegs	CPU1TOCPU2_IPC_REGS_CPU1VIEW	IPC_CPUXTOCPUX_BASE	0x0005_CE00	YES	-	-	-	YES
FlashPumpSemaphoreRegs	FLASH_PUMP_SEMAPHORE_REGS	FLASHPUMPSEMAPHORE_BASE	0x0005_CE24	YES	YES	-	-	YES
Cpu2toCmIpcRegs	CPU2TOCM_IPC_REGS_CPU2VIEW	-	0x0005_CE40	-	YES	-	-	YES
Cpu1toCmIpcRegs	CPU1TOCM_IPC_REGS_CPU1VIEW	IPC_CPUXTOCM_BASE	0x0005_CE40	YES	-	-	-	YES
DevCfgRegs	DEV_CFG_REGS	DEVCFG_BASE	0x0005_D000	YES	-	-	-	YES
ClkCfgRegs	CLK_CFG_REGS	CLKCFG_BASE	0x0005_D200	YES	YES	-	-	YES
CpuSysRegs	CPU_SYS_REGS	CPUSYS_BASE	0x0005_D300	YES	YES	-	-	YES
SysStatusRegs	SYS_STATUS_REGS	SYSSTAT_BASE	0x0005_D400	YES	YES	-	-	YES
SysPeriphAcRegs	CPU2_PERIPH_AC_REGS	PERIPHAC_BASE	0x0005_D500	-	YES	-	-	YES
SysPeriphAcRegs	CPU1_PERIPH_AC_REGS	PERIPHAC_BASE	0x0005_D500	YES	-	-	-	YES
AnalogSubsysRegs	ANALOG_SUBSYS_REGS	ANALOGSUBSYS_BASE	0x0005_D700	YES	-	-	-	YES
CmConfRegs	CM_CONF_REGS	CMCONF_BASE	0x0005_DC00	YES	-	-	-	YES
HwbistRegs	HWBIST_REGS	HWBIST_BASE	0x0005_E000	YES	YES	-	-	YES
PbistRegs	PBIST_REGS	PBIST_BASE	0x0005_E200	YES	-	-	-	YES
Dcc0Regs	DCC_REGS	DCC0_BASE	0x0005_E700	YES	-	-	-	YES
Dcc1Regs	DCC_REGS	DCC1_BASE	0x0005_E740	YES	-	-	-	YES
Dcc2Regs	DCC_REGS	DCC2_BASE	0x0005_E780	YES	-	-	-	YES
EradGlobalRegs	ERAD_GLOBAL_REGS	ERAD_GLOBAL_BASE	0x0005_E800	YES	YES	-	-	YES
EradHWBP1Regs	ERAD_HWBP_REGS	ERAD_HWBP1_BASE	0x0005_E900	YES	YES	-	-	YES
EradHWBP2Regs	ERAD_HWBP_REGS	ERAD_HWBP2_BASE	0x0005_E908	YES	YES	-	-	YES
EradHWBP3Regs	ERAD_HWBP_REGS	ERAD_HWBP3_BASE	0x0005_E910	YES	YES	-	-	YES
EradHWBP4Regs	ERAD_HWBP_REGS	ERAD_HWBP4_BASE	0x0005_E918	YES	YES	-	-	YES
EradHWBP5Regs	ERAD_HWBP_REGS	ERAD_HWBP5_BASE	0x0005_E920	YES	YES	-	-	YES
EradHWBP6Regs	ERAD_HWBP_REGS	ERAD_HWBP6_BASE	0x0005_E928	YES	YES	-	-	YES
EradHWBP7Regs	ERAD_HWBP_REGS	ERAD_HWBP7_BASE	0x0005_E930	YES	YES	-	-	YES
EradHWBP8Regs	ERAD_HWBP_REGS	ERAD_HWBP8_BASE	0x0005_E938	YES	YES	-	-	YES
EradCounter1Regs	ERAD_COUNTER_REGS	ERAD_COUNTER1_BASE	0x0005_E980	YES	YES	-	-	YES
EradCounter2Regs	ERAD_COUNTER_REGS	ERAD_COUNTER2_BASE	0x0005_E990	YES	YES	-	-	YES
EradCounter3Regs	ERAD_COUNTER_REGS	ERAD_COUNTER3_BASE	0x0005_E9A0	YES	YES	-	-	YES
EradCounter4Regs	ERAD_COUNTER_REGS	ERAD_COUNTER4_BASE	0x0005_E9B0	YES	YES	-	-	YES
EradCRCGlobalRegs	ERAD_CRC_GLOBAL_REGS	ERAD_CRC_GLOBAL_BASE	0x0005_EA00	YES	YES	-	-	YES
EradCRC1Regs	ERAD_CRC_REGS	ERAD_CRC1_BASE	0x0005_EA10	YES	YES	-	-	YES
EradCRC2Regs	ERAD_CRC_REGS	ERAD_CRC2_BASE	0x0005_EA20	YES	YES	-	-	YES
EradCRC3Regs	ERAD_CRC_REGS	ERAD_CRC3_BASE	0x0005_EA30	YES	YES	-	-	YES
EradCRC4Regs	ERAD_CRC_REGS	ERAD_CRC4_BASE	0x0005_EA40	YES	YES	-	-	YES
EradCRC5Regs	ERAD_CRC_REGS	ERAD_CRC5_BASE	0x0005_EA50	YES	YES	-	-	YES

Table 8-3. Peripheral Registers Memory Map (continued)

Bit Field Name		DriverLib Name	Base Address	CPU 1	CPU 2	DMA	CLA	Pipeline Protected
Instance	Structure							
EradCRC6Regs	ERAD_CRC_REGS	ERAD_CRC6_BASE	0x0005_EA60	YES	YES	-	-	YES
EradCRC7Regs	ERAD_CRC_REGS	ERAD_CRC7_BASE	0x0005_EA70	YES	YES	-	-	YES
EradCRC8Regs	ERAD_CRC_REGS	ERAD_CRC8_BASE	0x0005_EA80	YES	YES	-	-	YES
DcsmZ1Regs	DCSM_Z1_REGS	DCSM_Z1_BASE	0x0005_F000	YES	YES	-	-	YES
DcsmZ2Regs	DCSM_Z2_REGS	DCSM_Z2_BASE	0x0005_F080	YES	YES	-	-	YES
DcsmCommonRegs	DCSM_COMMON_REGS	DCSMCOMMON_BASE	0x0005_F0C0	YES	YES	-	-	YES
MemCfgRegs	MEM_CFG_REGS	MEMCFG_BASE	0x0005_F400	YES	YES	-	-	YES
AccessProtectionRegs	ACCESS_PROTECTION_REGS	ACCESSPROTECTION_BASE	0x0005_F500	YES	YES	-	-	YES
MemoryErrorRegs	MEMORY_ERROR_REGS	MEMORYERROR_BASE	0x0005_F540	YES	YES	-	-	YES
RomWaitStateRegs	ROM_WAIT_STATE_REGS	ROMWAITSTATE_BASE	0x0005_F580	YES	YES	-	-	YES
RomPrefetchRegs	ROM_PREFETCH_REGS	ROMPREFETCH_BASE	0x0005_F588	YES	YES	-	-	YES
TestErrorRegs	TEST_ERROR_REGS	TESTERROR_BASE	0x0005_F590	YES	YES	-	-	YES
Flash0CtrlRegs	FLASH_CTRL_REGS	FLASH0CTRL_BASE	0x0005_F800	YES	YES	-	-	YES
Flash0EccRegs	FLASH_ECC_REGS	FLASH0ECC_BASE	0x0005_FB00	YES	YES	-	-	YES
UidRegs	UID_REGS	UID_BASE	0x0007_0200	YES	YES	-	-	-
CpuIdRegs	CPU_ID_REGS	CPUID_BASE	0x0007_0223	YES	YES	-	-	-
DcsmZ1OtpRegs	DCSM_Z1_OTP	DCSM_Z1OTP_BASE	0x0007_8000	YES	-	-	-	-
DcsmZ2OtpRegs	DCSM_Z2_OTP	DCSM_Z2OTP_BASE	0x0007_8200	YES	-	-	-	-

8.3.4 EMIF Chip Select Memory Map

The EMIF1 memory map is the same for both CPU subsystems. EMIF2 is available only on the CPU1 subsystem. The EMIF memory map is shown in the EMIF Chip Select Memory Map table.

Table 8-4. EMIF Chip Select Memory Map

EMIF CS	SIZE(3)	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EMIF1 CS0n - Data(1)	256M x 16	0x8000 0000	0x8FFF FFFF		Yes
EMIF1 CS0n - Program + Data(1)	1M x 16	0x0020 0000	0x002F FFFF		Yes
EMIF1 CS2n - Program + Data	2M x 16	0x0010 0000	0x002F FFFF		Yes
EMIF1 CS3n - Program + Data	512K x 16	0x0030 0000	0x0037 FFFF		Yes
EMIF1 CS4n - Program + Data	393K x 16	0x0038 0000	0x003D FFFF		Yes
EMIF2 CS0n - Data(2)	32M x 16	0x9000 0000	0x91FF FFFF		
EMIF2 CS2n - Program + Data(2)	4K x 16	0x0000 2000	0x0000 2FFF	Yes (Data only)	

(1) Dual Map - When EMIF1 CS0n is mapped at address 0x2x_xxxx, EMIF1 CS2n is only avaialble from 0x10_0000 to 0x1F_FFFF (1M x 16).
(2) Only on the CPU1 subsystem.
(3) Available memory size listed in this table is the maximum possible size assuming 32-bit memory. This may not apply to other memory sizes because of pin mux setting.

8.3.5 CM Memory Map

Table 8-5. CM Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	µDMA ACCESS	ENET DMA ACCESS	ECC/ PARITY	ACCESS PROTECTION	SECURITY
Boot ROM	64K x 8	0x0000 0000	0x0000 FFFF			Parity	Yes(1)	
Secure ROM	32K x 8	0x0001 0000	0x0001 7FFF			Parity	Yes(1)	Yes
Flash	512K x 8	0x0020 0000	0x0027 FFFF			ECC	Yes(1)	Yes
TI OTP(2)	2K x 8	0x0038 0000	0x0038 07FF			ECC	Yes(1)	
USER OTP	2K x 8	0x003C 0000	0x003C 07FF			ECC	Yes(1)	
C1 RAM	8K x 8	0x1FFF C000	0x1FFF DFFF			Parity	Yes(1)	Yes
C0 RAM	8K x 8	0x1FFF E000	0x1FFF FFFF			Parity	Yes(1)	Yes
S0 RAM	16K x 8	0x2000 0000	0x2000 3FFF	Yes	Yes	Parity	Yes(1)	
S1 RAM	16K x 8	0x2000 4000	0x2000 7FFF	Yes	Yes	Parity	Yes(1)	
S2 RAM	16K x 8	0x2000 8000	0x2000 BFFF	Yes	Yes	Parity	Yes(1)	
S3 RAM	16K x 8	0x2000 C000	0x2000 FFFF	Yes	Yes	Parity	Yes(1)	
E0 RAM	16K x 8	0x2001 0000	0x2001 3FFF	Yes	Yes	ECC	Yes(1)	
CPU1 to CM MSGRAM0	2K x 8	0x2008 0000	0x2008 07FF	Yes	Yes	Parity	Yes(1)	Yes
CPU1 to CM MSGRAM1	2K x 8	0x2008 0800	0x2008 0FFF	Yes	Yes	Parity	Yes(1)	
CM to CPU1 MSGRAM0	2K x 8	0x2008 2000	0x2008 27FF	Yes	Yes	Parity	Yes(1)	Yes
CM to CPU1 MSGRAM1	2K x 8	0x2008 2800	0x2008 2FFF	Yes	Yes	Parity	Yes(1)	
CPU2 to CM MSGRAM0	2K x 8	0x2008 4000	0x2008 47FF	Yes	Yes	Parity	Yes(1)	Yes
CPU2 to CM MSGRAM1	2K x 8	0x2008 4800	0x2008 4FFF	Yes	Yes	Parity	Yes(1)	
CM to CPU2 MSGRAM0	2K x 8	0x2008 6000	0x2008 67FF	Yes	Yes	Parity	Yes(1)	Yes
CM to CPU2 MSGRAM1	2K x 8	0x2008 6800	0x2008 6FFF	Yes	Yes	Parity	Yes(1)	
Bit Band RAM Zone	32M x 8	0x2200 0000	0x23FF FFFF	Yes	Yes	Parity	Yes(1)	
CAN A Message RAM	4K x 8	0x4007 2000	0x4007 2FFF			Parity	Yes(1)	
CAN B Message RAM	4K x 8	0x4007 6000	0x4007 6FFF			Parity	Yes(1)	
MCAN Message RAM	17K x 8	0x4007 8000	0x4007 C3FF			ECC	Yes(1)	
EtherCAT RAM (direct access)	16K x 8	0x400A 1000	0x400A 4FFF	Yes		Parity	Yes(1)	

(1) Access protection is done via MPU.
(2) TI OTP is for TI internal use only.

8.3.6 CM Flash Memory Map

The CM Flash Memory Map table shows the CM Flash memory map.

Table 8-6. CM Flash Memory Map

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP	2K x 8	0x0038 0000	0x0038 07FF
User OTP[(1)]	2K x 8	0x003C 0000	0x003C 07FF
Sectors			
Sector 0	16K x 8	0x0020 0000	0x0020 3FFF
Sector 1	16K x 8	0x0020 4000	0x0020 7FFF
Sector 2	16K x 8	0x0020 8000	0x0020 BFFF
Sector 3	16K x 8	0x0020 C000	0x0020 FFFF
Sector 4	64K x 8	0x0021 0000	0x0021 FFFF
Sector 5	64K x 8	0x0022 0000	0x0022 FFFF
Sector 6	64K x 8	0x0023 0000	0x0023 FFFF
Sector 7	64K x 8	0x0024 0000	0x0024 FFFF
Sector 8	64K x 8	0x0025 0000	0x0025 FFFF
Sector 9	64K x 8	0x0026 0000	0x0026 FFFF
Sector 10	16K x 8	0x0027 0000	0x0027 3FFF
Sector 11	16K x 8	0x0027 4000	0x0027 7FFF
Sector 12	16K x 8	0x0027 8000	0x0027 BFFF
Sector 13	16K x 8	0x0027 C000	0x0027 FFFF
Flash ECC Locations			
TI OTP ECC	256 x 8	0x0088 0000	0x0088 00FF
User OTP ECC	256 x 8	0x0088 8000	0x0088 80FF
Flash ECC (Sector 0)	2K x 8	0x0080 0000	0x0080 07FF
Flash ECC (Sector 1)	2K x 8	0x0080 0800	0x0080 0FFF
Flash ECC (Sector 2)	2K x 8	0x0080 1000	0x0080 17FF
Flash ECC (Sector 3)	2K x 8	0x0080 1800	0x0080 1FFF
Flash ECC (Sector 4)	8K x 8	0x0080 2000	0x0080 3FFF
Flash ECC (Sector 5)	8K x 8	0x0080 4000	0x0080 5FFF
Flash ECC (Sector 6)	8K x 8	0x0080 6000	0x0080 7FFF
Flash ECC (Sector 7)	8K x 8	0x0080 8000	0x0080 9FFF
Flash ECC (Sector 8)	8K x 8	0x0080 A000	0x0080 BFFF
Flash ECC (Sector 9)	8K x 8	0x0080 C000	0x0080 DFFF
Flash ECC (Sector 10)	2K x 8	0x0080 E000	0x0080 E7FF
Flash ECC (Sector 11)	2K x 8	0x0080 E800	0x0080 EFFF
Flash ECC (Sector 12)	2K x 8	0x0080 F000	0x0080 F7FF
Flash ECC (Sector 13)	2K x 8	0x0080 F800	0x0080 FFFF

(1) CM User OTP is available for general-purpose use.

8.3.7 Peripheral Registers Memory Map (CM)

Table 8-7. Peripheral Registers Memory Map (CM)

DriverLib Name	Base Address
AES_SS_BASE	0x4004_AC00
AES_BASE	0x4004_A000
NVIC_BASE	0xE000_E000
CPUTIMER0_BASE	0x4008_4000
CPUTIMER1_BASE	0x4008_4010
CPUTIMER2_BASE	0x4008_4020
NMI_BASE	0x4008_1000
WD_BASE	0x4008_0000
CMSYSCTL_BASE	0x400F_C000
DMPU_BASE	0x400C_C000
EMPU_BASE	0x400C_D000
CMMEMCFG_BASE	0x400F_E000
CMMEMORYERROR_BASE	0x400F_E400
CMMEMORYDIAGERROR_BASE	0x400F_E800
GCRC_BASE	0x4004_0000
UDMA_BASE	0x400F_F000
GPIODATA_BASE	0x4008_3000
GPIODATAREAD_BASE	0x4008_3100
I2C0_BASE	0x4002_0000
SSI0_BASE	0x4000_8000
UART0_BASE	0x4000_C000
IPC_CMTOCPU1_BASE	0x400F_D000
IPC_CMTOCPU2_BASE	0x400F_D080
FLASH0CTRL_BASE	0x400F_A000
FLASH0ECC_BASE	0x400F_A600
FLASHPUMPSEMAPHORE_BASE	0x400F_D048
EMAC_BASE	0x400C_0000
EMAC_SS_BASE	0x400C_2000
CANA_BASE	0x4007_0000
CANB_BASE	0x4007_4000
MCAN_SS_BASE	0x4007_C400
MCAN_BASE	0x4007_C600
MCAN_ERROR_BASE	0x4007_C800
MCAN0_BASE	0x4007_8000
DCSM_Z1_BASE	0x4008_5000
DCSM_Z2_BASE	0x4008_5100
DCSMCOMMON_BASE	0x4008_5180
ESC_BASE	0x400A_0000
ESC_SS_BASE	0x400A_FC00
ESC_SS_CONFIG_BASE	0x400A_FE00
USB0_BASE	0x4005_0000

8.3.8 Memory Types

8.3.8.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has four dedicated ECC-capable RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). D0/D1 memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection).

8.3.8.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have ECC. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

Table 8-8 lists the master access for the LSx RAM.

Table 8-8. Master Access for LSx RAM (With Assumption That all Other Access Protections are Disabled)

MSEL_LSx	CLAPGM_LSx	CPU ALLOWED ACCESS	CLA ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

8.3.8.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Each shared RAM block can be owned by either CPU subsystem based on the configuration of respective bits in the GSxMSEL register.

All GSx RAM blocks have parity.

When a GSx RAM block is owned by a CPU subsystem, the CPUx and CPUx.DMA will have full access to that RAM block whereas the other CPUy and CPUy.DMA will only have read access (no fetch/write access).

Table 8-9 lists the master access for the GSx RAM.

Table 8-9. Master Access for GSx RAM (With Assumption That all Other Access Protections are Disabled)

GSxMSEL	CPU	INSTRUCTION FETCH	READ	WRITE	CPUx.DMA READ	CPUx.DMA WRITE
0	CPU1	Yes	Yes	Yes	Yes	Yes
	CPU2	–	Yes	–	Yes	–
1	CPU1	–	Yes	–	Yes	–
	CPU2	Yes	Yes	Yes	Yes	Yes

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

8.3.8.4 CPU Message RAM (CPU MSGRAM)

These RAM blocks can be used to share data between CPU1 and CPU2. Since these RAMs are used for interprocessor communication, they are also called IPC RAMs. The CPU MSGRAMs have CPU/DMA read/write access from its own CPU subsystem, and CPU/DMA read only access from the other subsystem.

This RAM has parity.

8.3.8.5 CLA Message RAM (CLA MSGRAM)

These RAM blocks can be used to share data between the CPU and CLA. The CLA has read and write access to the CLA-to-CPU MSGRAM. The CPU has read and write access to the CPU-to-CLA MSGRAM. The CPU and CLA both have read access to both MSGRAMs. This RAM has parity.

8.3.8.6 CLA - DMA Message RAM (CLA-DMA MSGRAM)

These RAM blocks can be used to share data between the DMA and CLA. The CLA has read and write access to the CLA-to-DMA MSGRAM. The DMA has read and write access to the DMA-to-CLA MSGRAM. The DMA and CLA both have read access to both MSGRAMs. This RAM has parity.

8.3.8.7 CPUx - CM Message RAM (CPUx-CM MSGRAM)

These RAM blocks can be used to share data between CPU1/CPU2 and the CM. CPU1/CPU2 has read and write access to the CPUx-to-CM MSGRAM. The CM has read and write access to the CM-to-CPUx MSGRAM. CPUx and the CM both have read access to both MSGRAMs. This RAM has parity.

8.3.8.8 Dedicated RAM (C0/C1 RAM)

The CM subsystem has two dedicated RAM blocks: C0 and C1. These RAM blocks are tightly coupled with the Cortex-M4 (that is, only the CPU has access to them) and are connected via the ICODE/DCODE bus. These RAM blocks have an interleaving feature to improve performance. These RAMs have parity.

8.3.8.9 Shared RAM (E0 and Sx RAM)

The CM subsystem has shared RAMs that are accessible from the Cortex-M4 as well as other masters like µDMA and EtherNET DMA. These RAMs are connected via the system bus. These RAMs have an interleaving feature to improve performance. There are two types of shared RAM:

- E0 – This shared RAM block has ECC.
- Sx – This shared RAM block has parity.

8.4 Identification

Table 8-10 lists the Device Identification Registers.

Table 8-10. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDH	0x0005 D00A	2	Device part identification number	
			TMS320F28388D	0x03FF 0300
			TMS320F28386D	0x03FD 0300
			TMS320F28384D	0x03FB 0300
			TMS320F28388S	0x03FF 0400
			TMS320F28386S	0x03FD 0400
			TMS320F28384S	0x03FB 0400
REVID	0x0005 D00C	2	Silicon revision number	
			Revision 0	0x0000 0000
			Revision A	0x0000 0001
UID_UNIQUE	0x0007 020C	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This can be used as a serial number in the application. This number is present only on TMS devices.	
CPU ID	0x0007 0223	1	CPU identification number	
			CPU1	0xXX01
			CPU2	0xXX02
	0x0038 0446	1	CM	0xXX03
JTAGID	N/A	N/A	JTAG Device ID	0x0BB4 002F

8.5 Bus Architecture – Peripheral Connectivity

The C28x Bus Master Peripheral Access table provides a broad view of the peripheral and configuration register accessibility from each bus master on the C28x. Peripherals can be individually assigned to the CPU1 or CPU2 subsystem (for example, ePWM can be assigned to CPU1 and eQEP assigned to CPU2).

Table 8-11. C28x Bus Master Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.CLA1	CPU2.DMA
Peripherals that can be assigned to CPU1 or CPU2 and have Secondary Masters						
Peripheral Frame 1: - ePWM - SDFM - eCAP[(1)] - eQEP[(1)] - CMPSS[(1)] - DAC[(1)] - HRPWM	Y	Y	Y	Y	Y	Y
Peripheral Frame 2: - SPI - McBSP - FSI - PMBus	Y	Y	Y	Y	Y	Y
Peripherals that can be assigned to CPU1 or CPU2 subsystems						
SCI			Y	Y		
I2C			Y	Y		
CAN[(5)]	Y		Y	Y		Y
ADC Configuration		Y	Y	Y	Y	
EMIF1	Y		Y	Y		Y
Peripherals and Device Configuration Registers only on CPU1 subsystem						
EMIF2		Y	Y			
USB[(5)]			Y			
EtherCAT[(5)]	Y	Y	Y			
DCC			Y			
Device Capability, Peripheral Reset, Peripheral CPU Select			Y			
GPIO Pin Mapping and Configuration			Y			
Analog System Control			Y			
Reset Configuration			Y			
Accessible by only one CPU at a time with Semaphore						
Clock and PLL Configuration			Y	Y		
Peripherals and Registers with Unique Copies of Registers for each CPU and CLA Master[(2)]						
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y	Y		
Flash Configuration[(3)]			Y	Y		
CPU Timers			Y	Y		
DMA and CLA Trigger Source Select			Y	Y		

Table 8-11. C28x Bus Master Peripheral Access (continued)

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1	CPU2	CPU2.CLA1	CPU2.DMA
ERAD			Y	Y		
GPIO Data(4)		Y	Y	Y	Y	
ADC Results	Y	Y	Y	Y	Y	Y

(1) These modules are on a Peripheral Frame with DMA access; however, they cannot trigger a DMA transfer.
(2) Each CPUx and CPUx.CLA1 can only access its own copy of these registers.
(3) At any given time, only one CPU can perform program or erase operations on the Flash.
(4) The GPIO Data Registers are unique for each CPUx and CPUx.CLAx. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO.
(5) Accessible from CM as well.

The CM Bus Master Peripheral Access table provides details about peripheral sharing between CPUx and the CM subsystem. It also provides details about accessibility from different masters within the CM subsystem to peripherals that are only accessible from the CM subsystem. Peripherals can be individually assigned to CPUx or to the CM subsystem (for example, CAN can be assigned to CPUx and USB assigned to CM).

Table 8-12. CM Bus Master Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	ETHERNET DMA	µDMA	M4	CPU1 SUBSYSTEM	CPU2 SUBSYSTEM
Peripherals that can be assigned to CM, CPU1, or CPU2 subsystem					
CAN		Y	Y	Y	Y
Peripherals that can be assigned to CM or CPU1 subsystem					
EtherCAT		Y	Y	Y	
USB		Y	Y	Y	
MCAN (CAN FD)			Y	Y	
Peripherals and System Registers only on CM subsystem					
AES		Y	Y		
GCRC		Y	Y		
CM-I2C		Y	Y		
CM-UART		Y	Y		
SSI		Y	Y		
EtherNet		Y	Y		
GPIO Data			Y		
Peripheral Reset			Y		
CM System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y		
Flash Configuration			Y		
CPU Timers			Y		
µDMA			Y		

8.6 Boot ROM and Peripheral Booting

On every reset, the device executes a boot sequence in the ROM, depending on the reset type and boot configuration. This sequence initializes the device to run the application code. For CPU1, the boot ROM also contains peripheral bootloaders that can be used to load an application into RAM. These bootloaders can be disabled for safety or security purposes.

Table 8-13 summarizes available boot features across CPU1, CPU2, and CM. Table 8-14 lists the sizes of the various ROMs on the device.

Table 8-13. Boot System Overview

BOOT FEATURE	CPU1 (MASTER)	CPU2	CM
Initiate boot process	Device Reset	CPU1 Application	CPU1 Application
Boot mode selection	GPIOs	IPC Register	IPC Register
Supported boot modes: • Flash boot • Secure Flash boot • RAM boot	Yes	Yes	Yes
Boot to User OTP	No	Yes	Yes
Copy from IPC Message RAM and boot to RAM	No	Yes	Yes
Peripheral boot loader support	Yes	No	No

Table 8-14. ROM Memory

ROM	CPU1 SIZE	CPU2 SIZE	CM SIZE
Unsecure boot ROM	192KB	64KB	64KB
Secure ROM	64KB	64KB	32KB
CLA data ROM	8KB	8KB	N/A

8.6.1 Device Boot

This section describes the general boot ROM procedure each time a CPU core is reset. CPU1 is the master and always boots first. Once CPU1 boots to the application, then the user's application code in CPU1 can configure the CPU2/CM boot IPC registers and release CPU2/CM from reset to boot. Table 8-15, Table 8-16, and Table 8-17 list the general boot-up procedures for each core.

During boot, each CPU's boot ROM code updates a boot status location in RAM that details the actions taken during this process. Additionally, CPU2 writes the boot status to the CPU2TOCPU1IPCBOOTSTS register and CM writes to CMTOCPU1IPCBOOTSTS to communicate the statuses to CPU1.

For more details, see the Boot Status information section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

Table 8-15. CPU1 Boot ROM Procedure

STEP	CPU1 ACTION
1	After reset, check for HWBIST reset. If there is a HWBIST reset, immediately branch and return to the user application. If there is no HWBIST reset, then continue boot and check the FUSE error register for any errors and handle accordingly.
2	Clock configuration and flash power up
3	Peripheral trimming and device configuration registers are loaded from OTP.
4	On power-on reset (POR), all CPU1 RAMs are initialized.
5	Nonmaskable interrupt (NMI) handling is enabled and DCSM initialization is performed.
6	Device calibration is performed; trimming the specified peripherals with set OTP values.
7	Determine if polling the GPIO pins are needed for determining the boot mode and, if so, read the boot mode GPIO pins to determine the boot mode to run.
8	Based on the boot mode and options, the appropriate boot sequence is executed. For a flow chart of the CPU1 boot sequences, see the CPU1 Device Boot Flow figure in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

Table 8-16. CPU2 Boot ROM Procedure

STEP	CPU2 ACTION
1	CPU2 is released from reset by CPU1 application.
2	Once CPU1TOCPU2IPCFLG0 is set, read the CPU1TOCPU2IPCBOOTMODE register. If it is not set correctly or has an invalid value, the IPC error command is sent to CPU1, and the CPU2 core will enter an infinite loop and will not continue booting until the user corrects the register values and reset the CPU2.
3	Flash power up
4	On POR, all CPU2 RAMs are initialized.
5	NMI handling is enabled.
6	Based on the boot mode set in the CPU1TOCPU2IPCBOOTMODE register, CPU2 either enters the "wait for command" mode to wait for a future CPU1 boot mode command, or CPU2 executes the requested boot sequence. For a flow chart of the CPU2 boot sequences, see the CPU2 Boot Flow figure in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

Table 8-17. CM Boot ROM Procedure

STEP	CM ACTION
1	CM is released from reset by the CPU1 application.
2	Once CPU1TOCMIPCFLG0 is set, read the CPU1TOCMIPCBOOTMODE register. If it is not set correctly or has an invalid value, the IPC error command is sent to CPU1, and the CM will enter an infinite loop and will not continue booting until the user corrects the register values and reset the CM.
3	Flash power up
4	On POR, all CM RAMs are initialized.
5	NMI handling is enabled.
6	Based on the boot mode set in the CPU1TOCPU2IPCBOOTMODE register, CM either enters the "wait for command" mode to wait for a future CPU1 boot mode command, or CM executes the requested boot sequence. For a flow chart of the CM boot sequences, see the CM Boot Flow figure in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

8.6.2 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes, supported on this device. The CPU1 boot ROM uses the boot-mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration. The CPU2 boot ROM uses the CPU1TOCPU2IPCBOOTMODE register to determine the boot mode configuration. The CM boot ROM uses the CPU1TOCMIPCBOOTMODE register to determine the boot mode configuration.

Table 8-18 lists the CPU1 boot mode options available for selection by the default boot-mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot-mode select pin GPIOs used.

All the available boot modes on the device are listed in Table 8-20.

Table 8-18. Device Default Boot Modes for CPU1

BOOT MODE	GPIO72 (DEFAULT BOOT MODE SELECT PIN 1)	GPIO84 (DEFAULT BOOT MODE SELECT PIN 0)
Parallel IO	0	0
SCI/Wait Boot(1)	0	1
CAN	1	0
Flash/USB(2)	1	1

(1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.
(2) On an unprogrammed device, selecting flash boot when the default flash entry address is unprogrammed will switch the boot mode from flash boot to USB boot. For more details, see Table 8-19.

Table 8-19. CPU1 Flash-to-USB Boot Decision Table

VALUE AT FLASH ENTRY POINT ADDRESS	REASON FOR VALUE	REALIZED BOOT MODE
0x00000000	Flash is locked/secured	Boot to Flash
0xFFFFFFFF	Flash is not programmed	USB Boot
Any other value	Flash is programmed	Boot to Flash

Note

The switch from flash boot mode to USB boot mode when flash is locked/secured or not programmed is *only available* as part of the default boot mode table on an unprogrammed device. Once a custom boot table is programmed in OTP or RAM, a selection of flash boot mode *will not* switch to USB boot even when the flash is unprogrammed.

Table 8-20. All Available Boot Modes

BOOT MODE	CPU SUPPORT	DETAILS
Parallel IO	CPU1	For functional details of the boot modes, see the Boot Modes section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*. For boot table values and GPIOs for the boot modes, see Section 8.6.4.
SCI / Wait	CPU1	
CAN	CPU1	
Flash	CPU1, CPU2, CM	
Wait	CPU1, CPU2, CM	
RAM	CPU1, CPU2, CM	
SPI	CPU1	
I2C	CPU1	
USB(1)	CPU1	
Secure Flash	CPU1, CPU2, CM	
User OTP	CPU2, CM	
IPC Message Copy to RAM	CPU2, CM	

(1) The USB Bootloader will switch the clock source to the external crystal oscillator (X1 and X2 pins). A 20-MHz crystal should be present on the board if this boot mode is selected.

Note

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this section, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

8.6.3 Device Boot Configurations

This device supports from 0 boot-mode select pin to up to 3 boot-mode select pins as well as from 1 configured boot mode to up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, do the following steps:

1. Determine all the various ways you want the application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, and so forth.)
2. Based on the number of boot modes needed, determine how many boot-mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot-mode options.)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO50, BMSP1 to GPIO51, and BMSP2 left as default which is disabled.) For details on performing these configurations, see the Configuring Boot Mode Pins for CPU1 section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. (For example, BOOTDEF0 = Boot to Flash, BOOTDEF1 = CAN Boot, BOOTDEF2 = SCI Boot; all other BOOTDEFx are left as default/nothing.) For details on setting up and configuring the custom boot mode table, see the Configuring Boot Mode Table Options for CPU1 section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

For example use cases on how to configure the BMSPs and custom boot tables, see the Boot Mode Example Use Cases section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

8.6.4 GPIO Assignments for CPU1

This section details the GPIOs and boot option values used for each CPU1 boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. See the Configuring Boot Mode Table Options for CPU1 section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual* on how to configure BOOT_DEF. When selecting a boot mode option, be sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Note

These configurations only apply to CPU1. For details on configuring CPU2 and CM boot modes, see the Booting CPU2 and CM section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

Table 8-21. SCI Boot Options

OPTION	BOOTDEF VALUE	SCITXDA GPIO	SCIRXDA GPIO
0 (default)	0x01	GPIO29	GPIO28
1	0x21	GPIO84	GPIO85
2	0x41	GPIO36	GPIO35
3	0x61	GPIO42	GPIO43
4	0x81	GPIO65	GPIO64
5	0xA1	GPIO135	GPIO136
6	0xC1	GPIO8	GPIO9

Table 8-22. CAN Boot Options

OPTION	BOOTDEF VALUE	CANTXA GPIO	CANRXA GPIO
0 (default)	0x02	GPIO37	GPIO36
1	0x22	GPIO71	GPIO70
2	0x42	GPIO63	GPIO62
3	0x62	GPIO19	GPIO18
4	0x82	GPIO4	GPIO5
5	0xA2	GPIO31	GPIO30

Table 8-23. I2C Boot Options

OPTION	BOOTDEF VALUE	SDAA GPIO	SCLA GPIO
0	0x07	GPIO91	GPIO92
1	0x27	GPIO32	GPIO33
2	0x47	GPIO42	GPIO43
3	0x67	GPIO0	GPIO1
4	0x87	GPIO104	GPIO105

Table 8-24. USB Boot Options

OPTION	BOOTDEF VALUE	USBDM GPIO	USBDP GPIO
0 (default)	0x09	GPIO42	GPIO43

Table 8-25. RAM Boot Options

OPTION	BOOTDEF VALUE	RAM ENTRY POINT (ADDRESS)
0	0x05	0x0000 0000

Table 8-26. Flash Boot Options

OPTION	BOOTDEF VALUE	FLASH ENTRY POINT (ADDRESS)	FLASH SECTOR
0 (default)	0x03	0x0008 0000	CPU1 Bank 0 Sector 0
1	0x23	0x0008 8000	CPU1 Bank 0 Sector 4
2	0x43	0x000A 8000	CPU1 Bank 0 Sector 8
3	0x63	0x000B E000	CPU1 Bank 0 Sector 13

Table 8-27. Secure Flash Boot Options

OPTION	BOOTDEF VALUE	FLASH ENTRY POINT (ADDRESS)	FLASH SECTOR
0	0x0A	0x0008 0000	CPU1 Bank 0 Sector 0
1	0x2A	0x0008 8000	CPU1 Bank 0 Sector 4
2	0x4A	0x000A 8000	CPU1 Bank 0 Sector 8
3	0x6A	0x000B E000	CPU1 Bank 0 Sector 13

Table 8-28. Wait Boot Options

OPTION	BOOTDEF VALUE	WATCHDOG
0	0x04	Enabled
1	0x24	Disabled

Table 8-29. SPI Boot Options

OPTION	BOOTDEF VALUE	SPISIMOA	SPISOMIA	SPICLKA	SPISTEA
0	0x06	GPIO58	GPIO59	GPIO60	GPIO61
1	0x26	GPIO16	GPIO17	GPIO18	GPIO19
2	0x46	GPIO32	GPIO33	GPIO34	GPIO35
3	0x66	GPIO16	GPIO17	GPIO56	GPIO57
4	0x86	GPIO54	GPIO55	GPIO56	GPIO57

Table 8-30. Parallel Boot Options

OPTION	BOOTDEF VALUE	D0-D7 GPIO	DSP CONTROL GPIO	HOST CONTROL GPIO
0 (default)	0x0	D0 - GPIO89 D1 - GPIO90 D2 - GPIO58 D3 - GPIO59 D4 - GPIO60 D5 - GPIO61 D6 - GPIO62 D7 - GPIO88	GPIO91	GPIO92

8.7 Dual Code Security Module (DCSM)

The dual code security module (DCSM) is a security feature incorporated in this device. It prevents access and visibility to on-chip secure memories (and other secure resources) by unauthorized persons. It also prevents duplication and reverse-engineering of proprietary code. The term “secure” means that access to on-chip secure memories and resources is blocked. The term “unsecure” means that access is allowed; that is, the contents of the memory could be read by any means (for example, through a debugging tool such as Code Composer Studio™).

There are two security zones, Zone1 (Z1) and Zone2 (Z2). Unlike earlier C2000 devices where each CPU subsystem had two security zones, on this device, both security zones are shared by each CPU subsystem. This means secure resources from each CPU subsystem are allocated to Zone1 or Zone2. All the security configurations are controlled by the CPU1 subsystem only (programmed in CPU1 USER OTP), but other CPU subsystems have access to these configurations via their own memory map registers.

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in CPU1 USER OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP.

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

8.8 C28x (CPU1/CPU2) Subsystem

8.8.1 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*. For more information on the C28x Floating Point Unit (FPU), Trigonometric Math Unit, and Cyclic Redundancy Check (VCRC) instruction sets, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*. A brief overview of the FPU, TMU, and VCRC are provided here.

8.8.1.1 Floating-Point Unit

The C28x plus floating-point (C28x+FPU64) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support both IEEE single-precision and double-percision floating-point operations.

Devices with the C28x+FPU64 include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point Result registers, RnH (where n = 0–7)
- Floating-point Status register (STF)
- Repeat Block register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

8.8.1.2 Trigonometric Math Unit

The TMU extends the capabilities of a C28x+FPU64 by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 8-31.

Table 8-31. TMU Supported Instructions

INSTRUCTIONS	C EQIVALENT OPERATION	PIPELINE CYCLES
MPY2PIF32/64 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32/64 RaH,RbH	a = b / 2pi	2/3
DIVF32/64 RaH,RbH,RcH	a = b/c	5
SQRTF32/64 RaH,RbH	a = sqrt(b)	5
SINPUF32/64 RaH,RbH	a = sin(b*2pi)	4
COSPUF32/64 RaH,RbH	a = cos(b*2pi)	4
ATANPUF32/64 RaH,RbH	a = atan(b)/2pi	4
QUADF32/64 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations.

8.8.1.3 Fast Integer Division Unit

The Fast Integer Division (FINTDIV) unit of the C28x CPU uniquely supports three types of integer division (Truncated, Modulus, Euclidean) of varying data type sizes (16/16, 32/16, 32/32, 64/32, 64/64) in unsigned or signed formats.

- Truncated integer division is naturally supported by C language (/, % operators).
- Modulus and Euclidean divisions are variants that are more efficient for control algorithms and are supported by C intrinsics.

All three types of integer division produce both a quotient and remainder component, are interruptible, and execute in a minimum number of deterministic cycles (10 cycles for a 32/32 division). In addition, the Fast Division capabilities of the C28x CPU uniquely support fast execution of floating-point 32-bit (in 5 cycles) and 64-bit (in 20 cycles) division.

For more information about fast integer division, see the *Fast Integer Division – A Differentiated Offering From C2000™ Product Family Application Report*.

8.8.1.4 VCRC Unit

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCRC can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCRC can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The following are the CRC polynomials used by the CRC calculation logic of the VCRC:

- CRC8 polynomial = 0x07
- CRC16 polynomial1 = 0x8005
- CRC16 polynomial2 = 0x1021
- CRC24 polynomial = 0x5d6dcb
- CRC32 polynomial1 = 0x04c11db7
- CRC32 polynomial2 = 0x1edc6f41

This module can calculate CRCs for a byte of data in a single cycle. The CRC calculation for CRC8, CRC16, CRC24, and CRC32 is done byte-wise (instead of computing on a complete 16-bit or 32-bit data read by the C28x core) to match the byte-wise computation requirement mandated by various standards.

The VCRC Unit also allows the user to provide the size (1b-32b) and value of any polynomial to fit custom CRC requirements. The CRC execution time increases to three cycles when using a custom polynomial.

8.8.2 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the System Event Counter units.

- The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events.
- The System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software.

This significantly increases the debug capabilities of many real-time systems. In the TMS320F2838x devices, the ERAD module contains eight Enhanced Bus Comparator units (which increases the number of Hardware breakpoints from two to ten) and four System Event Counter units. Figure 8-2 shows the ERAD module.

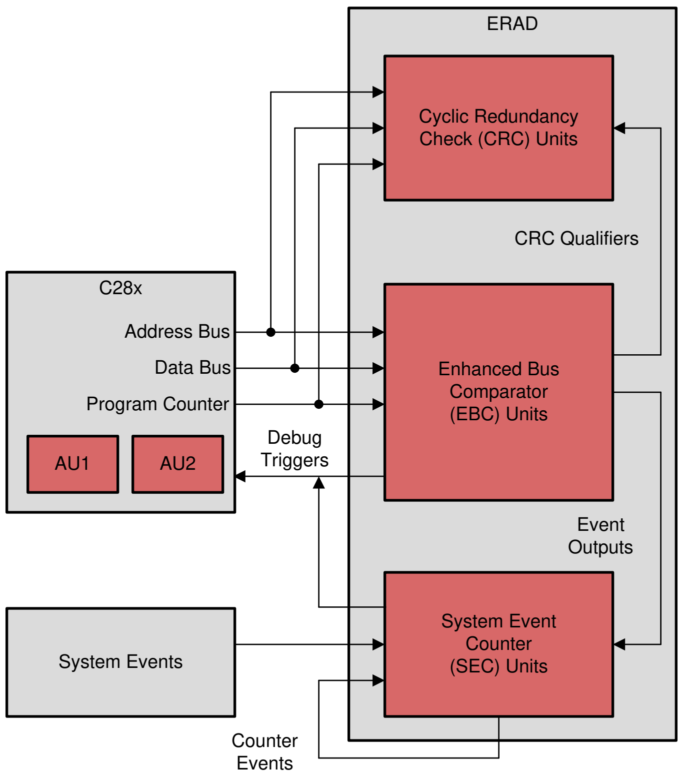


Figure 8-2. ERAD Overview

8.8.3 Background CRC-32 (BGCRC)

The Background CRC (BGCRC) module computes a CRC-32 on a configurable block of memory. It accomplishes this by fetching the specified block of memory during idle cycles (when the CPU, CLA, or DMA is not accessing the memory block). The calculated CRC-32 value is compared against a golden CRC-32 value to indicate a pass or fail. In essence, the BGCRC helps identify memory faults and corruption. There are two BGCRC modules (CPU_CRC and CLA_CRC) per CPU subsystem. The two BGCRC modules differ only in the memories they test.

The BGCRC module has the following features:

- One cycle CRC-32 computation on 32 bits of data
- No CPU bandwidth impact for zero wait state memory
- Minimal CPU bandwidth impact for non-zero wait state memory
- Dual operation modes (CRC-32 mode and scrub mode)
- Watchdog timer to time CRC-32 completion
- Ability to pause and resume CRC-32 computation

Figure 8-3 shows the memory map of the BGCRC module.

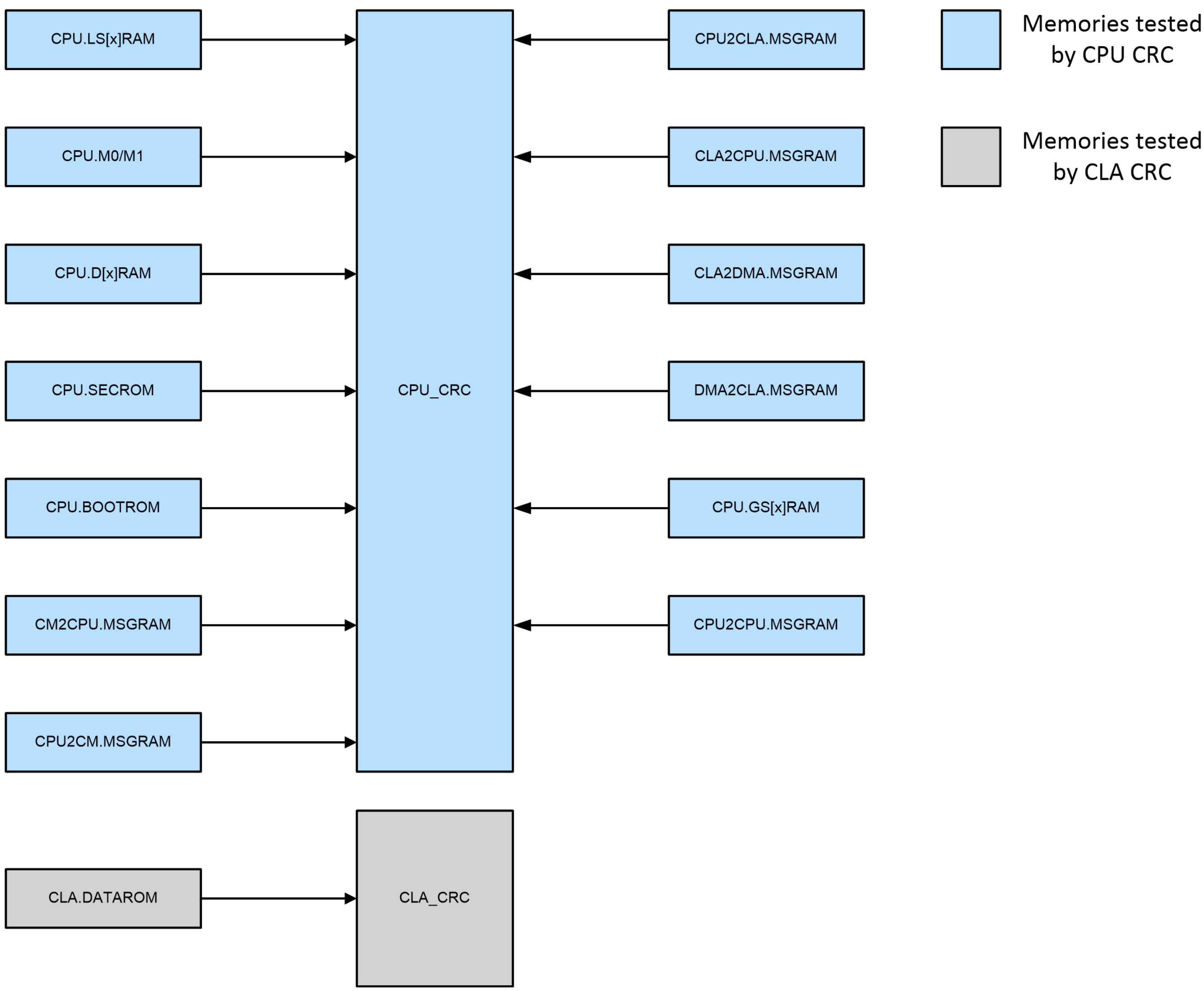


Figure 8-3. BGCRC Memory Map

8.8.4 Control Law Accelerator (CLA)

The CLA Type-2 is an independent, fully programmable, 32-bit floating-point math processor that brings concurrent control-loop execution to the C28x family. The low interrupt-latency of the CLA allows it to read ADC samples "just-in-time." This significantly reduces the ADC sample to output delay to enable faster system response and higher frequency control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics.

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Using the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently.

The following is a list of major features of the CLA:

- C compilers are available for CLA software development.
- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
  - Complete bus architecture:
    - Program Address Bus (PAB) and Program Data Bus (PDB)
    - Data Read Address Bus (DRAB), Data Read Data Bus (DRDB), Data Write Address Bus (DWAB), and Data Write Data Bus (DWDB)
  - Independent 8-stage pipeline
  - 16-bit program counter (MPC)
  - Four 32-bit result registers (MR0 to MR3)
  - Two 16-bit auxiliary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions
  - Conditional branch and call
  - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines, or seven tasks and a main background task.
  - The start address of each task is specified by the MVECT registers.
  - There is no limit on task size as long as the tasks fit within the configurable CLA program memory space.
  - One task is serviced at a time until its completion. There is no nesting of tasks.
  - Upon task completion, a task-specific interrupt is flagged within the PIE.
  - When a task finishes, the next highest-priority pending task is automatically started.
  - The Type-2 CLA can have a main task that runs continuously in the background, while other high-priority events trigger a foreground task.
- Task trigger mechanisms:
  - C28x CPU through the IACK instruction
  - Task1 to Task8: Up to 256 possible trigger sources from peripherals connected to the shared bus on which the CLA assumes secondary ownership
  - Task8 can be set to be the background task, while Tasks 1 to 7 take peripheral triggers.

- Memory and shared peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU.
  - Two dedicated message RAMs for communication between the CLA and the DMA.
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.

Figure 8-4 shows the CLA block diagram.

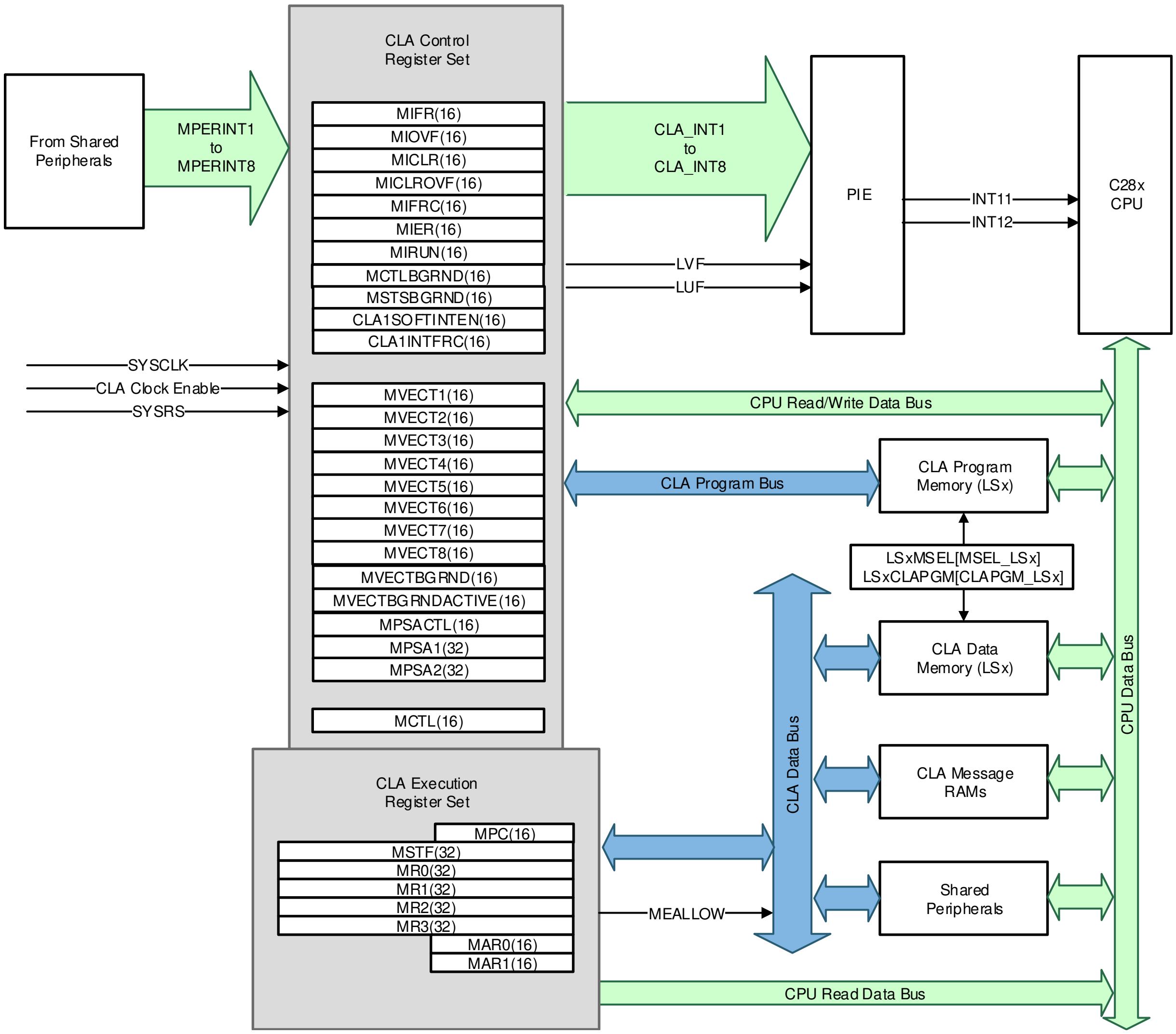


Figure 8-4. CLA Block Diagram

8.8.5 Direct Memory Access (DMA)

Each CPU has its own 6-channel DMA module. The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the DMA trigger source, there is no mechanism within the module itself to start memory transfers periodically. The DMA module has six independent DMA channels that can be configured separately. Each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others. At the heart of the DMA is a state machine and tightly coupled address control logic. It is this address control logic that allows for rearrangement of the block of data during the transfer as well as the process of ping-ponging data between buffers.

DMA features include:

- Six channels with independent PIE interrupts
- Each DMA channel can be triggered from multiple peripheral trigger sources independently.
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: 3 cycles/word without arbitration

Figure 8-5 shows a device-level block diagram of the DMA.

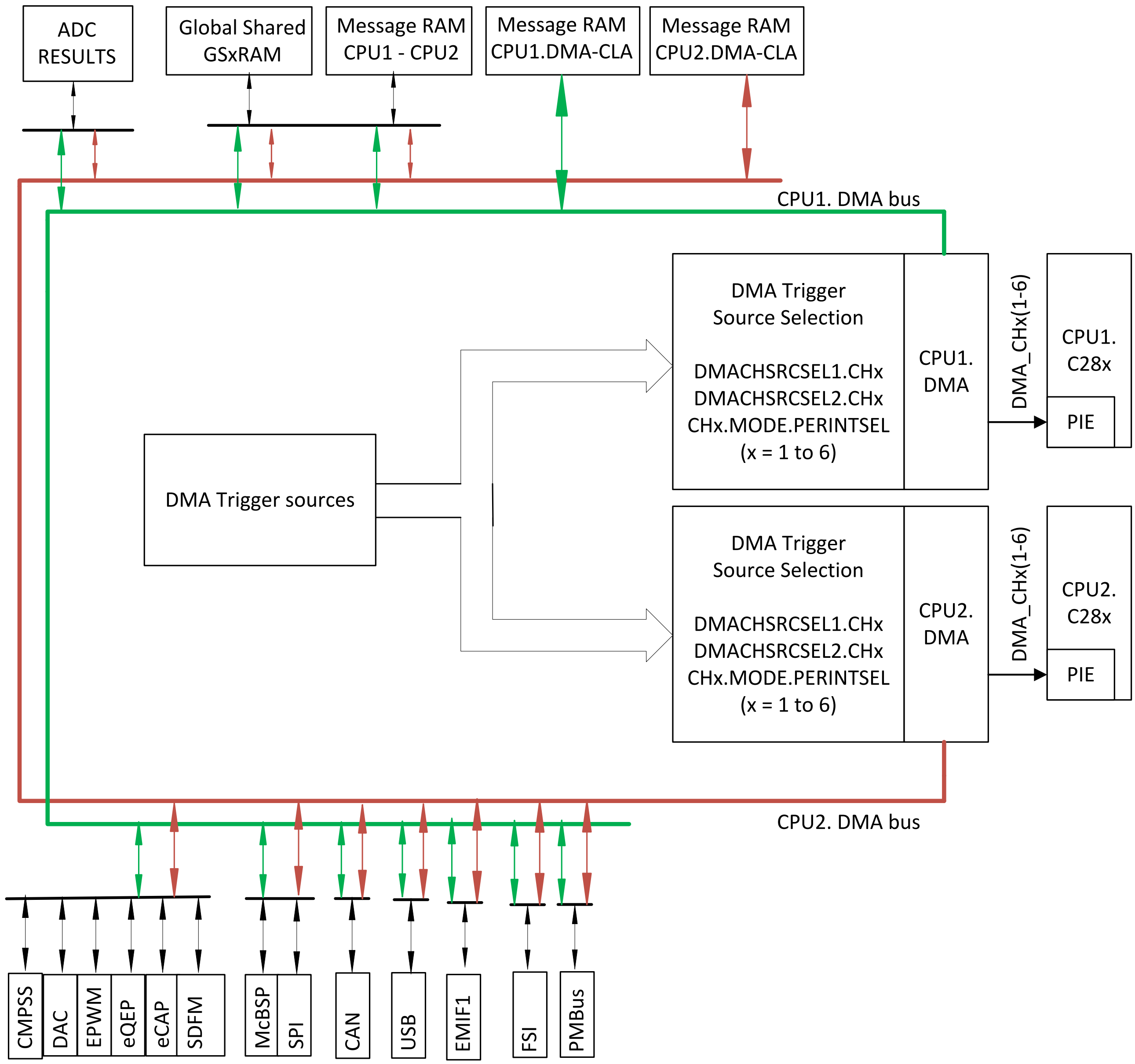


Figure 8-5. DMA Block Diagram

8.8.6 Interprocessor Communication (IPC) Module

The Interprocessor Communication (IPC) module allows communications between the CPU subsystems.

IPC features include:

- Message RAMs
- IPC flags and interrupts
- IPC command registers
- Flash pump semaphore
- Clock configuration semaphore
- Free-running counter

All IPC features are independent of each other, and most do not require any specific data format. There are also two registers for boot mode and status communication. For more information on these registers, see the ROM Code and Peripheral Booting chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

This device has three cores [one Cortex-M4 core and two C28x cores (CPU1, CPU2)] and three different IPC modules:

- CPU1_TO_CPU2 IPC architecture (see Figure 8-6)
- CPUx_TO_CM IPC architecture (where x = 1, 2) (see Figure 8-7)

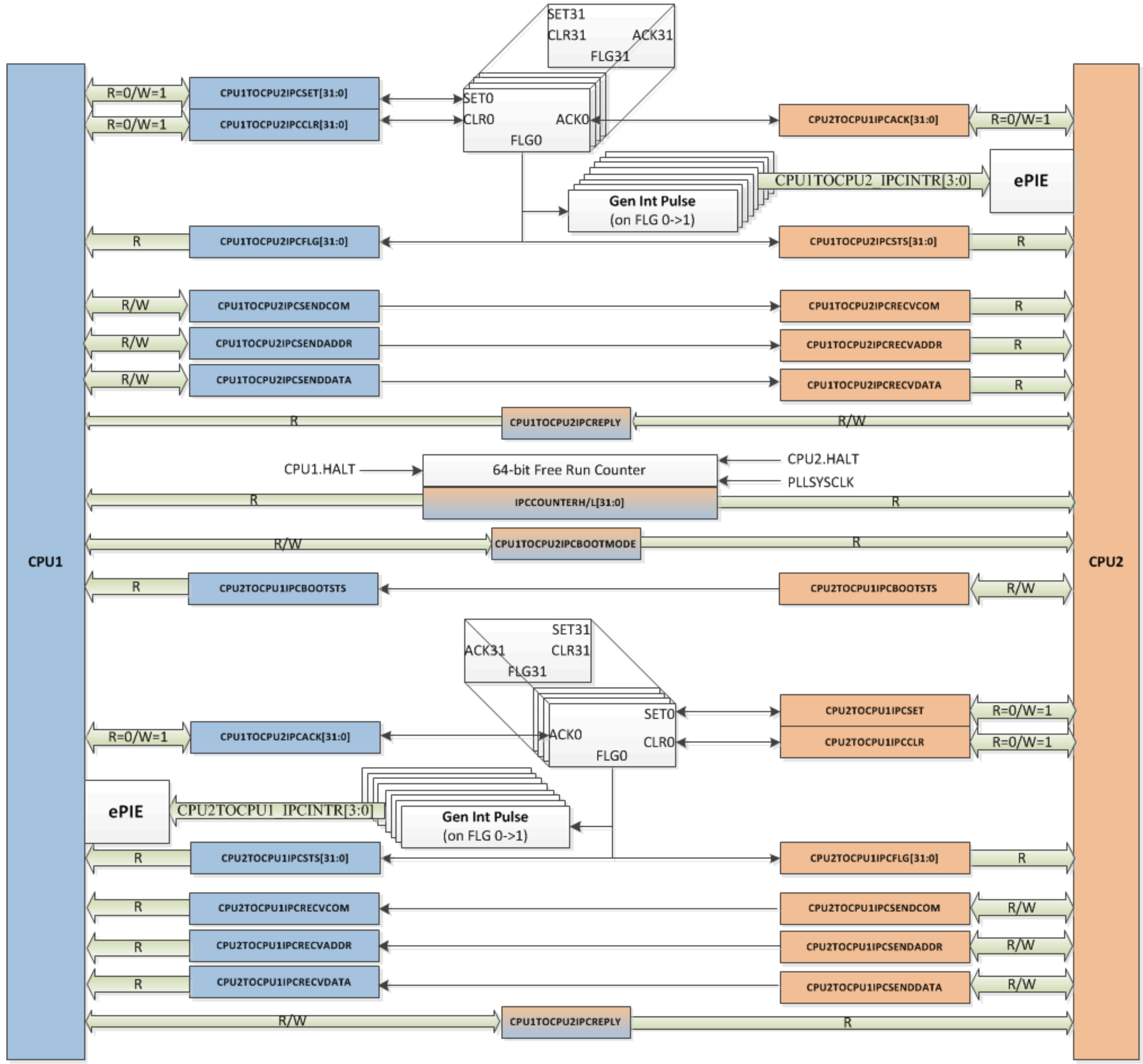


Figure 8-6. CPU1_TO_CPU2 IPC Module

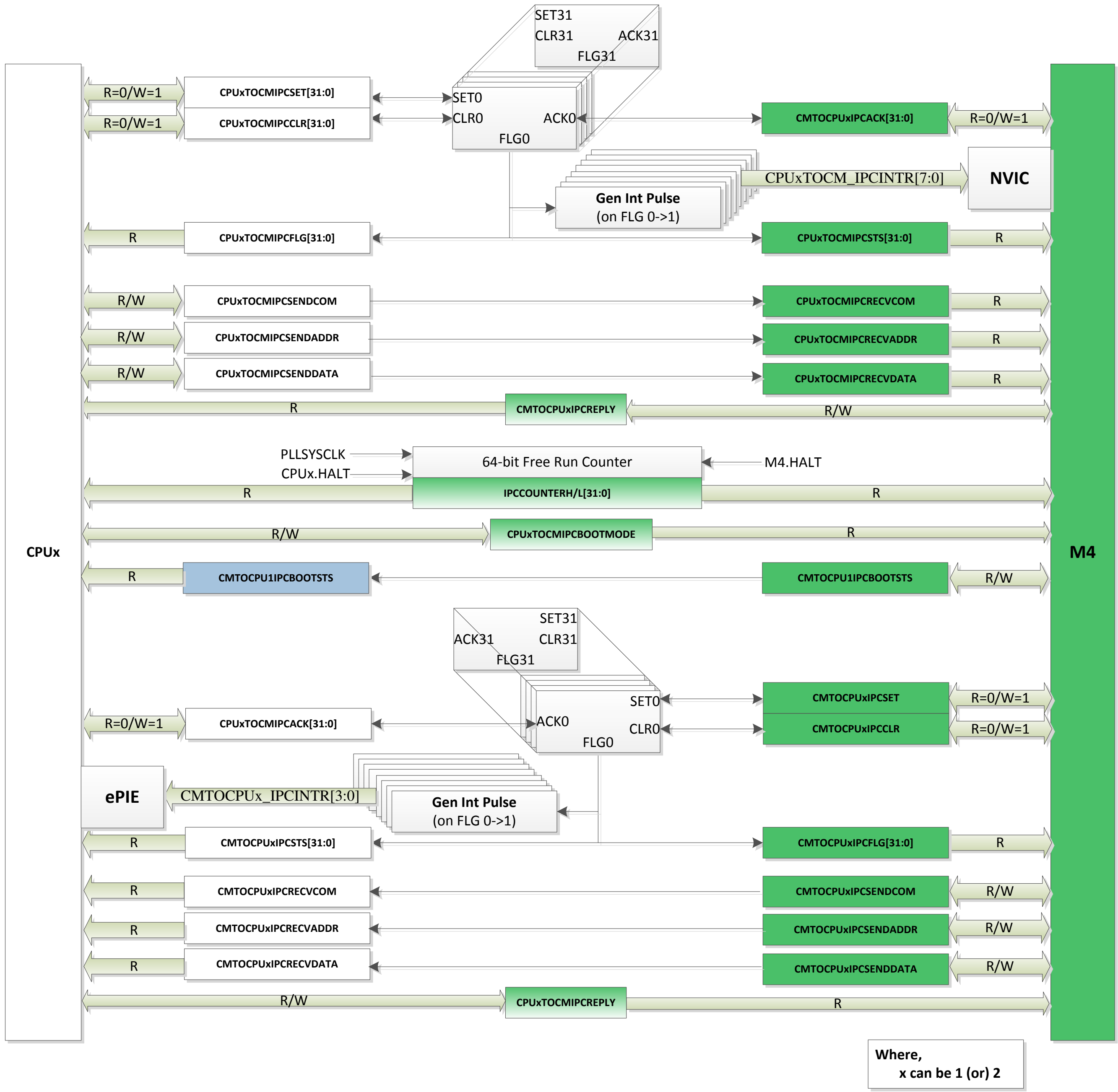


Figure 8-7. CPUx_to_CM IPC Module

8.8.7 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)
- AUXPLLCLK

8.8.8 Dual-Clock Comparator (DCC)

There are three Dual-Clock Comparators (DCC0, DCC1, and DCC2) on the device. All three DCCs are only accessible through CPU1. The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

8.8.8.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

8.8.8.2 Mapping of DCCx (DCC0, DCC1, and DCC2) Clock Source Inputs

Table 8-32. DCCx Clock Source0 Table

DCCxCLKSRC0[3:0]	CLOCK NAME
0x0	XTAL/X1
0x1	INTOSC1
0x2	INTOSC2
0x5	CPU1.SYSCLK
0x6	CPU2.SYSCLK
0xC	INPUT XBAR (Output16 of input-xbar)
others	Reserved

Table 8-33. DCCx Clock Source1 Table

DCCxCLKSRC1[4:0]	CLOCK NAME
0x0	PLLRAWCLK
0x1	AUXPLLRAWCLK
0x2	INTOSC1
0x3	INTOSC2
0x5	CMCLK
0x6	CPU1.SYSCLK
0x7	Ethernet RX Clock (ENET_MII_RX_CLK)
0x8	CPU2.SYSCLK
0x9	Input XBAR (Output15 of the input-xbar)
0xA	AUXCLKIN
0xB	EPWMCLK
0xC	LSPCLK
0xD	Ethercat MII0 RX Clock (ESC_RX0_CLK)
0xE	WDCLK
0xF	CAN0BITCLK
0x17	Ethercat MII1 RX Clock (ESC_RX1_CLK)
others	Reserved

8.8.9 Nonmaskable Interrupt With Watchdog Timer (NMIWD)

The NMIWD module is used to handle system-level errors. There is an NMIWD module for each CPU. The conditions monitored are:

- Missing system clock due to oscillator failure
- Uncorrectable ECC error on CPU access to flash memory
- Uncorrectable ECC or parity error on CPU, CLA, or DMA access to RAM
- Parity error on CPU access to ROM
- Vector fetch error on the other CPU
- CRC Fail error from BGCRC module
- Reset request from EtherCAT master or uncorrectable error on access to EtherCAT RAM
- CPU1/CPU2 HWBIST error
- NMI from ERAD module
- CPU1 only: Watchdog or NMI watchdog reset on CPU2
- CPU1 only: NMIWD reset on CM (configurable)

If the CPU does not respond to the latched error condition, then the NMI watchdog will trigger a reset after a programmable time interval. The default time is 65536 SYSCLK cycles.

8.8.10 Watchdog

The watchdog module is the same as the one on previous TMS320C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 8-8 shows the various functional blocks within the watchdog module.

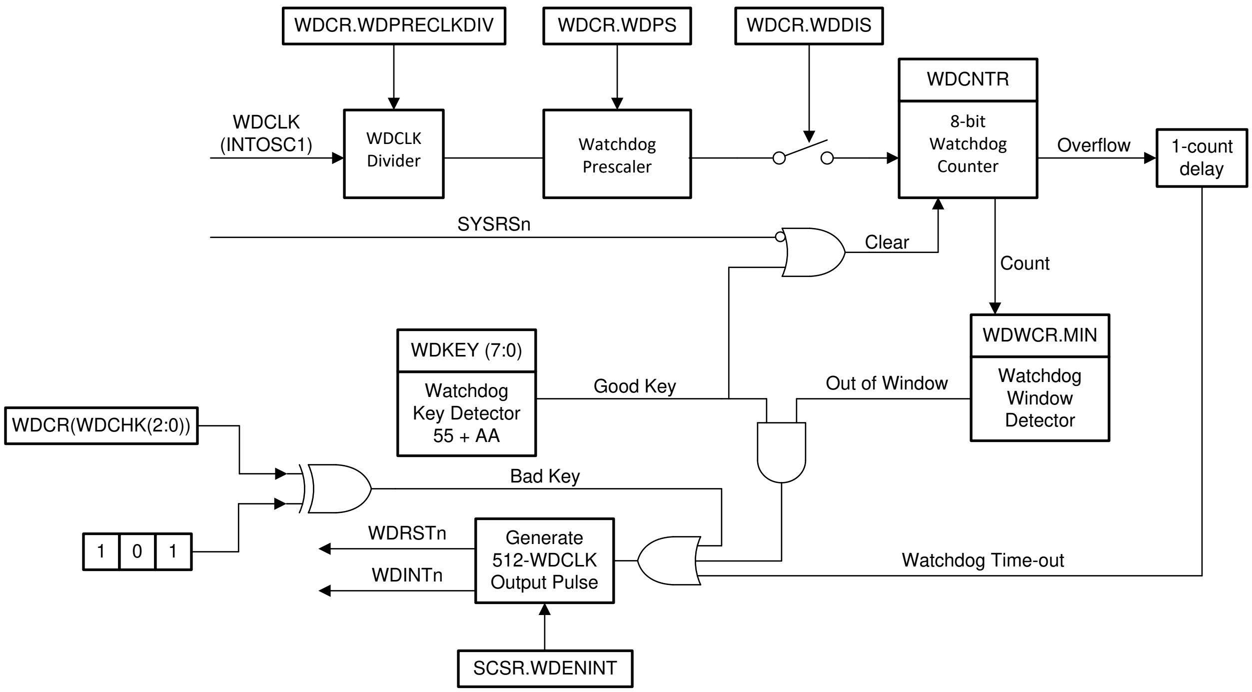


Figure 8-8. Windowed Watchdog

8.8.11 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

For normal operation, the clock frequency of the CLB peripheral is derived from device SYSCLK and can operate at a maximum frequency of 100 MHz. If a higher frequency is desired, then CLB pipeline mode can be enabled, allowing the CLB clock to operate at up to 150 MHz. (This pipeline mode requires lowering the SYSCLK to a maximum frequency of 150 MHz to support this CLB operation). The HLC is considered an integral part of CLB and will have the same set of frequency rules. The frequency of operation does not change with synchronizer or edge qualification. There are no delays that are provided for the CLB inputs and outputs. Whether a synchronizer or PIPELINE filter path on the input needs to be turned ON is purely dependent on the device level hookup table where the inputs are marked as requiring synchronization or not.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports and users guide, please refer to the following location in your C2000Ware package (C2000Ware_2_00_00_03 and higher):

C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc

- **C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc**
- *CLB Tool User's Guide*
- *Designing With the C2000™ Configurable Logic Block (CLB) Application Report*
- *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers Application Report*

The CLB module and its interconnects are shown in Figure 8-9.

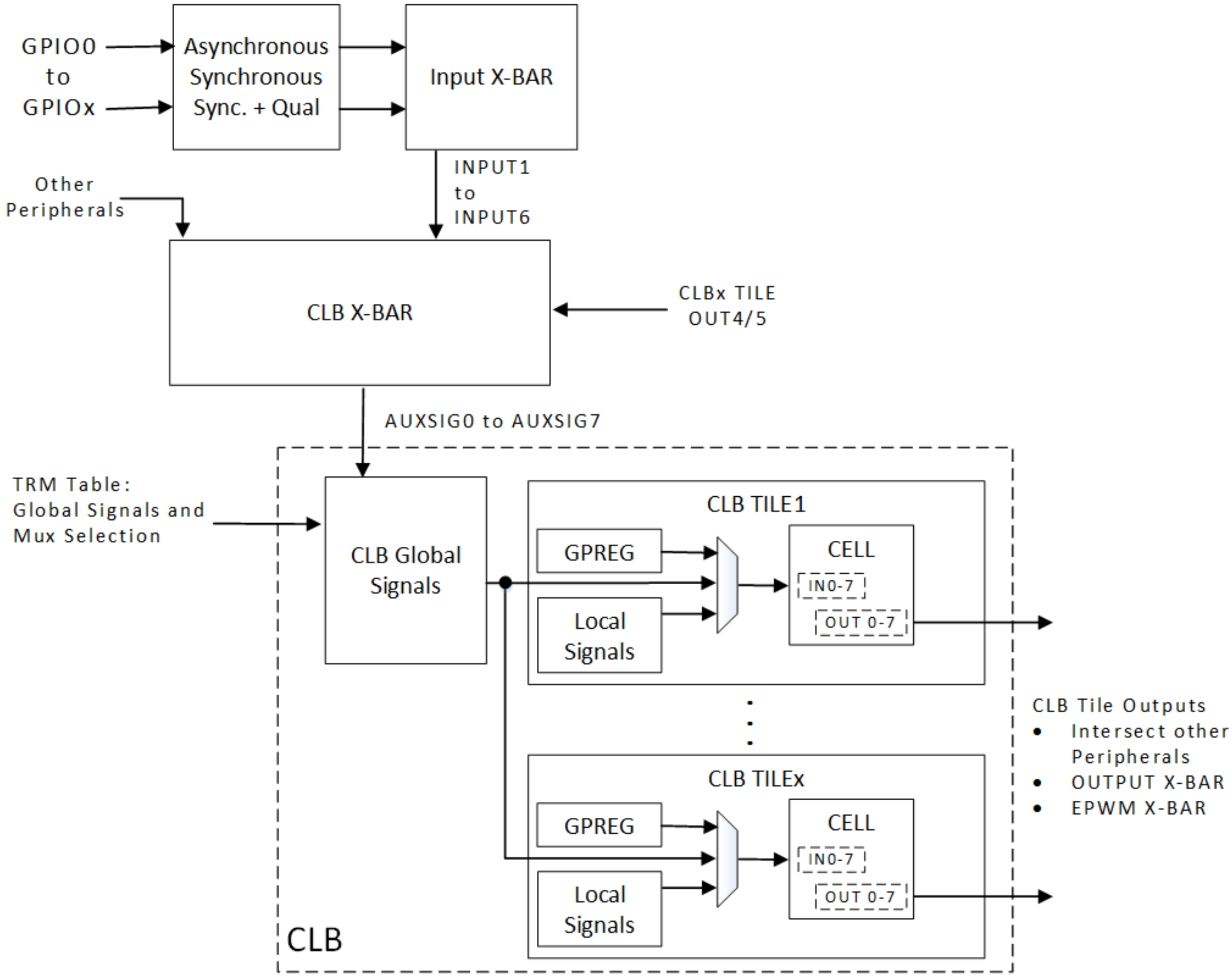


Figure 8-9. CLB Overview

Absolute encoder protocol interfaces are now provided as Position Manager solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with C2000Ware MotorControl SDK. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality.

8.9 Connectivity Manager (CM) Subsystem

The TMS320F2838x supports dual-core C28x architecture along with a new Connectivity Manager subsystem. The CM subsystem is based on the industry-standard 32-bit Arm® Cortex®-M4 CPU and features a wide variety of communication peripherals, including EtherCAT, Ethernet, USB, MCAN (CAN FD), DCAN, UART, SSI, I2C, and so on. Targeting performance and flexibility, the CM is based on 125-MHz Cortex-M4 architecture and provides a variety of integrated memories as well as multiple programmable GPIOs.

8.9.1 Arm Cortex-M4 Processor

The Arm Cortex-M4 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

The Arm Cortex-M4 processor includes the following:

- 32-bit Arm Cortex-M4 architecture optimized for small-footprint embedded applications
- Arm Cortex-M4 CPU can be operated at maximum frequency of 125 MHz
- Arm® Thumb®-2 mixed, 16-/32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system and memories
- Deterministic, high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities

8.9.2 Nested Vectored Interrupt Controller (NVIC)

The NVIC multiplexes interrupts from various peripherals into the CM interrupt lines. In essence, the NVIC is the PIE (Peripheral Interrupt Expansion) equivalent for the CM. The features supported by the NVIC are as follows:

- 80 interrupts
- A programmable priority level of 0–7 for each interrupt. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Low-latency exception and interrupt handling.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external nonmaskable interrupt.

For more information about the NVIC, see the Nested Vectored Interrupt Controller (NVIC) section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

8.9.3 Advance Encryption Standard (AES) Accelerator

The AES module provides hardware-accelerated data encryption and decryption operations based on a binary key. The AES is a symmetric cipher module that supports a 128-, 192-, or 256-bit key in hardware for encryption and decryption. The AES module is based on a symmetric algorithm, which means that the encryption and decryption keys are identical. To encrypt data means to convert it from plain text to an unintelligible form called cipher text. Decrypting cipher text converts previously encrypted data to its original plain text form. The main features of the AES accelerator are discussed below.

Basic AES encrypt and decrypt operations are supported by:

- Galois/Counter mode (GCM), with basic GHASH operation
- Counter mode with CBC-MAC (CCM)
- XTS mode

The following feedback operating modes are available:

- Electronic code book mode (ECB)
- Cipher block chaining mode (CBC)
- Counter mode (CTR)
- Cipher feedback mode (CFB), 128-bit
- F8 mode
- Key sizes: 128, 192, and 256 bits
- Support for CBC_MAC and Fedora 9 (F9) authentication modes
- Basic GHASH operation (when selecting no encryption)
- Key scheduling in hardware
- Support for µDMA transfers
- Fully synchronous design

Figure 8-10 shows the AES block diagram.

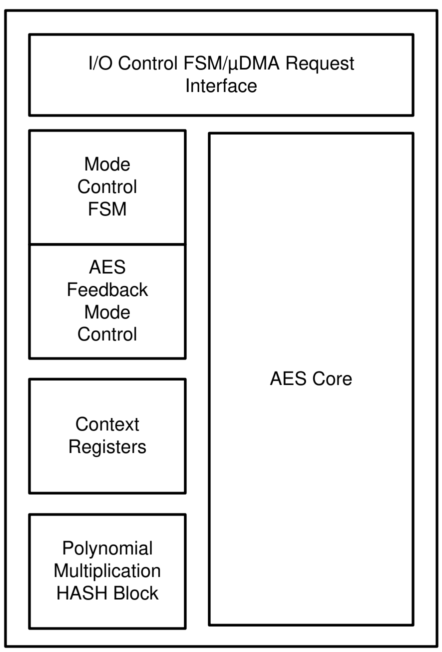


Figure 8-10. AES Block Diagram

For more information about the AES accelerator, see the Advance Encryption Standard Accelerator (AES) chapter of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

8.9.4 Generic Cyclic Redundancy Check (GCRC) Module

The Generic CRC (GCRC) is a designated Connectivity Manager module for computing the CRC value on a configurable block of memory. It accomplishes this by fetching the specified block of memory and using the integrated CRC engine. The calculated CRC value can be compared against a golden CRC value in software to indicate a pass or fail. In essence, the GCRC can help identify memory faults and corruption in the Connectivity Manager's accessible raw data.

The Generic CRC (GCRC) module has the following features:

- Support for programmable polynomials of any order between 1 and 32
- Calculate a CRC on byte (8-bit), halfword (16-bit), and word (32-bit) data blocks
- Define the endianness and data type of the source data
- Reverse the bit order
- Select which data bits participate in the CRC computation

Figure 8-11 shows the block diagram of the GCRC module.

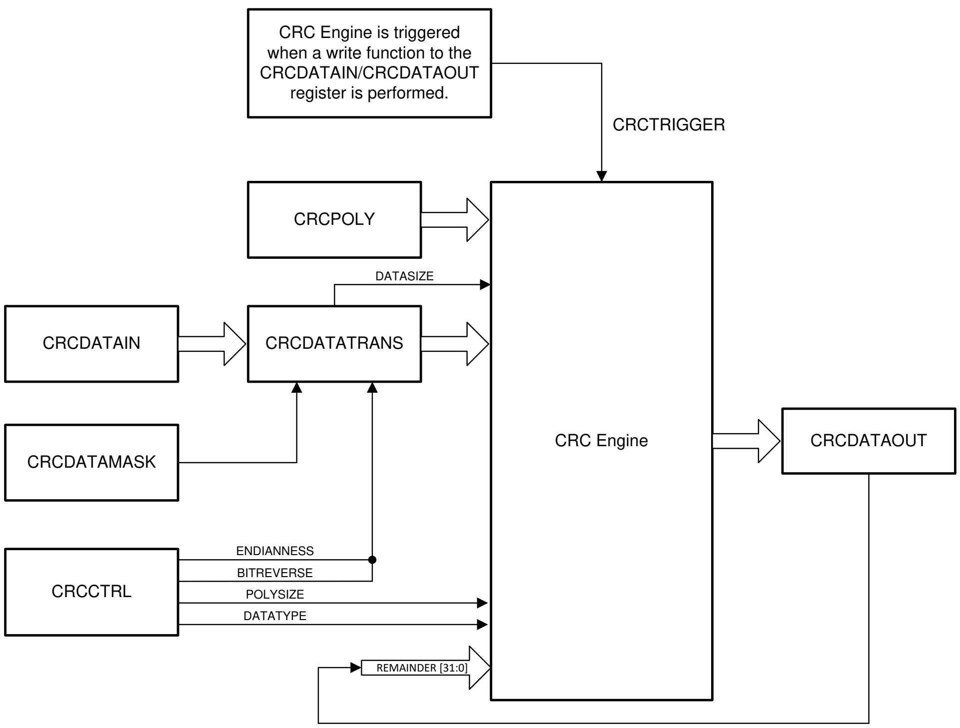


Figure 8-11. GCRC Block Diagram

8.9.5 CM Nonmaskable Interrupt (CMNMI) Module

The CM subsystem has the capability of detecting all serious errors that could occur in the entire system (including all the subsystems), and informing the main CPU core about the errors. An NMI exception to the Cortex-M4 CPU on the CM subsystem will be generated only when at least one or more of the below NMI error sources become active. For more details on each of the sources, see the CM Subsystem NMI Sources section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

1. RAM/ROM uncorrectable error
2. Reset request from the EtherCAT
3. Clock failure
4. MCAN uncorrectable error
5. CM windowed watchdog timed out
6. Flash uncorrectable error

All these NMI sources are "OR-ed" to generate the NMI input to the Cortex-M4 NVIC. The NMI triggers a CMNMIWD counter running at the CM subsystem frequency. The CMNMIWD counter will stop counting only if all the pending NMIs are acknowledged by clearing the pending flags in the CMNMIFLG register. If the pending NMI is not acknowledged before the CMNMIWD counter reaches the value programmed in the NMI Watchdog period register (CMNMIWDPRD), an NMIWD reset is generated to the CM subsystem, which will reset the entire device.

Figure 8-12 shows different sources that can trigger an NMI to the Cortex-M4 on the CM subsystem and the registers associated with them.

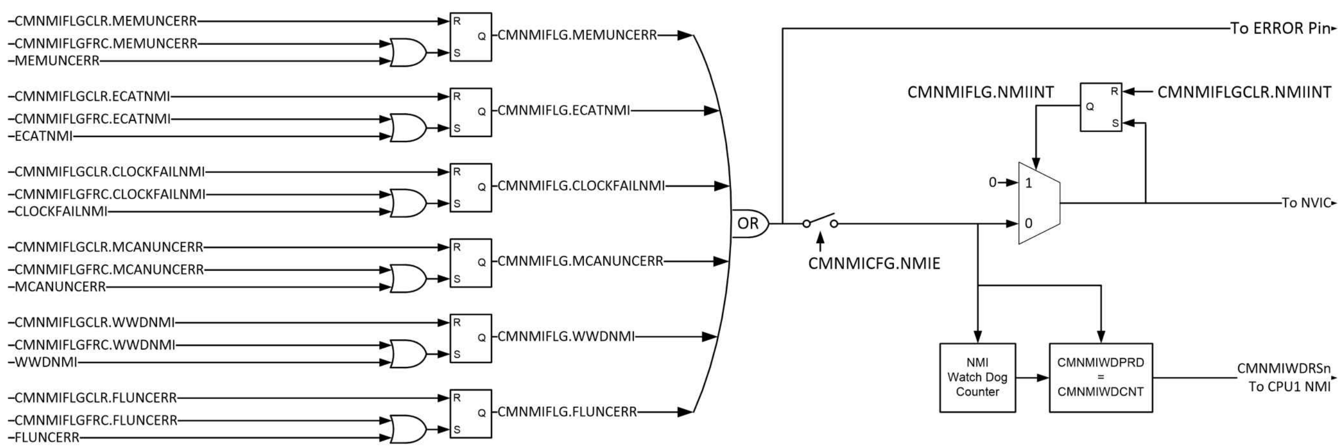


Figure 8-12. CM Subsystem NMI Sources and NMIWD

All the NMI sources shown in Figure 8-12 are enabled by default on reset. CMNMICFG.NMIE is disabled on reset and needs to be enabled by setting it to 1.

For more information about the CMNMI, see the CM Subsystem Non-Maskable Interrupt (CMNMI) Module section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

8.9.6 Memory Protection Unit (MPU)

The CM subsystem has multiple masters accessing the memory blocks and peripherals. Below is the list of masters on the CM subsystem:

- Cortex-M4
- µDMA
- EtherNET DMA

In a multimaster system, it is important to have a protection mechanism to prevent unauthorized access to critical code, data, or peripherals from different masters or threads. This protection mechanism will:

- Prevent a process or a task from accessing memory that is not allocated to it.
- Protect Cortex-M4 code from unintended corruption by other bus masters on the CM subsystem.
- Protect stack corruption by other bus masters on CM systems.

The Cortex-M4 has the ARM native MPU (Cortex-M4 MPU) that provides such protection (see the Memory Protection Unit chapter of the *ARM® Cortex®-M4 Processor Technical Reference Manual*). For other masters (µDMA and Ethernet DMA), a generic memory protection unit (CM-MPU) has been provided, which users can configure based on the use case, to enable the protection. Basically, one MPU for each master is provided to protect the accesses from that master. For more details, see the Memory Controller Module section of the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*.

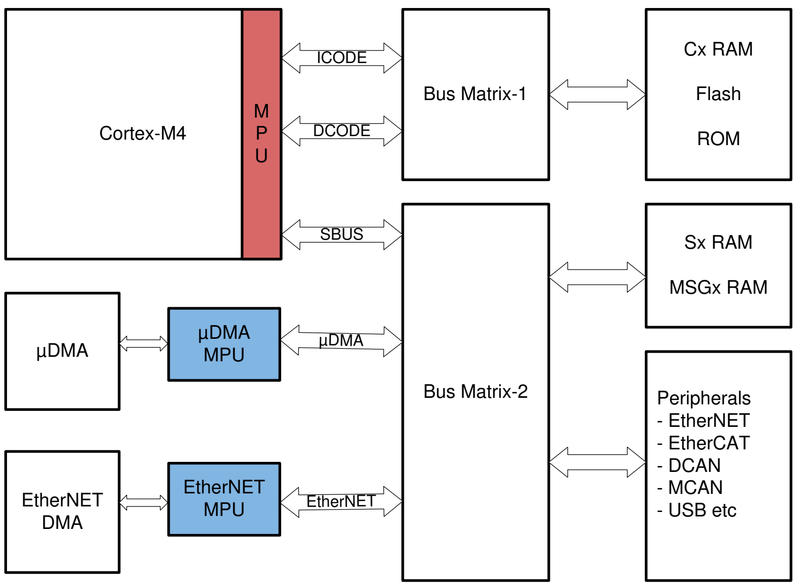


Figure 8-13. CM Block Diagram

8.9.7 Micro Direct Memory Access (µDMA)

The µDMA controller provides a way to offload data transfer tasks from the Arm Cortex-M4 processor, allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

The µDMA controller provides the following features:

- Arm® PrimeCell® 32-channel configurable µDMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes:
  - Basic mode
  - Ping-pong mode
  - Memory scatter-gather mode
  - Peripheral scatter-gather mode
  - Auto request mode
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - Flexible channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable priority scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Data sizes of 8, 16, and 32 bits
- Programmable transfer size in binary steps from 1 to 1024
- Source and destination address increment size of byte, halfword, word, or no increment
- Maskable peripheral requests
- Supports two interrupts:
  - µDMA Software interrupt: µDMA generates an interrupt when a software channel completes all its transfers
  - µDMA Error interrupt: µDMA generates an interrupt an when error is detected on a DMA transfer
- DMA transfers triggered by a peripheral event generates a corresponding peripheral interrupt when DMA completes all its transfers.

Figure 8-14 shows the µDMA block diagram.

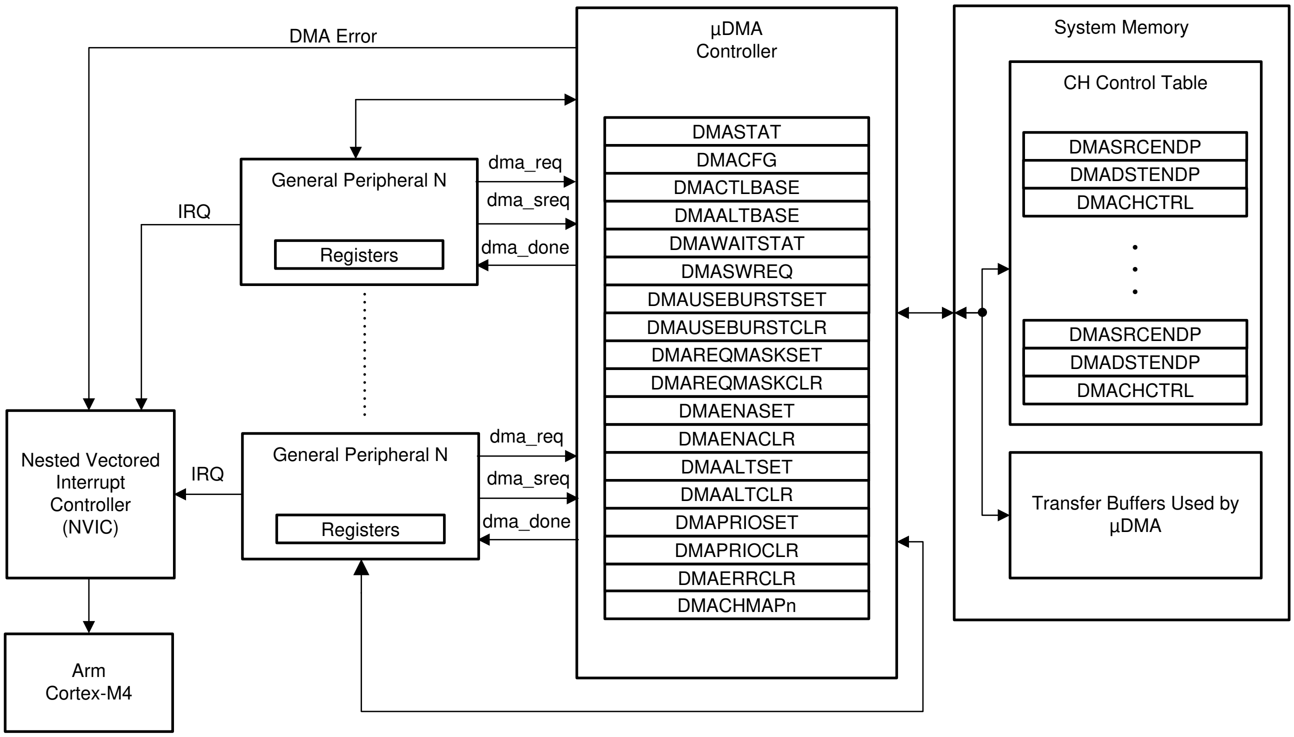


Figure 8-14. µDMA Block Diagram

8.9.8 Watchdog

The Connectivity Manager (CM) has one watchdog (also referred to as windowed watchdog) timer. The functionality of this watchdog timer is the same as the one used on CPUx subsystems. For details about this module, see the Watchdog Timers section of the System Control chapter in the *TMS320F2838x Real-Time Microcontrollers Technical Reference Manual*. Following are some differences in the configuration of the watchdog timer on the CM versus CPUx:

- The Watchdog timer on CM is disabled by default. Software needs to clear the WDDIS bit in the WDCR register to enable the watchdog.
- Whenever the watchdog counter (WDCR) overflows or an incorrect value is written to WDCR[WDCHK], an NMI gets generated (not reset or interrupt such as CPUx watchdog timers) to the CMNMIWD module. If software is not able to service the NMI, then the NMIWD module will trigger a reset to the CM.

The CM watchdog timer counter stops incrementing when the Cortex-M4 is halted during the debug session.

8.9.9 CM Clocking

8.9.9.1 CM Clock Sources

Table 8-34 lists four possible clock sources. Figure 8-15 provides an overview of the device's clocking system.

Table 8-34. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1	Can be used to provide clock for: • Watchdog block • Main PLL • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.
AUXCLKIN	Can be used to provide clock for: • Auxiliary PLL • CPU-Timer 2	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

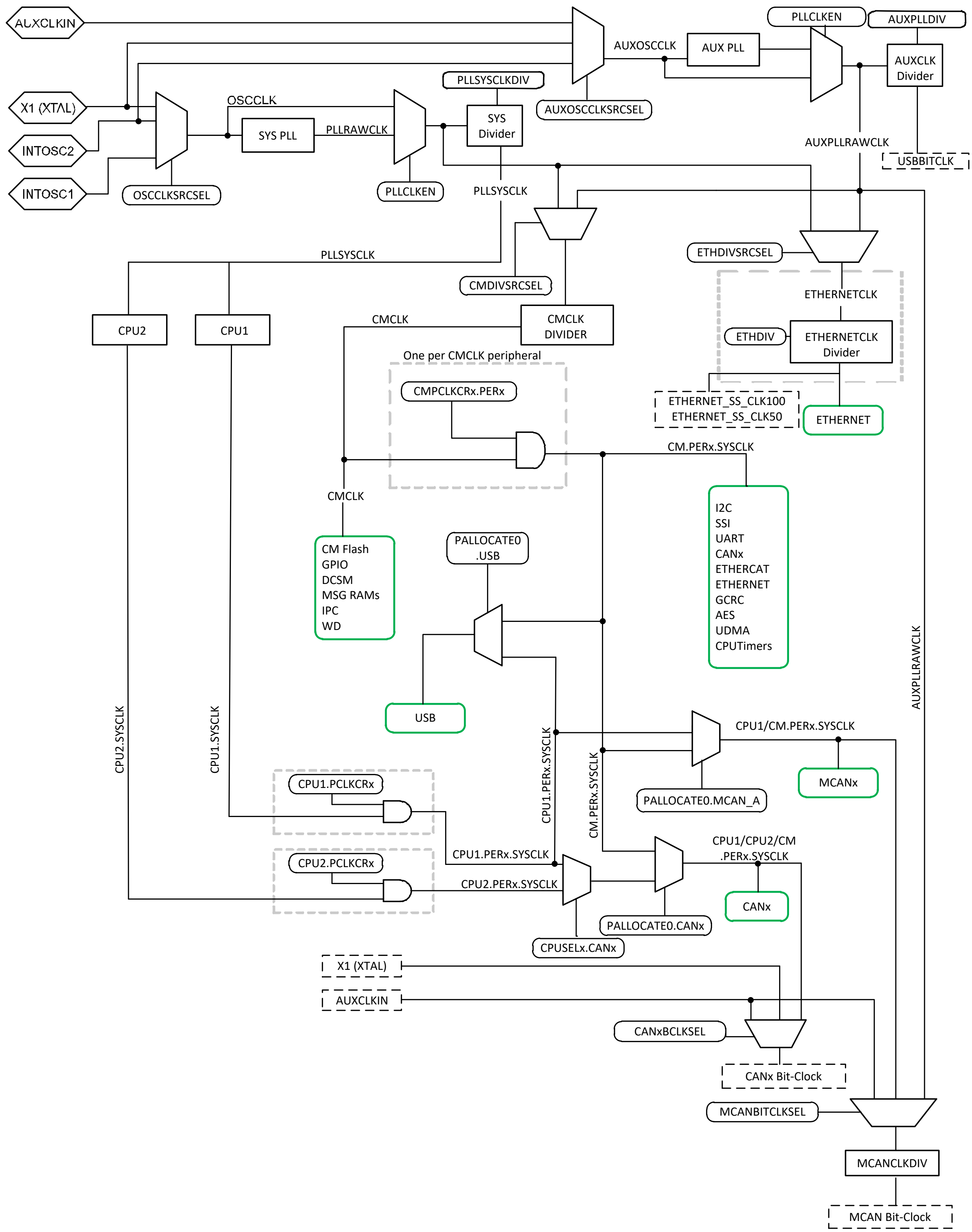


Figure 8-15. CM Clocking System

8.9.10 CM Timers

The Connectivity Manager (CM) has three 32-bit timers that are identical, with 16-bit clock prescaling. These timers operate on CMCLK. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

8.10 Functional Safety

Functional Safety-Compliant products are developed using an ISO 26262/IEC 61508-compliant hardware development process that is independently assessed and certified to meet ASIL D/SIL 3 systematic capability (see certificate). The TMS320F2838x has been certified to meet a component-level random hardware capability of ASIL B and SIL 2 (see certificate).

A functional safety manual that describes all of the hardware and software functional safety mechanisms is available. See the *Functional Safety Manual for TMS320F2838x Real-Time Microcontrollers*.

A detailed, tunable, fault-injected, quantitative FMEDA that enables the calculation of random hardware metrics—as outlined in the International Organization for Standardization ISO 26262 and the International Electrotechnical Commission IEC 61508 for automotive and industrial applications, respectively—is also available. This tunable FMEDA must be requested; see the *C2000™ Safety Package for Automotive and Industrial Real-Time Microcontrollers User's Guide*.

- A white paper outlining the value (or benefit) of a tunable FMEDA is available. See the *Functional Safety: A tunable FMEDA for C2000™ MCUs* publication.
- Part 1 and Part 2 of a five-part FMEDA tuning training are available from the TI Video Library. Part 1 is *Basics of FMEDA and how it is useful in system level safety analysis*. Part 2 is *Introduction to the C2000™ Tunable FMEDA*. Parts 3, 4, and 5 are packaged with the tunable FMEDA, and must be requested.

Two diagnostic libraries designed for the F2838x series of devices are available to aid in the development of functionally safe systems—the CLA Self-Test Library (CLA_STL) and the Software Diagnostic Library (SDL). The CLA_STL provides software tests of the CLA and has been independently assessed and certified. It is available upon request only, see the *C2000™ Safety Package for Automotive and Industrial Real-Time Microcontrollers User's Guide*. The SDL is a set of reference software providing example implementations of several safety mechanisms described in the device safety manual, such as HWBIST, software tests of SRAMs, software tests of Missing Clock Detect functionality, clock integrity checks using CPU Timers, and several other key features. The SDL is provided as part of C2000Ware.

C2000 real-time MCUs are also equipped with a TI release validation-based C28x and CLA Compiler Qualification Kit (CQKIT), which is available for free and may be requested at the Safety compiler qualification kit web page.

Additional details about how to develop functionally safe systems with C2000 real-time MCUs can be found in the following documents:

- *Automotive Functional Safety for C2000™ Real-Time Microcontrollers* summarizes the available functional safety products, documentation, software, and support available for aiding in the ISO 26262 certification process.
- *Industrial Functional Safety for C2000™ Real-Time Microcontrollers* summarizes the available functional safety products, documentation, software, and support available for aiding in the IEC 61508 certification process.
- *C2000™ Hardware Built-In Self-Test* discusses the Hardware Built-In Self-Test (HWBIST) feature in C2000™ real-time microcontrollers. The HWBIST provides a method of reaching a high level of diagnostic coverage on the C28x CPU, which is often needed to satisfy safety standards.
- *Error Detection in SRAM Application Report* provides technical information about the nature of the SRAM bit cell and bit array, as well as the sources of SRAM failures. It then presents methods for managing memory failures in electronic systems. This discussion is intended for electronic system developers or integrators who are interested in improving the robustness of the embedded SRAM.
- *C2000™ CPU Memory Built-In Self-Test* describes embedded memory validation using the C28x central processing unit (CPU) during an active control loop. It discusses system challenges to memory validation as well as the different solutions provided by C2000 devices and software. Finally, it presents the applicable Software Diagnostic Library features for memory testing.

9 Applications, Implementation, and Layout

9.1 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.2 Key Device Features

Table 9-1. Key Device Features

MODULE	FEATURE	SYSTEM BENEFIT
C28x PROCESSING		
Real-time control CPUs	Up to 800 MIPS Two C28x cores: 400 MIPS (2 x 200 MIPS) Two CLA cores: 400 MIPS (2 x 200 MIPS) Flash: Up to 1 MB (512KB on each C28x CPU) RAM : Up to 216 KB 64-bit Floating Point Unit (FPU64) Trigonometric Math Unit (TMU) CRC engine and instructions (VCRC) Fast Integer Division (FINTDIV)	TI's two 32-bit C28x DSP cores, provides 400 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM Provides 400 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. **CLA:** Allows user to execute time-critical control loops concurrently with main CPU **FPU64:** Native hardware support for IEEE-754 double-precision floating-point operations **TMU:** Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. Helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms **VCRC:** Provides a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. **FINTDIV:** Supports linear division operations such as Euclidean and Modulus division used in control algorithms See Real-time Benchmarks Showcasing C2000™ControlMCU's Optimized Signal Chain.
SENSING		
Analog-to-Digital Converter (ADC) (configurable 12-bit or 16-bit)	Four ADC modules 16-bit mode: (1.1 MSPS) Single-ended mode: Up to 24 channels Differential mode : Up to 12 channels 12-bit mode: (3.5 MSPS) Single-ended mode: Up to 24 channels	ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles. More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance.

Table 9-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Comparator Subsystem (CMPSS)	**CMPSS** 8 windowed comparators Three 12-bit DACs 60-ns detection to trip time DAC ramp generation Low DAC output on external pin Digital filters Slope compensation	**System protection without false alarms:** Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring. PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems. Provides better control accuracy. No need for further CPU configuration to control the PWM with the comparator and 12-bit DAC (CMPSS). Enables protection and control using the same pin.
Sigma Delta Filter Module (SDFM)	Up to 8 independently configurable digital comparator filter channels Up to 8 independently configurable digital data filter channels	Enables galvanic isolation with reinforced delta sigma modulators. SDFMs interface with external delta sigma modulator ADCs, which is ideal for signals that may require isolation. Comparator filter supports overcurrent and undercurrent protection but tripping the PWM without CPU intervention Digital data filter provides higher ENOBs for better control-loop performance
Enhanced Quadrature Encoder Pulse (eQEP)	3 eQEP modules	Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Also can be used in other applications to count input pulses from an external device (such as a sensor).
Enhanced Capture (eCAP)/High Resolution Enhanced Capture (HRCAP)	7 eCAP modules (2 with HRCAP capability) Measures elapsed time between events (up to 4 time-stamped events). Connects to any GPIO through the input X-BAR. When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).	**Applications for eCAP include:** Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors) Elapsed time measurements between position sensor pulses Period and duty-cycle measurements of pulse train signals Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors
	2 HRCAP channels Provides the capability to measure the width of external pulses with a typical resolution of 300 ps.	**Applications for HRCAP include:** High-resolution period and duty-cycle measurements of pulse train cycles Instantaneous speed measurements Instantaneous frequency measurements Voltage measurements across an isolation boundary Distance/sonar measurement and scanning Flow measurements Capacitive touch applications

Table 9-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
ACTUATION		
Enhanced Pulse Width Modulation (ePWM)/High-Resolution Pulse Width Modulation (HRPWM)	Up to 32 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window	Flexible PWM waveform generation with best power topology coverage. Shadowed Dead band itself and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency.
	HRPWM capability: All the 16 channels provide high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, deadband, and phase offsets for 99% greater precision	Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output.
	One-shot and global reload feature	Critical for variable-frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). Enables control of interleaved LLC topologies at high frequencies
	Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) trip event	Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control.
	Load on SYNC (support for shadow-to-active load on a SYNC event)	Enables variable-frequency applications (allows LLC control in power conversion).
	Ability to shut down the PWMs without software intervention (no ISR latency)	Fast protection under fault condition
	Delayed Trip Functionality	Helps implement the deadband with Peak Current Mode Control (PCMC) Phase-Shifted Full Bride (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events).
	Dead band Generator (DB) submodule	Prevents simultaneous ON conditions of High- and Low-side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges.
	Flexible PWM Phase Relationships and Timer Synchronization	Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges perfectly in synchronization with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching.
CONNECTIVITY		
Fast Serial Interface (FSI)	Up to 2 FSI transmitters and 8 FSI receivers Serial communication peripheral capable of reliable high-speed communication (up to 200 MHz) across isolation devices	More flexible communications options. Fast serial interface can be useful for low-pin count, high-speed communication even across isolation boundary at up to 200Mbps.
Serial Peripheral Interface (SPI)	4 high-speed SPI port	Supports 50 MHz
Serial Communication Interface (SCI)	4 SCI (UART) modules	Interfaces with controllers
Controller Area Network (CAN/DCAN)	2 DCAN module (can be assigned to Connectivity Manager (M4))	Provides compatibility with classic CAN modules

Table 9-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Controller Area Network (CAN FD/ MCAN)	1 CAN FD/MCAN module [can be assigned to Connectivity Manager (M4)]	CAN FD (flexible data-rate) is an enhancement to the classic CAN protocol. CAN FD facilitates dynamic switching to higher bit rates (>1 Mbps) for the data segment and allows for up to 64 bytes compared to 8 bytes in classic CAN. This is done without having to change the physical layer. This results in a bandwidth gain over traditional CAN. Systems using CAN FD benefit from faster in-the-field flash updates.
Inter-Integrated Circuit (I2C)	2 I2C modules	Interfaces with external EEPROMs, sensors, or controllers
Multichannel Buffered Serial Port (McBSP)	Up to 2 McBSP modules	Interface to high-speed external ADC or additional SPI peripheral
Power-Management Bus (PMBus)	1 PMBus module Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)	Seamless HW-based host communication
External Memory Interfaces (EMIFs) with ASRAM and SDRAM support	Two EMIF modules, to have a dedicated EMIF for each CPU subsystem.	Interface with External ASRAM and SDRAM
OTHER SYSTEM FEATURES		
Configurable Logic Block (CLB)	Collection of configurable blocks that can be inter-connected using software to implement custom digital logic functions	User customized PWM protection features, custom logic to off-load complex algorithms/state machines, custom peripherals, and used to implement absolute encoders used in servo drives User also used for protection of multilevel inverter/PFC or multilevel DC-DC Provides the ability to build logic around existing IPs like ETPWM, ECAP, QEP and GPIOs. Enables development of unique IP such as PWM Safety modules, Encoder engines, etc.
Security enhancers	Dual-zone Code Security Module (DCSM) Secure Boot JTAGLOCK AES acceleration BackGround CRC (BGCRC) Generic CRC (GCRC) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity Dual-Clock Comparator (DCC)	**DCSM:** Prevents duplication and reverse-engineering of proprietary code **Secure Boot:** Uses AES128 CMAC algorithm to ensure code that runs on the device is authentic **JTAGLOCK:** Ability to block emulation of the device **AES acceleration:** The hardware accelerator vastly improves the cycle time of processing cryptographic messages while freeing up the CPU bandwidth **BGCRC:** Checks memory integrity with no CPU overhead or system performance impact **GCRC:** Designated Connectivity Manager module for computing the CRC value on a configurable block of memory **Watchdog:** Generates reset if CPU gets stuck in endless loops of execution **Write Protection on Registers:** LOCK protection on system configuration registers Protection against spurious CPU writes **MCD:** Automatic clock failure detection **ECC and parity:** Single-bit error correction and double-bit error detection **DCC:** Used to detect faults in clock source

Table 9-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Crossbars (XBARs)	Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. • Input X-BAR • Output X-BAR • ePWM X-BAR • CLB Input X-BAR • CLB Output X-BAR • CLB X-BAR	**Enhances hardware design versatility:** **Input X-BAR:** Routes signals from any GPIO to multiple IP blocks within the chip **Output XBAR:** Routes internal signals onto designated GPIO pins **ePWM X-BAR:** Routes internal signals from various IP blocks to ePWM **CLB Input X-BAR:** Allows user to route signals directly from any GPIO to Configurable Logic Block (CLB) **CLB Output X-BAR:** Allows user to bring signals from CLB tiles to designated GPIO pins **CLB X-BAR:** Allows user to bring signals from various IP blocks to CLB
M4 PROCESSING		
Real-time connectivity	Dedicated, fully programmable communications sub-system Arm® Cortex®-M4 Up to 125 MIPS Flash: 512KB RAM : 96KB	Enables communication in parallel with real-time control. This increases overall system performance without sacrificing critical timing within the real-time control subsystem.
Micro Direct Memory Access (μDMA) controller	32-channels	The direct memory access (DMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up CPU bandwidth for other system functions.
Ethernet MAC		Supports Industrial networking and factory automation
EtherCAT	Integrated EtherCAT® Slave Controller (ESC) IP invented by Beckhoff Automation™	Develop Industrial Ethernet-based fieldbus systems with low latency and cycle times. Takes advantage of the "on-the-fly" frame processing and forwarding nature of EtherCAT hardware. Run an EtherCAT slave stack and application software to implement an EtherCAT slave node.
USB		Useful for system datalogging and boot to USB for updating on-chip flash

9.3 Application Information

9.3.1 Typical Application

The *Typical Applications* section details *some* applications of this device. For a more extensive list of applications, see the *Applications* section of this data sheet.

9.3.1.1 High-Voltage Traction Inverter

The traction drive subsystem is designed to drive an AC induction motor or some combination of interior permanent magnet synchronous motor (IPMSM) and synchronous reluctance motor (SynRM). A high-bandwidth, field-oriented control (FOC) scheme with dynamic decoupling is implemented with a C2000 real-time control MCU together with field-weakening and over-modulation techniques to driver motor to industry-leading high speed up to 20,000 RPM, which can enable cost and weight reduction to the traction motor.

A traction drive system normally uses a variable reluctance (VR) resolver, which matches the pole count of the motor, to directly measure the electric angle of the rotor. Resolver-to-digital conversion (RDC) is required to measure position and speed using the resolver signal. RDC is traditionally handled by a separate IC, such as PGA411-Q1. With a C2000 MCU, RDC for a high-speed traction inverter can be integrated into the main control MCU, where the excitation generation can be handled with the DMA without CPU involvement, and feedback is read through the ADC and decoded with the CPU.

A Phase-Shifted Full Bride (PSFB) topology allows the switching devices to switch with zero-voltage switching (ZVS), resulting in lower switching losses and higher efficiency. Peak Current Mode Control (PCMC) is a highly desired control scheme for power converters because of its inherent voltage feed forward, automatic cycle-by-cycle current limiting, flux balancing, and other advantages, which require generating complex PWM drive waveforms along with fast and efficient control loop calculations. This is made possible on C2000 microcontrollers by advanced on-chip control peripherals like PWM modules, analog comparators with DAC and slope compensation hardware, and 12-bit high-speed ADCs coupled with an efficient 32-bit CPU.

Figure 9-1 shows a high-level block diagram of a single TMS320F28388D C2000™ real-time MCU controlling both an HEV/EV traction inverter and a bidirectional DC-DC converter.

9.3.1.1.1 System Block Diagram

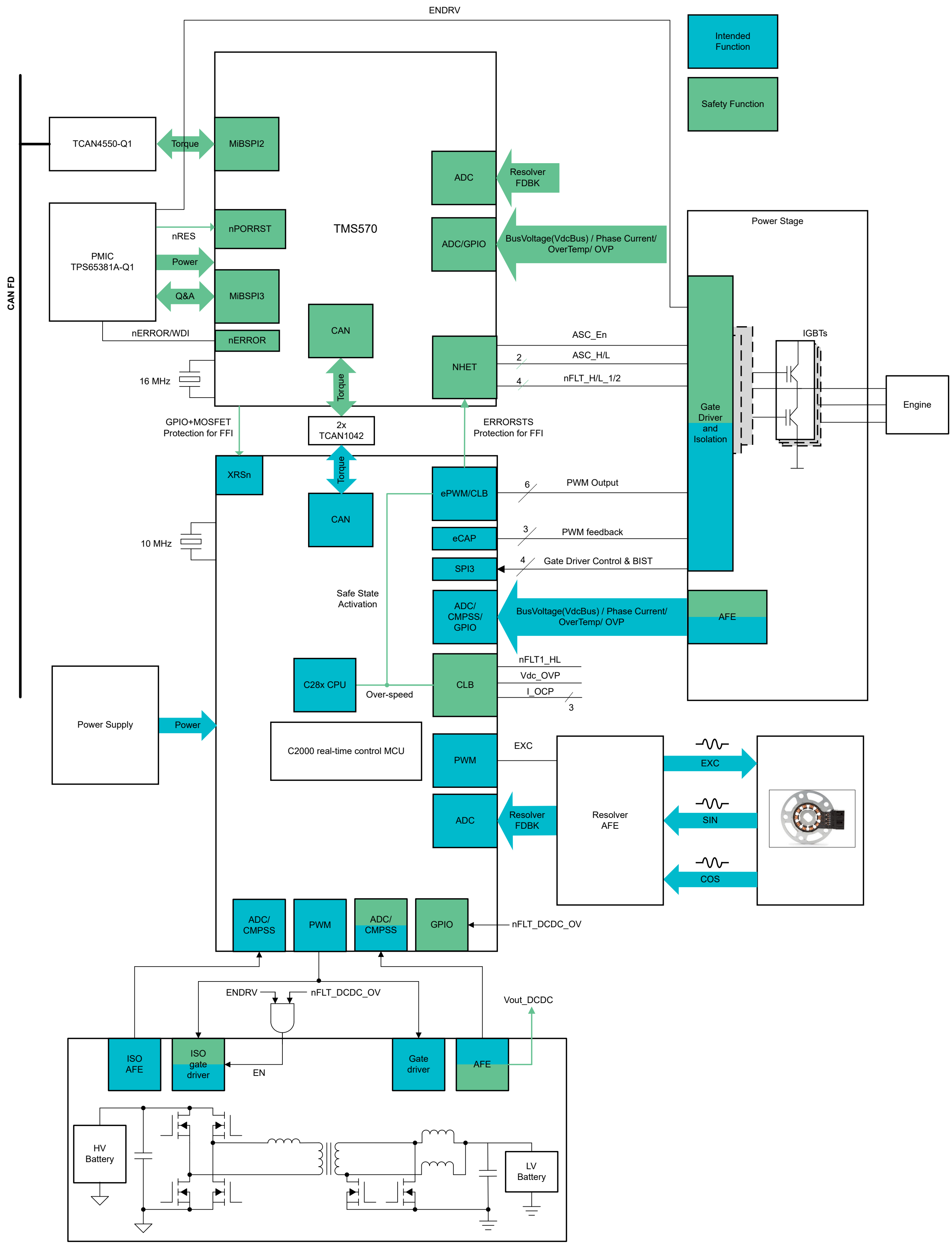


Figure 9-1. Traction Inverter High Voltage

9.3.1.1.2 High-Voltage Traction Inverter Resources

Reference Designs and Associated Training Videos

TIDM-02009 ASIL D Safety Concept-Assessed High-Speed Traction, Bi-directional DC/DC Conversion Reference Design
This reference design demonstrates control of HEV/EV traction inverter and bi-directional DC-DC converter by a single TMS320F28388D real-time C2000™ MCU. The traction control uses a software-based resolver to digital converter (RDC) driving the motor to a high speed up to 20,000 RPM. The DC-DC converter uses peak current mode control (PCMC) technique with phase-shifted full-bridge (PSFB) topology and synchronous rectification (SR) scheme. The traction inverter stage uses silicon carbide (SiC) power stage, driven by UCC5870-Q1 smart gate driver. PCMC waveform is generated using state-of-the-art PWM module and built-in slope compensation in the comparator sub-system (CMPSS). An ASIL decomposition based functional safety concept for the system has been assessed with TÜV SÜD to demonstrate system level safety integrity level up to ISO 26262 ASIL D for representative safety goals.

C2000™ MCUs - Electric vehicle (EV) | TI.com Training Series (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

PSFB Control Using C2000 Microcontrollers Application Report
This application report presents the implementation details of a digitally controlled PSFB system implemented on the high voltage phase shifted full bridge (HVPSFB) kit from Texas Instruments. This kit converts a 400 V DC input to a regulated 12 V DC output and is rated for operations up to 600W. Both peak current mode control (PCMC) and voltage mode control (VMC) implementations are described.

TIDA-BIDIR-400-12 *Bidirectional DC-DC Converter*
This document presents the details of this microcontroller-based implementation of an isolated bidirectional DC-DC converter. A phase-shifted full-bridge (PSFB) with synchronous rectification controls power flow from a 400-V bus or battery to the 12-V battery in step-down mode, while a push-pull stage controls the reverse power flow from the low-voltage battery to the high-voltage bus or battery in boost mode. This design is rated for up to 300 W of output power in either mode.

9.3.1.2 On-Board Charger (OBC)

An On-Board Charger (OBC) consists of two power stages: an AC-DC power converter and a subsequent DC-DC power converter stage. The OBC can be implemented by using a single MCU to control both the AC-DC and DC-DC power converters. For example: an 11-kW OBC can be implemented by using three 3.7-kW single-phase OBC modules, as shown in Figure 9-2. This approach allows us to easily support both single-phase 240 AC (North America) and 3-phase AC (rest of the world).

OBC-charging design requirements are as follows:

- High-performance and fast digital control loops enabling highly efficient power conversion and increased power density.
- Enabling precise control and fast shutdown in an overcurrent scenario by high bandwidth and fast response current sensing.
- Safely and efficiently controlling and protecting the power switch [insulated-gate bipolar transistor/silicon carbide (IGBT/SiC)].

9.3.1.2.1 System Block Diagram

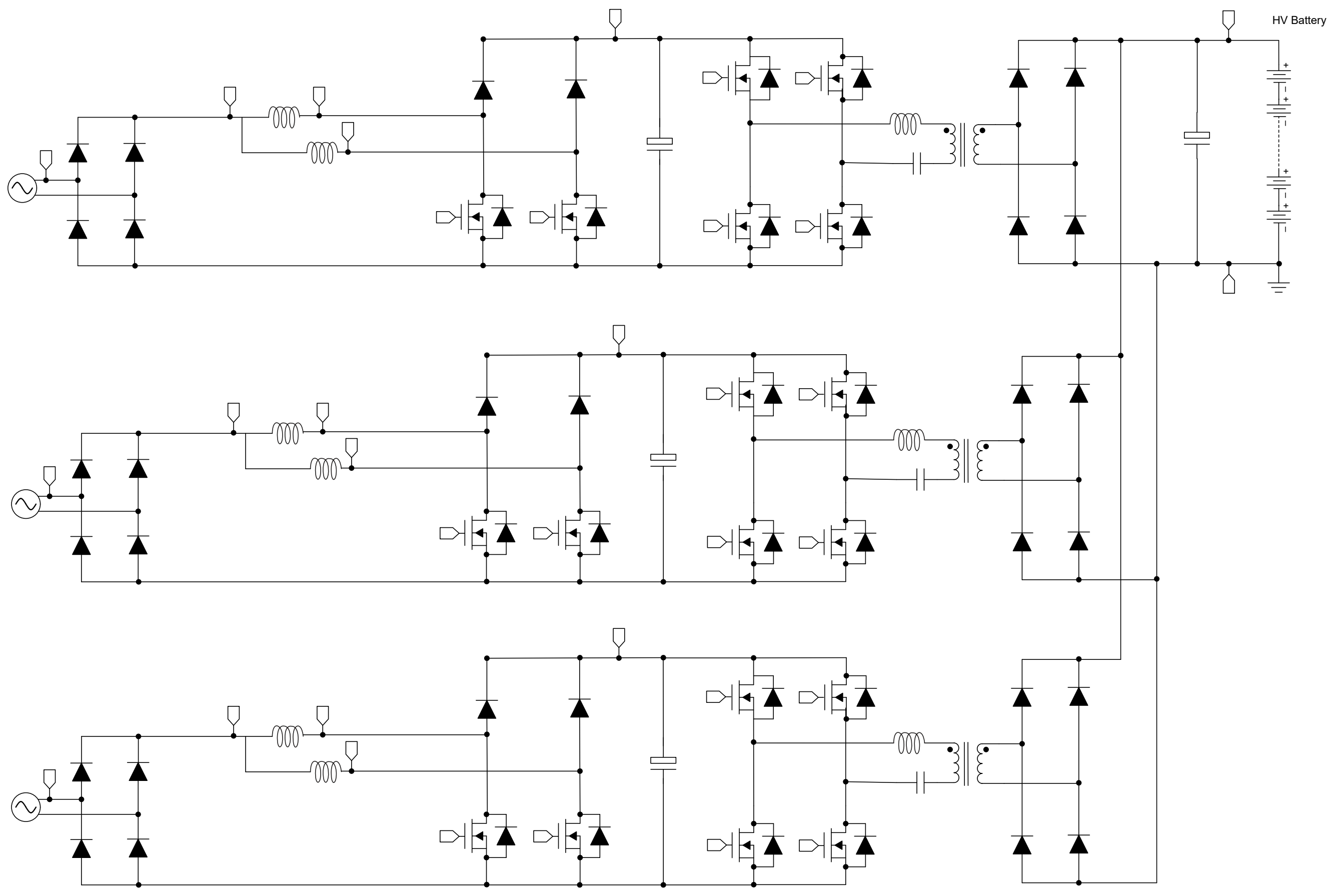


Figure 9-2. 11 kW Modular OBC Power Topology (Unidirectional, bridge PFC)

9.3.1.2.2 OBC Resources

Reference Designs and Associated Training Videos

C2000 Digital Power Training videos
This training series covers the basics of digital power control and how to implement it on C2000™ microcontrollers.

C2000™ MCUs - Electric vehicle (EV) training videos (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

PMP22650 GaN-based, 6.6-kW, bidirectional, onboard charger reference design
The PMP22650 reference design is a 6.6-kW, bidirectional, onboard charger. The design employs a two-phase totem pole PFC and a full-bridge CLLLC converter with synchronous rectification. The CLLLC utilizes both frequency and phase modulation to regulate the output across the required regulation range. The design uses a single processing core inside a TMS320F28388D microcontroller to control both the PFC and CLLLC. Synchronous rectification is implemented via the same microcontroller with Rogowski coil current sensors. High density is achieved through the use of high-speed GaN switches (LMG3522). The PFC is operating at 120 kHz and the CLLLC runs with a variable frequency from 200 kHz to 800 kHz. A peak system efficiency of 96.5% was achieved with an open-frame power density of 3.8 kW/L. While the design calculations were done for a 6.6-kW output power, the design represents a suitable starting point for a 7.x-kW (for example, 7.2-kW to 7.4-kW) rated OBC operating from a 240-V input with a 32-A breaker.

TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDUEG3A TIDM-1022 Valley switching boost power factor correction (PFC) reference design
This reference design illustrates a digital control method to significantly improve Boost Power Factor Correction (PFC) converter performance such as the efficiency and Total Harmonic Distortion (THD) under light load condition where efficiency and THD standards are difficult to meet. This is achieved using the integrated digital control feature of the C2000™ microcontroller (MCU). The design supports phase-shedding, valley-switching, valley-skipping, and Zero Voltage Switching (ZVS) for different load and instantaneous input voltage conditions. The software available with this reference design accelerates time to market.

9.3.1.3 Servo Drive Control Module

Servo drives require high precision current and voltage sensing for accurate torque control and often supports interfaces for multiple encoder types along with communication interfaces. F2838x can be used either as single chip solution for standalone servo drive (shown in Figure 9-3) or can be used in decentralized systems (shown in Figure 9-4). In the later case, F2838x functions as the controller which samples all the voltage and current inputs and generates the correct PWM signals for inverter. Each F2838x device serves as real-time controller for a target axis, running motor current control loop. Using the Fast Serial Interface (FSI) peripheral, up to 16 axes can be managed with one F2838x . F2838x as outer loop controller executes main axis motor control, controls data exchange with all secondary axis over FSI and communicates with a host or PLC through EtherCAT.

9.3.1.3.1 System Block Diagram

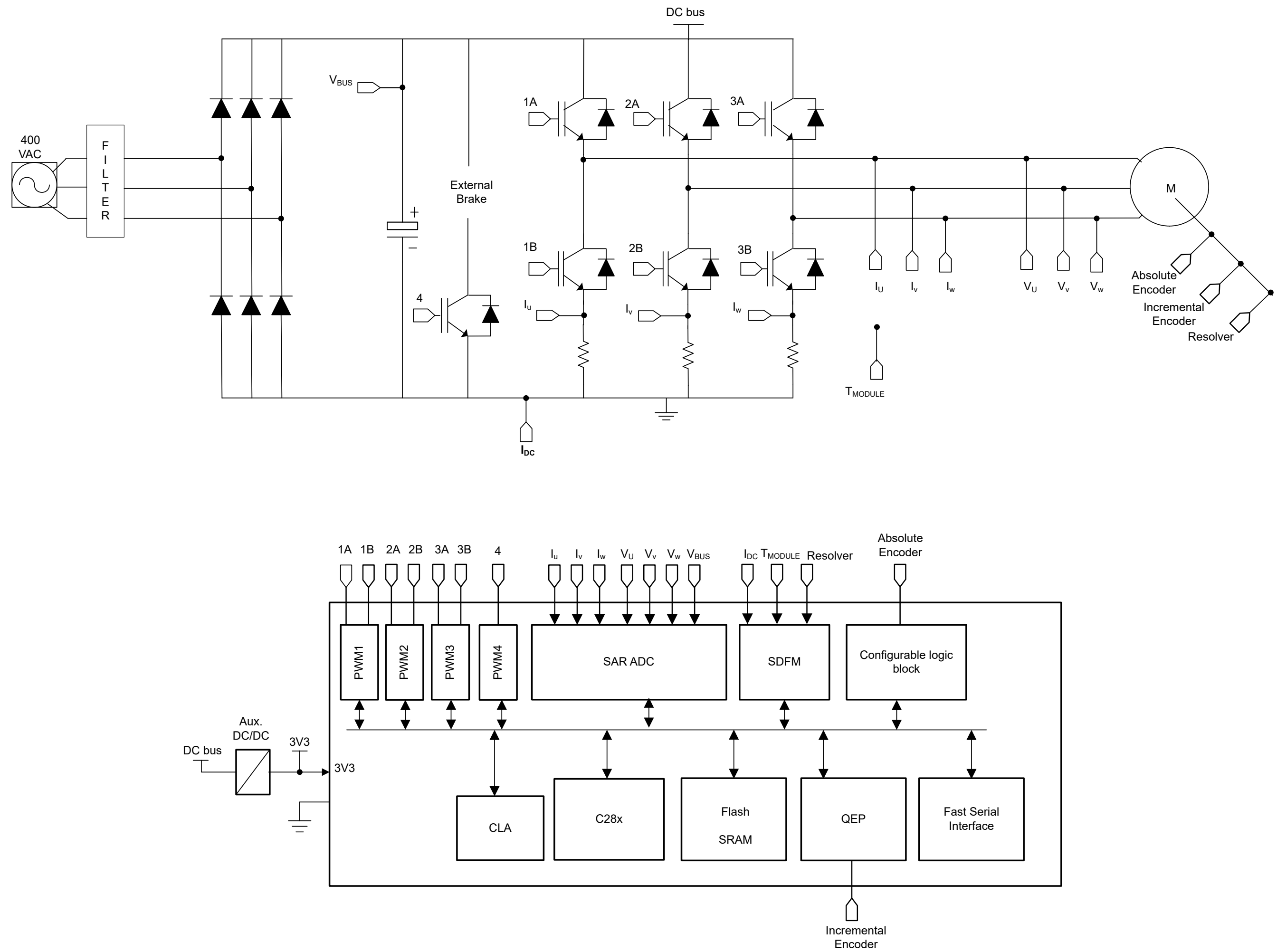


Figure 9-3. Servo Drive Control Module

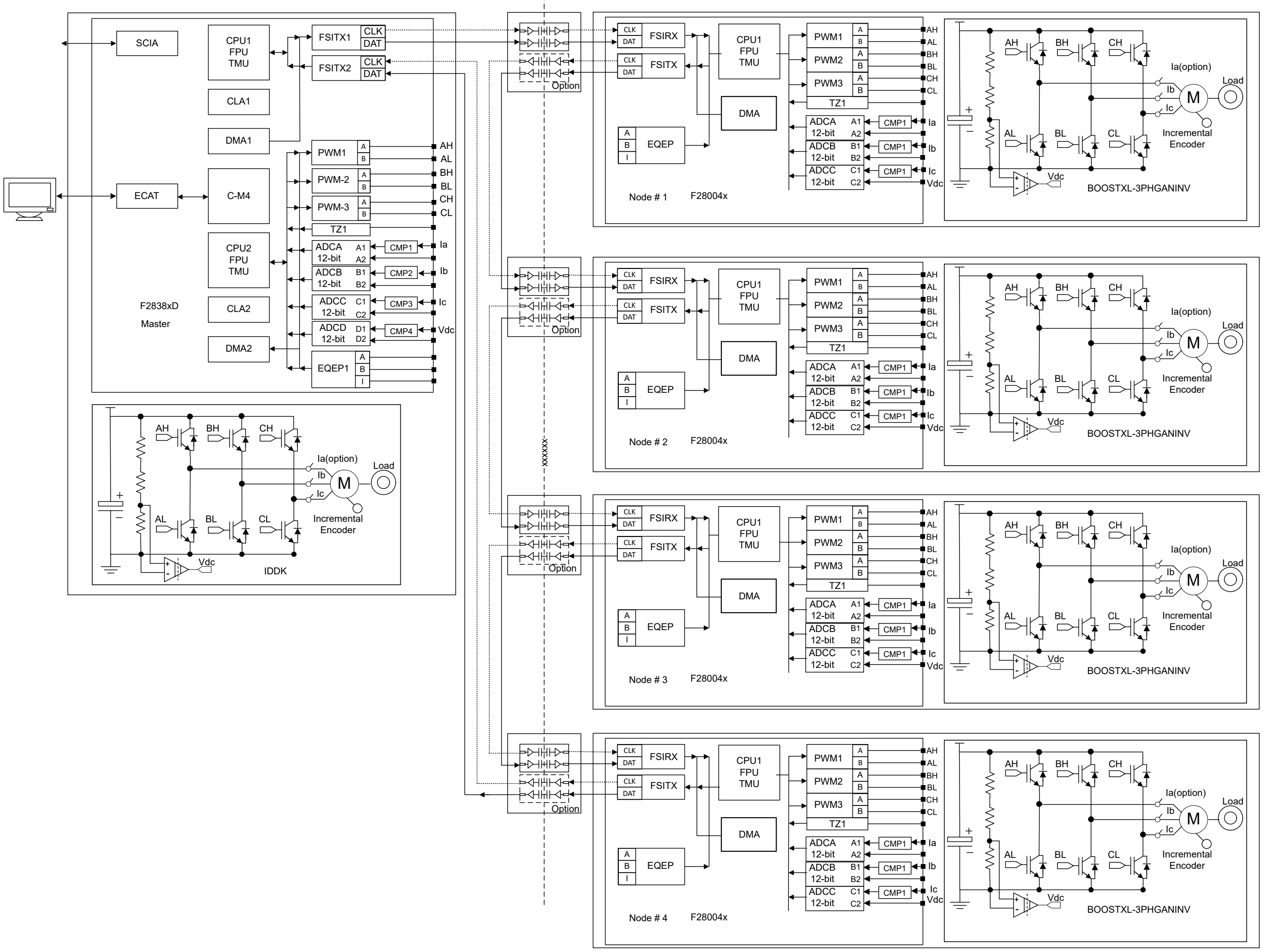


Figure 9-4. Distributed Multi-Axis Servo Drive

9.3.1.3.2 Servo Drive Control Module Resources

Reference Designs and Associated Training Videos

48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Evaluation Module

The BOOSTXL-3PHGANINV evaluation module features a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives.

C2000 DesignDRIVE Development Kit for Industrial Motor Control

The DesignDRIVE Development Kit (IDDK) hardware offers an integrated servo drive design with full power stage to drive a high voltage three-phase motor and eases the evaluation of a range of position feedback, current sensing and control topologies.

C2000 DesignDRIVE position manager BoosterPack™ plug-in module

The PositionManager BoosterPack is a flexible low voltage platform intended for evaluating interfaces to absolute encoders and analog sensors like resolvers and SinCos transducers. When combined with the DesignDRIVE Position Manager software solutions this low-cost evaluation module becomes a powerful tool for interfacing many popular position encoder types such as EnDat, BiSS and T-format with C2000 Real-Time Control devices. C2000 Position Manager technology integrates interfaces to the most popular digital and analog position sensors onto C2000 Real-Time Controller, thus eliminating the need for external FPGAs for these functions.

C2000Ware MotorControl SDK
MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs) which are targeted for industrial drives, robotics, appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications.

TIDM-02006 Distributed multi-axis servo drive over fast serial interface (FSI) reference design
This reference design presents an example distributed or decentralized multi-axis servo drive over Fast Serial Interface (FSI) using C2000™ real-time controllers. Multi-axis servo drives are used in many applications such as factory automation and robots. The cost per axis, performance and ease of use are always high concerns for such systems. FSI is a cost-optimized and reliable high speed communication interface with low jitter that can daisy-chain multiple C2000 microcontrollers. In this design, each TMS320F280049 or TMS320F280025 real-time controller serves as a real-time controller for a distributed axis, running motor current control loop. A single TMS320F28388D runs position and speed control loops for all axes. The same F2838x also executes a centralized motor control axis plus EtherCAT communication, leveraging its multiple cores. The design uses our existing EVM kits, the software is released within C2000WARE MotorControl SDK.

TIDM-02007 Dual-axis motor drive using fast current loop (FCL) and SFRA on a single MCU reference design
This reference design presents a dual-axis motor drive using fast current loop (FCL) and software frequency response analyzer (SFRA) technologies on a single C2000 controller. The FCL utilizes dual core (CPU, CLA) parallel processing techniques to achieve a substantial improvement in control bandwidth and phase margin, to reduce the latency between feedback sampling and PWM update, to achieve higher control bandwidth and maximum modulation index, to improve DC bus utilization by the drive and to increase speed range of the motor. The integrated SFRA tool enables developers to quickly measure the frequency response of the application to tune speed and current controllers. Given the system-level integration and performance of C2000 series, MCUs have the ability to support dual-axis motor drive requirements simultaneously that delivers very robust position control with higher performance. The software is released within C2000Ware MotorControl SDK.

EtherCAT Protocol: EtherCAT on C2000™ TMS320F2838x Device Family (Video)
This video covers details on the TMS320F2838x device EtherCAT slave controller features, details on the TMS320F2838x device EtherCAT slave controller subsystem and device integration, and comparison of TMS320F2838x device EtherCAT IP versus Beckhoff Automation ET1100 EtherCAT ASIC.

EtherCAT-Based Connected Servo Drive Using Fast Current Loop on PMSM Application Report
This application report helps to evaluate EtherCAT® communication and to perform frequency response analysis of fast current loop (FCL) enabled control loops of a connected servo drive using TI's TMS320F28388D real-time controller.

9.3.1.4 Solar Micro Inverter

A Solar Micro Inverter consists of a DC-AC inverter power stage and Maximum Power Point Tracking (MPPT) DC-DC power stage. Typical switching frequency for the inverter (DC-AC) is between 20kHz-50kHz and for DC-DC side can be in the range 100kHz-200kHz. A variety of power stages can be used to achieve this and the diagram only depicts a typical power stage and the control & communication requirements. A C2000 microcontroller has on-chip EPWM, ADC and analog comparator modules to implement complete digital control of such micro inverter system.

9.3.1.4.1 System Block Diagram

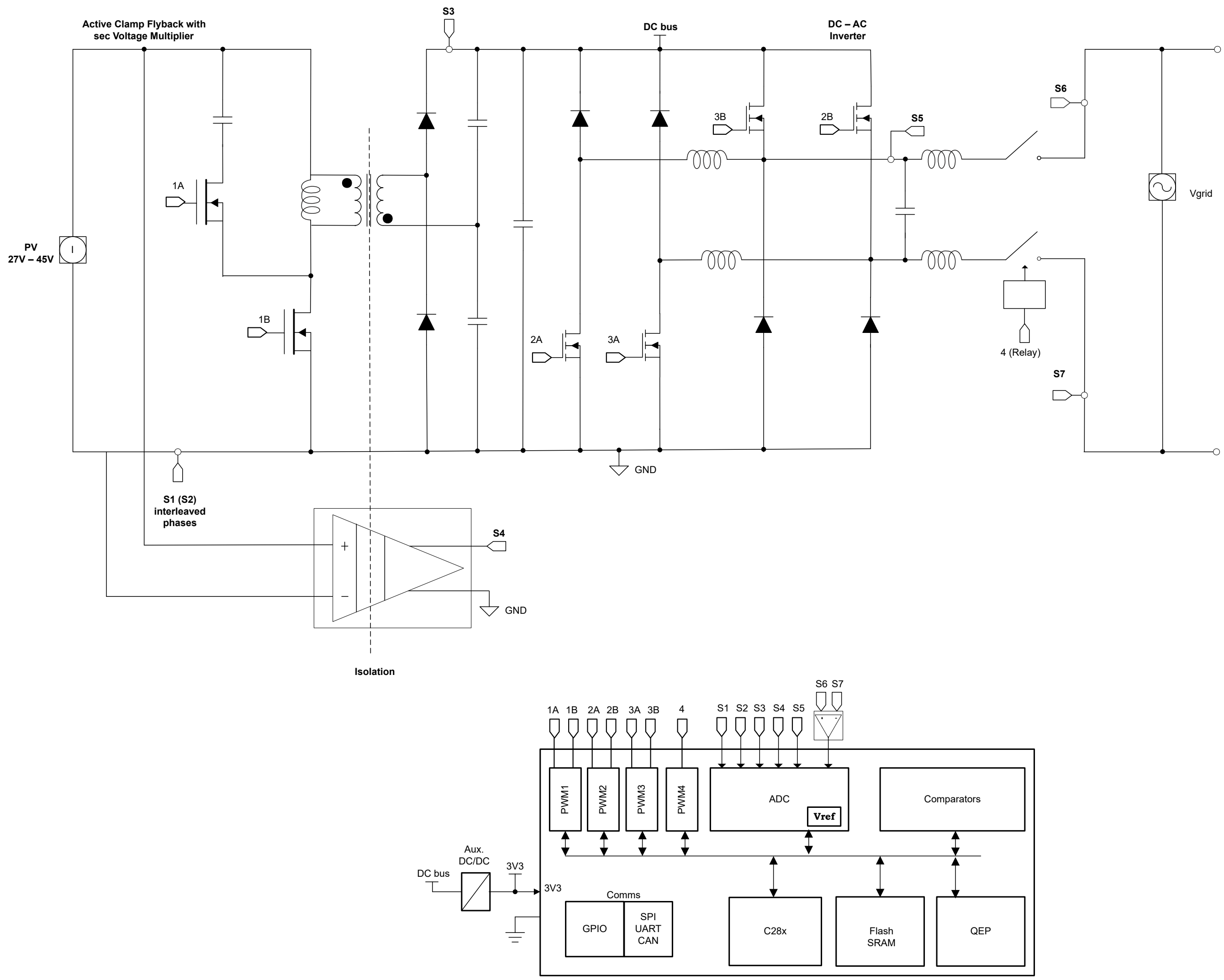


Figure 9-5. Solar Micro Inverter

9.3.1.4.2 Solar Micro Inverter Resources

Reference Designs and Associated Training Videos

C2000™ digital power training series (Video)
This training series covers the basics of digital power control and how to implement it on C2000 microcontrollers.

Four Key Design Considerations When Adding Energy Storage to Solar Power Grids
This white paper explores the design considerations in a grid-connected storage-integrated solar installation system

C2000WARE-DIGITALPOWER-SDK
DigitalPower SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs) which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power application

Digitally Controlled Solar Micro Inverter Design using C2000™ Piccolo Microcontroller
This document presents the implementation details of a digitally-controlled solar micro inverter using the C2000 microcontroller. A 250-W isolated micro inverter design presents all the necessary PV inverter functions using the Piccolo-B (F28035) control card. This document describes the power stages on the micro inverter board, as well as an incremental build level system that builds the software by verifying open loop operation and closed loop operation. This guide describes control structures and algorithms for controlling power flow, maximizing power from the PV panel (MPPT), and locking to the grid using phase locked loop (PLL), along with hardware details of Texas Instruments Solar Micro Inverter Kit (TMDSOLARUINVKIT)

TIDU405B Grid-tied Solar Micro Inverter with MPPT
This C2000 Solar Micro Inverter EVM hardware consists of two stages. These are: (1) an active clamp fly-back DC/DC converter with secondary voltage multiplier and, (2) a DC-AC inverter. A block diagram of this system is shown in Figure 1b. The DC-DC converter draws dc current from the PV panel such that the panel operates at its maximum power transfer point. This requires maintaining the panel output, i.e., the DC-DC converter input at a level determined by the MPPT algorithm. The MPPT algorithm determines the panel output current (reference current) for maximum power transfer. Then a current control loop for the fly-back converter ensures that the converter input current tracks the MPPT reference current. The fly-back converter also provides high frequency isolation for the DC-DC stage. The output of the fly-back stage is a high voltage DC bus which drives the DC-AC inverter. The inverter stage maintains the DC bus at a desired set point and injects controlled sine wave current into the grid. The inverter also implements grid synchronization in order to maintain its current waveform locked to phase and frequency of the grid voltage. A C2000 piccolo microcontroller with its on-chip PWM, ADC and analog comparator modules is able to implement complete digital control of such micro inverter system.

Software Phase Locked Loop Design Using C2000™ Microcontrollers for Single Phase Grid Connected Inverter Application Report
Grid connected applications require an accurate estimate of the grid angle to feed power synchronously to the grid. This is achieved using a software phase locked loop (PLL). This application report discusses different challenges in the design of software phase locked loops and presents a methodology to design phase locked loops using C2000 controllers for single phase grid connection applications.

10 Device and Documentation Support

10.1 Getting Started and Next Steps

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

10.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320 MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28386D). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

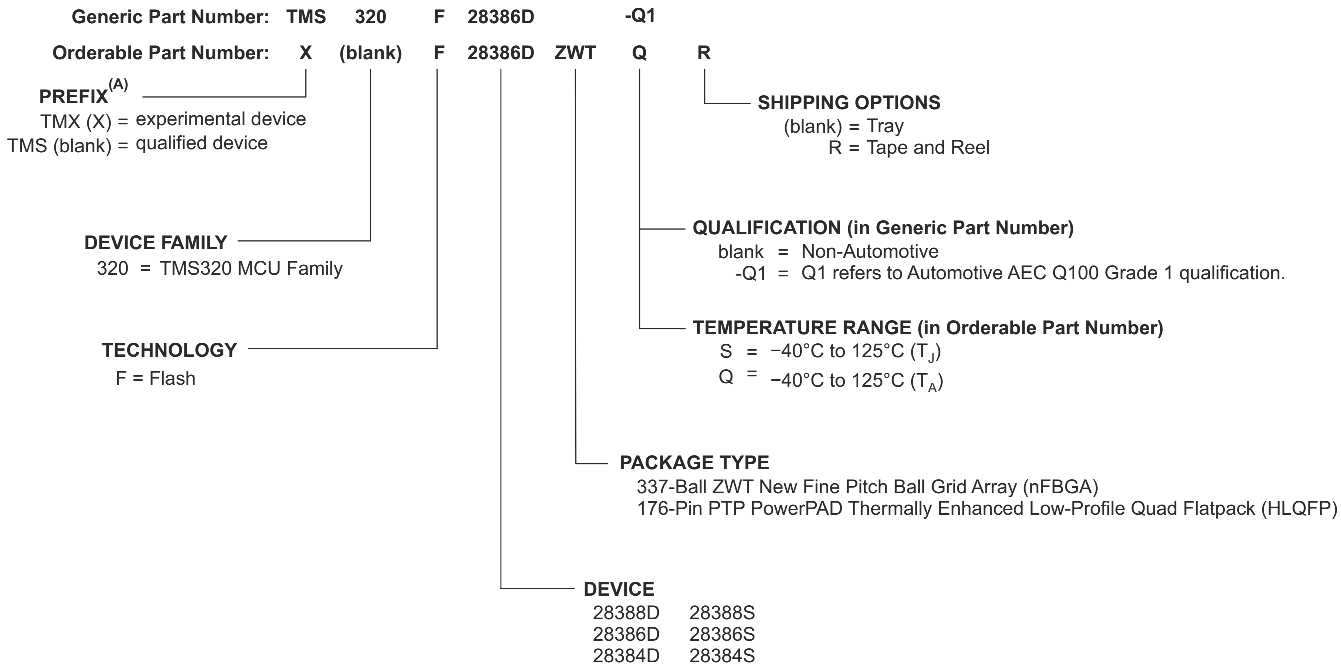
Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZWT) and temperature range (for example, S). Figure 10-1 provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F2838x Real-Time MCUs Silicon Errata*.



A. Prefix X is used in orderable part numbers.

Figure 10-1. Device Nomenclature

10.3 Markings

Figure 10-2 shows the package symbolization and Table 10-1 lists the silicon revision codes.

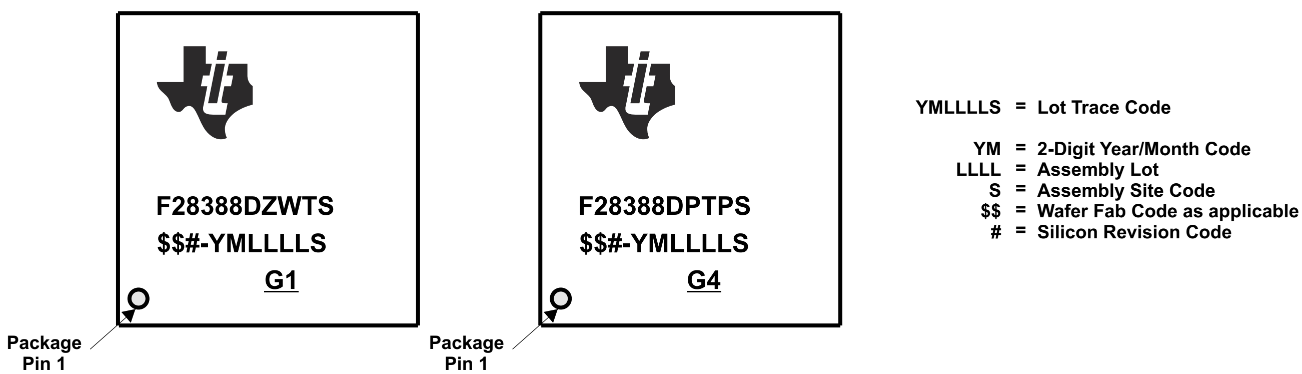


Figure 10-2. Package Symbolization

Table 10-1. Revision Identification

SILICON REVISION CODE	SILICON REVISION	REVID(1) Address: 0x5D00C	COMMENTS
Blank	0	0x0000 0000	This silicon revision is available as TMX.
A	A	0x0000 0001	This silicon revision is available as TMX and TMS.

(1) Silicon Revision ID

10.4 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

Development Tools

F28388D controlCARD for C2000 Real time control development kit
HSEC180 controlCARD development tool for the F2838xD and F2838xS series. controlCARDs are ideal to use for initial evaluation and system prototyping. They are complete board-level modules that provide a low-profile, single-board controller solution.

F28388D Experimenter Kit
The Experimenter Kit is an evaluation bundle that consists of a controlCARD and a TMDSHSECDOCK Baseboard Docking Station. The docking station provides power to the included controlCARD and has a breadboard area for prototyping. Access to the controller's key signals is available using a series of header pins.

Software Tools

C2000Ware for C2000 MCUs
C2000Ware for C2000 microcontrollers is a cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation. C2000Ware is now the recommended content delivery tool versus controlSUITE™.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 Microcontrollers
Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Pin mux tool
The Pin Mux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs.

F021 Flash Application Programming Interface (API)
The F021 Flash Application Programming Interface (API) provides a software library of functions to program, erase, and verify F021 on-chip Flash memory.

UniFlash Standalone Flash Tool
UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

C2000 Third-party search tool TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Design tools & simulation section of the Design & development page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site.

10.5 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

Errata

TMS320F2838x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

TMS320F2838x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2838x microcontrollers.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x DSPs.

Tools Guides

TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The SMT & packaging application notes website lists documentation on TI’s surface mount technology (SMT) and application notes on a variety of packaging-related topics.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

Fast Integer Division – A Differentiated Offering From C2000™ Product Family provides an overview of the different division and modulo (remainder) functions and its associated properties.

C2000™ Key Technology Guide provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

10.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.7 Trademarks

PowerPAD™, C2000™, Code Composer Studio™, TMS320™, controlSUITE™, and TI E2E™ are trademarks of Texas Instruments.
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EtherCAT® is a registered trademark of Beckhoff Automation GmbH, Germany.
Bosch® is a registered trademark of Robert Bosch GmbH.
Freescale® is a registered trademark of NXP USA, INC.
is a registered trademark of Beckhoff Automation GmbH.
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10.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.9 Glossary

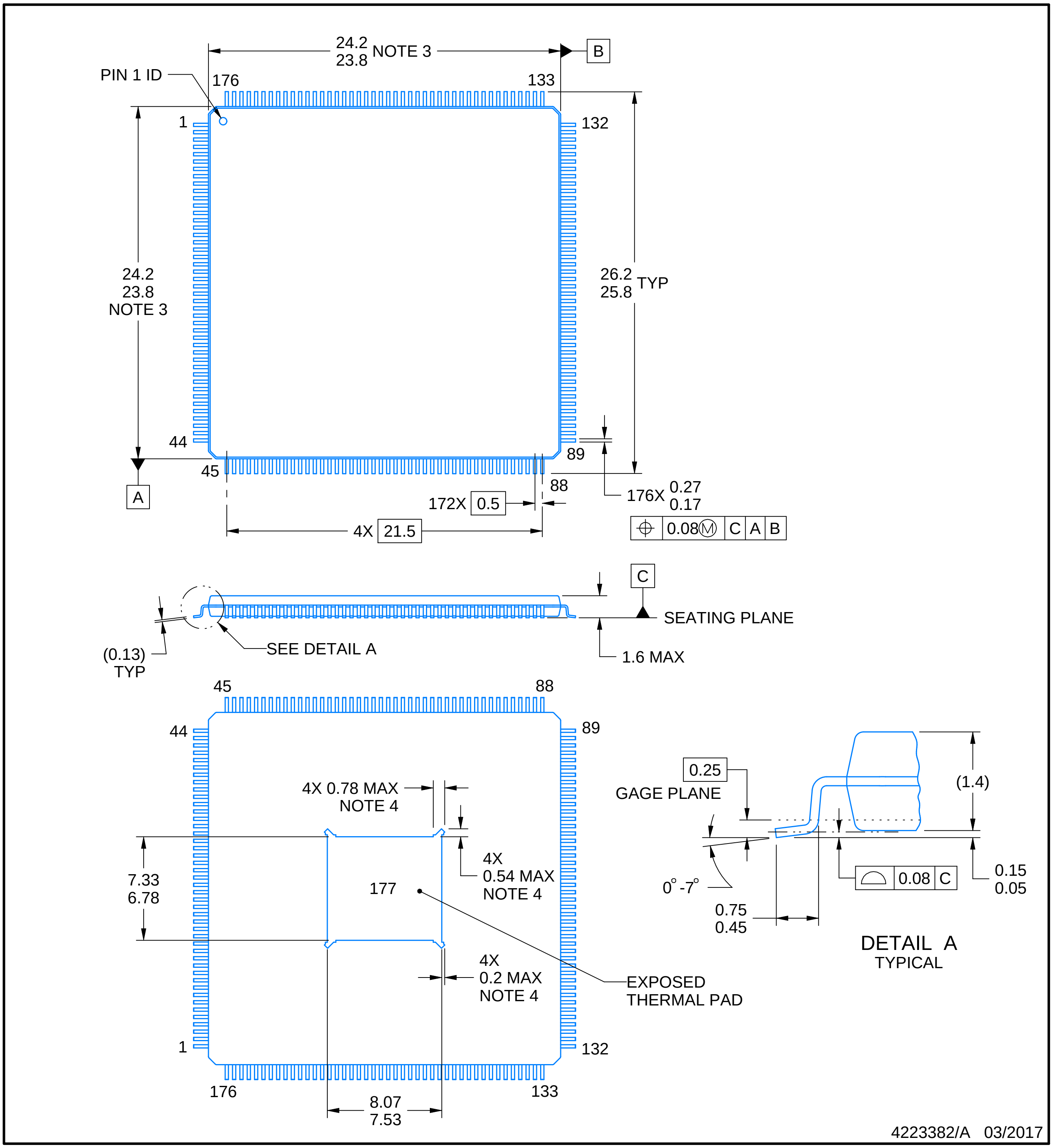
TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

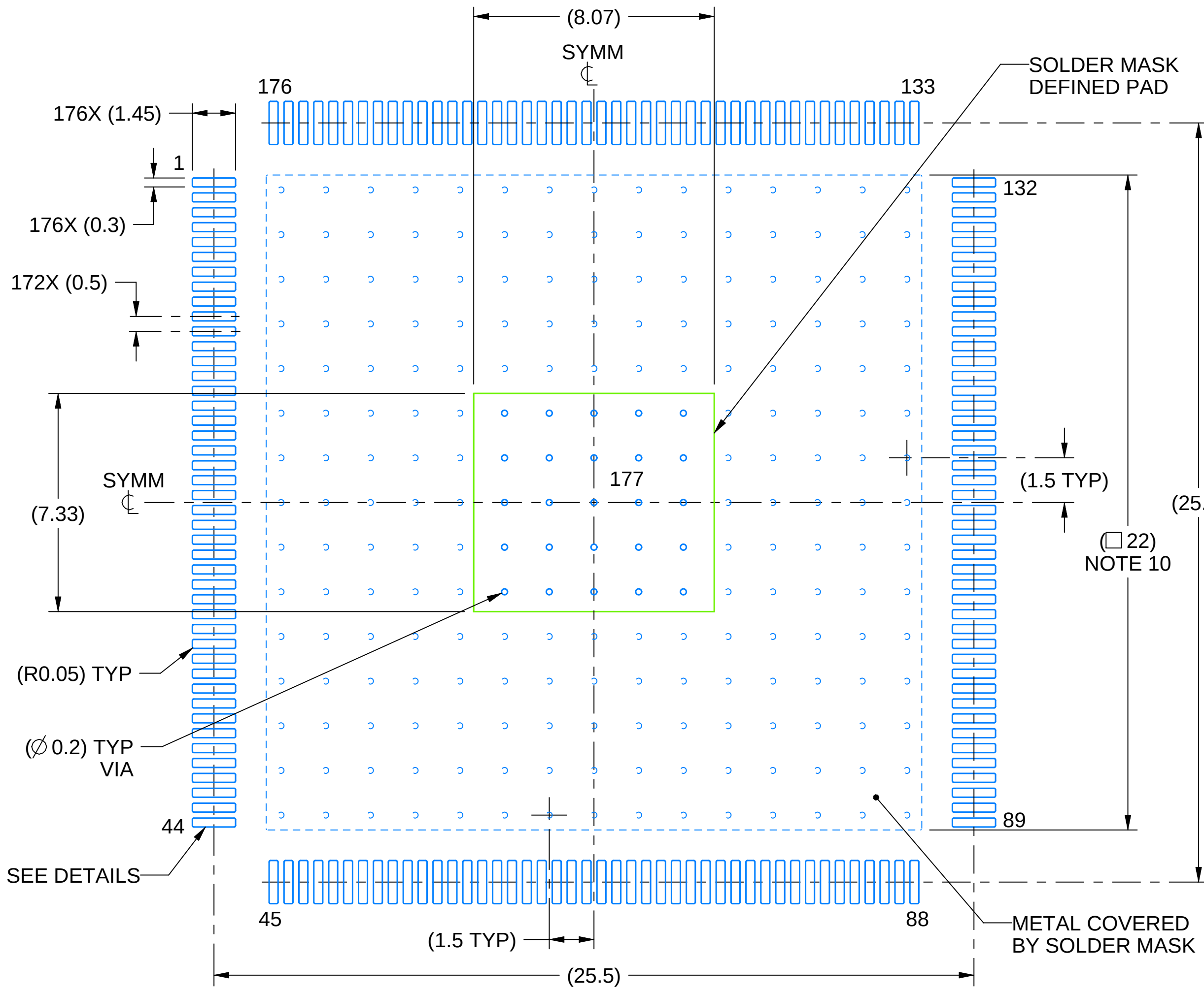
To learn more about TI packaging, visit the Packaging information website.



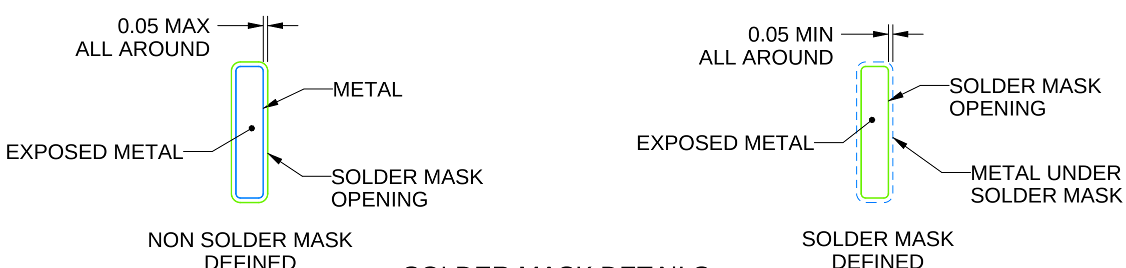
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features my not present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

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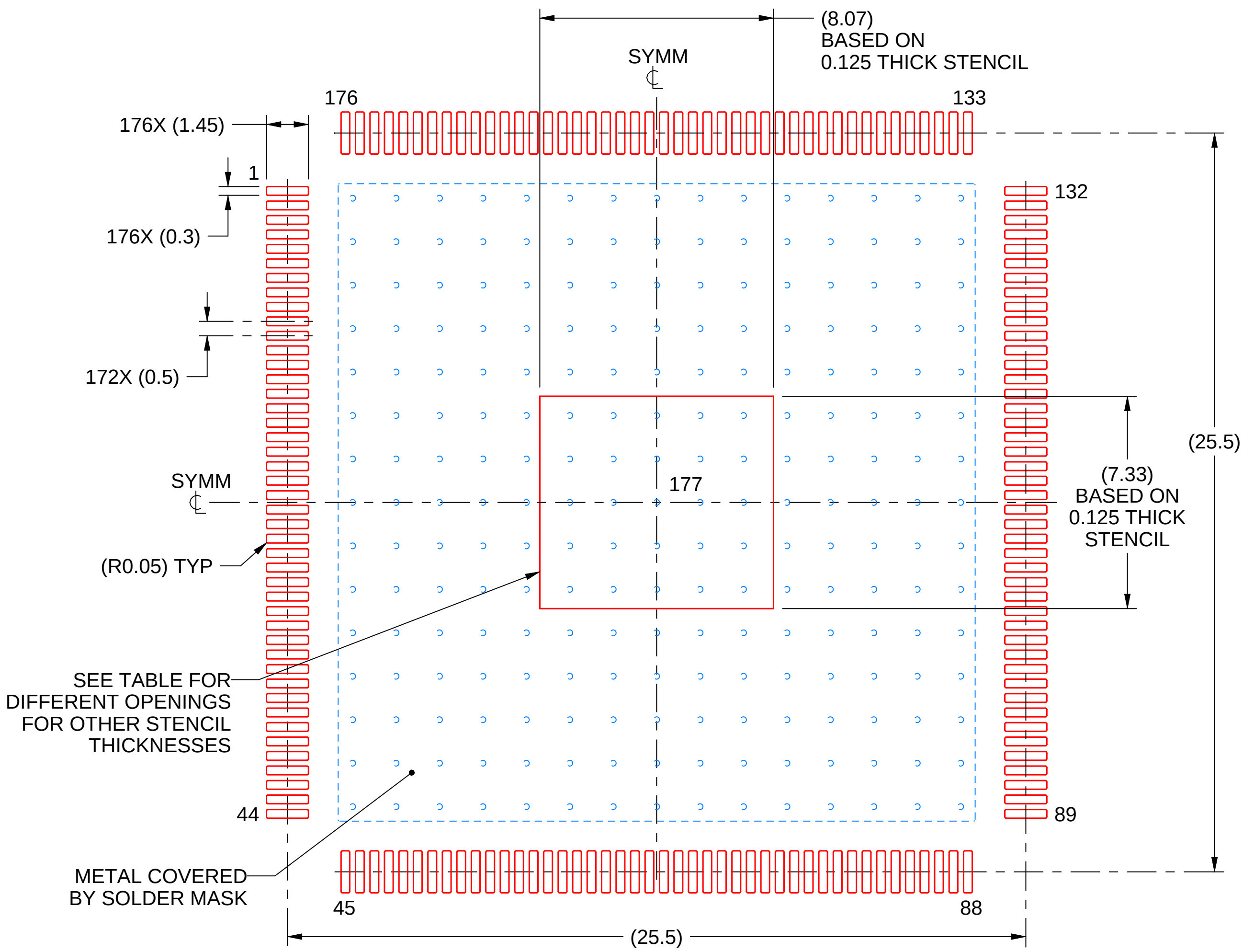
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:4X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	9.02 X 8.2
0.125	8.07 X 7.33 (SHOWN)
0.150	7.37 X 6.69
0.175	6.82 X 6.2

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
F28384DPTPQR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384DPTPQ
F28384DPTPQR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384DPTPQ
F28384DPTPQR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384DPTPQ
F28384DPTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384DPTPS
F28384DPTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384DPTPS
F28384DPTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384DPTPS
F28384DZWTQR	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384DZWTQ
F28384DZWTQR.A	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384DZWTQ
F28384DZWTQR.B	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384DZWTQ
F28384DZWTS	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384DZWTS
F28384DZWTS.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384DZWTS
F28384DZWTS.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384DZWTS
F28384SPTPQR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384SPTPQ
F28384SPTPQR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384SPTPQ
F28384SPTPQR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384SPTPQ
F28384SPTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384SPTPS
F28384SPTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384SPTPS
F28384SPTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28384SPTPS
F28384SZWTS	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384SZWTS
F28384SZWTS.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384SZWTS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
F28384SZWTS.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28384SZWTS
F28386DPTPQ	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPQ
F28386DPTPQ.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPQ
F28386DPTPQ.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPQ
F28386DPTPQR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPQ
F28386DPTPQR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPQ
F28386DPTPQR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPQ
F28386DPTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPS
F28386DPTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPS
F28386DPTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386DPTPS
F28386DZWTQ	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTQ
F28386DZWTQ.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTQ
F28386DZWTQ.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTQ
F28386DZWTQR	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTQ
F28386DZWTQR.A	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTQ
F28386DZWTQR.B	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTQ
F28386DZWTS	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTS
F28386DZWTS.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTS
F28386DZWTS.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386DZWTS
F28386SPTPQR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386SPTPQ
F28386SPTPQR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386SPTPQ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
F28386SPTPQR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386SPTPQ
F28386SPTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386SPTPS
F28386SPTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386SPTPS
F28386SPTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28386SPTPS
F28386SZWTS	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386SZWTS
F28386SZWTS.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386SZWTS
F28386SZWTS.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28386SZWTS
F28388DPTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388DPTPS
F28388DPTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388DPTPS
F28388DPTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388DPTPS
F28388DPTPSR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388DPTPS
F28388DPTPSR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388DPTPS
F28388DPTPSR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388DPTPS
F28388DZWTS	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388DZWTS
F28388DZWTS.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388DZWTS
F28388DZWTS.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388DZWTS
F28388DZWTSR	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388DZWTS
F28388DZWTSR.A	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388DZWTS
F28388DZWTSR.B	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388DZWTS
F28388SPTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388SPTPS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
F28388SPTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388SPTPS
F28388SPTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388SPTPS
F28388SPTPSR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388SPTPS
F28388SPTPSR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388SPTPS
F28388SPTPSR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28388SPTPS
F28388SZWTS	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388SZWTS
F28388SZWTS.A	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388SZWTS
F28388SZWTS.B	Active	Production	NFBGA (ZWT) | 337	90 | JEDEC TRAY (10+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388SZWTS
F28388SZWTSR	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388SZWTS
F28388SZWTSR.A	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388SZWTS
F28388SZWTSR.B	Active	Production	NFBGA (ZWT) | 337	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	F28388SZWTS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TMS320F28384D, TMS320F28384D-Q1, TMS320F28384S, TMS320F28384S-Q1, TMS320F28386D, TMS320F28386D-Q1, TMS320F28386S, TMS320F28386S-Q1 :

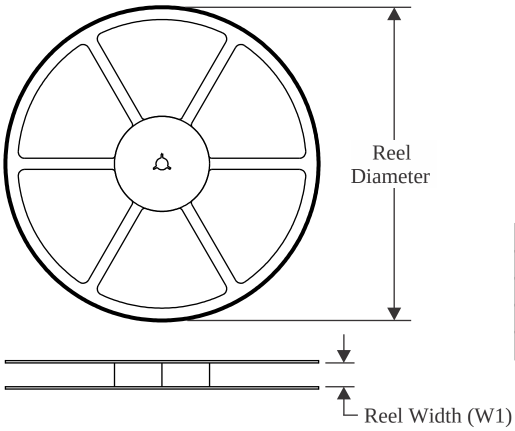
- Catalog : TMS320F28384D, TMS320F28384S, TMS320F28386D, TMS320F28386S
- Automotive : TMS320F28384D-Q1, TMS320F28384S-Q1, TMS320F28386D-Q1, TMS320F28386S-Q1

NOTE: Qualified Version Definitions:

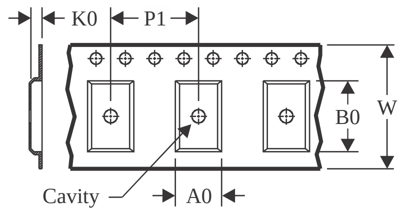
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

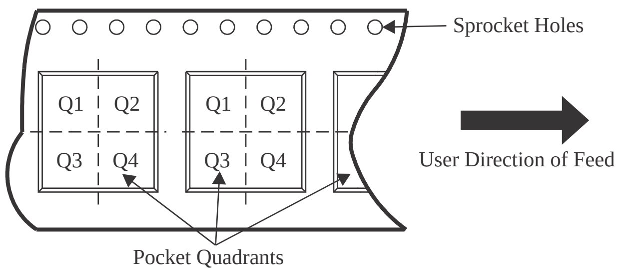


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

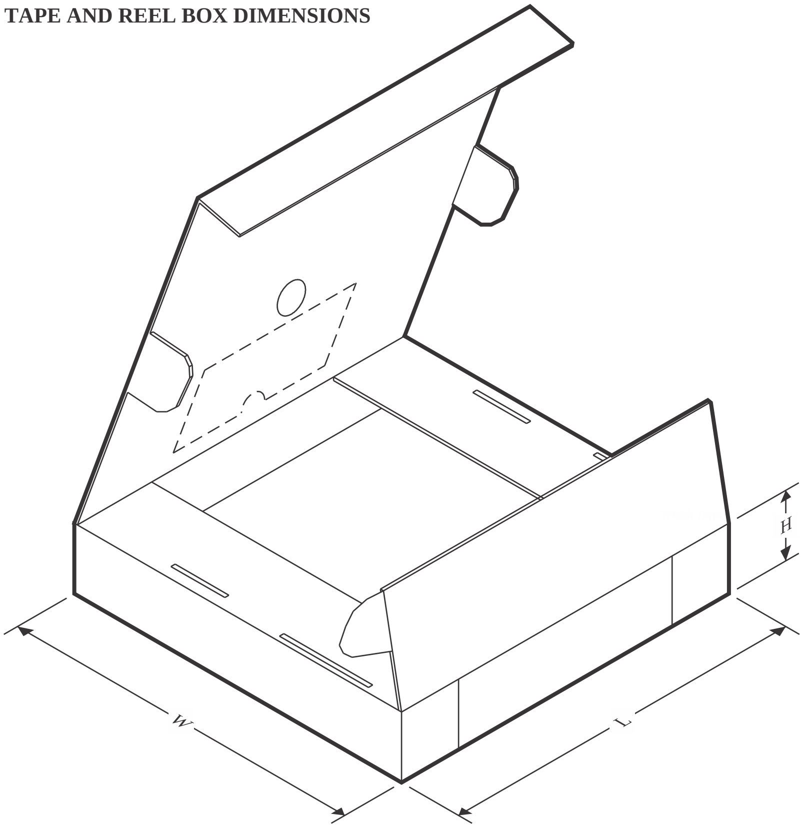
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
F28384DPTPQR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2
F28384DZWTQR	NFBGA	ZWT	337	1000	330.0	24.4	16.35	16.35	2.35	20.0	24.0	Q1
F28384SPTPQR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2
F28386DPTPQR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2
F28386DZWTQR	NFBGA	ZWT	337	1000	330.0	24.4	16.35	16.35	2.35	20.0	24.0	Q1
F28386SPTPQR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2
F28388DPTPSR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2
F28388DZWTSR	NFBGA	ZWT	337	1000	330.0	24.4	16.35	16.35	2.35	20.0	24.0	Q1
F28388SPTPSR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2
F28388SZWTSR	NFBGA	ZWT	337	1000	330.0	24.4	16.35	16.35	2.35	20.0	24.0	Q1

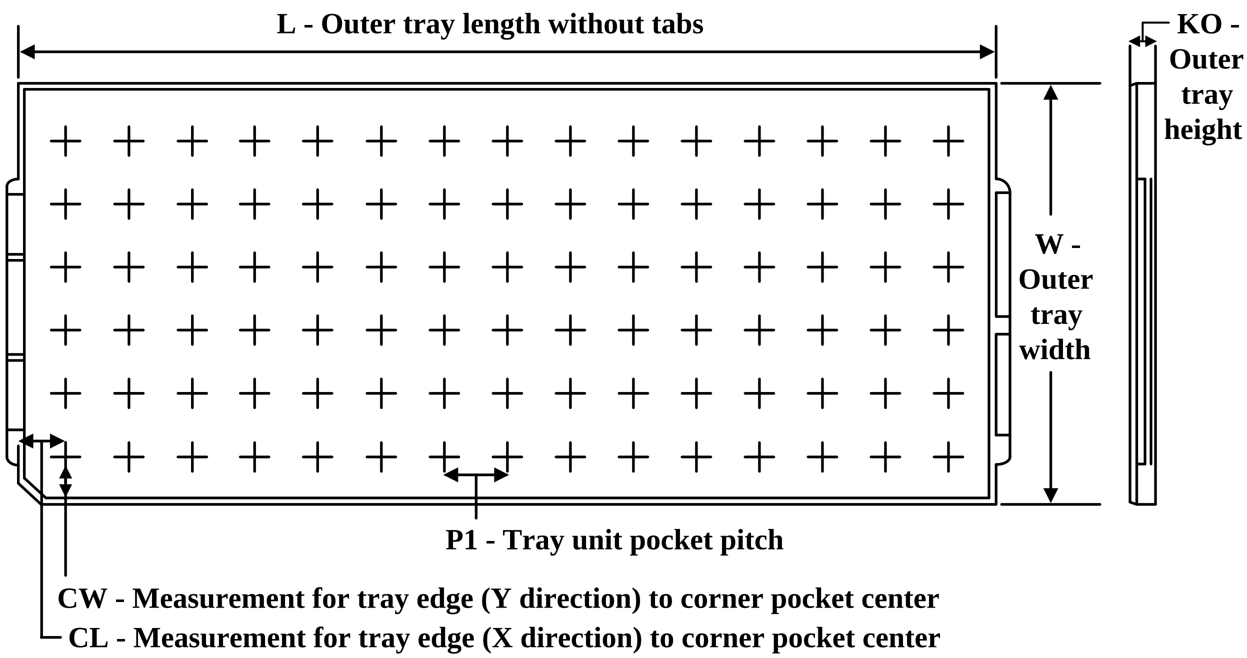
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
F28384DPTPQR	HLQFP	PTP	176	200	367.0	367.0	67.0
F28384DZWTQR	NFBGA	ZWT	337	1000	336.6	336.6	41.3
F28384SPTPQR	HLQFP	PTP	176	200	367.0	367.0	67.0
F28386DPTPQR	HLQFP	PTP	176	200	367.0	367.0	67.0
F28386DZWTQR	NFBGA	ZWT	337	1000	336.6	336.6	41.3
F28386SPTPQR	HLQFP	PTP	176	200	367.0	367.0	67.0
F28388DPTPSR	HLQFP	PTP	176	200	367.0	367.0	67.0
F28388DZWTSR	NFBGA	ZWT	337	1000	336.6	336.6	41.3
F28388SPTPSR	HLQFP	PTP	176	200	367.0	367.0	67.0
F28388SZWTSR	NFBGA	ZWT	337	1000	336.6	336.6	41.3

TRAY

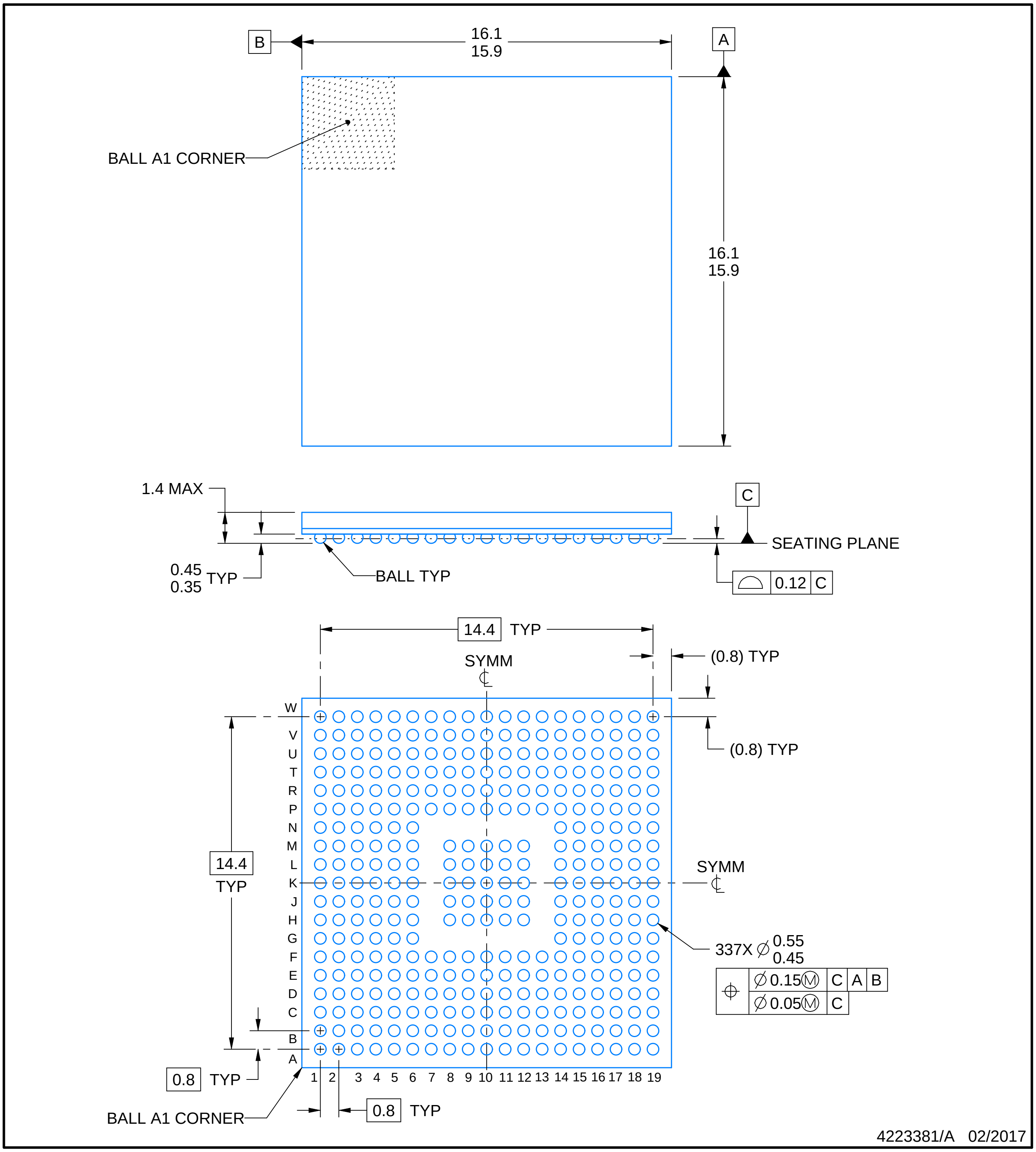


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

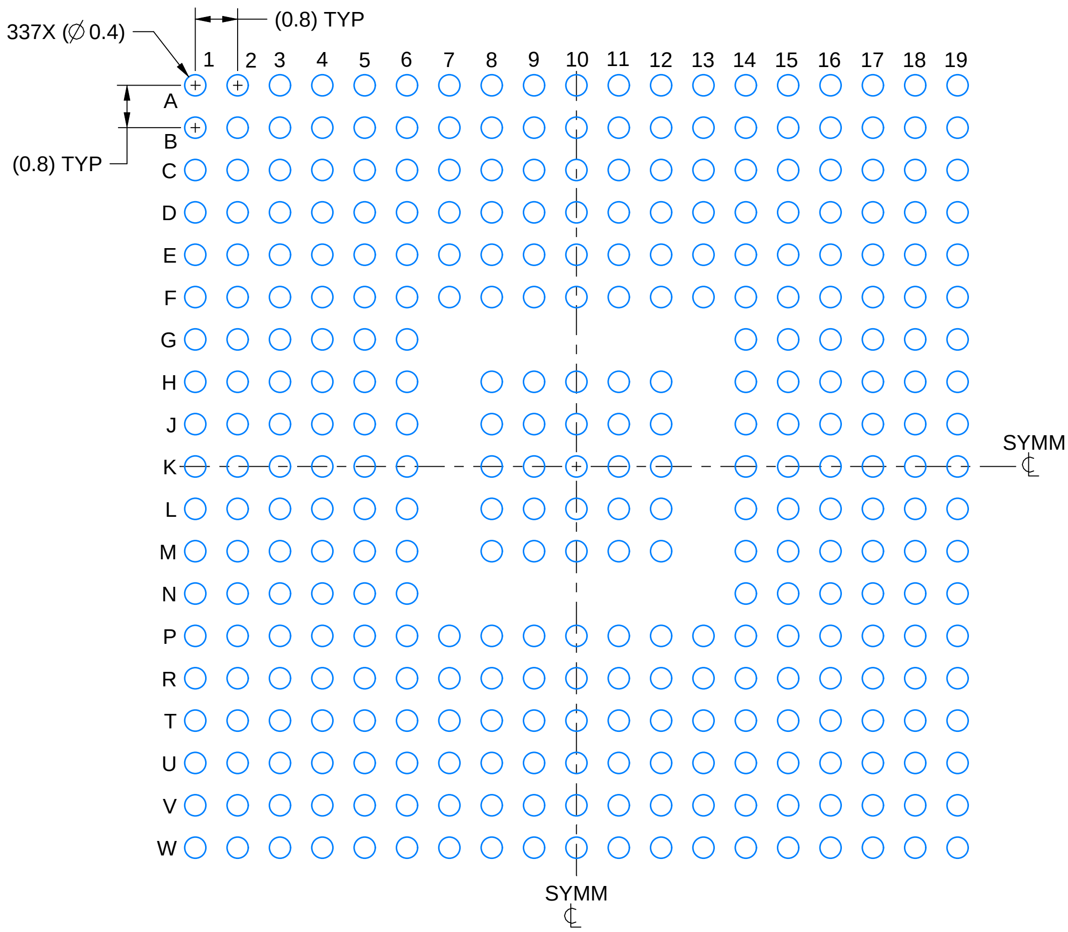
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
F28384DPTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28384DPTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28384DPTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28384DZWTS	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28384DZWTS.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28384DZWTS.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28384SPTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28384SPTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28384SPTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28384SZWTS	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28384SZWTS.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28384SZWTS.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386DPTPQ	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386DPTPQ.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386DPTPQ.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386DPTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386DPTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
F28386DPTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386DZWTQ	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386DZWTQ.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386DZWTQ.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386DZWTS	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386DZWTS.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386DZWTS.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386SPTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386SPTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386SPTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28386SZWTS	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386SZWTS.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28386SZWTS.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28388DPTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28388DPTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28388DPTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28388DZWTS	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28388DZWTS.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28388DZWTS.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28388SPTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28388SPTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28388SPTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
F28388SZWTS	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28388SZWTS.A	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45
F28388SZWTS.B	ZWT	NFBGA	337	90	6 X 15	150	315	135.9	7620	20	17.5	15.45

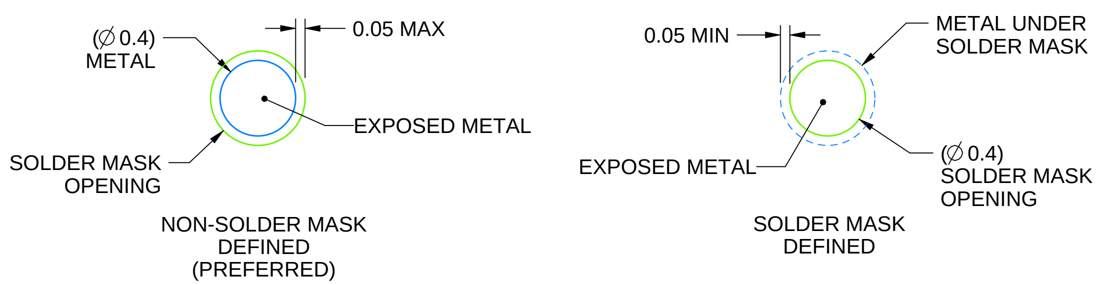


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:7X



SOLDER MASK DETAILS
NOT TO SCALE

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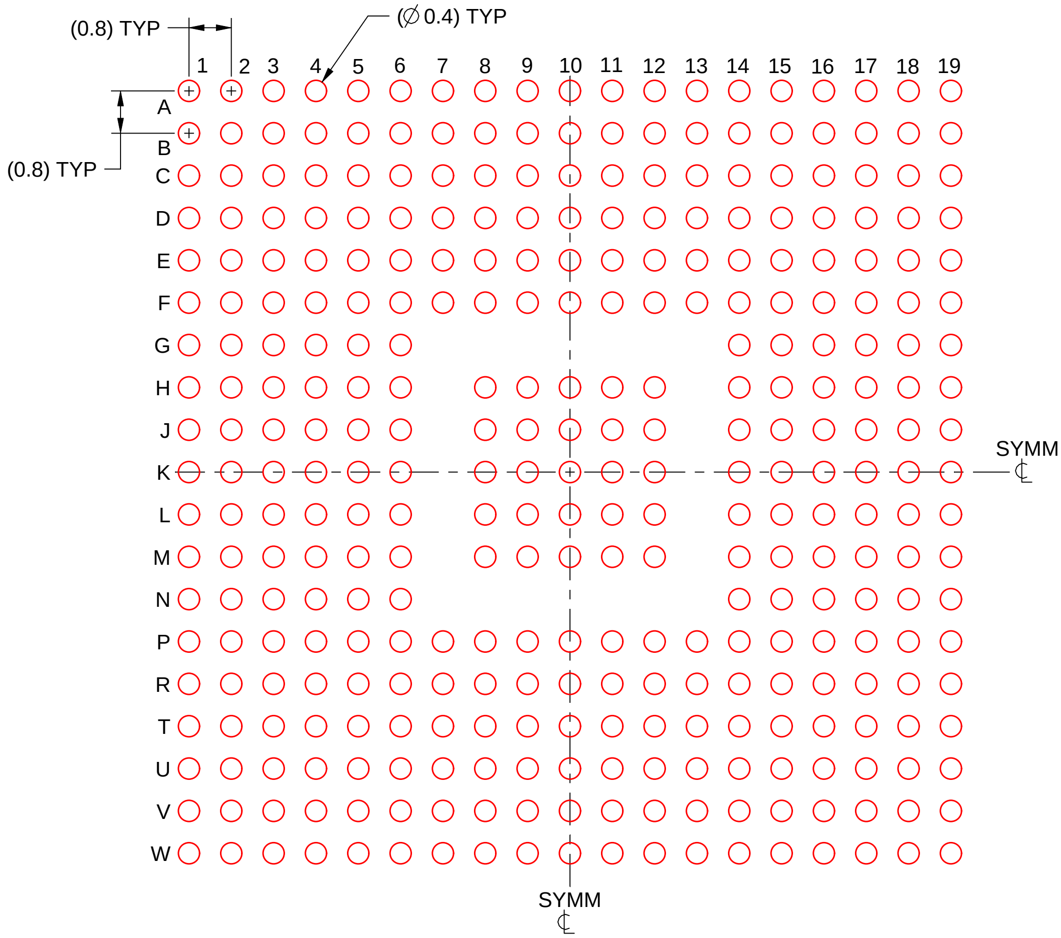
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.